

Article

Nonlinear Capacitance Compensation Method for Integrating a Metal–Semiconductor–Metal Varactor with a Gallium Nitride High Electron Mobility Transistor Power Amplifier

Ke Li ^{1,2,3}, Yitian Gu ^{1,2,3}, Haowen Guo ¹ and Xinbo Zou ^{1,*} 

- ¹ School of Information Science and Technology, ShanghaiTech University, Shanghai 201210, China; like3@shanghaitech.edu.cn (K.L.); guyt@shanghaitech.edu.cn (Y.G.); guohw@shanghaitech.edu.cn (H.G.)
- ² Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China
- ³ University of Chinese Academy of Sciences, Beijing 100049, China
- * Correspondence: zouxb@shanghaitech.edu.cn

Abstract: A nonlinear capacitance compensation technique is presented in this paper to enhance the linearity of a power amplifier (PA) in the GaN process. The method involves placing an MSM varactor device alongside the GaN HEMT device, which works as the amplifying unit such that the overall capacitance observed at the amplifier input is constant, thus improving linearity. This approach is a reliable and straightforward way to improve PA linearity in the GaN process. The proof-of-concept prototype in this study involves the fabrication of a PA device using a standard GaN HEMT process, which successfully integrates the proposed compensation technique and demonstrates excellent compatibility with existing processes. The prototype has a saturation output power of 18 dBm, a peak power-added efficiency of 51.8%, and a small signal gain of 15.5 dB at 1 GHz. The measured AM–PM distortion at the 5 dB compression point is reduced by more than 50% compared to that of an uncompensated device. Furthermore, the results of third-order intermodulation distortion demonstrate the effectiveness of the linearity enhancement concept, with values improved by more than 5 dB in the linear region compared to those of the uncompensated device. All of the results demonstrate the potential utility of this design approach for wireless communication applications.

Keywords: GaN HEMT; power amplifier; AM–PM distortion



Citation: Li, K.; Gu, Y.; Guo, H.; Zou, X. Nonlinear Capacitance Compensation Method for Integrating a Metal–Semiconductor–Metal Varactor with a Gallium Nitride High Electron Mobility Transistor Power Amplifier. *Electronics* **2024**, *13*, 1265. <https://doi.org/10.3390/electronics13071265>

Academic Editor: Jayant Parekh

Received: 30 January 2024

Revised: 3 March 2024

Accepted: 23 March 2024

Published: 28 March 2024



Copyright: © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

Gallium nitride (GaN) high electron mobility transistors (HEMTs) have emerged as a highly suitable technology for radio frequency (RF) and microwave PA applications, primarily due to their remarkable power density and efficiency. GaN HEMTs are widely recognized for their good performance in wireless communications and radar systems [1–3]. Nonetheless, the nonlinear behavior of GaN PAs has the following unique characteristics: (1) highly nonlinear transconductance and trapping effects lead to soft compression in the AM–AM characteristics, especially for complex modulation signals with high PAPR; (2) unlike silicon LDMOS devices, whose AM–PM distortion is determined by the output nonlinear capacitance, GaN HEMTs are determined by the variation of the input impedance due to the nonlinear gate–source capacitance (C_{gs}) and the input Miller–reflection gate–drain capacitance (C_{ds}). These properties present new challenges for the linearization of GaN PAs. In such cases, stringent requirements are placed on the amplifier linearity, both for AM–AM and AM–PM.

Several RF PAs have been published that use improved linearization techniques, either digital or analog, to support higher data rates and higher-order modulation signals. Digital predistortion based on baseband signal processing is also used to improve linearity [4]. Although very powerful, digital predistortion algorithms are based on black-box behavior

modelling and therefore do not provide designers with circuit-level feedback or solutions. Two general approaches for PA phase linearization have been developed. In one approach, a multi-transistor architecture or combination of nonlinear devices is employed as the power unit, and the nonlinear curves of individual devices are combined to compensate for the nonlinear characteristics of different devices [5]. In another approach, separate nonlinear circuits or cascaded/parallel amplifier stages are used to equalize the phase-power profile [6]. The first approach is aimed at optimizing the efficiency and bandwidth, with little consideration of linearity. Moreover, the second approach can be influenced by matching network effects, linearizer losses, and PM variations [7]. In CMOS PAs, the nonlinear input capacitance of NMOS transistors can be mitigated by introducing auxiliary PMOS transistors as varactors, which have complementary input capacitance characteristics [8]. The broadband compensation capability of this ultrawideband technology has been experimentally demonstrated [9]. However, this technique is impractical in GaN processes, as only N-channel transistors are available.

In this paper, we propose a method to compensate for the input capacitance of GaN-based PAs by leveraging the nonlinearity of Metal–Semiconductor–Metal (MSM) varactors. To validate the effectiveness of the proposed approach, we fabricate a prototype amplifier based on a theoretical design using a standard III–V process. Through small-signal tests, we observe a significant reduction in the variation in the input capacitance of the compensated device from 251 fF to 122 fF. This work demonstrates the successful compensation achieved by this method. Furthermore, single-tone and two-tone tests are conducted to evaluate the AM–PM characteristics and linearity of the compensated amplifier. The results illustrate the excellent AM–PM characteristics and high linearity of the proposed device, indicating the efficacy of our compensation method. This method offers a novel approach for designing high-linearity PAs that are fully compatible with current processes. This approach holds promise for the design of GaN-based MMICs and high-power PAs.

2. The Nonlinearity Generated by the Input Capacitance

The Class-AB PA typically operates near the threshold voltage of the transistor device. When subjected to a large input signal, the device swiftly alternates between the on and off states, leading to a substantial alteration in the gate-to-source capacitance (C_{gs}) [10]. This effect is further amplified when large transistors are used to increase the output power.

To gain insight into the nonlinearity in GaN HEMTs, a simplified, nonlinear model is presented in Figure 1. Figure 1 illustrates the major nonlinear sources in a GaN transistor and their interdependencies: the drain-to-source current (I_{ds}), the C_{gs} , and the C_{gd} . An analysis of Figure 1 allows us to determine the input capacitance (C_{in}). C_{gs} is connected to the ground, while C_{gd} exists between the input and output of the device. Therefore, the capacitance observed from the gate to the ground is the sum of C_{gs} and the Miller multiplication of C_{gd} , which can be expressed as:

$$C_{in}(v_{gs}) = C_{gs}(v_{gs}) + (1 - A_v(v_{gs}))C_{gd}, \quad (1)$$

where A_v is the voltage gain of the PA and is defined as $A_v = -g_m Z_L$ and Z_L is the load impedance of HEMT. The complex input impedance, represented as Z_{in} , is observed from the gate (G).

$$Z_{in}(v_{gs}) = \frac{1}{j\omega C_{in}(v_{gs})}, \quad (2)$$

The variation in $Z_{in}(j\omega)$ with respect to the input amplitude results in AM–PM distortion. This distortion is exclusively caused by nonlinear capacitors and is observed in the gate voltage and subsequently in the drain current.

As shown in Equation (1), the C_{gs} and g_m will not have linear behavior due to their dependence on v_{gs} . Hence, Z_{in} will not be constant during large-signal operation and cause nonlinearity [11]. In Equation (1), C_{gs} is the small-signal capacitance of the nonlinear capacitor. In small-signal operation, a certain phase shift appears from the input port to

the gate of the GaN HEMT, but as the input amplitude rises, the effective C_{in} changes and so does this phase shift. The changing phase shift with input amplitude gives rise to AM–PM distortion. The C_{gd} contribution is due to AM–AM gain variation, that is, to gain compression. As voltage gain A_v drops, the Miller-multiplied capacitance diminishes, resulting in the AM–PM distortion, like C_{gs} . The nonlinear input capacitance's impact on AM–AM characteristics is minor, as the design frequency is less than the cut-off frequency of the input RC impedance [12].

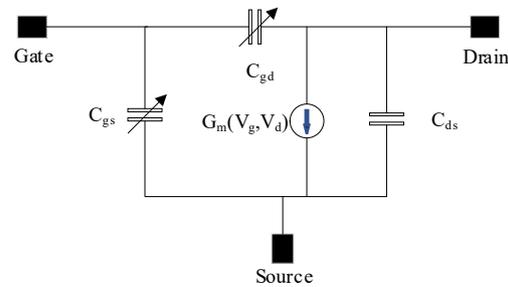


Figure 1. A simplified, nonlinear model for the GaN HEMT.

For a 10 W GaN HEMT device, the strongly nonlinear CV profile of the C_{gs} is depicted in Figure 2. The average input capacitance of a transistor is subjected to the gate bias condition and input signal magnitude. As shown in Figure 2, the GaN HEMT is biased in the Class-AB mode. For small-to-large input swings, the average C_{gs} of the HEMT is reduced, which is supposed to result in AM–PM distortion.

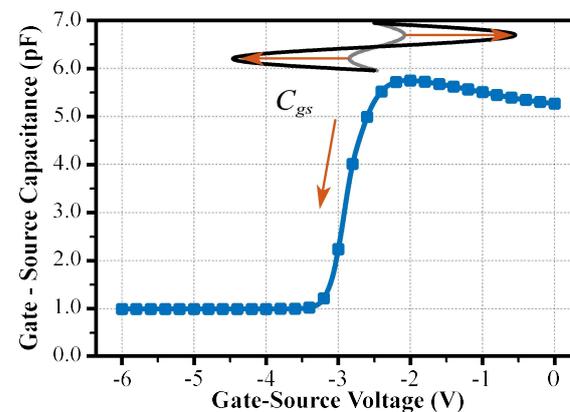


Figure 2. Simulation result of the commercial GaN HEMT device's gate–source capacitance as a function of gate–source voltage for a fixed drain–source voltage of 28 V.

3. Proposed Capacitance Compensation Method

To enhance the linearity characteristics of GaN PAs, AM–PM distortion can be mitigated by reducing the variation in the input capacitance. The input capacitance–compensation technique is widely used to improve linearity in CMOS PA [8]. However, this compensation technique is not effective in GaN processes, as only N-channel transistors are available.

The implementation of this idea can be achieved through the use of an MSM varactor, which has the potential to be integrated with GaN devices [13]. The MSM varactor is composed of two Schottky diodes with back-to-back contacts, as shown in Figure 3. By adjusting the electrode geometry, the capacitance swing of the MSM varactor can be altered [14]. In the unbiased state, the capacitance of the MSM varactor is determined by the electrode area and the distance to the 2DEG channel, which acts as an equipotential plane. When applying a bias voltage, depletion occurs in the channel beneath the reverse-biased electrode. As the bias voltage increases, the depletion region extends deeper into the device, resulting in a significant reduction in capacitance within a narrow voltage

range [13]. The transition voltage, which is closely related to the threshold voltage of the corresponding transistor, varies depending on the carrier density of the 2DEG. It facilitates the transition from high to low capacitance. The transition voltage is the threshold voltage of the reverse-biased contact added by the voltage drop at the forward-biased contact. When the MSM varactor and HEMT are integrated on the same epitaxial wafer, the trends of the nonlinear capacitance in both components exhibit similarities. The absence of P-type devices in the GaN process can also be overcome. This characteristic allows for the compensation of the input capacitance of the HEMT using the MSM varactor, which is similar to the approach applied in CMOS processes [8].

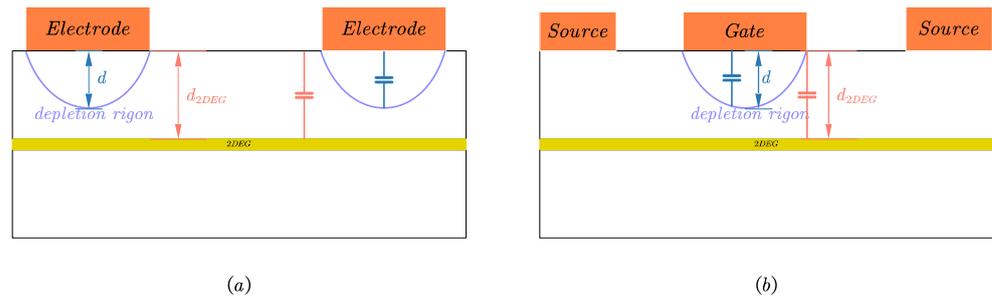


Figure 3. (a) The proposed MSM varactor structure and equivalent circuit model. (b) Equivalent circuit model for C_{gs} to HEMT.

The nonlinear C_{gs} - V_{gs} profile can be modeled as a tangent function, which is an anti-symmetric function for the center point V_0 . As shown in Figure 3, suppose the HEMT C_{gs} - V_{gs} profile is modeled as

$$C_{gs}(v) = C_0 + C_1 \cdot \tanh\left(\frac{v - V_0}{V_1}\right), \tag{3}$$

Figure 4 illustrates that by adding an ideal nonlinear compensating capacitor (C_{comp}) in parallel with the C_{gs} , the overall input capacitance can be maintained constant, unaffected by the V_{gs} . This concept can be realized by integrating an MSM varactor at the input of HEMT. The MSM varactor is biased at control voltage (V_c), which is derived from the sum of the V_0 of HEMT C_{gs} and the threshold voltage of the MSM varactor. Consequently, this compensatory arrangement reduces the AM-PM distortion resulting from the nonlinear input capacitance. However, compensating for the varactor increases the chip area due to the large size of the PA HEMT and an increase in the input capacitance.

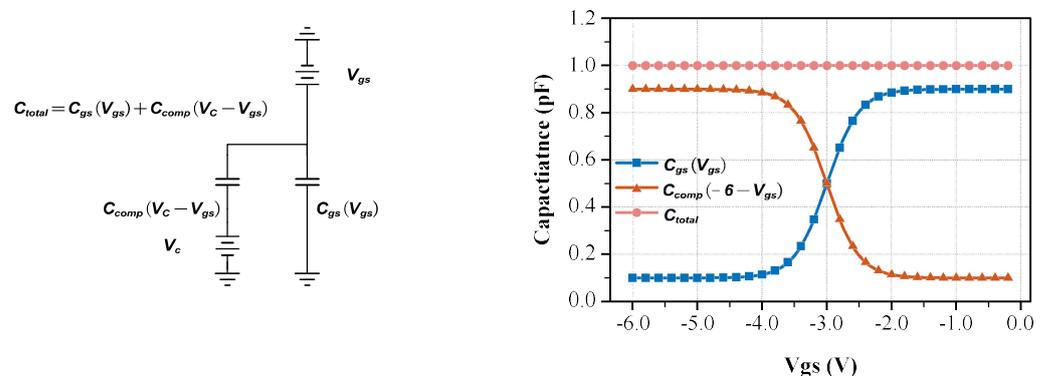


Figure 4. The proposed gate–source capacitance compensation technology for the GaN HEMT. The C_{gs} is $C_{gs}(v_{gs}) = 0.5 + 0.4 \cdot \tanh\left(\frac{v_{gs} - (-3)}{0.5}\right)$ and the compensation capacitance is $C_{comp}(v) = 0.5 + 0.4 \cdot \tanh\left(\frac{v - (-3)}{0.5}\right)$. When the MSM varactor is biased to -6 V, C_{total} equals $C_{total}(v_{gs}) = C_{gs}(v_{gs}) + C_{comp}(-6 - v_{gs}) = 1$.

4. Implementation

4.1. Fabrication

The device proposed in this study was fabricated on a 6 inch Si substrate through metal–organic chemical vapor deposition (MOCVD) and consisted of a 3 μm thick buffer layer, a 200 nm undoped GaN channel layer, a 1 nm AlN spacer layer, a 25 nm undoped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ layer, and a 3 nm GaN cap layer. The MSM varactors were co-fabricated alongside transistor devices, demonstrating their compatibility with HEMT technology. The devices were first processed with mesa insulation through Cl-based plasma etching, followed by a 60 °C TMAH surface pretreatment process to reduce GaN surface damage due to plasma etching and to achieve a better surface state [15]. Ohmic contacts were formed by annealing 20/50/150/80 nm Ti/Al/Ni/Au at 850 °C in N_2 for 45 s. A pre-gate, two-step treatment consisting of 1 min of low-power O_2 plasma and HCl wet etching was repeated three times to reduce the leakage current [16], followed by 20/200 nm Ni/Au gate metallization, 200 nm SiN_x passivation layer deposition through plasma-enhanced chemical vapor deposition (PECVD), and contact pad deposition. A multiple-finger MSM varactor structure was employed in this study to mitigate the transmission line effect arising from the use of metal pads [17].

4.2. Device Design

The MSM varactor, as shown in Figure 5, consists of two electrodes deposited on top of an AlGaIn/GaN structure. The fabricated MSM varactors are single-end devices with a G-S-G pad. The dimensions of the varactors can be described by four parameters, including the finger length (F_L), the finger width (F_w), the finger-to-finger spacing (d), and the number of fingers (N), as illustrated in Figure 5. A microphotograph of a fabricated MSM varactor is displayed in Figure 5.

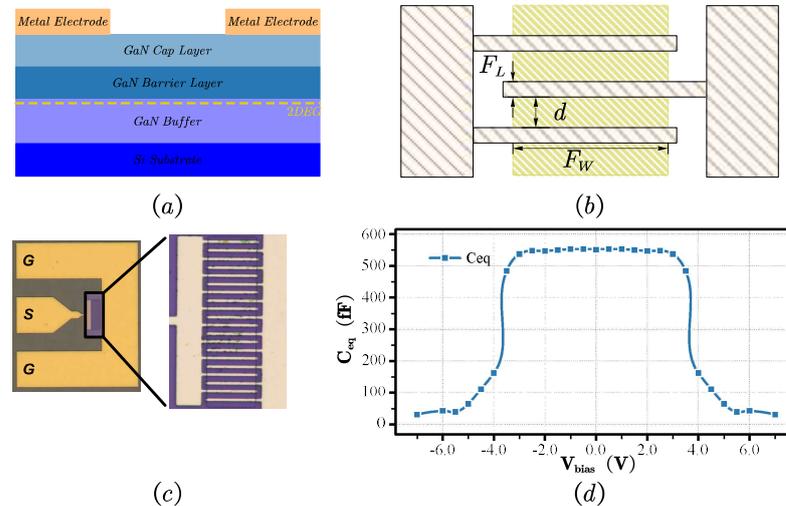


Figure 5. (a) The section of the epitaxy of MSM varactor; (b) the physical structure of the MSM varactors; (c) microphotograph of the MSM varactor; (d) the C-V characteristics of the MSM varactor with $F_L = 1.2 \mu\text{m}$, $F_w = 23 \mu\text{m}$, $d = 3 \mu\text{m}$, and $N = 10$.

The capacitance–voltage (C-V) characteristics are obtained using one-port S-parameter measurements up to 10 GHz obtained using a vector network analyzer (VNA). The measurements can be accurately fitted to a conventional varactor equivalent circuit with capacitance (C_{MSM}), parallel conductance (G_{MSM}), series resistance (R_{MSM}), and inductance (L_{MSM}) for frequencies within the measurement frequency range. This equivalent circuit is valid for the investigated electrode layouts across the entire measurement frequency range. Figure 5d illustrates the C-V characteristics of the MSM varactor. As shown in Figure 6a, Equation (3)

is used to fit the equivalent capacitance of the reverse-biased MSM varactor, where V_0 is -3.7 V and V_1 is 0.4 V.

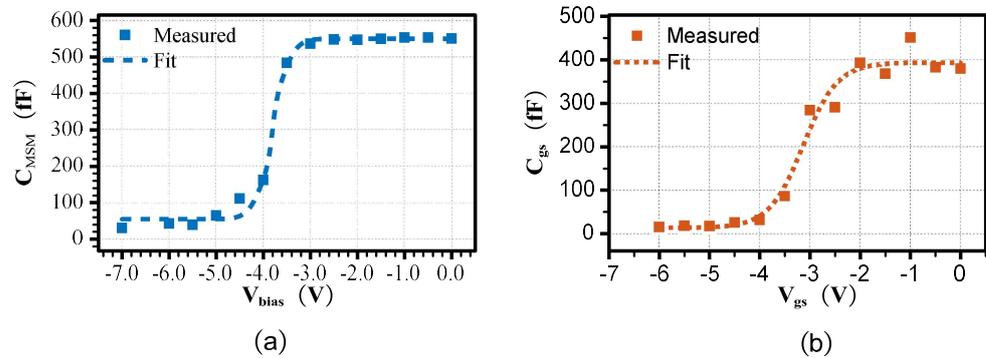


Figure 6. (a) The equivalent C-V characteristics of an MSM varactor with $F_L = 1.2 \mu\text{m}$, $F_w = 23 \mu\text{m}$, $d = 3 \mu\text{m}$, and $N = 10$. (b) C_{gs} - V_{gs} characteristics of the GaN HEMT with a $1.2 \mu\text{m}$ gate length and a $100 \mu\text{m}$ gate width.

Notably, the HEMT and MSM varactor both exhibit staircase patterns in terms of their C-V characteristics, as depicted in Figure 6. Specifically, Figure 6b highlights the behavior of the HEMT, and Equation (3) is used to fit the C_{gs} of the HEMT, where V_0 is -3 V and V_1 is 0.6 V.

As the compensated device, the capacitance of the unbiased MSM varactor should equal the maximum C_{gs} value of the device being compensated for. As shown in Figure 3b, the C_{gs} value of the GaN HEMT can be considered the depletion capacitance beneath the gate:

$$C_{gs} = \epsilon A_G \left(\frac{1}{d} + \frac{1}{d_{2DEG}} \right), \tag{4}$$

As shown in Figure 3a, the capacitance of the MSM varactor is given by [18]:

$$C_{MSM} = \frac{1}{2} \epsilon A_{MSM} \left(\frac{1}{d} + \frac{1}{d_{2DEG}} \right), \tag{5}$$

where d is the depth of the depletion region beneath the electrode influenced by the applied bias voltage, d_{2DEG} is the distance of the electrode to the 2DEG, A_G is the gate area of the HEMT, and A_{MSM} is the electrode area of MSM varactor. Within the same epitaxial layer and fabrication process, both d and d_{2DEG} are constants. To realize a linear input capacitance, the maximum capacitance of the MSM varactor and HEMT must be equal. Consequently, the electrode area of the MSM varactor produced with the same fabrication process should be twice the gate area of the HEMT.

The capacitance swing of the MSM varactor can be changed by manipulating the electrode geometry [14]. This is clearly demonstrated in Table 1 and Figure 7, which reveal the direct relationship between the capacitance of the MSM varactor and the electrode area ($N * F_w * F_L$). By appropriately adjusting the electrode area, the capacitance can be precisely controlled, allowing specific compensation requirements to be fulfilled.

Table 1. Summary of the key properties of the MSM varactor.

N	F_L (μm)	F_W (μm)	C_{min} (fF)	C_{max} (fF)	C_{max}/C_{min}
10	1.2	23	30	550	18.33
10	1.2	46	74.1	1160	15.65
20	1.2	23	154.8	1065	6.879
20	1.2	46	246.9	2170	8.788

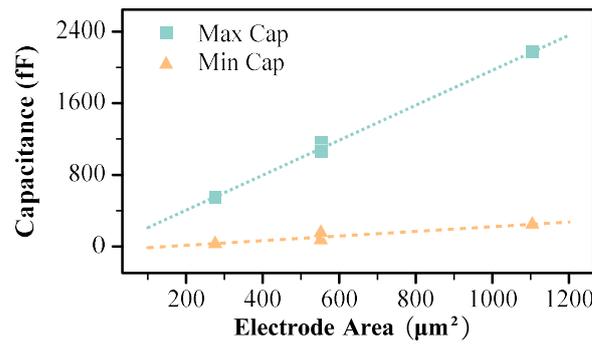


Figure 7. Measurement results for electrode area and capacitance characteristics.

Considering the distinct variations in the capacitance of the HEMT and MSM varactor at their respective bias voltages, the bias voltage (V_{MSM}) of the MSM varactor, as shown in Figure 8a, needs to be set as

$$V_{MSM} = V_0(HEMT) + V_0(MSM) \tag{6}$$

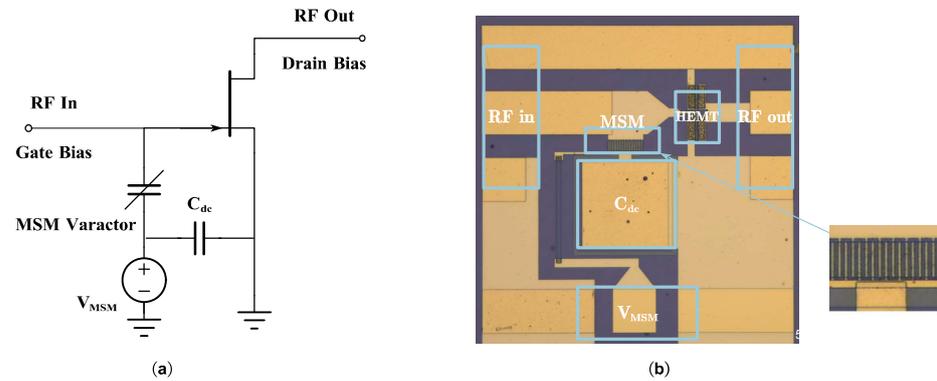


Figure 8. (a) Schematic of the proposed HEMT with a monolithic integrated MSM varactor. (b) Microphotograph of the prototype chip.

In the prototype, the HEMT gate length is 1.2 μm, and the width is 100 μm, while the connected MSM varactor includes an electrode with a width of 23 μm and a length of 1.2 μm and eight fingers. The ratio of the HEMT gate area to the MSM varactor electrode area is approximately 1:2. A schematic diagram and a microscope diagram are shown in Figure 8. Based on the test results depicted in Figure 6, the V_0 of the fabricated GaN HEMT and MSM varactor, C_{gs} , is estimated to be approximately −3 V, while the switching voltage of the MSM varactor is approximately −3.7 V. Therefore, the V_{MSM} should be adjusted to −6.7 V.

5. Measurement Results

In this section, the measurement results are presented to evaluate the effectiveness of the proposed compensation technique using MSM varactors to enhance the linearity of GaN HEMT PAs.

5.1. Small-Signal Measurements

The small signals of both the compensated and uncompensated devices were assessed using a VNA. The input capacitance is extracted from the small-signal S-parameters, which are measured under varied gate bias and a fixed drain bias of 12 V. Figure 9 shows a plot of the Port1-to-ground capacitance for both the compensated and uncompensated devices, obtained by calculating $Im\{y_{11} - y_{21}\}/\omega$. The difference in the maximum and minimum capacitance values of the fabricated prototype was significantly reduced, decreasing from

251 fF to 122 fF. The interdigital electrode structure of the MSM varactor caused parasitic capacitance, resulting in a capacitance difference of 122 fF. This result shows a substantial decrease in the overall capacitance variation at the amplifier's input after implementing the compensation technique involving MSM varactors.

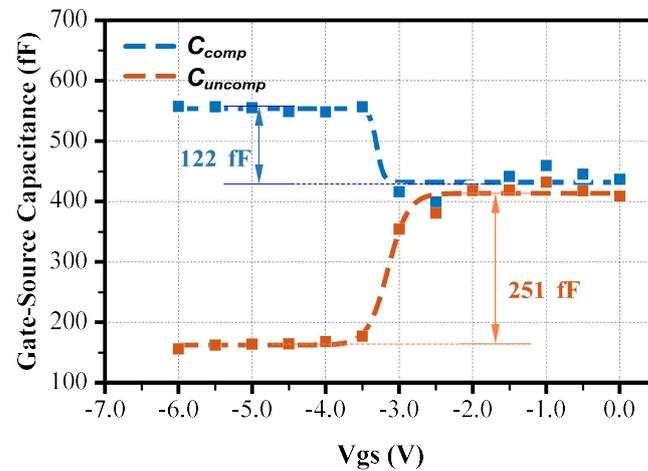


Figure 9. Measurement result of the Port1-to-ground capacitance for both devices.

5.2. Single-Tone RF Power Measurement

The RF power characteristics of the device were measured using a load-pull measurement system. The experimental setup for the CW measurements is shown in Figure 10. The CW input signal is generated by a signal source (R&S SMB-100A). The bias point selection aims to minimize changes in the source impedance of the load-pull system during the test and eliminate the influence of the source impedance on the AM-PM results. The same load impedance ($\Gamma = 0.782$, Phase = 2 deg) and source impedance ($\Gamma = 0.671$, Phase = 21.5 deg) values were used in all tests. The source impedance is chosen to balance the gain of both devices, and the load impedance is the maximum of the output power. The PA output is monitored by a VNA and Spectrum Analyzer to test the PA gain/power response and AM-PM distortion. Figure 10 presents the single-tone power characteristics for both the compensated and uncompensated devices at a frequency of 1 GHz, with $V_d = 12$ V and $V_{gs} = -2$ V, where $I_d = 20\%$ of I_{dss} . The compatibility of the HEMT with a range of bias voltages was examined by evaluating adjacent bias points within the ± 0.1 V range. The test results demonstrate the effectiveness of this compensation within the appropriate bias voltage range.

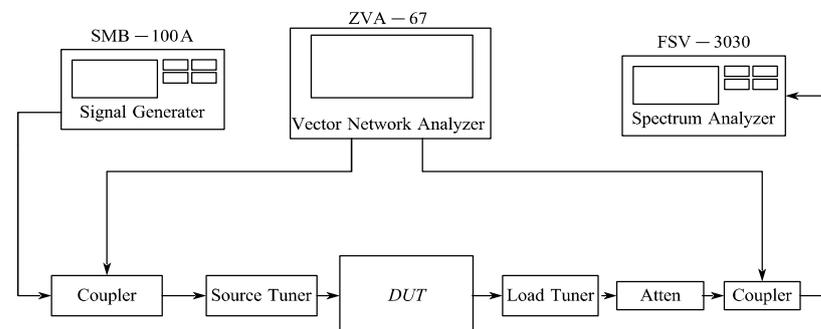


Figure 10. CW measurement setup.

PAs are first characterized using CW signals. The saturated output power (P_{sat}), power-added efficiency (PAE), gain, and AM-PM distortion are measured under the same load impedance ($\Gamma = 0.782$, Phase = 2 deg) and source impedance ($\Gamma = 0.671$, Phase = 21.5 deg).

Figure 11 shows the measured gain and power-added efficiency (PAE) of the two devices. As it can be seen, the uncompensated device achieves a small signal gain of 15.5 dB and a peak PAE of 49.7% at the output power of 18 dBm; the compensated device achieves similar PAE performance but with a gain that is 0.2 dB lower than the uncompensated device. This reduced gain is attributed to the increased input capacitance associated with the compensation scheme. The output power and PAE at the 3 dB compression point for the uncompensated and compensated devices are 43.9% at 15.3 dBm and 44.6% at 15.2 dBm, respectively.

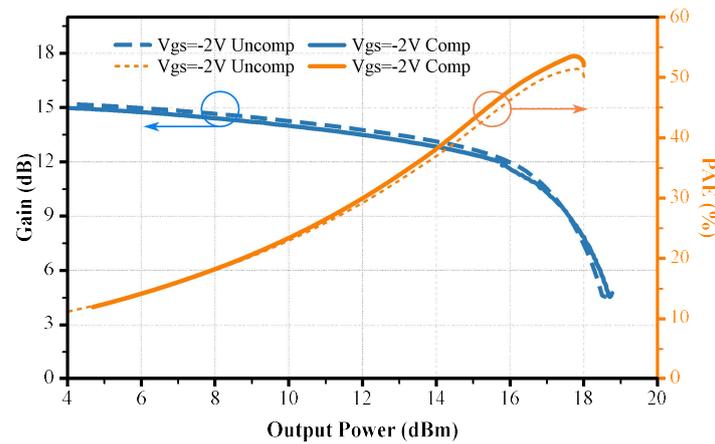


Figure 11. Measurement results for single-tone characteristics.

Figure 12a illustrates the AM–PM of the compensated and uncompensated devices at 1 GHz with $V_{gs} = -2$ V. The compensated device exhibits an AM–PM distortion of less than 1.3 degrees up to an output power of 18 dBm (approximately 5 dB compression point). On the other hand, the uncompensated device shows an AM–PM distortion exceeding 2.7 degrees at the same output power. As shown in Figure 11, the impact on the AM–AM conversion is minor because the frequency is much lower than the cut-off frequency of the input RC network [19].

Figure 12b,c demonstrate the impact of the proposed compensation scheme on AM–PM distortion. For the compensated device, at -1.9 V V_{gs} , the AM–PM distortion is reduced to 1.7 degrees, and at -2.1 V V_{gs} , the AM–PM distortion is only 2 degrees. Conversely, the uncompensated device exhibits AM–PM distortions of 4.3 degrees and 4.1 degrees at the same gate–source voltages. Thus, the input capacitance compensation scheme significantly reduces AM–PM distortion. Despite the application of compensation techniques, importantly, AM–PM distortion persists and is not eliminated. This residual distortion can be attributed to other nonlinear components, including C_{gd} and nonlinear g_m .

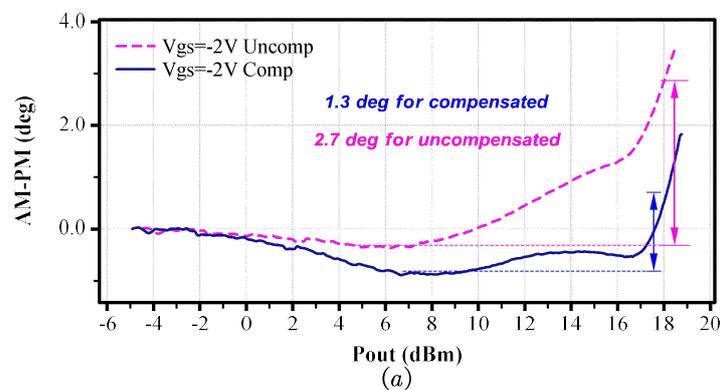


Figure 12. Cont.

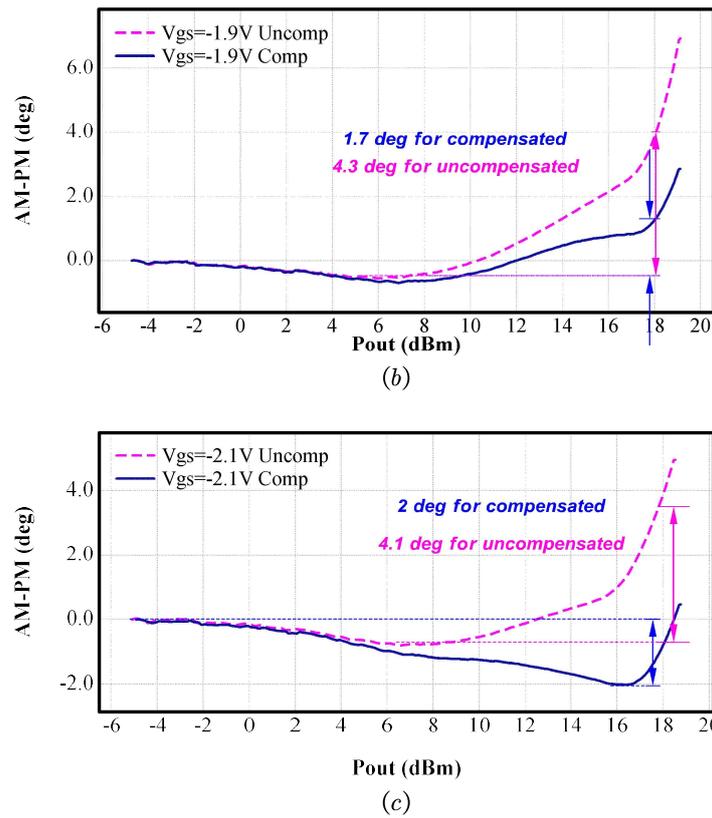


Figure 12. Measurement results for AM–PM characteristics at different gate bias (a) $V_{gs} = -2$ V (b) $V_{gs} = -1.9$ V (c) $V_{gs} = -2.1$ V.

5.3. Two-Tone Measurement

To verify the linearity of the performance, the device was tested under a fixed bias and various input powers using a two-tone signal. The two-tone measurement is performed at a fundamental frequency (f_0) of 1 GHz, with a spacing of 10 MHz (Δf), using the same bias conditions as in the single-tone measurement ($V_{gs} = -2$ V and $V_{ds} = 12$ V). The results of these measurements are depicted in Figure 13. Figure 13 reveals a notable improvement of at least 3 dB when the output power is less than 12 dBm in each tone and 5 dB in the small-signal region. AM to PM distortion effects can contribute significantly to IM products in the pre-compression zone, and AM–AM dominates IMD3 distortion when gain compression is increased [9]. This improvement in the pre-compression area highlights the enhanced linearity and reduced distortion of the proposed device when presented with modulation signals.

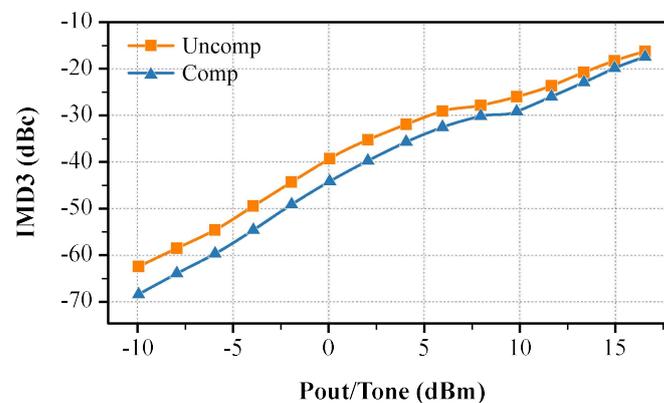


Figure 13. Measurement IMD3 result of the device versus the output power at $V_{gs} = -2$ V and $V_{ds} = 12$ V. The center frequency is 1 GHz for a two-tone spacing of 10 MHz.

6. Conclusions

This study presents a nonlinear capacitance compensation technique to enhance the linearity of GaN HEMT PAs. By reducing the overall capacitance variation at the amplifier input, the AM–PM linearity was improved. The experimental results obtained with a prototype amplifier developed utilizing a standard GaN HEMT process and implementing the proposed technique demonstrated linear enhancements in both two-tone IMD3 and AM–PM conversion. This study provides new linearization tools for GaN-based PAs. These results suggest the novelty of the proposed approach for achieving input capacitance compensation in GaN PAs, allowing convenient integration into GaN processes. The potential of the MSM varactor has been extensively investigated, revealing novel possibilities for its utilization in high-linear amplifiers. This advancement offers substantial benefits that facilitate its extensive integration into wireless communication systems and radar systems.

Author Contributions: Conceptualization, K.L., H.G. and X.Z.; methodology, K.L.; software, K.L.; validation, K.L. and H.G.; formal analysis, K.L.; investigation, K.L. and H.G.; resources, K.L. and Y.G.; data curation, K.L.; writing—original draft preparation, K.L.; writing—review and editing, K.L., Y.G. and H.G.; supervision, X.Z.; funding acquisition, X.Z. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by ShanghaiTech University Startup Fund 2017F0203-000-14, the National Natural Science Foundation of China (Grant No. 52131303), the Natural Science Foundation of Shanghai (Grant No. 22ZR1442300), and, in part, the CAS Strategic Science and Technology Program under Grant No. XDA18000000. The authors would also to sincerely thank to ShanghaiTech University Platform of Mechatronics, Energy, and Electronic Devices for equipment support.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

References

- Inoue, A. Millimeter-Wave GaN Devices for 5G: Massive MIMO Antenna Arrays for Sub-6-GHz and Mm-Wave Bandwidth. *IEEE Microw. Mag.* **2021**, *22*, 100–110. [[CrossRef](#)]
- Campbell, C.; Lee, C.; Williams, V.; Kao, M.-Y.; Tserng, H.-Q.; Saunier, P.; Balisteri, T. A Wideband Power Amplifier MMIC Utilizing GaN on SiC HEMT Technology. *IEEE J. Solid-State Circuits* **2009**, *44*, 2640–2647. [[CrossRef](#)]
- van Heijningen, M.; de Hek, P.; Dourlens, C.; Fellon, P.; Adamiuk, G.; Ayllon, N.; van Vliet, F. C-Band Single-Chip Radar Front-End in AlGaIn/GaN Technology. *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 4428–4437. [[CrossRef](#)]
- Mengozzi, M.; Gibiino, G.P.; Angelotti, A.M.; Florian, C.; Santarelli, A. GaN Power Amplifier Digital Predistortion by Multi-Objective Optimization for Maximum RF Output Power. *Electronics* **2021**, *10*, 244. [[CrossRef](#)]
- Joo, T.; Koo, B.; Hong, S. A WLAN RF CMOS PA with Large-Signal MGTR Method. *IEEE Trans. Microw. Theory Tech.* **2013**, *61*, 1272–1279. [[CrossRef](#)]
- Cai, Q.; Che, W.; Ma, K.; Zhang, M. A Simplified Transistor-Based Analog Predistorter for a GaN Power Amplifier. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *65*, 326–330. [[CrossRef](#)]
- Lim, K.H.; Ahn, G.; Jung, S.; Park, H.C.; Kim, M.S.; Van, J.H.; Cho, H.; Jeong, J.-H.; Park, C.-S.; Yang, Y. A 60-W Multicarrier WCDMA Power Amplifier Using an RF Predistorter. *IEEE Trans. Circuits Syst. II Express Briefs* **2009**, *56*, 265–269. [[CrossRef](#)]
- Wang, C.; Vaidyanathan, M.; Larson, L.E. A Capacitance-Compensation Technique for Improved Linearity in CMOS Class-AB Power Amplifiers. *IEEE J. Solid-State Circuits* **2004**, *39*, 1927–1937. [[CrossRef](#)]
- Vigilante, M.; Reynaert, P. A Wideband Class-AB Power Amplifier With 29–57-GHz AM–PM Compensation in 0.9-V 28-Nm Bulk CMOS. *IEEE J. Solid-State Circuits* **2018**, *53*, 1288–1301. [[CrossRef](#)]
- Cripps, S.C. *RF Power Amplifiers for Wireless Communications*; Artech House Publishers: Norwood, MA, USA, 2006.
- Nunes, L.C.; Cabral, P.M.; Pedro, J.C. AM/AM and AM/PM Distortion Generation Mechanisms in Si LDMOS and GaN HEMT Based RF Power Amplifiers. *IEEE Trans. Microw. Theory Tech.* **2014**, *62*, 799–809. [[CrossRef](#)]
- Golara, S.; Moloudi, S.; Abidi, A.A. Processes of AM-PM Distortion in Large-Signal Single-FET Amplifiers. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 245–260. [[CrossRef](#)]
- Marso, M.; Wolter, M.; Javorka, P.; Fox, A.; Kordoš, P. AlGaIn/GaN Varactor Diode for Integration in HEMT Circuits. *Electron. Lett.* **2001**, *37*, 1476. [[CrossRef](#)]
- Marso, M.; Fox, A.; Heidelberger, G.; Kordos, P.; Luth, H. Comparison of AlGaIn/GaN MSM Varactor Diodes Based on HFET and MOSHFET Layer Structures. *IEEE Electron Device Lett.* **2006**, *27*, 945–947. [[CrossRef](#)]
- Yoon, Y.J.; Seo, J.H.; Cho, M.S.; Kang, H.-S.; Won, C.-H.; Kang, I.M.; Lee, J.-H. TMAH-Based Wet Surface Pre-Treatment for Reduction of Leakage Current in AlGaIn/GaN MIS-HEMTs. *Solid-State Electron.* **2016**, *124*, 54–57. [[CrossRef](#)]

16. Lu, X.; Jiang, H.; Liu, C.; Zou, X.; Lau, K.M. Off-State Leakage Current Reduction in AlGa_N/Ga_N High Electron Mobility Transistors by Combining Surface Treatment and Post-Gate Annealing. *Semicond. Sci. Technol.* **2016**, *31*, 055019. [[CrossRef](#)]
17. San Chu, C.; Zhou, Y.; Chen, K.J.; Lau, K.M. Q-Factor Characterization of RF Ga_N-Based Metal-Semiconductor-Metal Planar Interdigitated Varactor. *IEEE Electron Device Lett.* **2005**, *26*, 432–434. [[CrossRef](#)]
18. Hsieh, Y.-L.; Lo, H.-Z.; Nee, T.-E.; Chang, C.-N.; Yang, C.-H. Study on Epitaxial Structure and Substrate Material Variations for Improving Electrical Reliability of the MSM AlGa_N/Ga_N 2DEG Varactors. *Microelectron. Reliab.* **2023**, *142*, 114905. [[CrossRef](#)]
19. Sarbishaei, H.; Wu, D.Y.-T.; Boumaiza, S. Linearity of Ga_N HEMT RF Power Amplifiers—A Circuit Perspective. In Proceedings of the 2012 IEEE/MTT-S International Microwave Symposium Digest 2012, Montreal, QC, Canada, 17–22 June 2012. [[CrossRef](#)]

Disclaimer/Publisher’s Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.