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Improved Quasi-Z-Source High Step-Up DC–DC Converter Based on Voltage-Doubler Topology

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Abstract: The step-up DC–DC converter is widely used for applications such as IoT sensor nodes, energy harvesting, and photovoltaic (PV) systems. In this article, a new topological quasi-Z-source (QZ) high step-up DC–DC converter for the PV system is proposed. The topology of this converter is based on the voltage-doubler circuits. Compared with a conventional quasi-Z-source DC–DC converter, the proposed converter features low voltage ripple at the output, the use of a common ground switch, and low stress on circuit components. The new topology, named a low-side-drive quasi-Z-source boost converter (LQZC), consists of a flying capacitor (C_F), the QZ network, two diodes, and a N-channel MOS switch. A 60 W laboratory prototype DC–DC converter achieved 94.9% power efficiency.

Keywords: high step-up DC–DC converter; quasi-Z-source; voltage-doubler; high-side driver free; low voltage stress

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1. Introduction

Step-up DC–DC converters are widely used for applications that require high voltage converted from low input voltage, such as energy harvesting systems [1,2], IoT node operating systems on low-voltage battery cells [3], and photovoltaic (PV) systems for grid connection [4–6]. Although the necessary power and voltage for application is different, the same dc–dc converter topology is applicable and effective to these applications. The basic boost converter (BBC) is an established technique with a long history by which CR is determined by CR = 1/(1–D), where D is duty cycle. However, it has difficulty of control at high duty cycle when the duty ratio increases because of its nonlinear characteristics and narrow pulse width [7]. In addition, it suffers from the voltage stress on the semiconductor switches and conduction loss that is due to the long ON status of the switches during period D to hold the high CR status. Of course, the high CR can be simply obtained by the series connection of BBC, but it increases loss, cost, and volume; therefore, it is not smart option. To overcome these obstacles, alternative types of high step-up dc–dc converters have been proposed [8–10]. There are two approaches to achieve the high CR; one is the isolated type and the other is the non-isolated type. The isolated type obtained the high voltage by changing the secondary and primary turn ratios of the transformers. However, it produces inductor leakage and the necessity for the custom-made transformer, which additionally often requires measurements of unknown key electric and magnetic parameters. In addition, the bulky equipment is not suitable for the harvesting system and IoT node operation system. On the other hand, non-isolated converters are suitable for these applications because of both volume and cost. In this category, there are some promising converters introduced. R-J. Wai et al. [11], S-M. Chen et al. [12], and H-C. Liu et al. [13] proposed a coupled inductor type. However, it required the snubber circuits to suppress the leakage of inductors. In addition, the coupled inductors are not off-the-shelf components—the same as the transformer. Recently, a quasi-Z-source network has been installed in

DC–DC converters [14–24]. Z-source networks typically consist of two inductors, two capacitors, and a diode that are connected to each other. Originally, Z-source networks were used for inverters to suppress shoot-through problems. L. Yang. et al. [14,15] applied the quasi-Z-source networks to the DC–DC converters. After that, several Z-source-type DC–DC converters were introduced. However, there are some drawbacks in previously introduced QZ DC–DC converters, such as low CR [14–16], an uncommon GND between input and output voltage [19,20,23], and complex implementation [18,21,22]. M. Veerachary et al. proposed the QZ boost converter [17], called a sixth-order quasi-Z-source DC–DC converter (SOQZCS). The achieved CR of the converter was (2–2D)/(1–2D). The operating duty cycle D is less than 0.5 to avoid narrow pulse-width control in the common GND configuration by simple implementation. However, it suffers from a large output ripple, requiring level shift circuits for the high-side switch, and high-voltage stress on circuit components. To eliminate these drawbacks, we reported a new QZ DC–DC converter [24].

Generally, a PV system has two approaches to connect the grid called DC-module type and AC-module type [25,26]. Since the output voltage of the one PV panel is small, that is from 15 V to 40 V [12], the DC-module type connects PV panels in series to build up the DC voltages for ensuring the grid voltage. However, the DC-module type has a drawback in principle for a partial shadow problem. When one PV panel is shadowed by obstacles such as clouds, leaves, and birds, the PV current becomes weak and the other series-connected PV-string currents are also weakened because they connect in series with each other. So, some avoiding methods are required [26]. On the other hand, the AC-module type connects the PV panels in parallel, and the partial shadow problem does not occur. However, instead, the AC-module type requires the high step-up DC–DC converter to ensure grid-connect voltage from the low output voltage of the one PV panel. The conventional AC-module installed BBC, so the aforementioned problems exist. A DC–DC converter for a PV system requires the following characteristics: the low input current for maximum point tracking (MPPT) control, low voltage stress at high step-up status, high efficiency, low cost, and reliability.

In general, to connect to the AC grid from the PV panels, an inverter circuit is inserted between the PV output and the grid to convert voltage from DC to AC. To the input terminal of the inverter, an electrolytic capacitor is connected to suppress the voltage ripple. The electrolytic capacitors are the most-aging components in the electric instruments, and they inflate the aging speed by their input voltage ripple. Of course, the electrolytic capacitor is a possible replacement of the film-type capacitor; however, the capacitance value of film-type capacitance is smaller and more expensive than the electrolytic capacitor. Therefore, the input voltage of the ripple is a significant parameter for the inverter from the viewpoint of cost and reliability. The proposed converter features high CR, low output voltage ripple, and low voltage stress for both semiconductor devices and flying capacitor, and is free from the high-side level shifter. A previously submitted paper [24] introduced the fundamental idea, the theoretical consideration, and the simulation results using a simulator. However, all elements used in the simulator are ideal elements. For example, the on resistance of transistor M, the parasitic resistance of inductor L, and the equivalent series resistance (ESR) of capacitor C are ignored. In addition, input voltage V_g and the output resistance R_o are ideal. So, the efficiency of the DC–DC converter was not evaluated. In this paper, we developed an actual 60 W laboratory prototype of the proposed DC–DC converter.

The operational principle is summarized in Section 2 and the topology comparison between [17] and LQZC are discussed in Section 3. Shown in the components selection, Section 4, are the measurement results of the conversion rate (CR), the measurement waveforms, and the measurement results of the efficiency. The measurement set-up and experimental results are shown in Section 4, and how the parasitic resistance of inductor R_{DC} affects the CR is considered theoretically and verified by a simulator in Section 5, and, finally, this work concludes in Section 6.

2. Circuits of the Proposed High Step-Up Converter

Figure 1a shows the proposed converter. The surrounded dot-line is a QZ network. It operates in two modes, Mode1 and Mode2.

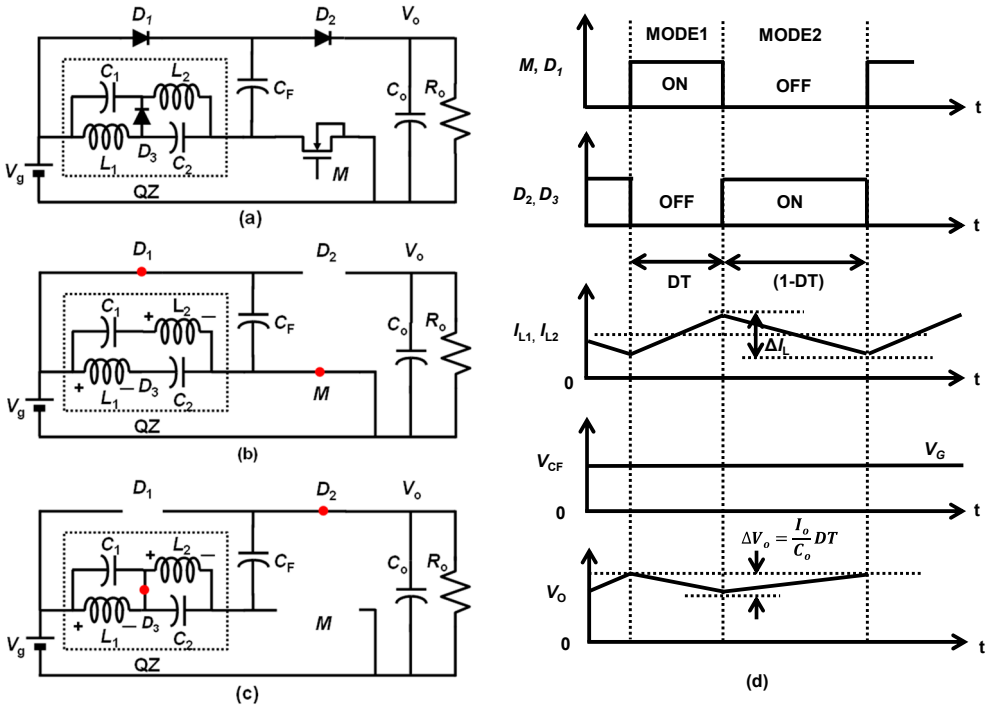


Figure 1. (**a**) Proposed high step-up DC–DC converter (LQZC). (**b**) Mode1 operation. (**c**) Mode2 operation [24]. (**d**) Key waveforms. Reprinted/adapted with permission from Ref. [24]. Copyright 2022, IEICE.

Mode1: The equivalent circuit for this mode of operation is depicted in Figure 1b. The diode D_1 and transistor M are turned ON and the diode D_2 and D_3 are turned OFF during this operation. The red circles denote the ON state of the switch transistor and diodes. Applying KVL to the closed loops, the following equations are obtained:

$$V_{\mathrm{g}} - V_{\mathrm{L1}} + V_{\mathrm{C2}} = 0 \tag{1}$$

$$V_{\mathrm{g}} + V_{\mathrm{C2}} - V_{\mathrm{L2}} = 0 \tag{2}$$

$$V_{\mathrm{CF}} = V_{\mathrm{g}} \tag{3}$$

Mode2: The equivalent circuit for this mode of operation is depicted in Figure 1c. The D_2 and D_3 are turned ON and diode D_1 and transistor M are turned OFF during this operation. Applying KVL to the closed loops, the following equations are obtained:

$$V_{\mathrm{L1}} = -V_{\mathrm{C1}} \tag{4}$$

$$V_{\mathrm{L2}} = -V_{\mathrm{C2}} \tag{5}$$

$$V_{\mathrm{g}} + V_{\mathrm{C1}} + V_{\mathrm{C2}} + V_{\mathrm{CF}} = V_{\mathrm{o}} \tag{6}$$

Applying the volt-second balance to inductor L_1 using Equations (1) and (4), assume $\mathrm{C}_1 = \mathrm{C}_2$:

$$(V_{\mathrm{C2}} + V_{\mathrm{g}})\mathrm{D} - V_{\mathrm{C1}}(1 - \mathrm{D}) = 0 \tag{7}$$

$$V_{\mathrm{C1}} = \frac{\mathrm{D}(V_{\mathrm{C2}} + V_{\mathrm{g}})}{1 - \mathrm{D}} \tag{8}$$

$$V_{C1} = V_{C2} = \frac{DV_g}{1-2D} \tag{9}$$

By substituting Equation (9) for Equation (6), and using Equation (3), V_o/V_g was obtained as follows:

$$\frac{V_o}{V_g} = \frac{2-2D}{1-2D} \tag{10}$$

Equation (10) shows the same CR (=V_o/V_g) as obtained by [17].

Figure 1d shows the key waveforms.

Figure 2 shows the CR of the BBC and the proposed converter. To eliminate narrow pulse-width control difficulty, the conventional converter [17] and the proposed converter [24] are designed to operate in a range from 0 to 0.5 of D, unlike BBT. The CR of Conv. [17] and Prop. [24] is obtained as 6.00 but that of BBT [7] becomes only 1.67 at D = 0.4.

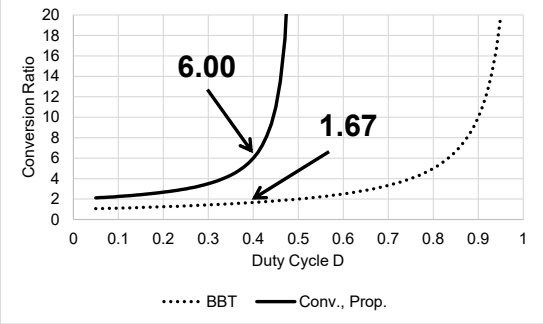


Figure 2. CR of BBC [7] and Conv. [17], Prop. [24] converters.

3. Topology Comparison of Converters

In this section, the topology difference between the conventional converter and proposed converter is described. Figure 3 shows the three converters. Figure 3a shows the voltage-doubler [27]. Figure 3b,c are the Mode1 and Mode2 operations of it, respectively. Figure 3d shows a conventional converter [17]. Figure 3e,f are the Mode1 and Mode2 operations of it, respectively. Figure 3g shows the proposed converter [24]. Figure 3h,i are the Mode1 and Mode2 operations of it, respectively. The conventional converter topology can be regarded as the QZ replaced from the S_4 in the voltage doubler. Considering other variations, we found the new topology, as shown Figure 3g. The proposed converter can be regarded as the QZ replaced from the S_3 in the voltage doubler. By this modification, the proposed converter improved the output ripple, power loss, and voltage stress.

3.1. Output Voltage Ripple

The output voltage of the proposed converter is significantly reduced compared to the converter. The droop voltage of the output comes up when the output capacitor C_o disconnects the source voltage V_g. This situation occurs in Mode2 in the conventional converter that is shown in Figure 3f. Since the output capacitor C_o connects to only the load current I_o, the output voltage V_o droops at the rate determined by $V_o = (C_o/I_o)$ t. As the high step-up DC–DC converter operates generally less than D = 0.5, the period of the operation time of Mode2 shown Figure 3f is longer than that of Mode1 shown Figure 3d. On the other hand, in the proposed converter, the period of time disconnected from source voltage V_g occurs in Mode1, as shown Figure 3h. This advantage results in that low EMI and the available small-output capacitor.

3.2. High Side Driver and Level Shifter

The switch S_3 in Figure 3d is given by the N-channel MOS transistor [17], where the drain terminal of the N-channel MOS transistor is connected to V_g and the source terminal is connected to QZ. It means that this is necessary for the high-side driver and the level shift

circuits for S_3. The level shift circuits consume operating power, and some additional circuits are required for proper start-up of the DC–DC converter. In contrast, The LQZC is high-side driver-free because the source terminal of S_4 is terminated to GND, as shown in Figure 3g. It can improve the efficiency and reduce the cost and complex design of the converter.

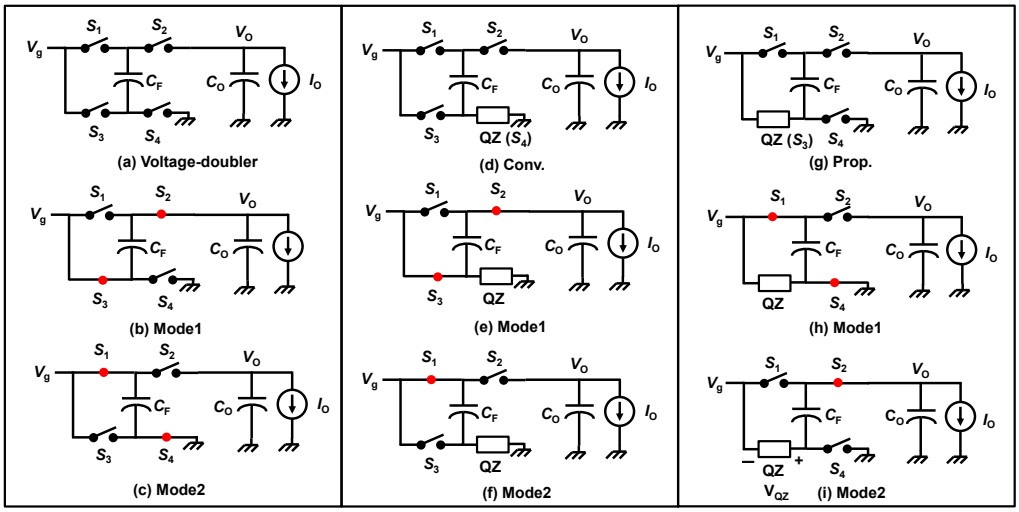


Figure 3. Comparison of converters: (**a**) voltage doubler, (**b**) Mode1 of voltage doubler, (**c**) Mode2 of voltage doubler, (**d**) Conv., (**e**) Mode1 of Conv., (**f**) Mode2 of Conv., (**g**) Prop., (**h**) Mode1 of Prop., and (**i**) Mode2 of the Prop. Reprinted/adapted with permission from Ref. [24]. Copyright 2022, IEICE.

3.3. Voltage Stress

The proposed converter provides the reduction in voltage stress for the flying capacitor C_F. The voltage stress of elements is shown in Table 1. In a conventional converter, the terminals of C_F are applied by V_o and V_g as shown in Figure 3e. Using Equation (10), the terminal voltage across C_F becomes:

$$V_o - V_g = \frac{2-2D}{1-2D}V_g - V_g = \frac{1}{1-2D}V_g \tag{11}$$

Table 1. Voltage stress of components.

Components	Conv.	Prop.
D_1, D_2	$V_O - V_g$	$V_O - V_g$
M	$\frac{1}{1-2D}V_g$	$\frac{1}{1-2D}V_g$
C_1, C_2	$\frac{D}{1-2D}V_g$	$\frac{D}{1-2D}V_g$
C_F	$\frac{1}{1-2D}V_g$	V_g

In contrast, the voltage stress of the C_F applied only V_g. The voltage across C_F is determined as follows:

$$V_o - \left(V_g + V_{QZ}\right) = V_o - \left(V_g + V_{C1} + V_{C2}\right) = V_o - \left(V_g + \frac{2D}{1-2D}V_g\right) = V_o - \frac{1}{1-2D}V_g = V_g \tag{12}$$

This is obvious from Figure 3h and Equation (3). Consequently, the proposed converter can mitigate the voltage stress of C_F. The stress voltages of other elements, D_1, D_2, M, C_1, and C_2, are same as those of a conventional converter [17].

4. Measurement Setup and Results

4.1. Measurement Setup

Figure 4 shows a photograph of the prototype. The values of the components and the part numbers are listed in Table 2. Here all capacitors are film type.

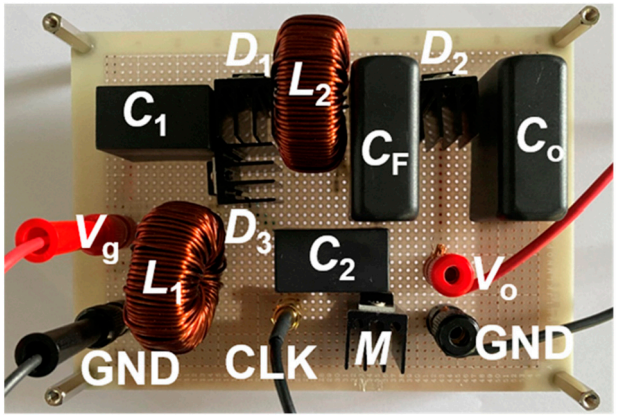


Figure 4. Photograph of prototype.

Table 2. Components specification.

Components	Values and Main Parameters	Parts No.
L_1, L_2	1 mH, 5 A, R_{DC} = 111 mΩ	TAMURA NAC-06-1001
C_1, C_2	10 uF, I_{RMS} = 7 A, ESR = 10 mΩ	VIHSAY MKP1848C61050JK2
C_F, C_O	20 uF, I_{RMS} = 8 A, ESR = 9 mΩ	VIHSAY MKP1848C62050JP2
D_1, D_2, D_3	300 V, 3 A, V_F = 1.66 V	POWER INTEGRATIONS LQA30T300
M	650 V, $I_{D,\,CNT}$ = 12 A_{MAX}, 190 mΩ	INFINEON IPP65R190CFD7

Figure 5 shows the block diagram of the measurement set-up. The clock frequency f_{CLK} is set to 100 kHz for all measurements. The duty cycle D is changed from 0.05 to 0.35 by function generator Textronix AFG3120. The drive voltage amplitude for the transistor M is set to 10 V. The input voltage V_g is set to 20 V, 30 V, and 40 V. The output voltage V_o connected the electric current load Array 3710 A, of which the output resistance R_o is set from 175 Ω to 500 Ω. The electrolytic capacitor C_{IN}, 470 uF (200 V), is connected between the V_g and GND as an input filter. The waveform of the output voltage V_o and the flying capacitor C_F are measured by a high-voltage differential probe, Textronix P5200A, on 50:1 attenuation, and the inductor current I_{L1} is measured by the current probe Textronix P6021A. The input voltage V_g and clock signal CLK are measured by the passive probe Textronix TPP0250 on 10:1 attenuation.

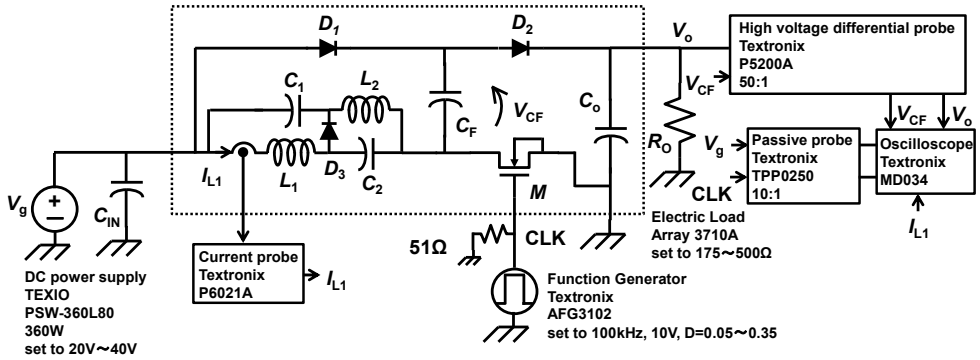
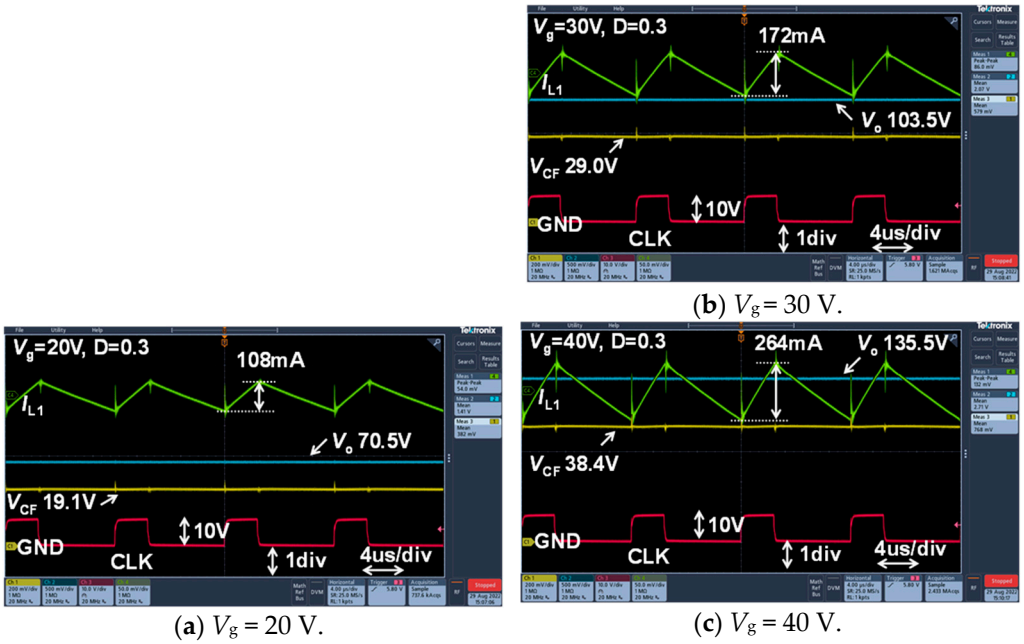


Figure 5. Measurement set-up.

4.2. Measurement Results

Figure 6 shows the steady-state measurement waveforms of I_{L1}, V_o, V_{CF}, and CLK when D = 0.3 and R_o = 500 Ω, and set to V_g = 20 V, 30 V, and 40 V, respectively.



(**a**) V_g = 20 V. (**b**) V_g = 30 V. (**c**) V_g = 40 V.

Figure 6. Experimental waveforms. Green line: I_{L1}. Blue line: V_o. Yellow line: V_{CF}. Red line: CLK.

Figure 7 shows the relationship between the measured output voltage V_o and duty cycle D drawn together with the calculated gain by the dotted lines. The duty cycle D changed from 0.05 to 0.35 for input voltage V_g = 20 V, 30 V, and 40 V, respectively, on R_o = 500 Ω. The measurement results agree well with the calculated results. When the duty cycle D is small, the output voltage V_o is slightly low because of the forward voltage V_F of D_1.

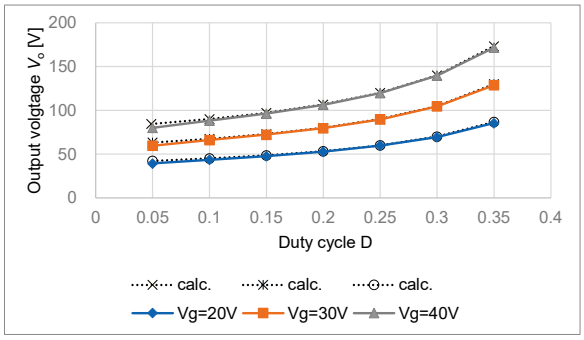


Figure 7. Output voltage V_o and duty cycle D.

Figure 8 depicts the relationship between the output power P_o and the efficiency η using the data of Figure 7. Figure 9 shows the efficiency versus the output power P_o at V_g = 40 V and D = 0.2 when R_o varies from 500 Ω to 175 Ω by 25 Ω steps. The peak efficiency 94.9 % is obtained. Table 3 summarizes the performance comparison of Conv. [17] and this work.

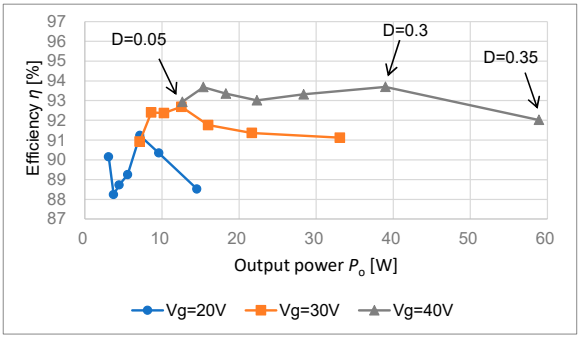


Figure 8. Efficiency η using data of Figure 7.

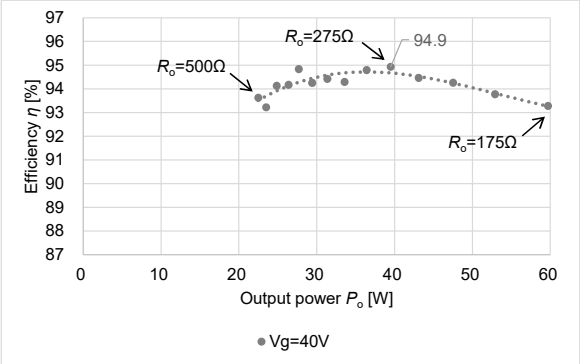


Figure 9. Peak efficiency η.

Table 3. Performance summaries.

Items	M. Veerachary ICSETS 2019 [11]	This Work
CR	$\frac{2-2D}{1-2D}$	$\frac{2-2D}{1-2D}$
Output Voltage Ripple	$\frac{V_O}{C_O}(1-D)T$	$\frac{V_O}{C_O}DT$
Voltage Stress of C_F	$\frac{1}{1-2D}V_g$	V_g
High Side Driver and Level Shifter	Necessary	Unnecessary
Efficiency	N/A	94.9%

5. Discussion

In this section, the effect of the parasitic element of the proposed converter is discussed. Generally, the equivalent series resistance (ESR) of the capacitors is relatively smaller than the DC resistance (R_{DC}) of the inductor [28–30]. So, we focus on the parasitic element of the inductors. Figure 10 shows the proposed converter, which includes the parasitic resistance depicted by the blue resistor symbol.

Considering the steady-state condition, the average current through a capacitor operating in a periodic steady state is zero and the average current through an inductor operating in a periodic steady state is zero [7]; therefore, the average inductor current I_{L1} can be written as follows.

$$I_{L1} = I_g - I_o \tag{13}$$

By substituting Equation (10) with Equation (13) and using $V_gI_g = V_oI_o$, the following equation is obtained.

$$I_{L1} = \left(\frac{V_o}{V_g} - 1\right) I_o = \frac{1}{1-2D} I_o \tag{14}$$

Equation (14) indicates that the inductor current I_{L1} is larger than the output current I_o. For example, $I_{L1} = 5I_o$ when D = 0.4 and $I_{L1} = 1.67I_o$ when D = 0.2. This means that the

equivalent series resistance (R_{DC}) of inductors affects the efficiency of the converter and CR, too. Here, we focus on how much the CR is affected by the R_{DC} of L_1 and L_2.

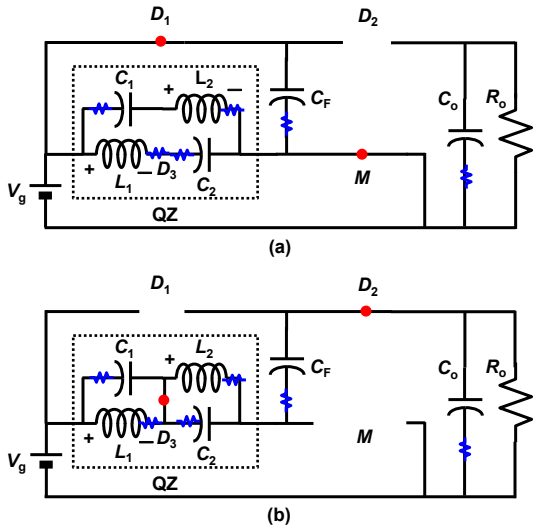


Figure 10. Proposed high step-up DC–DC converter (LQZC) with parasitic resistances. (**a**) Mode1. (**b**) Mode2.

In Mode1, the voltage expressions obtained using KVL are:

$$V_g - V_L - V_r + V_C = 0 \tag{15}$$

where $V_r = R_{DC} \times I_L$.

In Mode2, the voltage expressions obtained using KVL are:

$$-V_L - V_r - V_C = 0 \tag{16}$$

Applying the volt–second balance to inductor L:

$$(V_g + V_C - V_r)D - (V_C + V_r)(1 - D) = 0 \tag{17}$$

$$V_C = \frac{DV_g - V_r}{1 - 2D} \tag{18}$$

Compared to Equation (9), Equation (18) indicates that when the voltage of capacitor V_c is reduced by V_r, it results in reducing V_o. This is attributed to the voltage across inductors V_L being reduced in Mode1 by R_{DC}.

By substituting Equation (18) for Equation (6), $V_{CF} = V_g$, V_o/V_g is obtained as follows:

$$\frac{V_o}{V_g} = \frac{2 - 2D}{1 - 2D} - \frac{2V_r}{(1 - 2D)V_g} \tag{19}$$

To verify Equation (19), the output voltage V_o was checked by the PSIM [30] simulator when conditions changed. In the simulator circuit, the output resistance R_o is set to 100Ω, and R_{DC} are added to L_1 and L_2, respectively, in Figure 11. In this situation, four cases are tested. Figure 12 shows the simulation results of output voltage V_o in four cases. The blue line is output voltage V_o, and the red line is input voltage V_g. Table 4 shows the results of calculations and the simulation results.

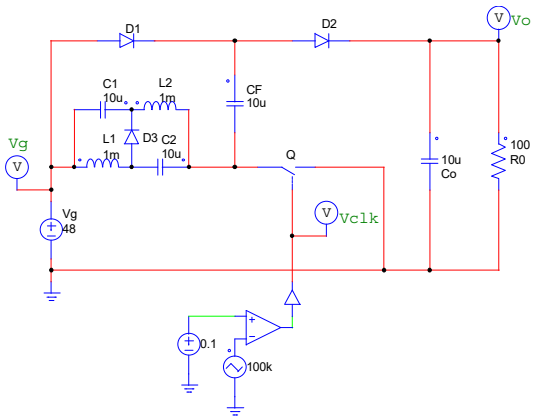


Figure 11. Simulation circuits.

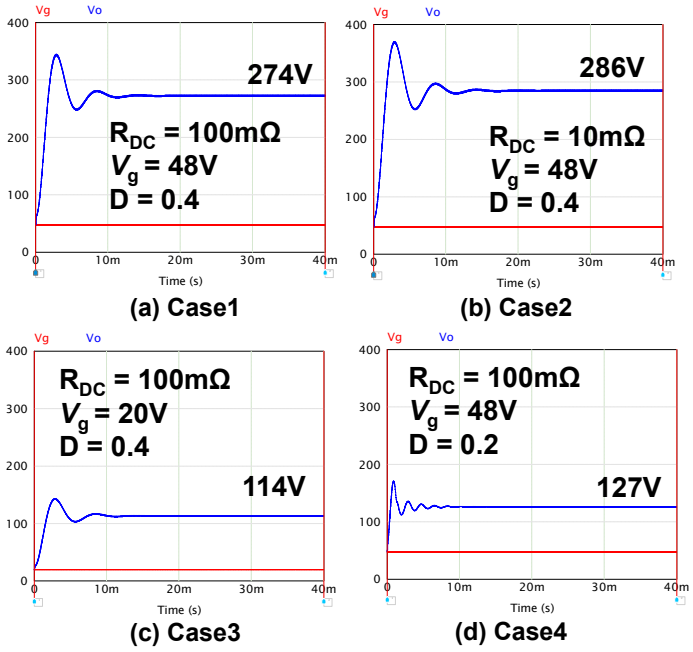


Figure 12. V_O and V_g. (**a**) Case1. (**b**) Case2. (**c**) Case3. (**d**) Case4.

Table 4. Comparison of calculation and simulation results in four cases.

Case	R_{DC}	V_g	D	Vo_calc.	Vo_sim.
Case1	100 mΩ	48 V	0.4	274.3 V	274 V
Case2	10 mΩ	48 V	0.4	286.6 V	286 V
Case3	100 mΩ	20 V	0.4	114.3 V	114 V
Case4	100 mΩ	48 V	0.2	127.3 V	127 V

Calculated numerical equations in Case4 are shown as follows by Equations (19) and (14); $I_{L1} = I_o/(1–D) = 1.67I_o$, $I_o = 127\ V/R_o = 127\ V/100\ \Omega$, and V_o becomes:

$$\frac{V_o}{V_g} = \frac{2-2D}{1-2D} - \frac{2I_{L1}R_{DC}}{(1-2D)V_g} = \frac{2-2\times0.2}{1-2\times0.2} - \frac{2\times1.67\times\frac{127\ V}{100\ \Omega}\times100\ m\Omega}{(1-2\times0.2)48\ V} = 2.652 \quad (20)$$

$$V_o = 48\ V \times 2.652 = 127.3\ V \quad (21)$$

Table 4 shows that the calculation results correspond well to the simulation results.

6. Conclusions

This article has introduced a new high step-up DC–DC converter. The LQZC realizes a low output ripple, is free from the use of a level shifter and a high-side switch, and is plus the low stress on a flying capacitor C_F. The proposed converter makes the following contributions: (i) by the low output ripple, a reliability and cost reduction for the DC–DC converter itself and the inverter circuit for the PV system because the low ripple voltage reduces the size of the capacitors and its aging. (ii) By omitting the level shifter circuit, the consuming loss is definitely reduced because the level shifter circuits and their accompanied circuits are not necessary. (iii) By reducing the voltage stress of the components, the equipment volume becomes small and reduces cost. The achieved efficiency of the converter was more than 94.9% in this prototype. Although the prototype design focuses on a PV application, the proposed architecture can be applied to applications that require the high step-up DC–DC converter, such as energy harvesting and low voltage battery systems for IoT sensor nodes, by power scaling down.

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