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Dual-Coupled-Inductor-Based High-Step-Up Boost Converter with Active-Clamping and Zero-Voltage Switching

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Abstract: Many applications, such as photovoltaic systems, uninterruptible power supplies, and automobile headlamps, need a high step-up DC–DC converter without isolation. The conventional boost converter has the advantages of simple topology and easy control. However, it has some shortcomings, such as insufficient step-up voltage ratio and poor efficiency when operating at large duty-cycle conditions. One of the popular topologies used to overcome these problems is the coupled-inductor boost converter. It utilizes the turn ratio of the coupled inductor to realize a higher step-up voltage ratio. The drawback is that the leakage inductance of the coupled inductor causes a huge voltage spike when the power switches are turned off. Moreover, because coupled inductors are characterized by their large volume and high profile, a conventional coupled-inductor boost converter is unsuited for photovoltaic systems, such as the solar microinverter. This study proposes a novel high-step-up boost converter to solve these problems. This proposed converter uses dual coupled inductors instead of the conventional coupled-inductor boost converter. The secondary side of the coupled inductor is connected in series to increase the step-up voltage ratio. The proposed converter utilizes active clamping to achieve zero-voltage switching (ZVS) for suppressing voltage spike and improving conversion efficiency. In addition, low-profile designs can be fulfilled easily for solar microinverters. The proposed converter and its control method are introduced. The operation principle, circuit characteristics, and circuit analysis are presented. A prototype converter with 300 W output power 25–40 VDC input voltage and 200 VDC output voltage was tested. All functions, including high step-up voltage ratio, ZVS, and active clamping, were achieved, and the highest efficiency was around at 94.7%.

Keywords: coupled inductor; high step-up voltage gain; zero-voltage switching (ZVS)

Citation: Chen, S.-H.; Chen, C.-T.; Lin, Y.-F. Dual-Coupled-Inductor-Based High-Step-Up Boost Converter with Active-Clamping and Zero-Voltage Switching. *Energies* **2024**, *17*, 2018. https://doi.org/10.3390/en17092018

Academic Editor: Mario Marchesoni

Received: 20 March 2024
Revised: 13 April 2024
Accepted: 19 April 2024
Published: 25 April 2024

1. Introduction

At present, many applications, such as photovoltaic systems [1–3], uninterruptible power supplies [4,5], automobile headlamps [6–8], and other telecommunication systems [9–11], still require a high-step-up DC–DC converter as the power supply. Moreover, most solar microinverters require cooling through free air convection and a lower profile, which translates to the need for high conversion efficiency and lower-profile magnetic components. The conventional boost converter is widely used in voltage step-up applications [12]. However, it has some shortcomings that cause difficulties in practical applications. The voltage gain ratio is limited to about five times because the non-ideal resistance of the line, inductor, and diode limit the maximum practical output voltage [12]. The method of integrated magnetic boost converter (IMBC) with both input/output current ripple cancellation and right-half-plane (RHP) zero elimination has been proposed [13]. IMBC has many advantages, such as small ripple, increased bandwidth, and reduced weight. Nevertheless, IMBC has a wide-duty-cycle problem when it is applied to high step-up conversion conditions. The high step-up voltage gain requires a wide duty cycle,

but the duty cycle causes poor control and instability when it is close to one. The voltage and current stress of the main power components (switches and diodes) are determined by output voltage and input current. When the duty cycle is operating at large conditions, a larger root-mean-square (RMS) current flows through the power switch, thereby causing great conduction losses. The selection of a power switch becomes more difficult, and the conversion efficiency is remarkably decreased. The development of high-step-up voltage-gain-ratio converters is important to solve these problems.

Figure 1 shows the basic coupled-inductor boost converter [14]. This boost converter uses the coupled inductor to replace the conventional inductor and utilizes the turn ratio to greatly increase the output voltage [15–19]. The basic coupled-inductor boost converter still has a critical disadvantage, where the leakage inductance of coupled inductor causes a high voltage spike when the power switch is turned off. Although increasing the turn ratio can increase the voltage gain, the leakage inductance is also increased. A lossless clamped circuit can reduce the voltage stress on the main switch as the circuit cannot realize ZVS of the main switch. The active clamp method utilizes resonance of the clamp capacitor and resonant inductor to recover energy. This method not only absorbs voltage spikes on power switches but also enables power switches to achieve ZVS [20–22]. Although increasing the duty cycle of power switch in the conventional coupled-inductor boost converter can achieve a higher voltage gain ratio, the power switch experiences a larger conduction loss due to the increase in turned-on time. Furthermore, the coupled inductor volume is larger than the inductor of the conventional boost converter because the coupled inductor has extra added due to the winding of the secondary side. Therefore, it is unsuitable for application in the solar microinverter. This method has a large DC current flows through the primary side of the coupled inductor. Finally, the passive components are increased, and the topology composition becomes more complex.

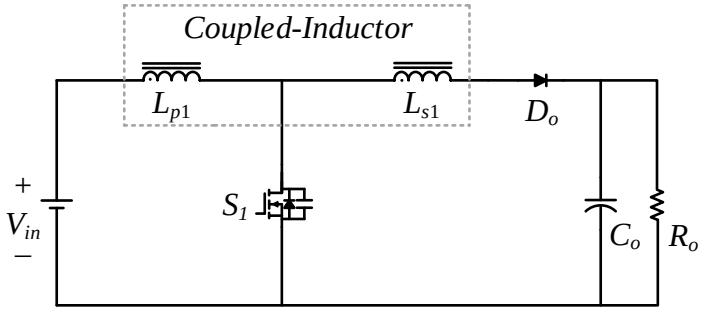

Figure 1. Conventional coupled-inductor boost converter.

The cascaded coupled-inductor method is presented; this is different to the conventional boost converter [23,24]. This method can alleviate the voltage spike problem and recycle the leakage energy, but the clamping circuit causes extra losses. The stacked coupled inductor utilizes the flyback output directly to augment the boost output [25,26]. However an extra voltage balance control is required because the output terminal is divided into two capacitors. Similar to the stacked coupled inductor, a synchronous rectifier switch replaces the power diode in [27], allowing the main power switch to achieve ZVS, thereby improving conversion efficiency. Similar to the cascaded coupled-inductor method, the multi-winding coupled-inductor method uses additional windings to improve voltage gain and reduce power-diode voltage stress [28,29]. However, this approach increases passive component count and complicates the topology. The integrated coupled-inductor method [30–32] utilizes the characteristics of a boost or SEPIC converter to minimize input current ripple and reduce winding inductor core losses. This method exhibits higher topology complexity than the multi-winding coupled-inductor method and fails to achieve ZVS in the power switch. The above method has the problem of a large DC current flowing through the input inductor, and this problem remains unaddressed. The interleaved coupled-inductor method uses multiple converters operating in tandem to alleviate the current stress at

the primary side of coupled inductors, but it does not increase the voltage gain [33,34]. Unfortunately, using multiple converter sets causes the circuit volume to increase and poses challenges in switch control for the interleaved method.

A dual-coupled-inductor-based high-step-up boost converter with active-clamping and zero-voltage switching is proposed. This method uses a stabilizing capacitor loop and dual coupled inductor, which is an innovative coupled-inductor converter and is different from existing inductor converter topology. The stabilizing capacitor voltage at stable conditions is equivalent to the input voltage; the energy of the dual coupled inductors is provided by the input voltage and stabilizing capacitor. The dual coupled inductors share the large input current at the primary side of coupled inductors and the secondary side of coupled inductors is connected in series to achieve high step-up voltage ratio. It extends the voltage gain dramatically and decreases the switch voltage stress. In addition, the active clamp method can transfer the energy released by the leakage inductance to the output load. Thus, the proposed topology can have more efficient performance.

Figure 2 shows that the primary side of the present topology is different from the basic coupled-inductor boost converter and interleaved method. Compared with basic coupled-inductor boost converters, the use of dual coupled inductors enables shared energy storage, allowing for the use of smaller magnetic components. Additionally, connecting the secondary sides of coupled inductors in series achieves a high step-up voltage ratio and the presented converter effectively reduces the duty cycle, thereby decreasing conduction losses in the main power switch because of reduced turn-on time. The proposed converter uses active clamping to suppress the voltage spikes and utilizes the leakage inductance of coupled inductors for ZVS operation in the power switches. Compared with the interleaved coupled-inductor converters and multiple coupled-inductor converters, it not only requires fewer circuit components but also features simpler switch control.

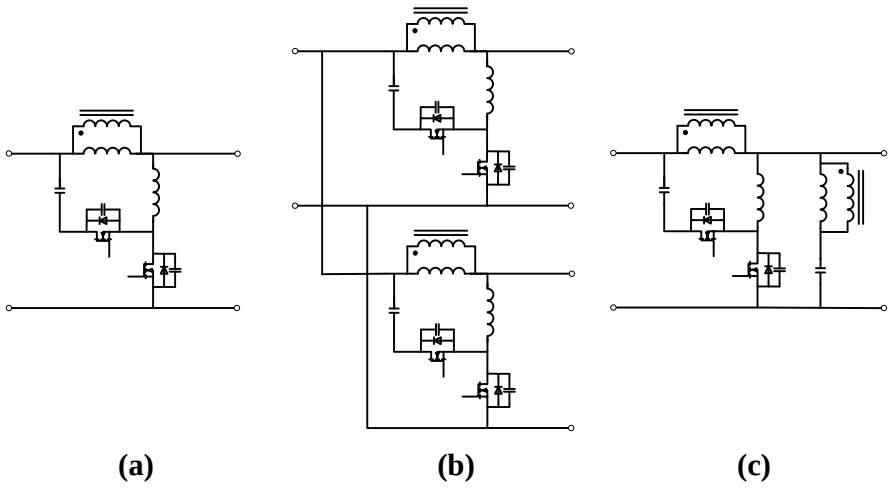

Figure 2. Primary side of coupled-inductor boost converters includes (**a**) basic, (**b**) interleaved, and (**c**) stabilizing capacitor loops.

In Section 2, analyses of the circuit operations, operation waveform, and time domain are provided. In Section 3, analysis of circuit characteristics, component stress, and DC gain is outlined. This includes circuit design, which is discussed and calculated. In Section 4, testing of a prototype converter with 300 W output power, 25–40 V_{DC} input voltage, and 200 V_{DC} output voltage is described; the highest efficiency was around 94.7%.

2. Operation of the Proposed Converter

Figure 3 shows the schematic of the proposed boost converter using dual coupled inductors to achieve a high step-up ratio while implementing active clamping for ZVS. This topology comprises two identical coupled inductors CI_1 and CI_2, the main switch S_1, the auxiliary switch S_2, a resonant inductor L_r, a clamp capacitor C_a, a stabilizing capac-

itor C_b, and the output diode D_o. Both coupled inductors share identical characteristics, and the ideal coupling coefficient is one. A transformer T model is used to describe the coupled inductors. The resonant inductor L_r was designed to enable ZVS for the S_1 and S_2 operations. The control method is pulse-width modulation (PWM). In this study, the v_s signal is obtained by dividing the output voltage. The v_s signal is compared with V_{ref}, and the digital value is converted by the analog-to-digital converter (ADC) of the DSP. The CMPx value is derived after executing the proportional integral differential (PID) in the z-domain. Finally, intelligent EPWM generates the gate signal. PWM control maintains a fixed frequency while adjusting the pulse width to ensure a stable output voltage, as illustrated in Figure 4.

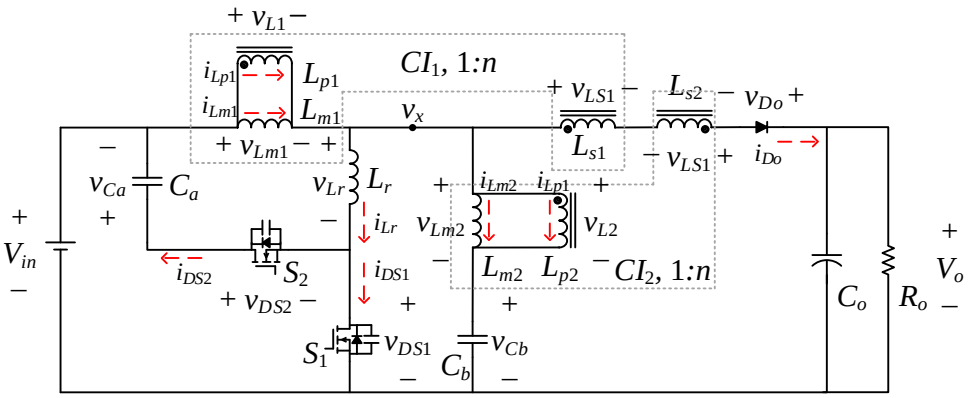

Figure 3. Schematic of the proposed boost converter using dual coupled inductors to achieve high step-up ratio with active clamping for ZVS.

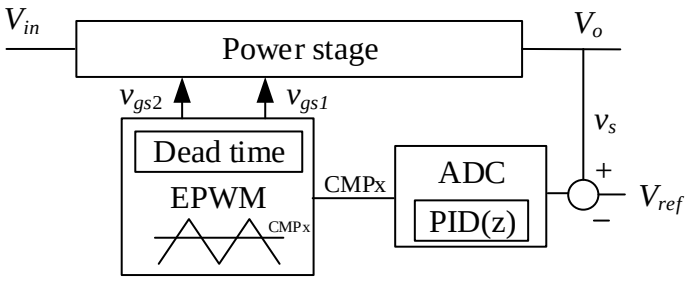

Figure 4. Control mode of the proposed high step-up ratio boost converter.

To analyze the proposed boost converter with dual coupled inductors and a high step-up ratio, the following assumptions are made:

- The turn ratio of the two coupled inductors is the same, which is 1:n.
- The magnetizing inductance of both coupled inductors is the same, which is L_m ($L_{m1} = L_{m2} = L_m$).
- The clamping capacitors C_a and C_b and the output capacitor C_o are much larger than the output capacitance of power switches C_{r1} and C_{r2}. Their steady-state voltages can be viewed as constant voltage sources, dependent on the input voltage and duty cycle.
- The on times of S_1 and S_2 are DT_s and $(1 - D)T_s$, respectively, where D is the duty cycle of main switch S_1, T_s is the switching period, and the dead time is assumed to be smaller than other conduction times.
- All components are considered ideal such that the conduction losses of all switches and diodes are ignored.

From the above assumptions, C_a and C_b in the steady state can be calculated. When the main switch S_1 is turned on, the voltage across the primary side of CI_1 approximates the input voltage V_{in}. On the contrary, when the main switch S_1 is turned off, the voltage

across the primary side of CI_1 is approximately $-v_{Ca}$. From the flux balance of magnetizing inductance L_m under the steady state, v_{Ca} can be expressed as

$$v_{Ca} = \frac{D}{(1-D)} V_{in} \tag{1}$$

The voltage across the primary side of CI_2 approximates $-v_{Cb}$ when S_1 is turned on, and the voltage across the primary side of CI_2 is $V_{in} + v_{Ca} - v_{Cb}$ when main switch S_1 is turned off. In accordance with Equation (1) and to maintain flux balance, the steady-state value of v_{Cb} can be determined as

$$v_{Cb} = V_{in} \tag{2}$$

The definitions of the direction of voltage and current are shown in Figure 3. i_{DS1} and i_{DS2} are the currents of switches, i_{Lr} is the resonant inductor current, i_{Lm1} and i_{Lm2} are the magnetizing inductor currents, i_{Lp1} and i_{Lp2} are the currents of coupled inductors at the primary side, and i_{Do} is the output diode current. Figure 5 shows the operation waveform of the proposed topology. The waveform can be divided into six parts in one cycle. The descriptions of each state are given below. Figure 6 provides a visual representation of these six operation states.

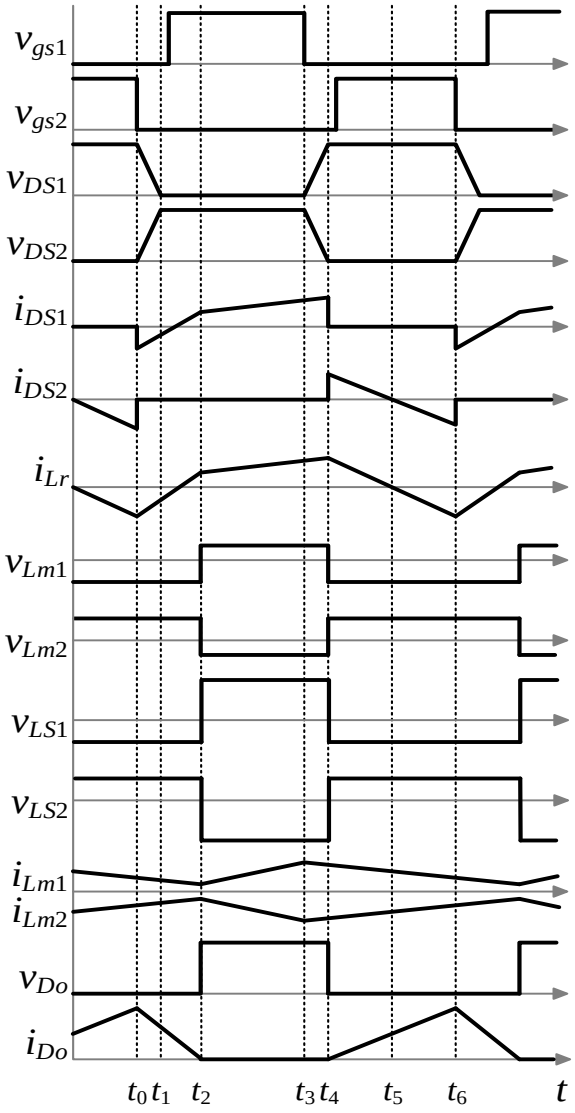

Figure 5. Key waveforms of the proposed high step-up ratio boost converter with ZVS.

- State 1 (t_0–t_1)

In this state, auxiliary switch S_2 is turned off at t_0, whereas the main switch S_1 remains off. The resonant inductor L_r has two parasitic capacitors C_{r1} and C_{r2}, and the direction of resonant inductor current i_{Lr} is negative. This state ends when capacitor C_{r1} is discharged to zero and capacitor C_{r2} is charged to $V_{in} + v_{Ca}$. The values of C_{r1} and C_{r2} are extremely small, so this state is extremely short. The resonant inductor L_r must meet the following conditions to achieve ZVS:

$$L_r \geq \frac{(C_{r1} + C_{r2})[v_{DS1}(t_0)]^2}{[i_{Lr}(t_0)]^2} \tag{3}$$

- State 2 (t_1–t_2)

At t_1, C_{r1} is discharged to zero, the body diode operates across S_1, and S_1 is turned on to achieve ZVS. At the same time, both coupled inductors still provide energy to the output side, and the output diode current i_{Do} continually decreases linearly until it reaches zero. i_{Lr} changes from negative to positive until it is equal to the sum of absolute value of magnetizing inductor currents i_{Lm1} and i_{Lm2}, and this stage ends. The node voltage v_x and the magnetizing inductor voltages v_{Lm1} and v_{Lm2} can be expressed as

$$v_x = \frac{2nV_{in} + V_o}{2n+1} \tag{4}$$

$$v_{Lm1} = \frac{V_{in} - V_o}{2n+1} \tag{5}$$

$$v_{Lm2} = \frac{-(V_{in} - V_o)}{2n+1} \tag{6}$$

The magnetizing inductor currents $i_{Lm1}(t)$ and $i_{Lm2}(t)$, resonant inductor current $i_{Lr}(t)$, and diode current $i_{Do}(t)$ can be expressed as

$$i_{Lm1}(t) = \frac{V_{in} - V_o}{(2n+1)L_m}(t) + i_{Lm1}(t_1) \tag{7}$$

$$i_{Lm2}(t) = \frac{-(V_{in} - V_o)}{(2n+1)L_m}(t) + i_{Lm2}(t_1) \tag{8}$$

$$i_{Lr}(t) = \frac{2nV_{in} + v_o}{(2n+1)L_r}(t) + i_{Lr}(t_1) \tag{9}$$

$$i_{Do}(t) = \frac{i_{Lm1}(t) - i_{Lm2}(t) - i_{Lr}(t)}{2n+1} \tag{10}$$

- State 3 (t_2–t_3)

In state 3, S_1 remains on and carries the resonant inductor current i_{Lr}, and i_{Lr} is equal to the sum of the absolute value of magnetizing inductor currents i_{Lm1} and i_{Lm2}. S_2 is remains off, v_{Lm1} is approximately equal to the input voltage V_{in}, and v_{Lm2} is approximately equal to the negative input voltage $-V_{in}$, so the input energy is shared between the two primary magnetizing inductances of coupled inductor. This interval ends when S_1 is turned off. The output diode is reverse biased, and the output current is supplied only by the output capacitor C_o. The node voltage v_x and the magnetizing inductor voltages v_{Lm1} and v_{Lm2} can be expressed as

$$v_x = V_{in}\frac{2L_r}{L_m + 2L_r} \tag{11}$$

$$v_{Lm1} = V_{in}\frac{L_m}{L_m + 2L_r} \tag{12}$$

$$v_{Lm2} = -V_{in}\frac{L_m}{L_m + 2L_r} \tag{13}$$

The magnetizing inductor currents $i_{Lm1}(t)$ and $i_{Lm2}(t)$ and resonant inductor current $i_{Lr}(t)$ can be expressed as

$$i_{Lm1}(t) = \frac{V_{in}}{L_m}\frac{L_m}{L_m + 2L_r}t + i_{Lm1}(t_2) \tag{14}$$

$$i_{Lm2}(t) = \frac{V_{in}}{L_m}\frac{-L_m}{L_m + 2L_r}t + i_{Lm2}(t_2) \tag{15}$$

$$i_{Lr}(t) = V_{in}\frac{2L_r}{L_m + 2L_r}t + i_{Lr}(t_2) \tag{16}$$

- State 4 (t_3–t_4)

At t_3, S_1 and S_2 are turned off. The resonant inductor L_r is resonant with parasitic capacitors C_{r1} and C_{r2}. This stage ends when capacitor C_{r1} is charged to V_{in} + v_{Ca} and capacitor C_{r2} is discharged to zero. This stage is extremely short because the values of capacitances C_{r1} and C_{r2} are extremely small. The ZVS condition is expressed as

$$L_r \geq \frac{(C_{r1} + C_{r2})[v_{DS2}(t_3)]^2}{[i_{Lr}(t_3)]^2} \tag{17}$$

- State 5 (t_4–t_5)

Figure 6e shows the operation station at this state, where the voltage v_{DS1} is to be charged to V_{in} + v_{Ca}. The resonant inductor current i_{Lr} flows through the body diode of S_2, and S_2 is turned on to achieve ZVS. Given that v_{Lm1} is approximately equal to the negative v_{Ca} and v_{Lm2} is approximately equal to v_{Ca}, the output diode D_o is forward biased and starts to operate. The energies stored in the magnetizing inductors L_{m1} and L_{m2} are transferred to the output load. The diode current i_{Do} starts to increase linearly, and clamp capacitor voltage v_{Ca} begins to rise. This stage ends when the resonant inductor current i_{Lr} decreases to zero. The node voltage v_x and the magnetizing inductor voltages v_{Lm1} and v_{Lm2} can be expressed as

$$v_x = \frac{2nV_{in} + V_o}{2n + 1} \tag{18}$$

$$v_{Lm1} = \frac{V_{in} - V_o}{2n + 1} \tag{19}$$

$$v_{Lm2} = \frac{-(V_{in} - V_o)}{2n + 1} \tag{20}$$

The currents i_{Lm1}, i_{Lm2}, i_{Lr}, and i_{Do} are given as

$$i_{Lm1}(t) = \frac{V_{in} - V_o}{(2n + 1)L_m}(t) + i_{Lm1}(t_4) \tag{21}$$

$$i_{Lm2}(t) = \frac{-(V_{in} - V_o)}{(2n + 1)L_m}(t) + i_{Lm2}(t_4) \tag{22}$$

$$i_{Lr}(t) = \frac{2nV_{in} + v_o}{(2n + 1)L_r}(t) + i_{Lr}(t_4) \tag{23}$$

$$i_{Do}(t) = \frac{i_{Lm1}(t) - i_{Lm2}(t) - i_{Lr}(t)}{2n + 1} \tag{24}$$

- State 6 (t_5–t_6)

The circuit operations in this interval are the same as those in State 5, except for the directions of i_{Lr}. The capacitor voltage v_{Ca} starts to decrease, and the ampere-second balance is completed in States 5 and 6.

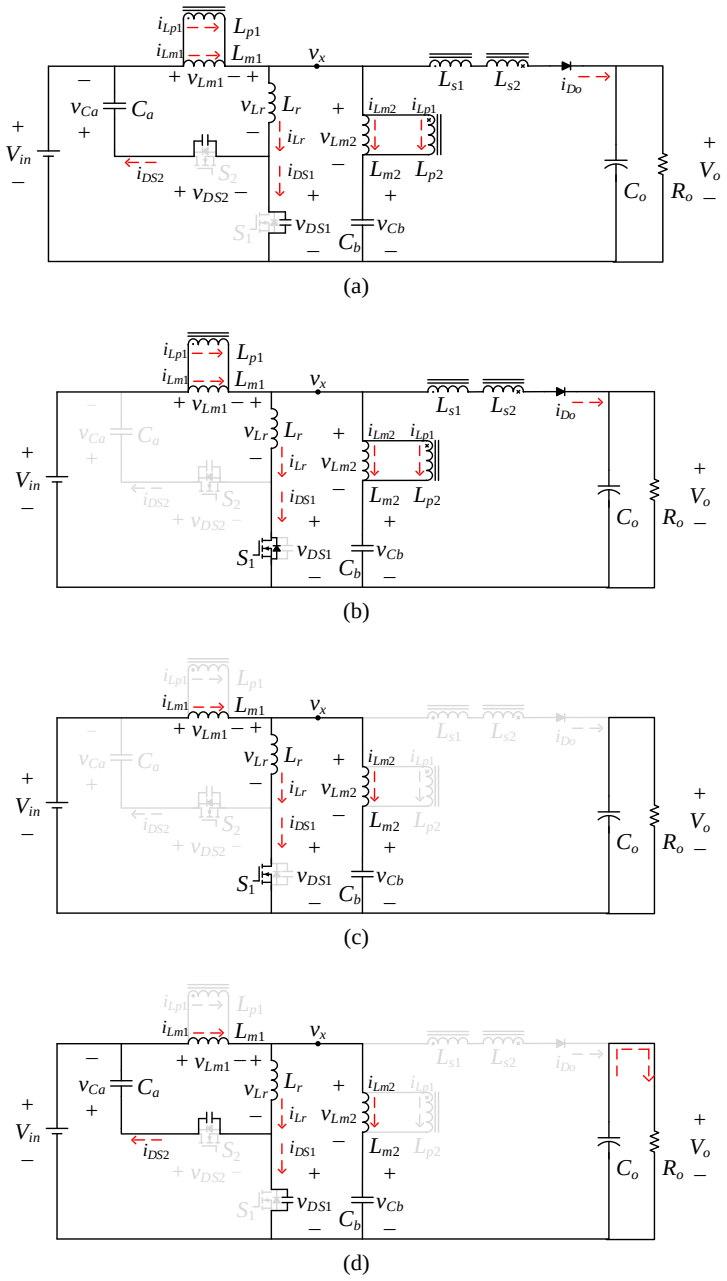

Figure 6. *Cont.*

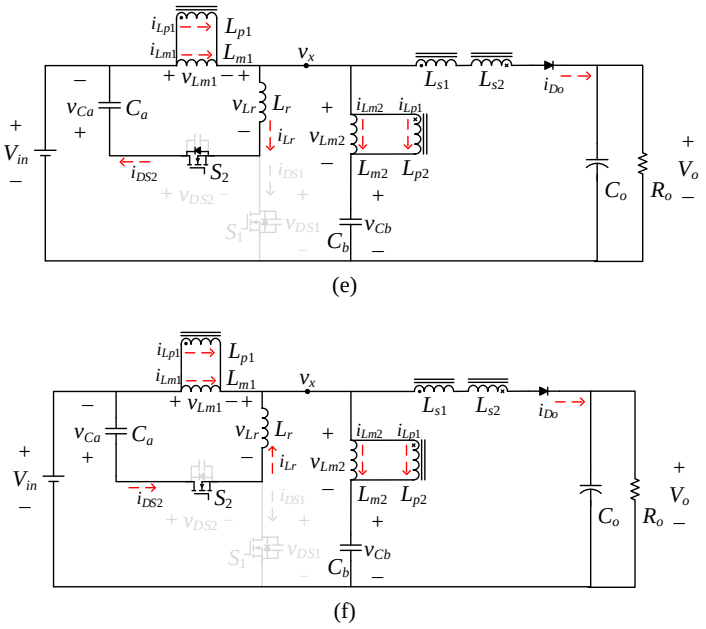

Figure 6. Conduction paths of (**a**) State 1, (**b**) State 2, (**c**) State 3, (**d**) State 4, (**e**) State 5, and (**f**) State 6 for the proposed boost converter with high step-up ratio and ZVS during one switching period.

3. Analysis of the Proposed Converter

Figure 7 ignores the intervals t_0–t_1 and t_3–t_4 of Figure 3. The intervals t_0–t_1 and t_3–t_4 can be ignored because the time is extremely short. Simplifications are needed to derive the ideal transfer function of the proposed topology. Figure 5 shows the simplified waveform, where D is the duty cycle of metal–oxide–semiconductor field-effect transistor (MOSFET) S_1, and D_{er} is the duty loss. The resonant inductor current i_{Lr} can be divided into stages A, B, and C, in accordance with its shape.

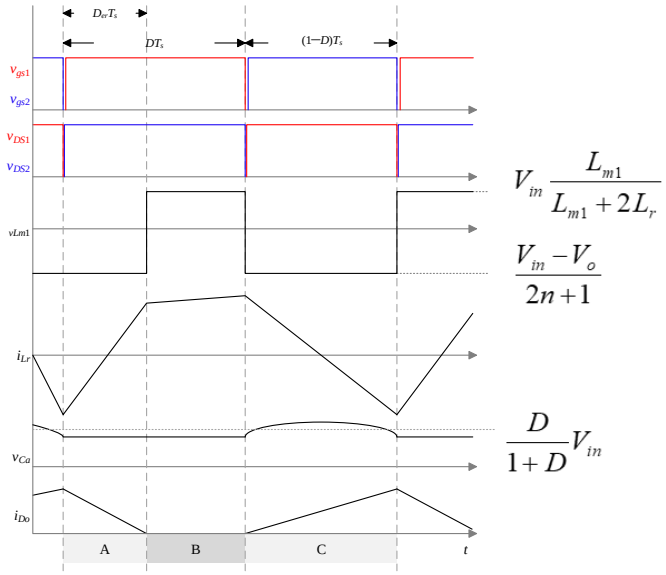

Figure 7. Simplified waveform.

3.1. Clamped Voltage v_{Ca}

As shown in Equation (1), v_{Ca} is determined by D and V_{in}. As depicted in Figure 8, the clamp capacitor voltage v_{Ca} will be higher than the input voltage V_{in} if duty cycle D is higher than 0.5. If duty cycle D is close to 1, then the clamp capacitor voltage v_{Ca} will be extremely high. Therefore, in applications, the duty cycle should be designed around 0.5.

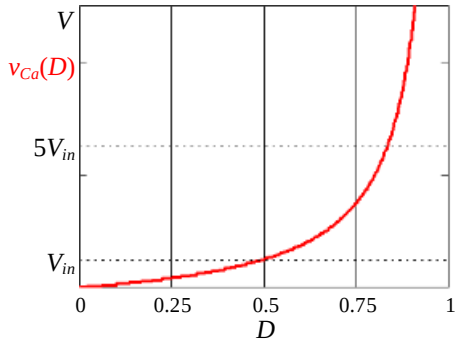

Figure 8. Voltage stress of clamp capacitor v_{Ca}.

3.2. Voltage Transfer Ratio

In accordance with the simplified waveform at Figure 6, the volt-second balance equation of magnetizing inductor L_{m1} is

$$\frac{V_{in}-V_o}{2n+1}D_{er}+V_{in}\frac{\frac{1}{2}L_{m1}}{\frac{1}{2}L_{m1}+L_r}(D-D_{er})+\frac{V_{in}-V_o}{2n+1}(1-D)=0 \tag{25}$$

In general, resonant inductor L_r is smaller than magnetizing inductors L_{m1} and L_{m2}. If the effects of duty loss D_{er} and resonant inductor L_r are ignored, then Equation (25) can be simplified as Equation (26), and ideal transfer function M_{ideal} is derived as Equation (27).

$$V_{in}D+\frac{V_{in}-V_o}{2n+1}(1-D)=0 \tag{26}$$

$$M_{ideal}=\frac{2nD+1}{1-D} \tag{27}$$

Figure 9 shows the comparison of ideal transfer ratio M_{ideal} and conventional boost converter transfer ratio $M = 1/(1 - D)$. The proposed topology has a relatively higher transfer ratio. The transfer gain increases relatively because the transformer turn ratio is higher. In accordance with Equation (27), if the transfer ratio is around 10 times, then the turn ratio $n = 1$ is unsuitable.

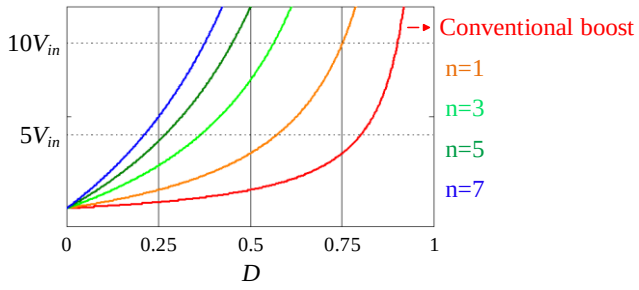

Figure 9. Transfer ratio comparison of the proposed topology and conventional boost converter.

Figure 10 shows the transfer ratio comparison of the proposed topology and coupled-inductor boost converter, where the transfer ratio of the proposed topology is $(nD + 1)/(1 - D)$. From Figure 10, the transfer ratio of the proposed topology is higher than coupled-inductor boost converter when the turn ratio is the same.

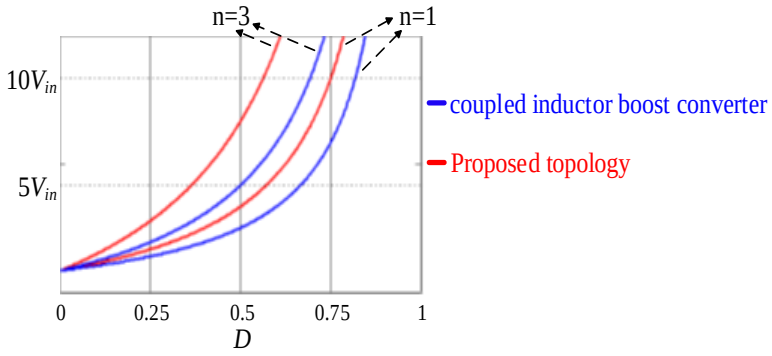

Figure 10. Transfer ratio comparison of the proposed topology and conventional coupled-inductor boost converter.

The voltage of the magnetizing inductor L_{m1} is inconsistent in duty cycle D due to the influence of duty loss D_{er}. The effect of the inductor is also reconsidered, so Equation (28) is rederived, and the transfer ratio $M = V_o/V_{in}$ can be expressed as

$$\frac{V_o}{V_{in}} = \frac{\frac{L_m}{L_m+2L_r}(D - D_{er})(2n+1)}{1-(D-D_{er})} \tag{28}$$

Equation (25) is used to derive duty loss D_{er} as follows:

$$D_{er} = \frac{-i_{Do_{Max}}(2n+1)}{T_s} \frac{1}{\left(\frac{v_{Lm1}(A)}{L_{m1}} - \frac{v_{Lm2}(A)}{L_{m2}} - \frac{v_{Lr}(A)}{L_r}\right)} \tag{29}$$

where i_{Do_Max} is the peak current of diode, and the value can be derived as

$$i_{Do\_Max} = \frac{(1-D)T_s}{2n+1}\left(\frac{v_{Lm1}(C)}{L_{m1}} - \frac{v_{Lm2}(C)}{L_{m2}} - \frac{v_{Lr}(C)}{L_r}\right) \tag{30}$$

In accordance with the current waveform in Figure 5, the output current I_o can be expressed as

$$I_o = \frac{i_{Do\_Max}}{2}[1-(D-D_{er})] \tag{31}$$

Figure 11 shows the relationship between transfer ratio M, output current I_o, and duty cycle D, plotted using Equations (28)–(31). The transfer ratio M is affected by output current I_o and duty cycle D. Duty loss D_{er} increases with the increase in load current, which indicates that more duty cycle D is required to reach the required voltage. Assuming that the transfer ratio M is 8, duty cycle D changes from 0.52 to 0.69 if the output current I_o changes from 0 to 3.

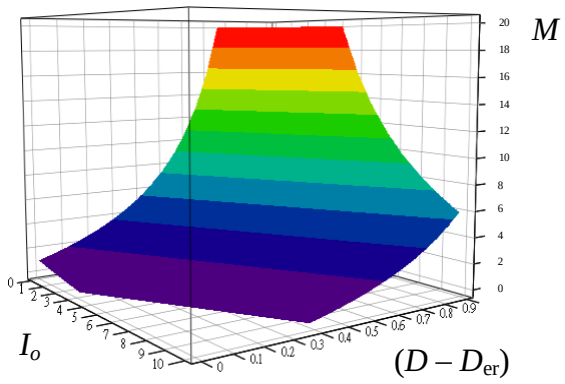

Figure 11. Output transfer ratio.

3.3. Voltage and Current Stress

In accordance with Section 2, the voltage stresses of switches S_1 and S_2, and diode D_o can be derived as Equations (32) and (33). Resonant inductor L_r is smaller than magnetizing inductors L_{m1} and L_{m2}, so voltage stress v_{Do} can be simplified to facilitate subsequent comparison.

$$v_{DS1} = v_{DS2} = V_{in} + v_{Ca} = \frac{1}{(1-D)} V_{in} \tag{32}$$

$$V_{Do} = V_{in} \frac{2nL_m}{L_m + 2L_r} - V_{in} \frac{2L_r}{L_m + 2L_r} + V_o \tag{33}$$

Figure 12 shows the relationship of magnetizing inductor currents i_{Lm1} and i_{Lm2}, diode current i_{Do}, and output current I_o. From Equation (30), the value of output current I_o is the average of diode current i_{Do}. From Section 2, the diode current i_{Do} is composed of magnetizing inductor currents i_{Lm1} and i_{Lm2} and resonant inductor current i_{Lr}. Two transformers provide current to the output, so the current stress of the transformer is lower.

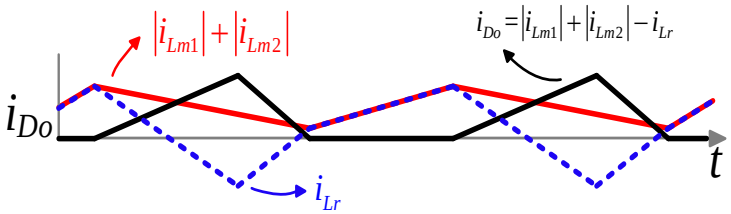

Figure 12. Relationship of magnetizing inductor, diode, and output currents.

Table 1 compares the modern topology and the proposed topology, which includes the number of components, voltage gain, control method, input current stress, diode voltage stress, and efficiency. Comparison is made under the same output load and current ripple conditions and the same output load conditions. The cascade coupled-inductor method increases the number of turns. As a result, the winding area of the magnetic components is increased, requiring the use of larger iron cores. Therefore, the voltage stress on the output diode also increases [21]. The stacked coupled inductor approach requires redundant rectifier diodes to control the output capacitor voltage [26]. Similar to stacked coupled inductors, the multi-winding coupled inductor approach uses additional windings to increase the voltage gain. The additional windings require magnetic components to be designed using larger cores [29]. However, the approach of stacked and multi-winding increases passive component count and complicates the topology. In the above method, the problem of a large DC current flowing through the input inductor remains unaddressed. The interleaved coupled-inductor method uses multiple converters operating in tandem to alleviate the current stress at the primary side of the coupled inductors [34]. Unfortunately, using multiple converter sets causes the circuit volume to increase and poses challenges in switch control for the interleaved method. Compared with previous studies, the primary side of the coupled inductor has a lower current stress under the same output load conditions. Considering the high output transfer ratio condition, the voltage stress of the proposed topology is around V_{in}, and the voltage stress of the conventional boost converter is higher than V_{in}.

Table 1. Comparison of the conventional boost converter and the proposed topology.

Topologies	Propose Converter	[21]	[26]	[29]	[34]
Number of coupled inductors	2	1	1	1	2
Number of switches	2	2	2	1	2
Number of diodes	1	2	4	4	4
Voltage gain	$\frac{2nD+1}{1-D}$	$\frac{1+n}{1-D}$	$\frac{1+(1+D)n}{1-D}$	$\frac{2-D+n}{1-D}+n$	$\frac{2n+1}{1-D}$
Control method	PWM	PWM	PWM	PWM	Interleave
Soft-switching performance	ZVS	ZVS	Hard switching	Hard switching	Hard switching
Input-current stress	Medium	High	High	High	Medium
Diode-voltage stress	High	High	Low	Low	Medium
Conduction losses	Low	High	High	High	High

4. Experimental Results

A 300 W prototype was designed and built to verify the feasibility of the proposed topology, as shown in Figure 13. The dimensions were approximately $120 \times 100 \times c$ mm^3. The specifications of the prototype are shown in Table 2, and the selection of components is shown in Table 3. In addition, to verify the assumptions in Section 2, the parameters are listed in Table 4.

The inductance of resonant inductor was designed in accordance with Equations (3) and (29). The magnetizing inductance was based on Equations (12), (19) and (29). The parasitic capacitor was the output capacitance of MOSFET. Efficiency data were obtained from the experimental results. The DC power source utilized was the Keysight E35234A, the DC load was the Chroma 63108A, and the power meter was the HIOKI PW3337.

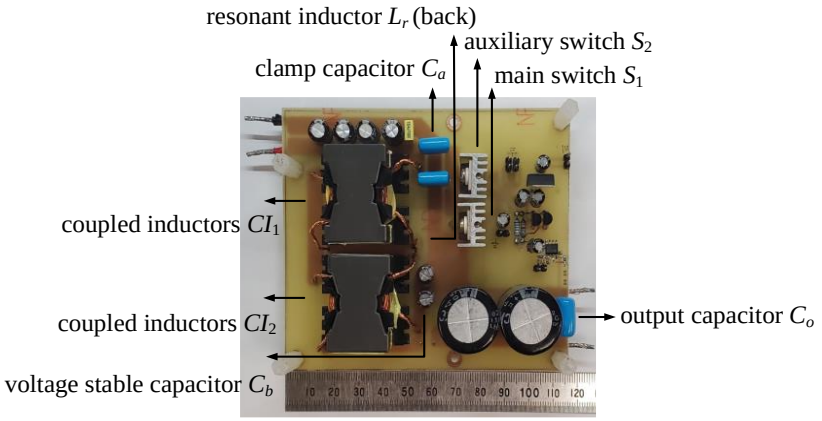

Figure 13. Prototype of the proposed topology.

Table 2. Specification of Prototype.

Item	Value
V_{in}	25–40 V
V_o	200 V
I_{o_MAX}	1.5 A
P_{o_MAX}	300 W
Switching frequency f_s	100 kHz

Table 3. Component Selection.

Item	Value
MOSFET S_1 / S_2	FDP2614
Diode D_o	BYC200-600P
Transformer turn ratio	1:3
Core material/type	PC 40/PQ35-35

Table 4. Parameters of Components.

Item	Value
Resonant inductor L_r	1 μH
Magnetizing inductance L_m	15 μH
Parasitic capacitor C_r	500 pF
Voltage-stable capacitor C_a	66 μF
Clamping capacitor C_b	8 μF

Figures 14–16 show the operation waveforms at 25 V V_{in} and full load condition. The voltage stress of v_{DS2} mostly conformed to Equation (31). The voltage stress of v_{DS1} was slightly higher than the calculation because the capacitance v_{Ca} was small (this phenomenon can be referred to as State C in Figure 5). Figure 14 illustrates the ZVS waveforms. Before v_{gs1} and v_{gs2} were turned on, the drain-to-source voltages v_{DS1} and v_{DS2} were clamped at zero. Therefore, ZVS operations for S_1 and S_2 were achieved. Figures 15 and 16 show the current waveform of resonant inductor i_{Lr}, diode i_{Do}, and two switches i_{DS2} and i_{DS2}.

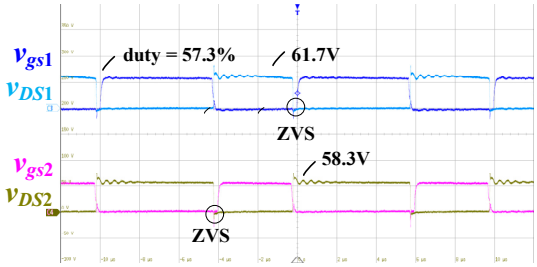

Figure 14. Operation waveforms of v_{gs1}, v_{gs2}, v_{DS1}, and v_{DS2} at 100% load. (Time: 2 μs/div; v_{gs1}: 10 V/div; v_{gs2}: 10 V/div; v_{DS1}: 50 V/div; v_{DS2}: 50 V/div).

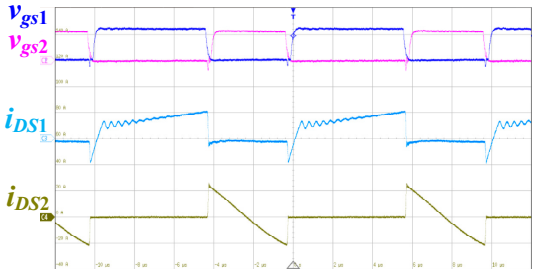

Figure 15. Operation waveforms of v_{gs1}, v_{gs2}, i_{DS1}, and i_{DS2} at 100% load. (Time: 2 μs/div; v_{gs1}: 10 V/div; v_{gs2}: 10 V/div; i_{DS1}: 20 A/div; i_{DS2}: 20 A/div).

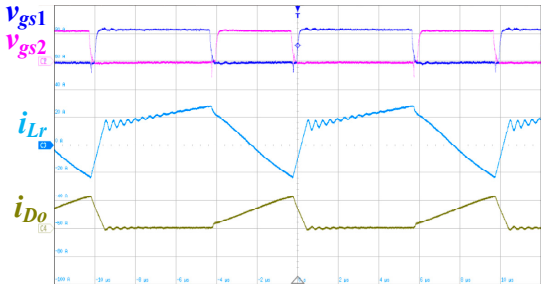

Figure 16. Operation waveforms of v_{gs1}, v_{gs2}, i_{Lr}, and i_{Do} at 100% load. (Time: 2 μs/div; v_{gs1}: 10 V/div; v_{gs2}: 10 V/div; i_{Lr}: 20 A/div; i_{Do}: 5 A/div).

Figure 17 illustrates the waveforms of the gate signals, v_{gs1} and v_{gs2}, and the couple inductors voltage, v_{Lm1} and v_{Lm2} at 40 V V_{in} and full load condition. Both v_{Lm1} and v_{Lm2} had the identical voltage level through one complete switching cycle, and the operating condition was at 40 V V_{in} and full-load.

Figure 18 shows the waveforms of the gate-to-source v_{gs1}, the secondary side's voltage of the coupled inductors v_{LS1} and v_{LS2}, and the current of the output diode i_{Do} at 40 V V_{in} and full load condition. v_{LS1} and v_{LS2}, had the identical voltage level through the one complete switching cycle, and when the output diode D_o was to be forward-bias, the output current i_{Do} was flowing through the secondary side of the coupled inductors L_{S1} and L_{S2} This meant that the dual coupled inductors provided energy to output capacitor C_o and load.

Figures 19 and 20 show the voltage levels of capacitors C_a and C_a at 25 V V_{in}, 40 V V_{in}, and 100% load. The average voltage value of v_{Ca} was approximately 53.3 V, which is similar to the result of Equation (1).

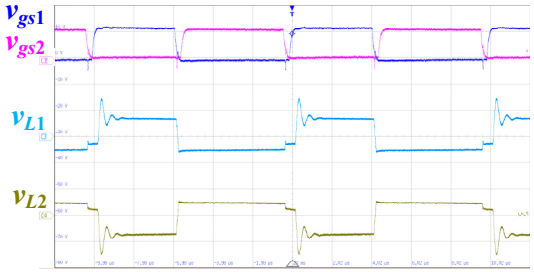

Figure 17. Operation waveforms of v_{gs1}, v_{gs2}, v_{L1}, and v_{L2} at 100% load. (Time: 2 µs/div; v_{gs1}: 10 V/div; v_{gs2}: 10 V/div; v_{L1}: 50 V/div; v_{L2}: 50 A/div).

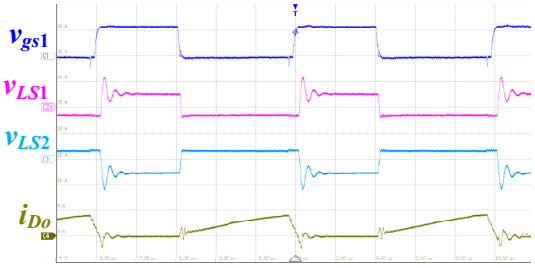

Figure 18. Operation waveforms of v_{gs1}, v_{LS1}, v_{LS2} and i_{Do} at 100% load. (Time: 2 µs/div; v_{gs1}: 10 V/div; v_{LS1}: 200 V/div; v_{LS2}: 200 V/div; i_{Do}: 5 A/div).

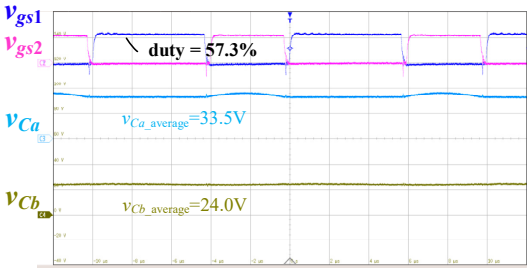

Figure 19. Voltage levels of capacitors C_a and C_b at 25 V V_{in}, 100% load. (Time: 2 µs/div; v_{gs1}: 10 V/div; v_{gs2}: 10 V/div; v_{Ca}: 20 V/div; v_{Cb}: 20 V/div).

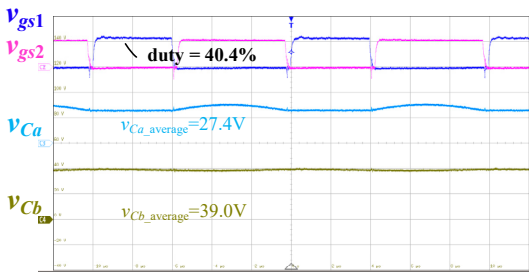

Figure 20. Voltage levels of capacitors C_a and C_b at 40 V V_{in}, 100% load. (Time: 2 µs/div; v_{gs1}: 10 V/div; v_{gs2}: 10 V/div; v_{Ca}: 20 V/div; v_{Cb}: 20 V/div).

Figure 21 shows the efficiency curves at 25 V and 40 V V_{in}. The highest efficiency point was at 40 V V_{in} under 40% load.

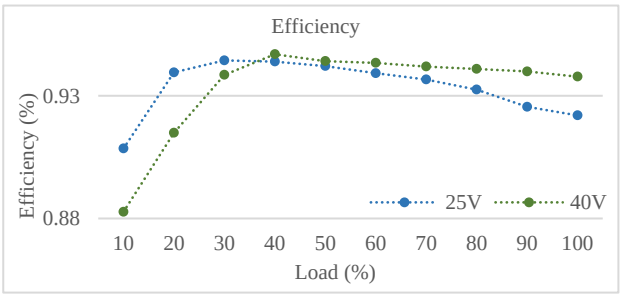

Figure 21. Efficiency curve.

The loss analysis is obtained by recording the stress of the components experimentally and bringing it into the loss Equation (34). P_{S_sw} is the switching loss of the main switch S_1 and the auxiliary switch S_2. P_{S_con} is the conduction loss of the main switch S_1 and the auxiliary switch S_2. P_{D_con} is the conduction loss of the output diode. P_{Tr_core} is the core loss of the two coupled inductors. P_{Tr_core} is the core loss of the two coupled inductors. P_{Lr_core} is the core loss of the resonant inductor. P_{Lr_core} is the core loss of the resonant inductor. The loss obtained by the component parameters and the stress equations was consistent with the actual efficiency. Figure 22 shows the loss distribution at 50% and 100% loads. The highest power loss was the coupled inductor core loss. Although the two switches reached ZVS, the turn-off loss remained high and was the second highest power loss.

$$\begin{aligned} Loss_{total} = {} & P_{S_{sw1}} + P_{S_{con1}} + P_{S_{sw2}} + P_{S_{con2}} + P_{D_{con}} \\ & +2\left(P_{Tr\_core} + P_{Tr\_copper}\right) + P_{Lr\_core} + P_{Lr\_copper} \end{aligned} \tag{34}$$

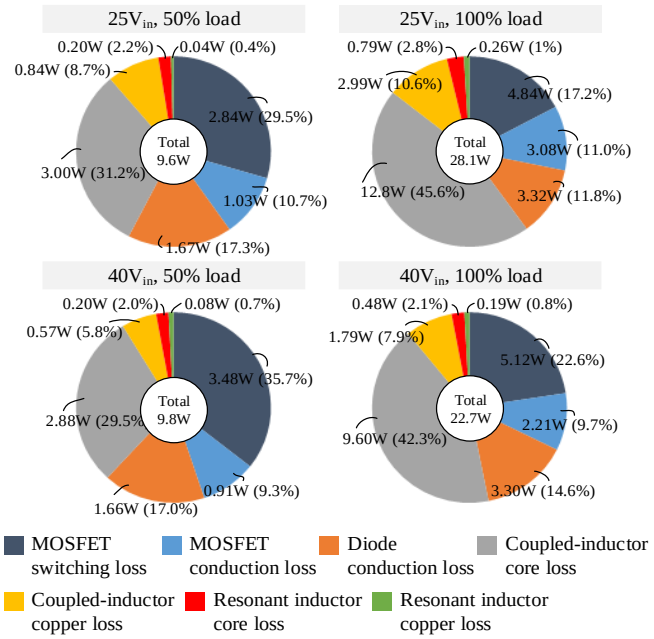

Figure 22. Loss distribution.

5. Conclusions

This study introduces an innovative high-step-up boost converter design featuring two separate coupled inductors. This approach enables the creation of a low-profile implementation, with the secondary side of coupled inductors connected in series to increase the step-up voltage ratio. An active clamp is also incorporated to achieve ZVS, making it

particularly well-suited for the design of low-profile solar microinverters. Operating modes throughout a complete switching cycle are described, and key equations are derived. The experimental results on a 300 W, input voltage 25–40 V, and output voltage 200 V prototype are recorded to verify the theoretical analysis. The maximum efficiency was around 94.7%. The proposed converter not only facilitates low-profile designs but also meets the stringent requirements of high step-up voltage ratios.

Author Contributions: Software, C.-T.C.; Validation, C.-T.C.; Writing—original draft, S.-H.C.; Writing—review & editing, Y.-F.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Aghdam, F.H.; Abapour, M. Reliability and cost analysis of multistage boost converters connected to PV panels. *IEEE J. Photovolt.* **2016**, *6*, 981–989. [CrossRef]
2. Agorreta, J.L.; Reinaldos, L.; Gonzalez, R.; Borrega, M.; Balda, J.; Marroyo, L. Fuzzy switching technique applied to PWM boost converter operating in mixed conduction mode for PV systems. *IEEE Trans. Ind. Electron.* **2009**, *56*, 4363–4373. [CrossRef]
3. Liu, J.; Wang, K.; Zheng, Z.; Li, C.; Li, Y. A dual-active-clamp quasi-resonant isolated boost converter for PV integration to medium-voltage DC grids. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *8*, 3444–3456. [CrossRef]
4. Ma, G.; Qu, W.; Yu, G.; Liu, Y.; Liang, N.; Li, W. A zero-voltage-switching bidirectional dc–dc converter with state analysis and soft-switching-oriented design consideration. *IEEE Trans. Ind. Electron.* **2009**, *56*, 2174–2184.
5. Ma, K.W.; Lee, Y.S. A novel uninterruptible dc-dc converter for UPS applications. *IEEE Trans. Ind. Appl.* **1992**, *28*, 808–815. [CrossRef]
6. Kovatchev, E.; Evstatieva, N. Design of a digitally controlled boost converter for automotive headlamp applications. In Proceedings of the 2017 International Scientific Conference Electronics (ET), Sozopol, Bulgaria, 13–15 September 2017; pp. 1–4.
7. Gacio, D.; Calleja, A.J.; García, J.; Ribas, J.; Rico-Secades, M. Suitable switching converter topologies for automotive signal lamps and headlamps using power LEDs. In Proceedings of the 2008 IEEE Industry Applications Society Annual Meeting, Edmonton, AB, Canada, 5–9 October 2008; pp. 1–7.
8. Sreeja, P.; Suresh, L.P. Optimized design of ZVZCS switched non isolated DC-DC boost converter with high voltage gain. In Proceedings of the 2013 International Conference on Circuits, Power and Computing Technologies (ICCPCT), Nagercoil, India, 20–21 March 2013; pp. 500–505.
9. Barbi, I.; Gules, R. Isolated DC-DC converters with high-output voltage for TWTA telecommunication satellite applications. *IEEE Trans. Power Electron.* **2003**, *18*, 975–984. [CrossRef]
10. Kiran, R.; Kalpana, R. Design and development of modular dual-input DC/DC step down converter for telecom power supply. In Proceedings of the 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 18–21 December 2018; pp. 1–6.
11. Akerlund, J. -48 V DC computer equipment topology-an emerging technology. In Proceedings of the INTELEC-Twentieth International Telecommunications Energy Conference (Cat. No. 98CH36263), San Francisco, CA, USA, 4–8 October 1998; pp. 15–21.
12. Tofoli, F.L.; Pereira, D.D.C.; de Paula, W.J.; de Sousa Oliveira Júnior, D. Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter. *IET Power Electron.* **2015**, *8*, 2044–2057. [CrossRef]
13. Gu, Y.; Zhang, D.; Zhao, Z. Input/output current ripple cancellation and RHP zero elimination in a boost converter using an integrated magnetic technique. *IEEE Trans. Power Electron* **2015**, *30*, 747–756. [CrossRef]
14. Vazquez, N.; Estrada, L.; Hernandez, C.; Rodriguez, E. The tapped-inductor boost converter. In Proceedings of the 2007 IEEE International Symposium on Industrial Electronics, Vigo, Spain, 4–7 June 2007; pp. 538–543.
15. Ai, J.; Lin, M. Ultra large gain step-up coupled-inductor DC-DC converter with an asymmetric voltage multiplier network for a sustainable energy system. *IEEE Trans. Power Electron* **2017**, *31*, 6896–6903. [CrossRef]
16. Tintu, V.R.; George, M. Tapped inductor technology based DC-DC converter. In Proceedings of the 2011 International Conference on Signal Processing, Communication, Computing and Networking Technologies, Thuckalay, India, 21–22 July 2011; pp. 747–753.
17. Lee, J.J.; Cho, B.H. A novel high step-up zero-current-switching tapped-inductor boost converter. In Proceedings of the 8th International Conference on Power Electronics-ECCE Asia, Jeju, Republic of Korea, 30 May–3 June 2011; pp. 1869–1872.
18. Berkovich, Y.; Axelrod, B. Switched-coupled inductor cell for DC–DC converters with very large conversion ratio. *IET Power Electron.* **2011**, *4*, 309–315. [CrossRef]

19. Li, W.; He, X. Review of non-isolated high-step-up DC/DC converters in photovoltaic grid-connected applications. *IEEE Trans. Ind. Electron.* **2010**, *58*, 1239–1250. [CrossRef]
20. Duarte, C.M.C.; Barbi, I. A Family of ZVS-PWM Active-Clamping DC-to-DC Converters: Synthesis, Analysis, Design, and Experimentation. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **1997**, *44*, 698–704. [CrossRef]
21. Zhao, Y.; Li, W.; He, X. Single-phase improved active clamp coupled inductor-based converter with extended voltage doubler cell. *IEEE Trans. Power Electron.* **2012**, *27*, 2869–2878. [CrossRef]
22. Hwz, K.I.; Yau, Y.T. High step-up converter based on coupling inductor and bootstrap capacitors with active clamping. *IEEE Trans. Power Electron.* **2014**, *29*, 2655–2660.
23. Zhao, Q.; Lee, F.C. High-efficiency, high step-up DC-DC converters. *IEEE Trans. Power Electron.* **2003**, *18*, 65–73. [CrossRef]
24. Van de Sype, D.M.; De Gusseme, K.; Renders, B.; Van den Bossche, A.R.; Melkebeek, J.A. A single switch boost converter with a high conversion ratio. In Proceedings of the Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005, Austin, TX, USA, 6–10 March 2005; pp. 1581–1587.
25. Hsieh, Y.P.; Chen, J.F.; Liang, T.J.; Yang, L.S. Novel high step-up DC–DC converter with coupled-inductor and switched-capacitor techniques. *IEEE Trans. Ind. Electron.* **2011**, *59*, 998–1007. [CrossRef]
26. Liang, T.J.; Chen, S.M.; Yang, L.S.; Chen, J.F.; Ioinovici, A. Ultra-large gain step-up switched-capacitor DC-DC converter with coupled inductor for alternative sources of energy. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2012**, *59*, 864–874. [CrossRef]
27. Spiazzi, G.; Mattavelli, P.; Costabeber, A. Effect of parasitic components in the integrated boost-flyback high step-up converter. In Proceedings of the 2009 35th Annual Conference of IEEE Industrial Electronics, Porto, Portugal, 3–5 November 2009; pp. 420–425.
28. Wai, R.J.; Lin, C.Y.; Duan, R.Y.; Chang, Y.R. High-efficiency DC-DC converter with high voltage gain and reduced switch stress. *IEEE Trans. Ind. Electron.* **2007**, *54*, 354–364. [CrossRef]
29. Tseng, K.C.; Lin, J.T.; Huang, C.C. High step-up converter with three-winding coupled inductor for fuel cell energy source applications. *IEEE Trans. Power Electron.* **2014**, *30*, 574–581. [CrossRef]
30. Hu, X.; Gong, C. A high voltage gain DC–DC converter integrating coupled-inductor and diode–capacitor techniques. *IEEE Trans. Power Electron.* **2013**, *29*, 789–800.
31. Deng, Y.; Rong, Q.; Li, W.; Zhao, Y.; Shi, J.; He, X. Single-switch high step-up converters with built-in transformer voltage multiplier cell. *IEEE Trans. Power Electron.* **2012**, *27*, 3557–3567. [CrossRef]
32. Chen, S.M.; Liang, T.J.; Yang, L.S.; Chen, J.F. A cascaded high step-up DC–DC converter with single switch for microsource applications. *IEEE Trans. Power Electron.* **2010**, *26*, 1146–1153. [CrossRef]
33. Dwari, S.; Parsa, L. An efficient high-step-up interleaved DC–DC converter with a common active clamp. *IEEE Trans. Power Electron.* **2010**, *26*, 66–78. [CrossRef]
34. Li, W.; Zhao, Y.; Deng, Y.; He, X. Interleaved converter with voltage multiplier cell for high step-up and high-efficiency conversion. *IEEE Trans. Power Electron.* **2010**, *25*, 2397–2408. [CrossRef]