

Review

Research on the Reliability of Threshold Voltage Based on GaN High-Electron-Mobility Transistors

Pengfei Dai ¹, Shaowei Wang ² and Hongliang Lu ^{2,*} ¹ Nanjing Electronic Devices Institute, Nanjing 210016, China; iamdaipengfei@163.com² Key Laboratory for Wide Band Gap Semiconductor Materials and Devices of Education Ministry, School of Microelectronics, Xidian University, Xi'an 710071, China; wsw97382810@163.com

* Correspondence: hllv@mail.xidian.edu.cn

Abstract: With the development of high-voltage and high-frequency switching circuits, GaN high-electron-mobility transistor (HEMT) devices with high bandwidth, high electron mobility, and high breakdown voltage have become an important research topic in this field. It has been found that GaN HEMT devices have a drift in threshold voltage under the conditions of temperature and gate stress changes. Under high-temperature conditions, the difference in gate contact also causes the threshold voltage to shift. The variation in the threshold voltage affects the stability of the device as well as the overall circuit performance. Therefore, in this paper, a review of previous work is presented. Temperature variation, gate stress variation, and gate contact variation are investigated to analyze the physical mechanisms that generate the threshold voltage (V_{TH}) drift phenomenon in GaN HEMT devices. Finally, improvement methods suitable for GaN HEMT devices under high-temperature and high-voltage conditions are summarized.

Keywords: GaN HEMT; V_{TH} drift; high temperature and high voltage



Citation: Dai, P.; Wang, S.; Lu, H. Research on the Reliability of Threshold Voltage Based on GaN High-Electron-Mobility Transistors. *Micromachines* **2024**, *15*, 321. <https://doi.org/10.3390/mi15030321>

Academic Editors: Milka Potrebic and Dejan Tošić

Received: 21 January 2024
Revised: 17 February 2024
Accepted: 20 February 2024
Published: 25 February 2024



Copyright: © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

The high-electron-mobility transistor (HEMT) is a heterojunction field-effect transistor that generates a conducting channel through the formation of a high concentration of two-dimensional electron gas (2DEG) at the heterojunction, thus realizing the conduction of the device [1–3]. At the same time, GaN material has a strong, spontaneous, and piezoelectric polarization effect; this characteristic can improve the density and mobility of 2DEG in the HEMT structure [4]. So, GaN-based HEMTs have become a hot spot in the field of RF/Microwave Filtering and power switching devices.

A lot of breakthroughs have been made in research targeting GaN HEMT devices. Miller et al. [5] designed a temperature-dependent ASM-HEMT for modeling GaN HEMTs at elevated temperatures that can accurately capture DC and RF measurements collected at different temperatures. Sahebghalam et al. [6] studied and proposed a physically based analytical model for HEMTs that can be operated continuously from room temperature to high temperatures in both linear and saturated states. Khan et al. [7] theoretically and experimentally analyzed the temperature dependence of 2DEG for AlGaIn/GaN HEMTs and AlGaIn/InGaIn/GaN pHEMTs. Wu et al. [8] studied the time-resolved threshold voltage (V_{TH}) instability of 650-V Schottky-type gate GaN HEMTs under high-temperature gate bias conditions. By applying forward and reverse bias conditions, it was found that the V_{TH} of GaN HEMTs shifted negatively under high-temperature forward gate bias and positively under high-temperature reverse gate bias. Nuo et al. [9] proposed a time-resolved extraction method for studying the V_{TH} evolution of Schottky-type gate GaN HEMTs biased at a high V_{DS} . The gate heterostructures of p-GaN gate HEMTs are Schottky-type gates and ohmic-type gates [10,11]. The Schottky-type contact formation causes the p-GaN body to electrically float [12], which leads to the threshold voltage (V_{TH}) instability problem.

The ohmic-type gate HEMT has also been found to exhibit less severe V_{TH} instability after stress [13], but it requires large gate drive currents and specially designed gate drive circuits. Wei et al. [12] studied the V_{TH} evolution of GaN HEMTs with a drain-induced dynamic V_{TH} shift in GaN HEMTs with Schottky gate contacts and explained the underlying mechanism with a charge storage model. Tang S. W. et al. [14] investigated gate current characteristics to explain the phenomenon of threshold voltage shift in AlGaIn/GaN HEMTs with p-GaN gates. The threshold voltage shift was observed by applying a positive gate bias for a set stress time, and consistent trap energy levels with activation energies of $E_A \sim 0.6$ eV were found. Tang S. W. et al. [15] reported the capacitance-dependent stability of V_{TH} in p-GaN power HEMTs under high dV_G/dt conditions. It was also found that the charging capacitance due to displacement current directly affects the V_{TH} stability in high dV_G/dt events. Zhou X. et al. [16] investigated the effect of total ionizing doses (TIDs) on the dynamic V_{TH} in p-GaN HEMTs. A non-monotonic dependence of V_{TH} on dynamic gate stress was observed, indicating the mechanism of the effect of irradiation damage on metal/p-GaN/AlGaIn. Finally, the variations in gate current, drain leakage, and gate capacitance were provided in order to verify the mechanism. Chen J. et al. [17] investigated the device stability of p-GaN gate HEMTs under self-heating effects using the on-drain current injection technique. By analyzing the gate leakage current as well as simulating the TCAD of the electrically heated device, it was shown that the self-heating-induced V_{TH} instability is electron trapping in the p-GaN gate stack. In order to analyze the V_{TH} degradation mechanism of AlGaIn/GaN HEMTs with hot-electron stress (HES) in the semi-conducting state, Lin J. H. et al. [18] proposed a complete V_{TH} mechanism model. By analyzing the characteristic curves of drain current versus gate voltage (I_D - V_G), it was found that V_{TH} shifts in the positive direction after stress. However, an instability of V_{TH} in the positive direction was observed even after recovery. In addition, light experiments and Silvaco simulations were performed to verify the accuracy of the proposed model. However, the problem of GaN HEMT V_{TH} drift still has not been effectively addressed. Threshold instability seriously affects the switching speed of GaN power devices, which introduces unpredictable timing delays and reduces the power switching efficiency to the point of failure. Therefore, the study of GaN HEMT threshold drift and its mechanism is necessary.

In this paper, a review of previous work is presented. The existing methods for analyzing V_{TH} drift are studied. The variation rule of V_{TH} under the switching stress conditions of GaN HEMT devices is analyzed, and the variation rule of V_{TH} under variable temperature conditions of GaN HEMT devices is also analyzed. Finally, a method for effectively improving the structure of GaN HEMT devices is presented.

2. Factors Affecting V_{TH} Drift

In RF power-switching circuit applications, with a low on-resistance and high transconductance of the device, GaN HEMT devices fully open only the conducting channel at high gate voltages [19]. To ensure that the gate voltage is in a safe operating range, the magnitude of the gate leakage current needs to be small. As seen in Table 1 [20], the safe operating gate voltage range of a GaN HEMT that satisfies the above two conditions is only 1 to 2 V. Therefore, the drift in V_{TH} not only affects the switching speeds and the characteristic parameters of GaN HEMTs but also influences the safe gate voltage range of the devices. Therefore, GaN HEMT threshold instability is a critical issue that needs to be solved to promote the application of GaN HEMTs in power circuits and systems.

Table 1. Gate characteristics of different GaN devices.

Manufacturer	V_{TH} (V)	$V_{GSmin} \sim V_{GSmax}$ (V)	Gate Drive Voltage (V)
EPC [21]	1.4	−4~6	4~5
Panasonic [22]	1.2	−10~4.5	3~5
GaN System [23]	1.3	−10~7	5~6.5

2.1. Effect of Switching Stress

Nowadays, GaN HEMTs exist in various device structures, as shown in Figures 1–3 [24–26]. When the device is under switching stress conditions, the body defects and interface defects in the device may capture electrons or holes. When the release of electrons or holes from deep energy level defects does not keep up with the switching response frequency, it causes the charge distribution in the gate region of the GaN HEMT power device to change, leading to a change in V_{TH} as well [27].

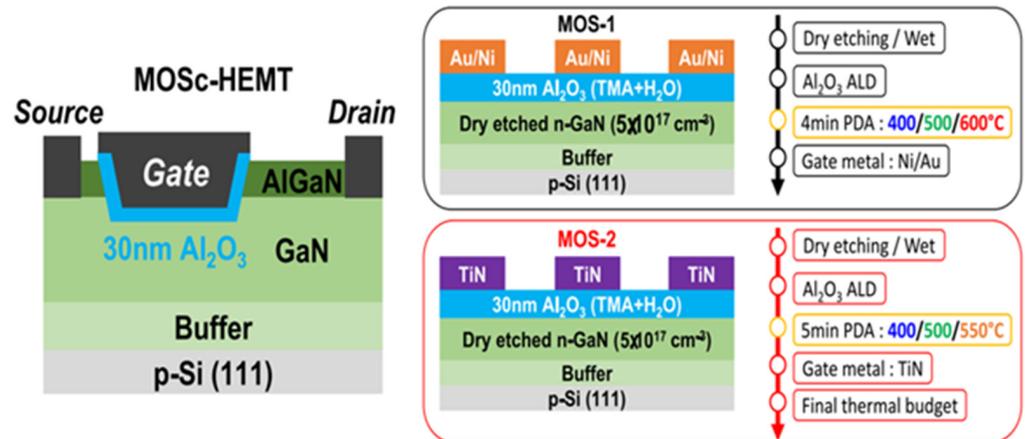


Figure 1. Schematic diagram of MOSc HEMT and a schematic diagram and process flow of MOS-1 and MOS-2 [24].

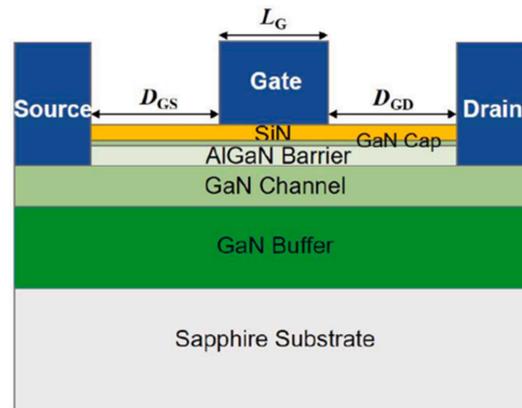


Figure 2. Cross-section of the proposed MIS-HEMT with a SiN passivation layer [25].

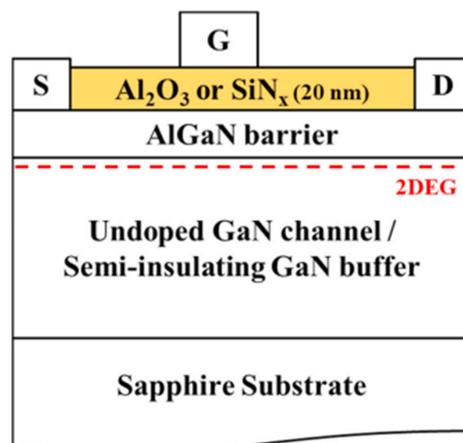


Figure 3. Different gate dielectric layers.

Myeongsu Chae et al. [28] investigated the degradation of a p-GaN gate induced by forward gate voltage stress in a GaN HEMT with a Schottky-type p-GaN gate. The results of the study are presented in Figure 4. A positive shift in V_{TH} occurred during the stress test at $V_G = 2$ V. However, a negative offset of V_{TH} was observed during the stress test at $V_G = 8$ V.

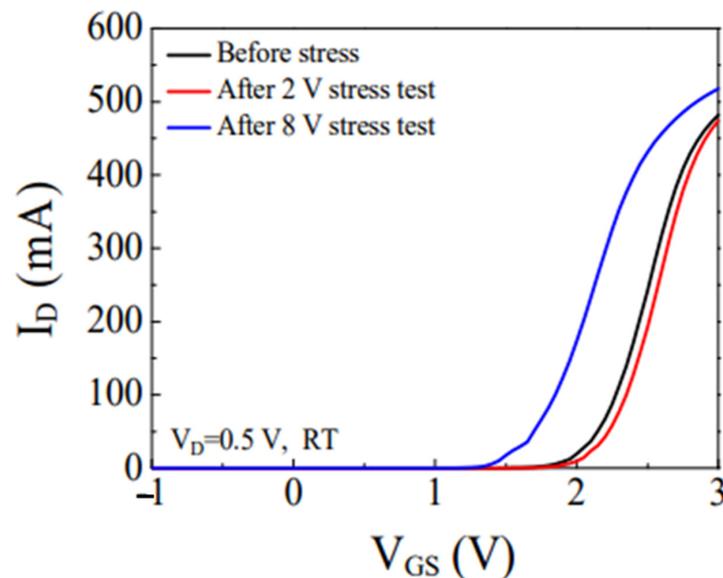


Figure 4. I_D - V_G characteristics of a p-GaN gate HEMT before and after different gate voltage stress tests at room temperature [28].

Wang et al. [20] measured the pulse transfer characteristics of GaN HEMT devices with V_{DS} set at 1 V. Additionally, to assess the stability of V_{TH} under forward gate bias voltage, the pulse transfer characteristics were measured at positive V_{GSQ} (up to 8 V) and V_{DSQ} (0 V). The V_{DSQ} value of 0 V was intended to allow for an even distribution of the 2DEG channel voltage to ensure symmetry in the gate toward the source and drain sides. In this experiment, it was observed that the value of V_{TH} increased as the V_{GSQ} increased.

Meneghini et al. [29] measured the pulse transfer characteristics of a GaN HEMT device for a V_{DS} value of 5 V. As shown in Figure 5, it was found that the value of V_{TH} decreased with an increase in V_{GSQ} .

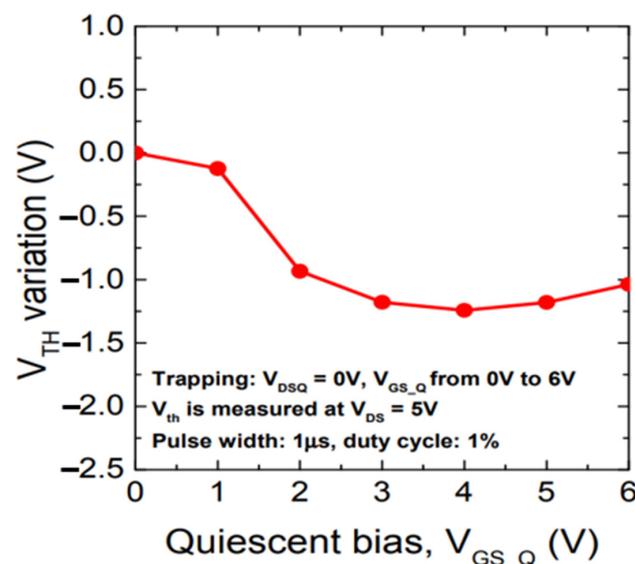


Figure 5. The trend in the threshold voltage change [29].

Loizos Efthymiou et al. [30] investigated the threshold voltage instability that occurs in p-GaN-gated AlGaIn/GaN-on-Si HEMT devices under off-state drain stress. The threshold voltage drift could increase by up to 40% under drain bias conditions of less than 50 V. This was attributed to the phenomenon where, under off-state conditions, high drain bias conditions caused the Mg receptor to ionize, generating a positive V_{TH} offset charge through contact with the gate. However, the increase in threshold voltage at drain biases greater than 50 V appeared to saturate.

Luca Sayadi et al. [31] investigated the effect of gate contact on threshold voltage stability in p-GaN gate GaN HEMTs using double-pulse measurements of p-GaN gate devices. It was found that in the case of high-leakage Schottky contacts, the accumulation of holes in the p-GaN region leads to a negative shift in the threshold voltage. On the contrary, in the case of low-leakage Schottky contacts, hole depletion in the p-GaN region caused a positive threshold voltage shift.

Lai Y. C. et al. [32] investigated the shutdown state characteristics of 650 V-enhanced p-GaN gate AlGaIn/GaN HEMTs after applying different levels of gate stress bias. As shown in Figure 6, the threshold voltage exhibited a positive bias at low gate stresses and a negative bias at gate stresses greater than 6 V.

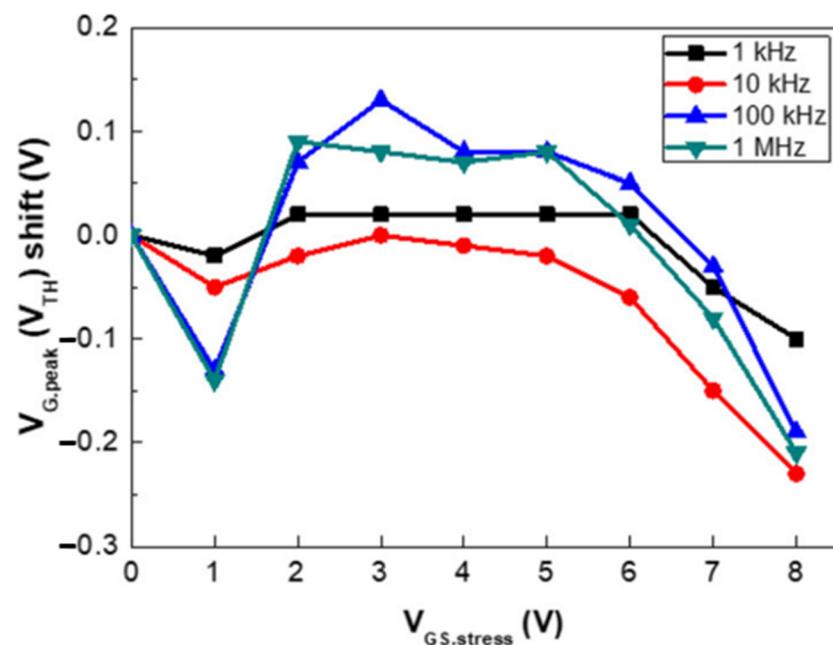


Figure 6. V_{TH} offset relative to different gate stress voltages [32].

Favero D. et al. [33] investigated in detail the effect of electronic gate leakage on the stability of the threshold voltage of normally turned-off GaN HEMTs using p-GaN gates. The analysis was based on a combination of DC, pulsed, and transient measurements conducted on two test wafers with different gate processes, leading to varying levels of gate leakage currents. In Figure 7, the drift results of the threshold voltage for the different cases are shown.

From the above discussion, it is evident that the gate drive voltage can cause a GaN HEMT device to experience current collapse and V_{TH} instability. It is also observed that the off-state bias stress affects not only the dynamic on-resistance but also the stability of the threshold voltage. The shift in V_{TH} of the Schottky contact at the p-GaN gate under high- and low-leakage conditions is also investigated. Negative threshold voltage offsets can result in false conduction, which can significantly impact the overall performance of the circuit. Positive threshold voltage offsets can affect the on-resistance of the device, leading to a degradation in the performance of the power switching circuit. Next, the reasons for these phenomena will be analyzed and discussed.

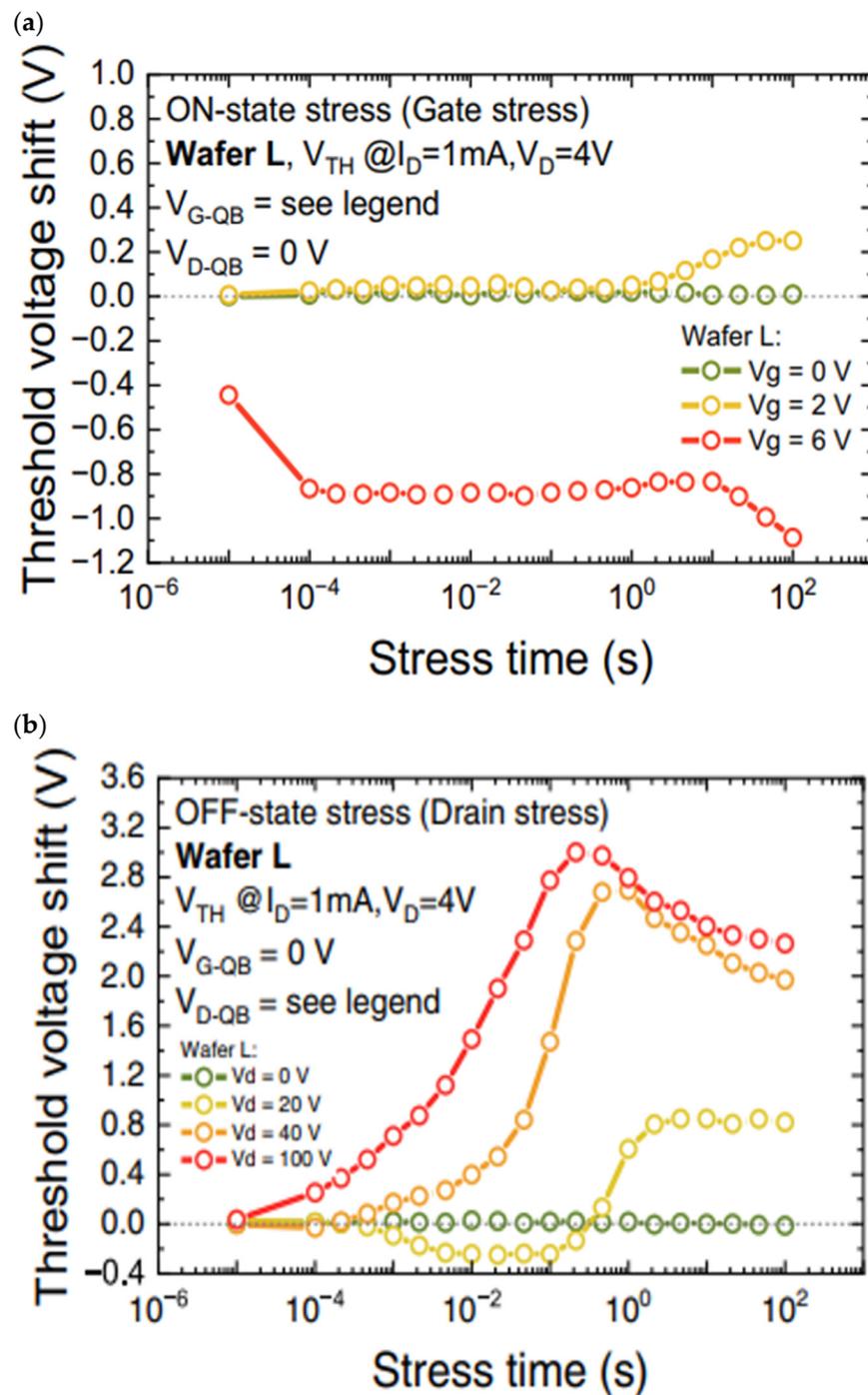


Figure 7. Threshold voltage drift case: (a) low gate voltage and (b) high gate voltage [33].

2.2. Effects of Thermal Stress

At present, p-GaN gate HEMT devices are widely used in high-power applications, such as fast chargers and universal power supplies (UPSs) [34,35]. As the chip area continues to shrink, devices become more and more compact, leading to an increase in their temperature. In Figure 8, the heat flux density of various heat sources is displayed. It can be seen that the heat flux density of the GaN HEMT is three times higher than that of silicon-based IGBTs [36]. Therefore, in order to enhance the gate stability and reliability of p-GaN gate HEMTs, it is essential to investigate the temperature dependence on V_{TH} instability and its underlying physical mechanisms.

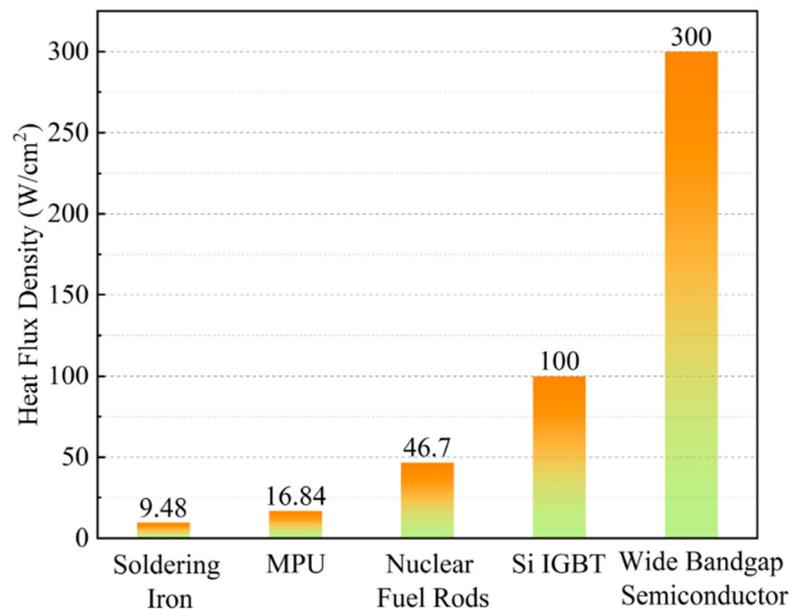


Figure 8. Heat flux density of different heat sources [36].

Kaihong Wang et al. [36] investigated the variation rules of saturation voltage with low current injection, threshold voltage, and diode voltage drop with temperature for a GaN-HEMT. In Figure 9, the V_{th} - T_j curves are displayed for various currents. It can be seen from the figure that V_{th} increases with temperature at a constant current.

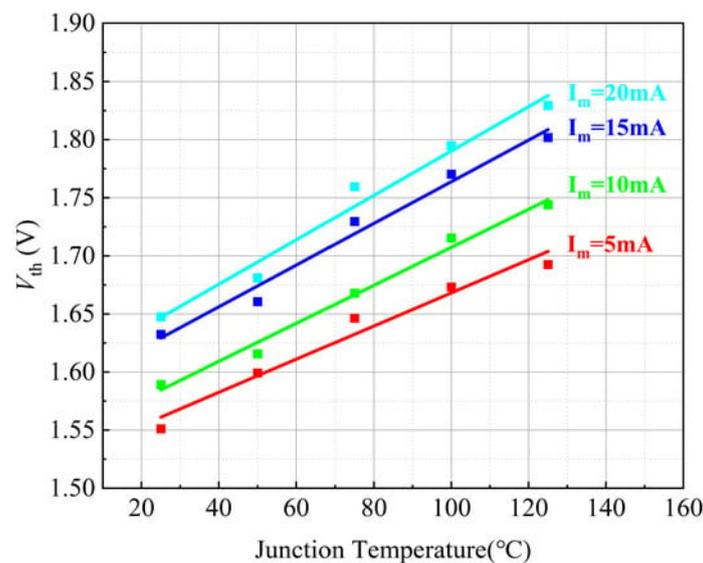


Figure 9. Relationship between V_{TH} and junction temperature under different current conditions [36].

Hao Wu et al. [8] investigated time-resolved threshold voltage instability under high-temperature gate bias. Under the application of high-temperature forward gate bias conditions (HTGB), the threshold voltage of a p-GaN-AlGa_N/GaN-HEMT showed a negative shift, which could be attributed to the defects present in the AlGa_N layer. Under the application of high-temperature reverse gate bias conditions (HTRB), the threshold voltage of the device exhibited a positive shift. This shift was attributed to the accelerated movement of holes in the p-GaN layer and electrons trapped within the AlGa_N layer at elevated temperatures, which in turn accelerated the inter-particle complexation. This also indicated that the positive threshold voltage shift under HTRB showed a positive correlation with temperature.

Under thermal stress conditions, Wang et al. [37] studied the phenomenon of V_{TH} shift in GaN HEMTs based on an ohmic-type gate and a Schottky-type gate. The variation in V_{TH} shift with temperature was tested for both Schottky-type gate devices and ohmic-type gate devices when V_{DS} was set to 5 V. The GaN HEMT device with a Schottky-type gate showed an increase in the value of V_{TH} as the temperature increased. The GaN HEMT device with an ohmic-type gate showed a decrease in the value of V_{TH} as the temperature increased.

Pilati M. et al. [38] investigated the effects of low- and high-temperature operating life (LTOL and HTOL) of GaN HEMTs for RF applications. Based on several stress experiments conducted at various temperature levels, the presence of two degradation modes—negative and positive shifts in the threshold voltage—was demonstrated. The results of the threshold voltage shift are presented in Figure 10.

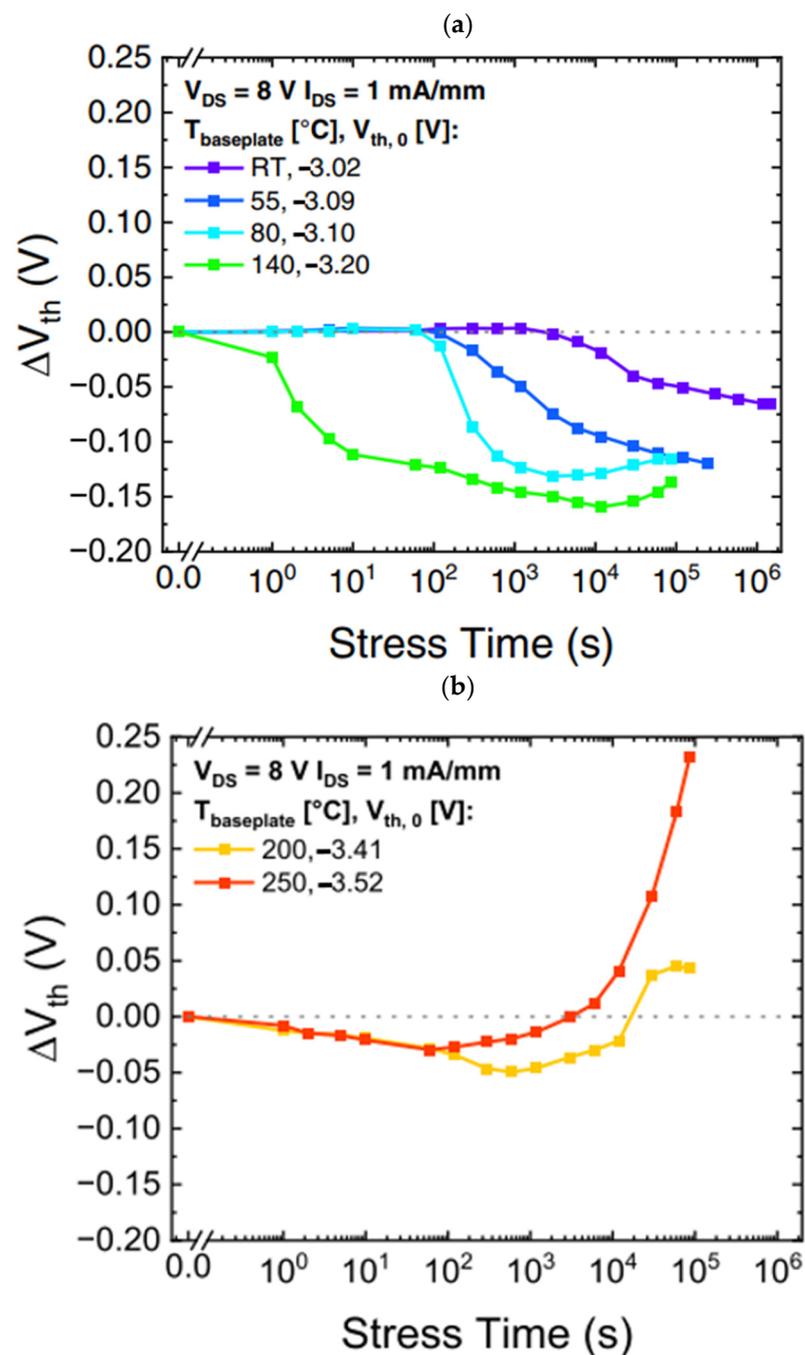


Figure 10. Threshold voltage shift [38]: (a) negative shift and (b) positive shift.

Based on the above analysis, the threshold voltage exhibited a negative drift phenomenon under the HTGB condition. Under the HTRB condition, the threshold voltage exhibits a positive drift phenomenon. Not only that, but the difference in threshold voltage drift between Schottky gate devices and ohmic gate devices occurs under varying temperature conditions. The devices vary in their performance based on changes in the operating environment. The effect of temperature difference on the threshold voltage of the devices is also an important factor to study. In the next section, the effect of temperature on the threshold voltage of devices and variations among different devices will be analyzed and summarized.

3. Reasons for V_{TH} Drift

V_{TH} drift is affected by switching and thermal stresses. However, there is uncertainty regarding the direction of the V_{TH} drift, which significantly limits the application of GaN HEMT devices. Therefore, there is a need to investigate the V_{TH} drift phenomenon in GaN HEMT devices.

3.1. Analysis of Switching Stresses

In order to analyze the gate voltage distribution of GaN HEMT devices, Tallarico et al. [39] proposed a schematic diagram illustrating the equivalent diode distribution of GaN HEMT gates. In this experiment, it was found that the GaN HEMT gate mainly consists of two back-to-back diodes in series. When $V_G > 0$ V, Schottky diode D1 is reverse-biased, and the p-GaN/AlGaIn/GaN diode D2 is forward-biased. The voltages across diodes D1 and D2 are denoted as V_1 and V_2 , respectively. The gate voltage (V_G) is the sum of V_1 and V_2 .

In order to analyze the mode of electron and hole transport at the gate of GaN HEMT devices, the Space Charge-Limited Conduction (SCLC) model was utilized to simulate the gate current pattern in relation to the voltage.

When the GaN HEMT conducting channel is not open (OFF region, $V_G < V_{TH}$), the gate voltage V_G is mainly supported by diode D2. The voltage value of V_2 is much larger than that of V_1 .

When $V_{TH} < V_G < V_{SAT}$ (ON-I area), the conducting channel of the GaN HEMT is not yet saturated. The negative charge near the gate of the device increases. As the negative charge repels the channel electrons, it results in a positive shift in the V_{TH} of the GaN HEMT.

When $V_{SAT} < V_G < V_{GT}$ (ON-II area), the conducting channel of the device is saturated. When the voltage across diode D2 saturates, the main gate voltage is then carried by diode D1. The negative charge near the gate increases, causing the V_{TH} of the device to continue drifting forward.

When $V_G > V_{GT}$, holes are injected from the gate metal, and some of them cross the potential barrier into the channel. This process leads to an accumulation of positive charge near the gate. When V_G is much larger than V_{GT} , many holes are injected, causing the V_{TH} of the device to drift negatively.

In order to validate the methodology's accuracy, Yuanyuan Shi et al. [40] examined the off-state gate current (I_G-V_D) and leakage current (I_D-V_D) of GaN HEMTs when V_G is set to 0 V. The experiment revealed that when V_{GSQ} is less than 6 V, the off-state leakage current I_D-V_D curves of GaN HEMT devices after the initial scan align with the pre-stress off-state leakage current curves. When V_{GSQ} exceeds 6 V, the gate stress triggers the GaN HEMT device to switch on, leading to the injection of holes from the gate into the GaN channel. After the gate stress dissipates, the holes injected into the GaN channel combine with electrons, resulting in a significant increase in I_D . In this experiment, it was observed that the off-state I_D-V_D curve during the second scan almost perfectly aligns with the pre-stress I_D-V_D curve. This indicates that the holes injected into the channel attract channel electrons, causing the V_{TH} to shift negatively.

In order to investigate the effect of gate contact on threshold voltage stability, Luca Sayadi et al. [31] fabricated ohmic-gate and Schottky-gate p-GaN HFETs. The results

of double-pulse gate stress measurements and device simulations were analyzed and compared between the two types of gates. This analysis was conducted using double-pulse gate stress measurements and extensive device simulations. In the case of ohmic gate contacts, V_{TH} was consistently negative and increased in magnitude with higher gate stress voltage. In the case of Schottky gate contacts, the threshold voltage offset was nonlinear with the applied gate stress voltage. In their study, it was found that the variation in the threshold voltage was mainly related to the hole tunneling current through the Schottky barrier and the hot ion current through the AlGaIn barrier. To verify the reliability of the experiments, a negative threshold voltage shift was tested and found in the case of a high-leakage Schottky contact. A positive threshold voltage shift was tested and found in the case of a low-leakage Schottky contact. The proposed theory effectively explains the experimental phenomenon.

In Figure 11, the mechanism of the device's threshold voltage instability is shown. The symbol (a) indicates hole depletion in p-GaN, leading to a positive V_{TH} drift. The symbol (b) indicates electron trapping at the AlN/GaN interface and/or in the AlN trap, suggesting a positive V_{TH} drift. The symbol (c) denoted hole accumulation in 2DHG and the subsequent hole trapping in AlGaIn, leading to negative V_{TH} drift. The symbol (d) indicates hole trapping in the GaN buffer, leading to a negative drift in V_{TH} . The symbol (b1) represents the mechanism that occurs in the wafer to stabilize the V_{TH} . This also indicates the presence of four different charge-trapping processes, whose interactions determine the sign and magnitude of the threshold voltage change. A moderate increase in gate leakage helped eliminate negative threshold voltage instability under positive gate bias and significantly reduced positive threshold shift under off-state stress.

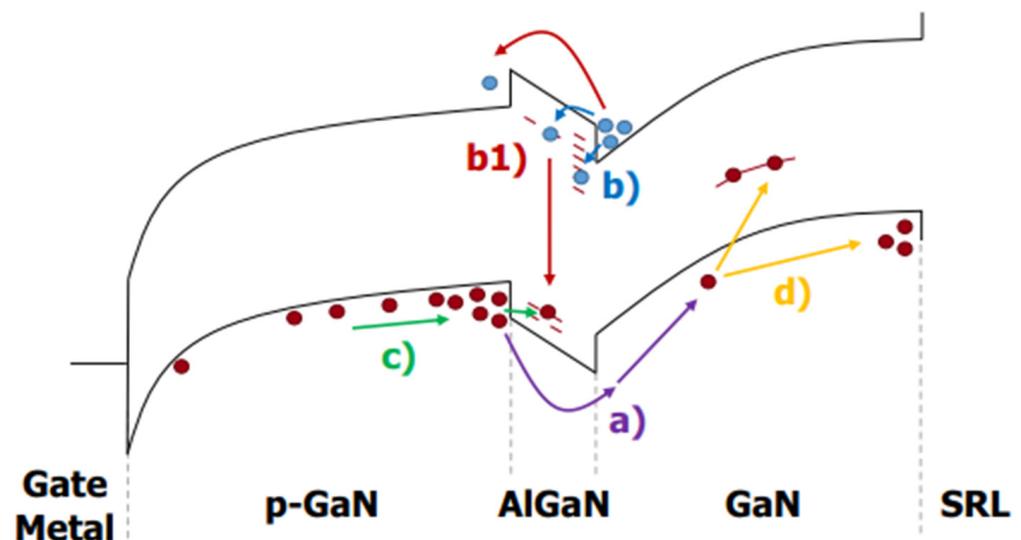


Figure 11. Mechanism of device threshold voltage instability [32].

Based on the above discussion, the phenomenon of threshold voltage drift in GaN HEMTs under forward gate stress is analyzed for the first time. The gate voltage is divided into three regions, and the gate current is divided into electron and hole currents. The movement in the threshold voltage at different stages is analyzed using the SCLC theory. It is summarized that when $0\text{ V} < V_G < 6\text{ V}$, the main reason for the forward drift in the threshold voltage is the predominant electron capture in the AlGaIn barrier. At $6\text{ V} < V_G < 9\text{ V}$, the negative shift in the threshold voltage is primarily due to dominant hole capture in the AlGaIn barrier and hole injection into the GaN buffer. In addition, the impact of high-leakage Schottky contacts and low-leakage Schottky contacts on the threshold voltage drift is also analyzed. Under gate stress, the device experiences negative threshold voltage drift in the case of high-leakage Schottky contacts due to the accumulation of holes in the p-GaN region. On the contrary, in the case of low-leakage Schottky contacts, the negative threshold

voltage drift is hole depletion in the p-GaN region. Overall, the varying leakage of the device under gate stress conditions results in a modification of the total charge stored in the p-GaN region, leading to a shift in the threshold voltage.

3.2. Analysis of Thermal Stress

In order to analyze the relationship between the ohmic-type gate devices, the Schottky-type gate devices, and V_{TH} drift, Wang et al. [37] tested and analyzed the relevant characteristics of ohmic gate devices and Schottky gate devices.

In the experiments, the characteristic parameters of an ohmic-type gate device were demonstrated. The I-V characteristics between two contact pads with different channel distances were shown. The test revealed a knee point voltage, which may have been caused by the surface of the GaN material being affected during the fabrication of the device [37]. It was shown that the presence of the knee voltage (V_{Knee}) makes the effective bias on the p-i-n junction (V_{p-i-n}) smaller than the applied gate bias (V_{Bias}), which, in turn, affects the conduction of the ohmic-type gate device. The voltage values of V_{Knee} under various temperature conditions were displayed. It could be visualized that in ohmic-type devices, the value of V_{Knee} decreases with increasing temperature. The relationship between V_{PIN} and temperature was demonstrated. It was found that the value of V_{PIN} varies less with different temperatures. V_{TH} comprised V_{Knee} and V_{PIN} . Therefore, the ohmic-type gate device showed a negative shift in the V_{TH} under high-temperature conditions.

In the experiment, the characteristic parameters of the Schottky-type gate device were demonstrated. It was found that when the bias voltage is within the range of 0–2 V, most of the applied gate bias voltage is taken by the P-I-N junction. At bias voltages greater than 2 V, the MS junction begins to absorb some of the voltage. As the bias voltage exceeds 4.5 V, the MS junction begins to bear more of the bias voltage than the P-I-N junction. It was also observed that as the temperature increases, the V_{MS} shows an increasing trend, while the V_{p-i-n} shows a decreasing trend. It was shown that V_{p-i-n} decreases as the temperature increases at a constant gate bias. A trend of gradual increase in V_{TH} with increasing temperature was observed. This indicates that the device needs to apply a larger bias voltage to the gate to maintain sufficient V_{p-i-n} and open the channel at high temperatures. This was the reason why the Schottky-type gate device showed positive V_{TH} drift at high temperatures.

For 650 V Schottky-type p-GaN gate HEMT devices, Hao Wu et al. [8] conducted forward and reverse bias experiments under various temperature conditions. Their study also investigates how changes in temperature affect the threshold voltage offset under reverse gate bias conditions. It was summarized and found that under HTFB conditions, the tunneling effect induced by trapped cavities leads to a negative V_{TH} drift, which is independent of the temperature. Under HTRB conditions, the positive V_{TH} drift is primarily influenced by temperature. This was mainly due to the trapping of electrons by defects created through hole emission and hot holes. Also, the higher the temperature, the greater the positive V_{TH} drift.

Pilati M. et al. [38] found that a negative V_{TH} shift was attributed to the temperature and magnetic field-assisted electron de-trapping of the passivated/aluminum nitride stack under the gate, in agreement with previous reports. A positive V_{TH} shift occurred only at high temperatures and was due to the trapping of the passivated/aluminum nitride stack under the gate. In Figures 12–14, the movement of hot electrons through the device structure is depicted.

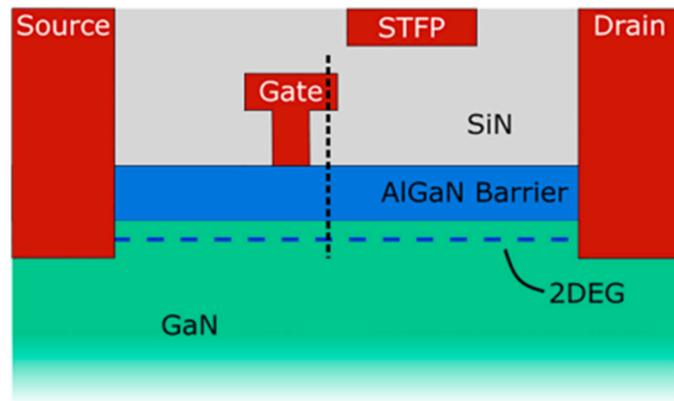


Figure 12. Simplified structure of the DUT [38].

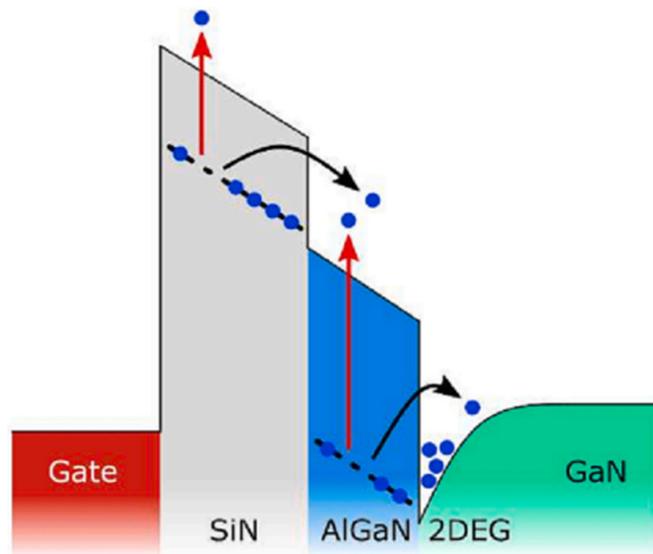


Figure 13. Band diagram at the gate stack, with temperature and field-assisted electron de-capture indicated by red and black arrows, respectively [38].

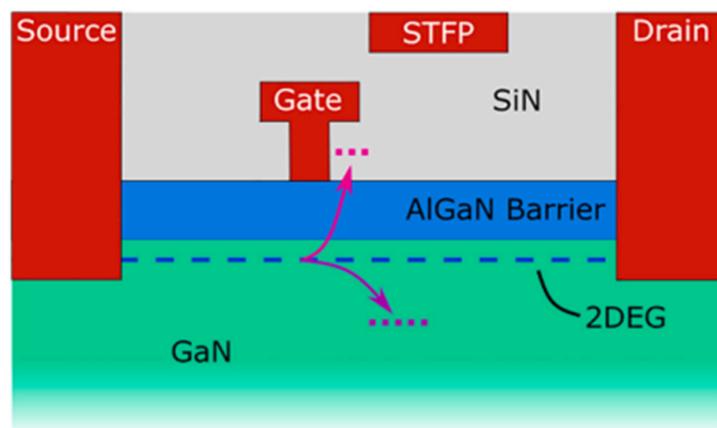


Figure 14. Visual representation of the hot electron capture location during the process [38].

In summary, Schottky-type gate devices exhibit a positive V_{TH} shift at high temperatures. This shift is primarily attributed to the rise in gate current caused by high temperatures. The increase in gate current results in a higher bias voltage across the Schottky metal/p-GaN junction in the device, consequently shifting the threshold voltage positively. A negative V_{TH} shift occurs in ohmic gate devices at high temperatures. This shift is primarily caused

by the increase in hole injection at high temperatures, leading to a decrease in the inflection voltage of the ohmic metal/p-GaN contact in ohmic devices. Consequently, this results in a negative shift in V_{TH} . Meanwhile, when applying forward and reverse bias voltages to Schottky gate devices under high-temperature conditions, it is observed that the threshold voltage of the Schottky gate p-GaN devices shifts negatively under forward gate bias. It is found that defects in the AlGaIn layer trap the accumulated 2D hole gas in the p-GaN layer near the p-GaN/AlGaIn interface. It can be determined that the negative shift in the threshold voltage under HTFB is independent of temperature. However, the threshold voltage of Schottky-gated p-GaN devices exhibits a positive shift under reverse gate bias. It is found that defects generated by thermal cavities at high temperatures trap hole emissions in the p-GaN layer and electrons within the AlGaIn layer. Thus, the conclusion that the positive threshold voltage shift at HTRB is temperature-dependent is obtained.

4. Conclusions and Future Perspectives

In this paper, a review of previous research is presented. The relationship between switching stress and V_{TH} drift is analyzed and discussed. It is also stated that the reverse turn-on of the gate Schottky junction plays a significant role in the rapid increase in the gate current in GaN HEMT devices. To minimize on-resistance, it is necessary to operate a GaN HEMT device in the ON-II area. Therefore, the optimization of the GaN HEMT gate structure aims to increase the gate voltage range between channel saturation and gate Schottky junction turn-on. The instability in the threshold voltage instability of p-GaN gate devices is examined using double-pulse measurements on Schottky-contacted p-GaN devices and compared with device simulations. It is shown that the threshold voltage depends on the balance between the hole-tunneling current through the Schottky barrier and the thermionic current through the AlGaIn barrier. This balance may result in a change in the total charge stored in the p-GaN, ultimately leading to a shift in the threshold voltage. The effect of the AlGaIn back-barrier is also investigated, and the results show an almost permanent but limited negative threshold voltage shift due to hole accumulation at the channel/back-barrier interface. The following optimization methods can be used to optimize the device structure: 1. The selection of a suitable metal is crucial to increase the height of the resulting metal/p-GaN Schottky barrier [41–43]. Figure 15 shows a Schottky barrier diode (SBD) structure with a double-barrier design that was proposed to achieve a low conduction AlGaIn/GaN SBD and an ultra-high breakdown voltage. In Figure 16, different SBD-type devices with the same physical dimensions are shown. In Figure 17, a detailed manufacturing procedure is shown. 2. Optimization of the p-GaN layer thickness and doping concentration to increase the voltage withstand capability of the layer [44]. In Figure 18a, details of the doping in a GaN layer are shown. In Figure 18b, an 80 nm thick undoped GaN layer is shown. 3. Insertion of a thin layer of AlN between the p-GaN/AlGaIn layers to restrict hole injection.

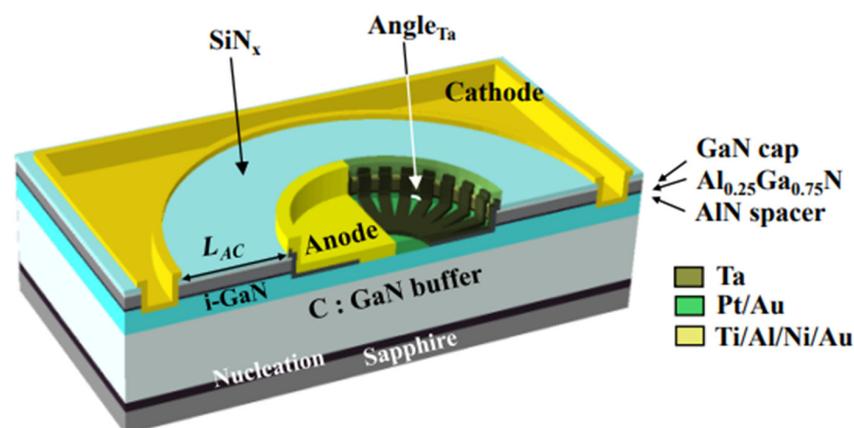


Figure 15. Schematic cross-section of an AlGaIn/GaN lateral SBD with a DBA structure on sapphire [43].

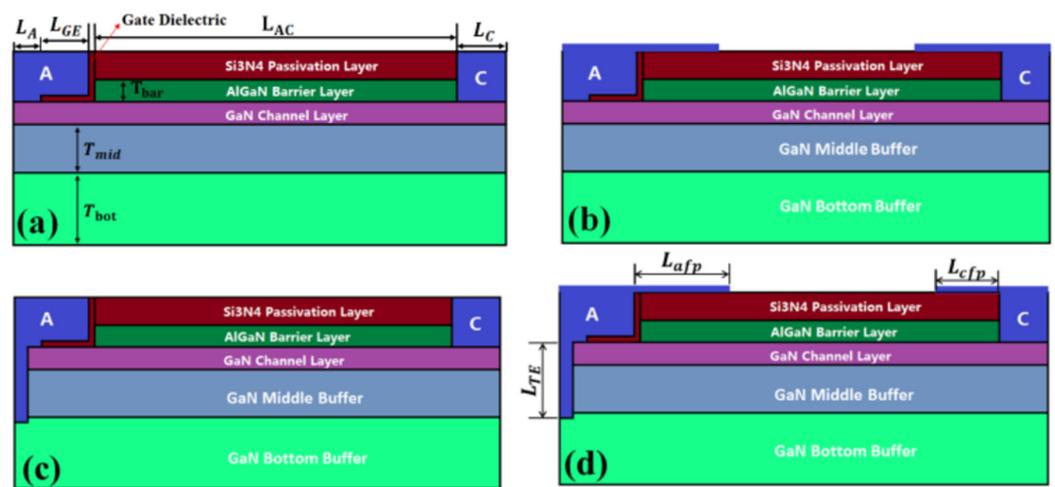


Figure 16. Cross-section: (a) SBD with gate edge termination, (b) SBD with gate edge termination in combination with a field plate, (c) T-type anode located deep in the buffer layer at the bottom of the SBD, and (d) T-anode in combination with a field plate located deep in the bottom buffer layer of the Schottky barrier diode [42].

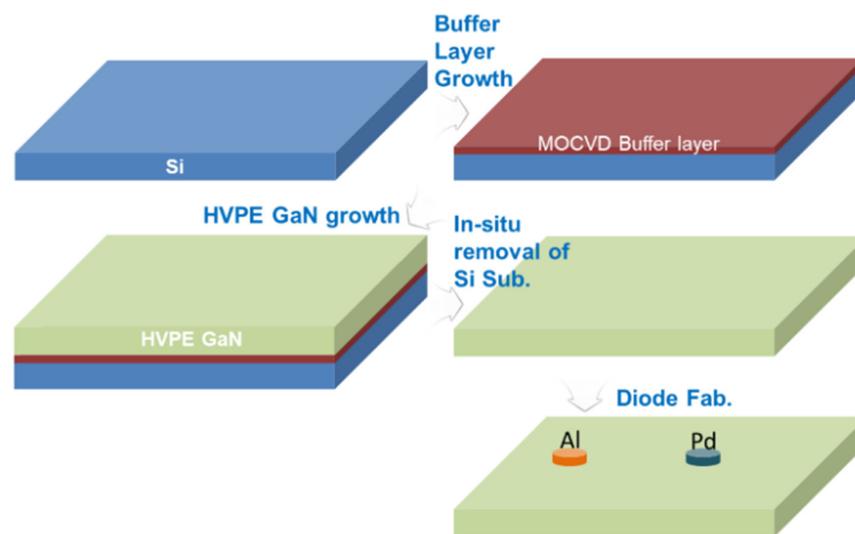


Figure 17. The preparation process of a Pd/Si-based FS-GaN Schottky diode [43].

In this paper, a review of previous research is presented. The V_{TH} shift in GaN HEMT devices with Schottky-type and ohmic-type gates at different temperatures is investigated. At elevated temperatures, ohmic-gated devices show a negative V_{TH} shift, which is attributed to the decrease in the inflection point voltage at the ohmic metal/ p^+ -GaN interface. As the temperature increases, a positive V_{TH} offset occurs in devices with Schottky-type gates. This is due to the increase in gate current at high temperatures, which causes a rise in voltage across the Schottky metal/ p -GaN junction. The time-resolved threshold voltage instability in Schottky-type p -GaN gate HEMTs has been investigated under HTFB and HTRB conditions. Under HTFB conditions, the negative shift in V_{TH} mainly comes from the tunneling effect induced by holes and is independent of temperature. Under HTRB conditions, the positive shift in V_{TH} is temperature-dependent due to electron trapping by defects created by hole emission and hot holes. The choice of gate metal material can be further optimized next, aiming to balance the relationship between output characteristics, V_{TH} , and reliability, which can achieve a greater breakthrough in device performance [45]. In Figure 19a, a proposed air-cavity-P-GaN connected HEMT is shown. In Figure 19b, an air-cavity-P-GaN separated HEMT is shown.

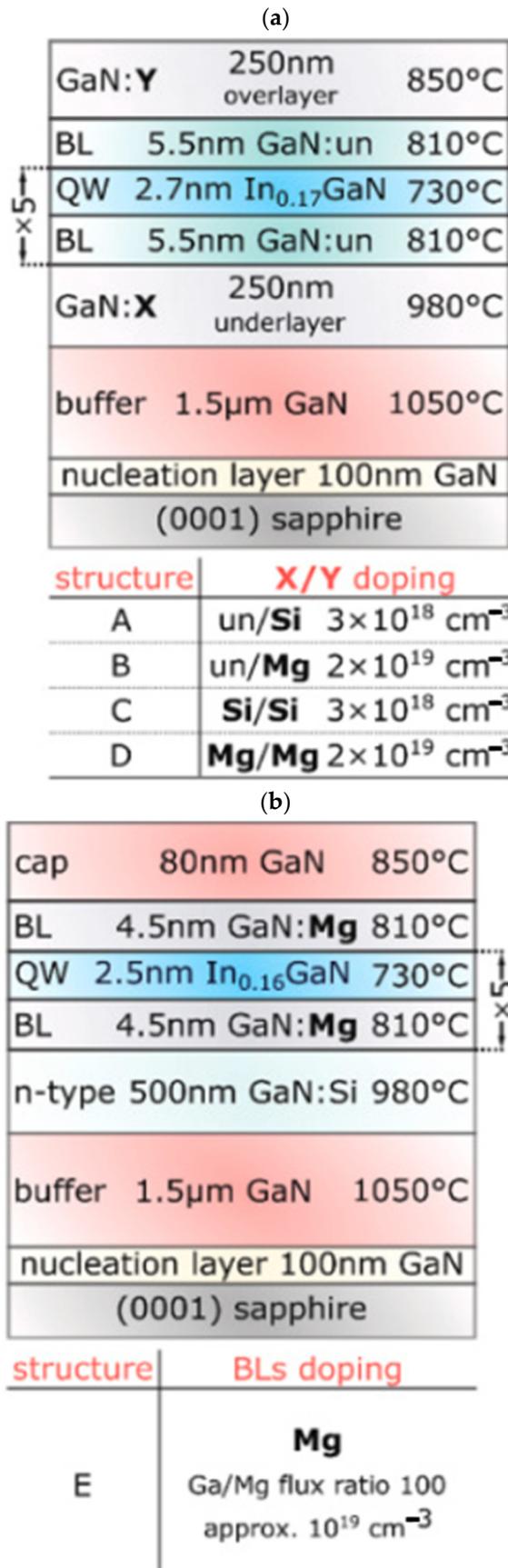


Figure 18. Schematic representation of an epitaxial structure with (a) different doping in the lower and upper GaN layers and (b) a Mg-doped barrier layer [44].

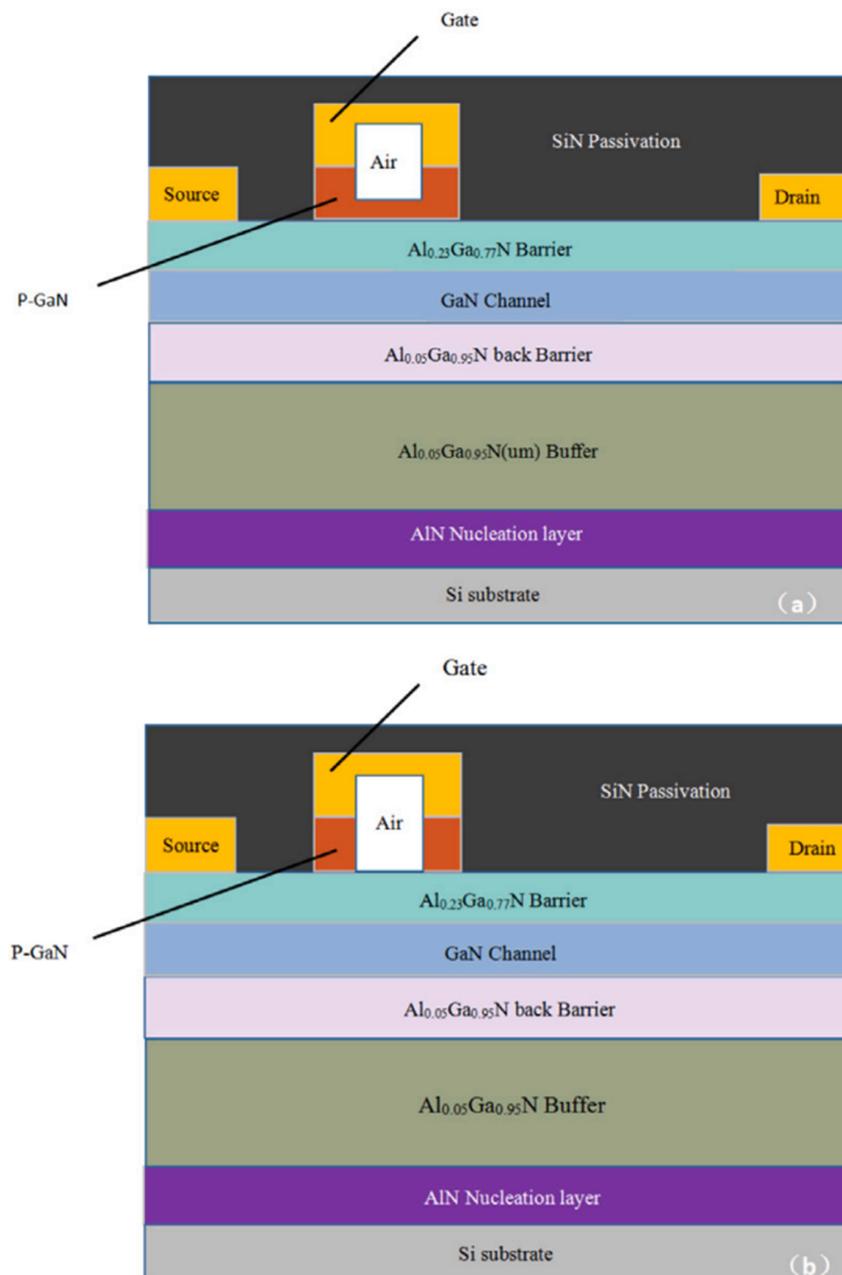


Figure 19. Schematic cross-sections of (a) AC-PC HEMT and (b) AC-PS HEMT [45].

Author Contributions: Conceptualization, P.D. and S.W.; methodology, P.D.; validation, P.D.; investigation, S.W.; resources, P.D.; data curation, H.L.; writing—original draft preparation, H.L.; writing—review and editing, H.L. and S.W.; visualization, S.W.; supervision, H.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: The data presented in this study are available upon request from the corresponding author.

Acknowledgments: The research cyberinfrastructure resources and services provided by the Key Laboratory for Wide Band Gap Semiconductor Materials and Devices of Education Ministry are gratefully acknowledged.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Khandelwal, S.; Goyal, N.; Fjeldly, T.A. A Physics-Based Analytical Model for 2DEG Charge Density in AlGaIn/GaN HEMT Devices. *IEEE Trans. Electron Devices* **2011**, *58*, 3622–3625. [CrossRef]
2. Swamy, N.S.; Dutta, A.K. Analytical Models for the 2DEG Density, AlGaIn Layer Carrier Density, and Drain Current for AlGaIn/GaN HEMTs. *IEEE Trans. Electron Devices* **2018**, *65*, 936–944. [CrossRef]
3. Shi, Y.; Chen, W.; Sun, R.; Liu, C.; Xin, Y.; Xia, Y.; Wang, F.; Xu, X.; Deng, X.; Chen, T.; et al. Modeling the Influence of the Acceptor-Type Trap on the 2DEG Density for GaN MIS-HEMTs. *IEEE Trans. Electron Devices* **2020**, *67*, 2290–2296. [CrossRef]
4. Lee, D.S.; Gao, X.; Guo, S.; Kopp, D.; Fay, P.; Palacios, T. 300-GHz InAlN/GaN HEMTs With InGaIn Back Barrier. *IEEE Electron Device Lett.* **2011**, *32*, 1525–1527. [CrossRef]
5. Miller, N.C.; Brown, A.; Elliott, M.; Gilbert, R.; Davis, D.T.; Islam, A.E.; Walker, D.; Hughes, G.; Liddy, K.; Chabak, K.D. An ASM-HEMT for Large-Signal Modeling of GaN HEMTs in High-Temperature Applications. *IEEE J. Electron Devices Soc.* **2023**, *11*, 531–538. [CrossRef]
6. Sahebghalam, N.; Shalchian, M.; Chalechale, A.; Jazaeri, F. High-Temperature HEMT Model. *IEEE Trans. Electron Devices* **2022**, *69*, 4821–4827. [CrossRef]
7. Khan, A.K.; Alim, M.A.; Gaquiere, C. 2DEG transport properties over temperature for AlGaIn/GaN HEMT and AlGaIn/InGaIn/GaN pHEMT. *Microelectron. Eng.* **2021**, *238*, 111508. [CrossRef]
8. Wu, H.; Fu, X.; Guo, J.; Wang, Y.; Liu, T.; Hu, S. Time-Resolved Threshold Voltage Instability of 650-V Schottky Type p-GaN Gate HEMT under Temperature-Dependent Forward and Reverse Gate Bias Conditions. *IEEE Trans. Electron Devices* **2022**, *69*, 531–535. [CrossRef]
9. Nuo, M.; Wu, Y.; Yang, J.; Hao, Y.; Wang, M.; Wei, J. Time-Resolved Extraction of Negatively Shifted Threshold Voltage in Schottky-Type p-GaN Gate HEMT Biased at High VDS. *IEEE Trans. Electron Devices* **2023**, *70*, 3462–3467. [CrossRef]
10. Uemoto, Y.; Hikita, M.; Ueno, H.; Matsuo, H.; Ishida, H.; Yanagihara, M.; Ueda, T.; Tanaka, T.; Ueda, D. Gate injection transistor (GIT)—A normally-off AlGaIn/GaN power transistor using conductivity modulation. *IEEE Trans. Electron Devices* **2007**, *54*, 3393–3399. [CrossRef]
11. Zhong, Y.; Su, S.; Chen, X.; Zhou, Y.; He, J.; Gao, H.; Zhan, X.; Guo, X.; Liu, J.; Sun, Q.; et al. Normally-off HEMTs with regrown p-GaN gate and low-pressure chemical vapor deposition SiNx passivation by using an AlN pre-layer. *IEEE Electron Device Lett.* **2019**, *40*, 1495–1498. [CrossRef]
12. Wei, J.; Xie, R.; Xu, H.; Wang, H.; Wang, Y.; Hua, M.; Zhong, K.; Tang, G.; He, J.; Zhang, M.; et al. Charge storage mechanism of drain induced dynamic threshold voltage shift in p-GaN gate HEMTs. *IEEE Electron Device Lett.* **2019**, *40*, 526–529. [CrossRef]
13. Wei, J.; Xu, H.; Xie, R.; Zhang, M.; Wang, H.; Wang, Y.; Zhong, K.; Hua, M.; He, J.; Chen, K.J. Dynamic threshold voltage in p-GaN gate HEMT. In Proceedings of the 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 19–23 May 2019; pp. 291–294.
14. Tang, S.W.; Bakeroot, B.; Huang, Z.H.; Chen, S.C.; Lin, W.S.; Lo, T.C.; Borga, M.; Wellekens, D.; Posthuma, N.; Decoutere, S.; et al. Using Gate Leakage Conduction to Understand Positive Gate Bias Induced Threshold Voltage Shift in p-GaN Gate HEMTs. *IEEE Trans. Electron Devices* **2023**, *70*, 449–453. [CrossRef]
15. Tang, S.W.; Lin, W.S.; Huang, Z.H.; Wu, T.L. Capacitance-Dependent VTH Instability Under a High dVg/dt Event in p-GaN Power HEMTs. *IEEE Electron Device Lett.* **2022**, *43*, 1617–1620. [CrossRef]
16. Zhou, X.; Wang, Z.; Wu, Z.; Zhou, Q.; Qiao, M.; Li, Z.; Zhang, B. Total-Ionizing-Dose Radiation Effect on Dynamic Threshold Voltage in p-GaN Gate HEMTs. *IEEE Trans. Electron Devices* **2023**, *70*, 4081–4086. [CrossRef]
17. Chen, J.; Su, Y.; Pan, C.; Kuang, W.; Yang, K.; Wang, H.; Wang, M.; Zhang, B.; Zhou, Q. The Device Instability of p-GaN Gate HEMTs Induced by Self-Heating Effect Investigated by on-State Drain Current Injection (DCI) Technique. *IEEE Trans. Electron Devices* **2022**, *69*, 5496–5502. [CrossRef]
18. Lin, J.H.; Ciou, F.M.; Chang, T.C.; Lin, Y.S.; Hsu, J.T.; Jin, F.Y.; Chang, K.C.; Kuo, T.T.; Chen, K.H.; Hung, Y.H.; et al. Abnormal Threshold Voltage Degradation Under Semi-On State Stress in Si₃N₄/AlGaIn/GaN-HEMT. *IEEE Electron Device Lett.* **2022**, *43*, 1420–1423. [CrossRef]
19. Jiang, H.; Zhu, R.; Lyu, Q.; Lau, K.M. High-Voltage p-GaN HEMTs With OFF-State Blocking Capability After Gate Breakdown. *IEEE Electron Device Lett.* **2019**, *40*, 530–533. [CrossRef]
20. Wang, H.; Wei, J.; Xie, R.; Liu, C.; Tang, G.; Chen, K.J. Maximizing the Performance of 650-V p-GaN Gate HEMTs: Dynamic RON Characterization and Circuit Design Considerations. *IEEE Trans. Power Electron.* **2017**, *32*, 5539–5549. [CrossRef]
21. EPC2025 Datasheet, EPC. 2015. Available online: <http://epc-co.com/epc> (accessed on 10 October 2023).
22. PGA26E19BA Datasheet, Panasonic, Osaka, Japan. 2015. Available online: <http://www.mouser.hk> (accessed on 10 October 2023).
23. GS66504B Datasheet, GaN Systems, Ottawa, ON, Canada. 2015. Available online: <http://www.gansystems.com> (accessed on 10 October 2023).
24. Rocha, P.F.P.P.; Vauche, L.; Mohamad, B.; Vandendaele, W.; Martinez, E.; Veillerot, M.; Spelta, T.; Rochat, N.; Gwoziecki, R.; Salem, B.; et al. Impact of post-deposition anneal on ALD Al₂O₃/etched GaN interface for gate-first MOSc-HEMT. *Power Electron. Devices Compon.* **2023**, *4*, 100033. [CrossRef]
25. Yoon, Y.J.; Lee, J.S.; Kang, I.M.; Lee, E.J.; Kim, D.S. Impact of process-dependent SiNx passivation on proton-induced degradation in GaN MIS-HEMTs. *Results Phys.* **2021**, *31*, 105013. [CrossRef]

26. Lee, J.H.; Kim, D.S.; Kim, J.G. Effect of gate dielectrics on characteristics of high-energy proton-irradiated AlGa_N/Ga_N MISHEMTs. *Radiat. Phys. Chem.* **2021**, *184*, 109473. [[CrossRef](#)]
27. Zhong, K.; Xu, H.; Zheng, Z.; Chen, J.; Chen, K.J. Characterization of Dynamic Threshold Voltage in Schottky-Type p-GaN Gate HEMT Under High-Frequency Switching. *IEEE Electron Device Lett.* **2021**, *42*, 501–504. [[CrossRef](#)]
28. Chae, M.; Kim, H. Investigation of the Gate Degradation Induced by Forward Gate Voltage Stress in p-GaN Gate High Electron Mobility Transistors. *Micromachines* **2023**, *14*, 977. [[CrossRef](#)] [[PubMed](#)]
29. Meneghini, M.; Hilt, O.; Wuerfl, J.; Meneghesso, G. Technology and reliability of normally-off Ga_N HEMTs with p-type gate. *Energies* **2017**, *10*, 153. [[CrossRef](#)]
30. Efthymiou, L.; Murukesan, K.; Longobardi, G.; Udrea, F.; Shibib, A.; Terrill, K. Understanding the Threshold Voltage Instability During OFF-State Stress in p-GaN HEMTs. *IEEE Electron Device Lett.* **2019**, *40*, 1253–1256. [[CrossRef](#)]
31. Sayadi, L.; Iannaccone, G.; Sicre, S.; Häberlen, O.; Curatola, G. Threshold Voltage Instability in p-GaN Gate AlGa_N/Ga_N HFETs. *IEEE Trans. Electron Devices* **2018**, *65*, 2454–2460. [[CrossRef](#)]
32. Lai, Y.C.; Zhong, Y.N. Gate Capacitance and Off-State Characteristics of E-Mode p-GaN Gate AlGa_N/Ga_N High-Electron-Mobility Transistors After Gate Stress Bias. *J. Electron. Mater.* **2021**, *50*, 1162–1166. [[CrossRef](#)]
33. Favero, D.; De Santi, C.; Stockman, A. Trade-off between gate leakage current and threshold voltage stability in power HEMTs during ON-state and OFF-state stress. *Microelectron. Reliab.* **2023**, *150*, 115129. [[CrossRef](#)]
34. Amano, H.; Baines, Y.; Beam, E.; Borga, M.; Bouchet, T.; Chalker, P.R.; Charles, M.; Chen, K.J.; Chowdhury, N.; Chu, R.; et al. The 2018 Ga_N power electronics roadmap. *J. Phys. D Appl. Phys.* **2018**, *51*, 163001. [[CrossRef](#)]
35. Chu, R. Ga_N power switches on the rise: Demonstrated benefits and unrealized potentials. *Appl. Phys. Lett.* **2020**, *116*, 090502. [[CrossRef](#)]
36. Wang, K.; Zhu, Y.; Zhao, H.; Zhao, R.; Zhu, B. Steady-State Temperature-Sensitive Electrical Parameters' Characteristics of Ga_N HEMT Power Devices. *Electronics* **2024**, *13*, 363. [[CrossRef](#)]
37. Wang, H.; Lin, Y.; Jiang, J.; Dong, D.; Ji, F.; Zhang, M.; Jiang, M.; Gan, W.; Li, H.; Wang, M.; et al. Investigation of Thermally Induced Threshold Voltage Shift in Normally-OFF p-GaN Gate HEMTs. *IEEE Trans. Electron Devices* **2022**, *69*, 2287–2292. [[CrossRef](#)]
38. Pilati, M.; Buffolo, M.; Rampazzo, F. Impact of high-temperature operating lifetime tests on the stability of 0.15 μm AlGa_N/Ga_N HEMTs: A temperature-dependent analysis. *Microelectron. Reliab.* **2023**, *150*, 115131. [[CrossRef](#)]
39. Tallarico, A.N.; Stoffels, S.; Magnone, P.; Posthuma, N.; Sangiorgi, E.; Decoutere, S.; Fiegna, C. Investigation of the p-GaN Gate Breakdown in Forward-Biased Ga_N-Based Power HEMTs. *IEEE Electron Device Lett.* **2017**, *38*, 99–102. [[CrossRef](#)]
40. Shi, Y.; Zhou, Q.; Cheng, Q.; Wei, P.; Zhu, L.; Wei, D.; Zhang, A.; Chen, W.; Zhang, B. Carrier Transport Mechanisms Underlying the Bidirectional V_{TH} Shift in p-GaN Gate HEMTs Under Forward Gate Stress. *IEEE Trans. Electron Devices* **2019**, *66*, 876–882. [[CrossRef](#)]
41. Xu, R.; Chen, P.; Liu, X.; Zhao, J.; Zhu, T.; Chen, D.; Xie, Z.; Ye, J.; Xiu, X.; Wan, F.; et al. A Lateral AlGa_N/Ga_N Schottky Barrier Diode with 0.36 V Turn-on Voltage and 10 kV Breakdown Voltage by Using Double Barrier Anode Structure. *Chip* **2023**, 100079. [[CrossRef](#)]
42. Sun, Y.; Wang, Y.; Tang, J.; Wang, W.; Huang, Y.; Kuang, X. A Breakdown Enhanced AlGa_N/Ga_N Schottky Barrier Diode with the T-Anode Position Deep into the Bottom Buffer Layer. *Micromachines* **2019**, *10*, 91. [[CrossRef](#)] [[PubMed](#)]
43. Lee, M.; Ahn, C.W.; Vu, T.K.O.; Lee, H.U.; Jeong, Y.; Hahm, M.G.; Kim, E.K.; Park, S. Current Transport Mechanism in Palladium Schottky Contact on Si-Based Freestanding Ga_N. *Nanomaterials* **2020**, *10*, 297. [[CrossRef](#)] [[PubMed](#)]
44. Artur, L.; Ewa, G.; Robert, C. Effect of doping of layers surrounding Ga_N/InGa_N multiple quantum wells on their thermal stability. *Mater. Sci. Semicond. Process.* **2023**, *166*, 107752.
45. Huang, Z.H.; Sun, H.Q.; Ding, X. Novel gate air cavity Ga_N HEMTs design for improved RF and DC performance. *Results Phys.* **2021**, *29*, 104718. [[CrossRef](#)]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.