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Single-Stage Step-Down Power Factor Corrector without Full-Bridge Rectifier

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Abstract: In this paper, a single-stage step-down power factor corrector without a full-bridge rectifier is developed, which is designed to operate in discontinuous conduction mode (DCM). In terms of control, the DCM has the advantages of simple control and easy realization, no slope compensation, zero current switching, and no diode reverse current. By sampling the output voltage and using the voltage-follower control to generate the necessary control force to drive the power switch, not only can the output voltage be stabilized at the desired value, but also the input current can be, as much as possible, in the form of a sinusoidal waveform and can follow the phase of the input voltage. Moreover, the harmonic distortion meets the requirements of the IEC6100-3-2 Class D harmonics standard, and, thus, the proposed rectifier is appropriate for the computer, computer monitor, and television receiver. Eventually, by means of mathematical deductions, simulations by PSIM version 9.1, and experimental results, the feasibility and effectiveness of the proposed circuit can be verified.

Keywords: DCM; PFC; full bridge; voltage-follower control; single stage

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1. Introduction

Thanks to the rapid development of technology and power electronics, low-frequency harmonic currents created by the characteristics of nonlinear loads of power electronics products flow into the power system in large quantities, thereby leading to increasingly serious harmonic pollution of the power system. As generally acknowledged, the harmonic current will change the output voltage waveform of the power system. When the harmonic current generated is larger or exceeds the permissible value, it may cause other products in its vicinity to operate incorrectly, measurement errors, efficiency degradation, or even burnout. Therefore, harmonics are regulated in various countries around the world. The International Electrotechnical Commission (IEC) in Europe has issued the IEC61000-3-2 harmonic standard [1], and Japanese specifications have also been issued, JIS-C-C. The Japanese authority also promulgated the JIS-C-61000-3-2 standard [2], which formally regulates the harmonics generated by electronic equipment products, and stipulates that all electronic equipment products with an output power of 75 W or more must pass a harmonics test.

In order to improve harmonic and power-factor problems, it is necessary to add a power factor correction (PFC) circuit. The main function of this circuit is to make the input voltage and input current in the same phase, so that the load observed by the utility is similar to the resistive load. They can be categorized into passive and active power factor correction circuits, depending on the components used.

Passive power factor correctors [3] are composed of passive components, including inductors, capacitors, diodes, etc. These circuits have the advantages of a simple circuit structure, low cost, and low electromagnetic interference, etc. However, they are bulky, heavy, inefficient, and lack flexibility in the circuits. That is to say, the passive

power factor correction is ineffective, and they are not suitable for today's stringent power factor requirements.

Due to the above disadvantages of passive PFC rectifiers, active PFC rectifiers were developed. Generally, the circuit components of the active PFC rectifier [4] include switching switches, inductors, and diodes, etc. According to the input conditions and output load requirements, the timing of the main power switch can be controlled by appropriate feedback compensation control and pulse width modulation (PWM) to make the phase of the input current closely follow the phase of the input voltage, so as to stabilize the output voltage, as well as to control the input current waveform to meet the harmonic specification.

Commonly used single-stage active power PFC rectifiers are classified into two types, boost-derived and buck-derived, among which the boost PFC circuits have been widely used [5–18]. The boost PFC rectifier has the following advantages: (i) the inductor is directly connected to the power supply at the input end, and in the continuous conduction mode (CCM), the input current is continuous; so that the input current spike can be suppressed, the electromagnetic interference is smaller, and the power factor can be higher; (ii) the main power switch driver does not need to be isolated, so that the driver circuit is easy to design; (iii) the input current is the inductor current, which makes it easy to realize current mode control; (iv) it has a high output voltage, so compared to other circuit topologies, it has a better hold-up time after a power failure when using the same capacitor size. However, because of the higher output voltage, there are some drawbacks: (i) the voltage tolerance of the power switch has to be large enough; (ii) to meet the demand of the back-end load voltage, an additional regulation stage or isolation step-down circuit is required, thereby increasing the cost; and (iii) the high output voltage is prone to causing a high common-mode noise.

The studies [19–31] present buck PFC rectifiers, which can convert a higher input AC voltage into a lower DC voltage. The advantage of this circuit is that the voltage stress of the power switch is the maximum value of the input voltage, and compared with the boost PFC rectifier, the power switch can be selected with a smaller withstand voltage, and thus the cost is cheaper. However, there is no input current when the input voltage is lower than the output voltage, resulting in zero-crossing distortion. Consequently, the input current does not follow the phase of the input voltage at this time, so the power factor is relatively low, as shown in Figure 1. In addition, the switch is floating, which makes it complicated to drive.

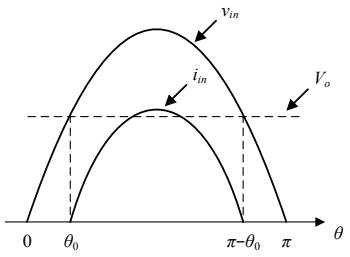

Figure 1. Input voltage and input current of the buck active PFC rectifier.

The studies [32–34] propose buck–boost rectifiers, which have the advantage of being able to step up and step down the input voltage in CCM, thereby providing a wide output voltage range and being easy to design according to the requirements of the back-end circuits. However, the voltage stress of the switch and output diode is the sum of the input voltage and the output voltage. Consequently, the use of components with higher withstand voltages is required. In addition, the switch is floating, which makes it complicated to drive.

In general, traditional active PFC rectifiers are not suitable for high-power applications because when these rectifiers are activated, the full-bridge rectifiers, diodes, and switching elements will have large currents flowing through them, resulting in large conduction losses and switching losses, and hence leading to a reduction in the overall efficiency. In view of

this, if the loss of the bridge rectifier can be decreased, the overall efficiency of the circuit can be improved. Therefore, bridgeless active PFC rectifiers are presented [11–31,35–38].

As is generally acknowledged, the PFC control methods can be roughly categorized into the following four types: (1) peak current mode control [7]; (2) average current mode control [8,39]; (3) critical mode control [9,40]; (4) voltage-follower control [36].

For the peak current mode control, if the duty cycle is greater than 50%, the current is prone to sub-harmonic oscillations, so if no proper slope compensation is added to this control, it will result in the distortion of the input current. For the average current control, it makes the transient response of the PFC rectifier slow but is suitable for high-power applications. For the critical mode control, it is difficult to design the filter because it is a variable-frequency control. For the voltage-follower control, due to the high peak current in the power switch when the circuit operates in the discontinuous conduction mode (DCM), it is necessary to select power components with a higher current withstand performance, so it is only suitable for low-power applications.

Accordingly, as shown in Figure 2a, the proposed single-stage step-down power factor corrector without a full-bridge rectifier is presented, which is modified from the existing bridgeless high-PF buck converter [22], as shown in Figure 2b. From these two figures, it can be seen that the former has a lower number of components than the latter.

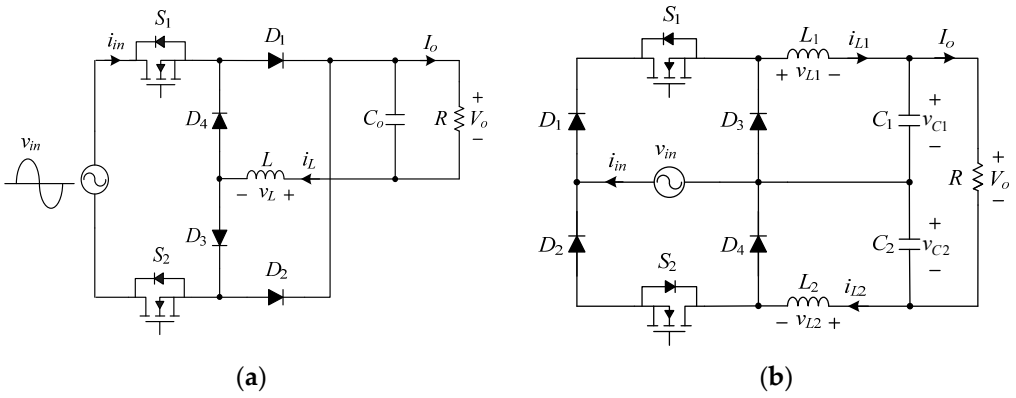

Figure 2. Single-stage step-down power factor corrector without full-bridge rectifier: (**a**) the proposed; (**b**) the existing [22].

Firstly, the system configuration is depicted in Section 2. Sequentially, Section 3 describes the operating principle in detail. After this, the design considerations are given in Section 4. Accordingly, in Section 5, some experimental results are presented to validate the theoretical analysis and designed parameters. Eventually, Section 6 presents a conclusion.

2. System Configuration

Figure 3 displays the system configuration of the proposed rectifier. As for the main power stage, it is constructed by the switches S_1 and S_2, the diodes D_1, D_2, D_3, and D_4, the output inductor L, the output capacitor C_o, and the output resistor R. As for the control stage, it is built up by one voltage divider, one analog-to-digital converter (ADC), one gate driver, and one FPGA, which is used to realize voltage-follower control. It is noted that only one gate driving signal is needed to drive the switches S_1 and S_2. Regarding the control concept, the output voltage is sensed by the voltage divider and sent to the ADC to obtain the corresponding digital signal, which is sent to the FPGA to create suitable gate driving signals to drive the switches S_1 and S_2, so as to attain the prescribed output voltage, along with a high PF, due to the proposed circuit being operated in DCM. In addition, there is a voltage controller constructed by a proportional-integral (PI) controller and a pulse-width-modulated (PWM) generator inside the FPGA.

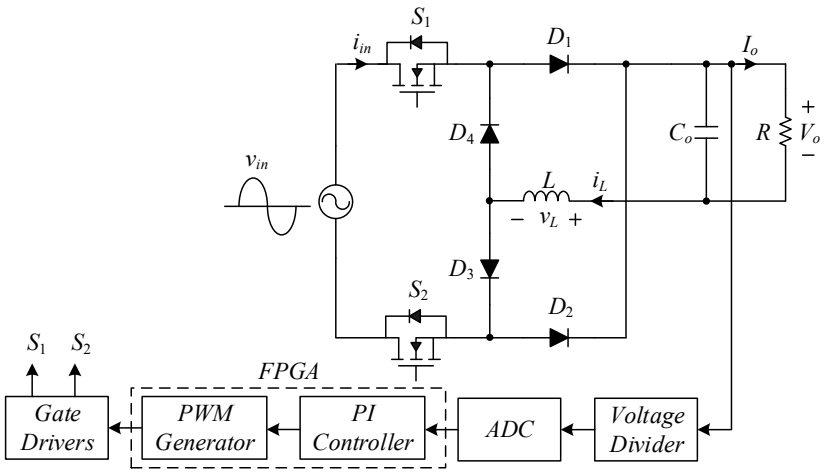

Figure 3. System configuration.

3. Operating Principle

The operating principle of the proposed single-stage step-down power factor corrector without a full bridge is analyzed, and then the corresponding related theoretical derivation is followed. For analysis convenience, the following assumptions are made first:

(1) All power switches, diodes, inductors, and capacitors are viewed as ideal components.
(2) The value of the output capacitor C_o is large enough so that the voltage across C_o is stabilized at some output voltage.
(3) The converter is operated in steady state under DCM.

Based on the above assumptions, the illustrated waveforms of the inductor voltage and current in DCM are shown in Figure 4.

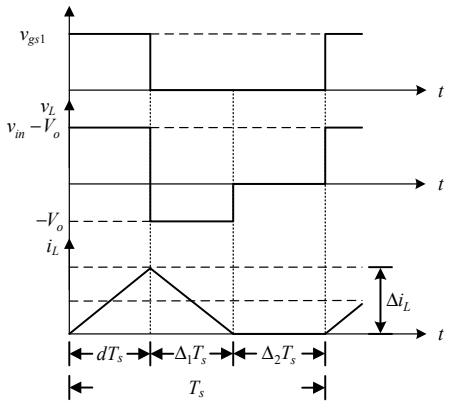

Figure 4. Illustrated waveforms of inductor voltage and current in DCM in a positive half-cycle.

State 1 $[0 \leq t \leq dT_s]$: As shown in Figure 5, when the input voltage v_{in} is in a positive half-cycle, the switch S_1 is turned on. The input current i_{in} flows through the switch S_1, the body diode of the switch S_2, the diodes D_1 and D_3, the output inductor L, and the output capacitor C_o. During this state, the voltage across the output inductor L, called v_L, is the input voltage v_{in} minus the output voltage V_o, so the output inductor L is in magnetization mode and hence the inductor current i_L rises linearly. At the same time, the input power supply charges the output capacitor C_o and provides energy to the load R. Moreover, the corresponding time experienced in this state is dT_s. In the following, for the first three states, the switch S_2 is always off, whereas for the last three states, the switch S_1 is always off. As a result, the dead-time effect on switches [41] does not be considered for the proposed rectifier in the actual applications.

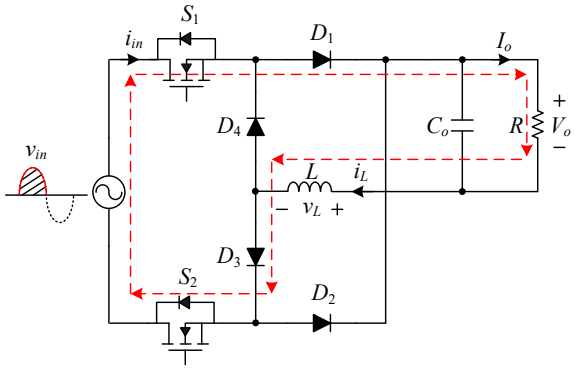

Figure 5. State 1.

State 2 $[dT_s \leq t \leq T_s]$: As shown in Figure 6, when the input voltage v_{in} is in a positive half-cycle, the switch S_1 is cut off, the input current i_{in} is zero, the diodes D_1, D_2, D_3, and D_4 conduct, and the inductor current i_L continues to flow through these four diodes. During this state, the voltage across the output inductor L is zero minus the output voltage V_o, so the output inductor L is in demagnetization mode and hence the inductor current decreases linearly. At the same time, the output capacitor C_o and the output inductor L provide energy to the load R. Moreover, the corresponding time experienced in this state is $\Delta_1 T_s$.

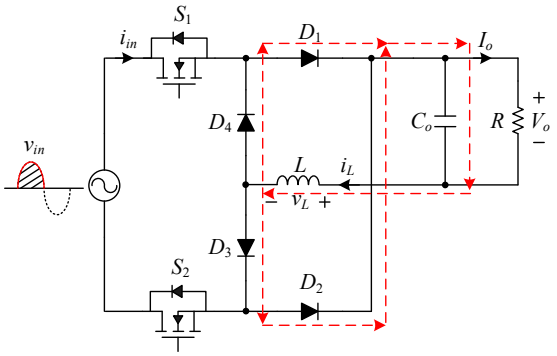

Figure 6. State 2.

State 3 $[(d + \Delta_1)T_s \leq t \leq T_s]$: As shown in Figure 7, when the input voltage v_{in} is in a positive half-cycle, the switch S_1 is still off and the diodes D_1, D_2, D_3, and D_4 are all cut off. During this state, there is no current flowing through the inductor L. At the same time, the energy required for the load R is supplied by the output capacitor C_o. Moreover, the corresponding time experienced in this state is $\Delta_2 T_s$.

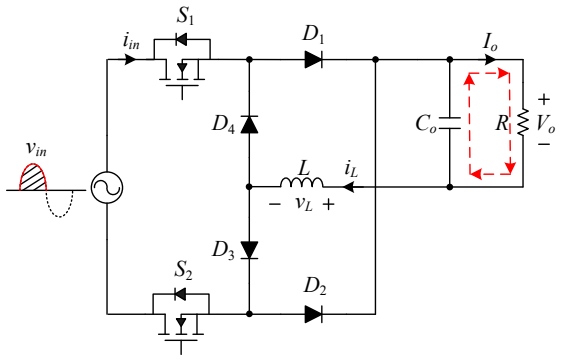

Figure 7. State 3.

State 4 $[0 \leq t \leq dT_s]$: As shown in Figure 8, when the input voltage is in a negative half-cycle, the switch S_2 is turned on, and the input current i_{in} flows through the switch

S_2, the body diode of the switch S_1, the diodes D_2 and D_4, the output inductor L, and the output capacitor C_o. During this state, the voltage across the output inductor L, called v_L, is the input voltage v_{in} minus the output voltage V_o, so the output inductor L is in magnetization mode and hence the inductor current i_L rises linearly. At the same time, the input power supply charges the output capacitor C_o and provides energy to the load R. Moreover, the corresponding time experienced in this state is DT_s.

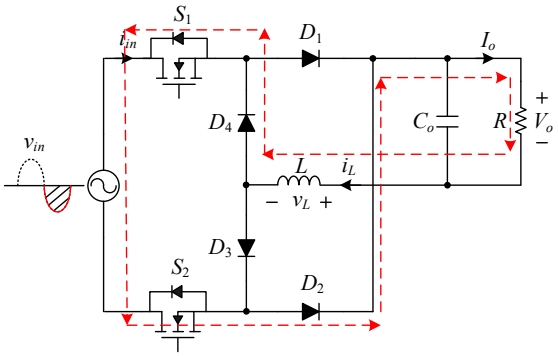

Figure 8. State 4.

State 5 $[dT_s \leq t \leq T_s]$: When the input voltage is in a negative half-cycle, the switch S_2 is cut off, and the behavior is the same as that of state 2, as shown in Figure 6. Moreover, the corresponding time experienced in this state is $\Delta_1 T_s$.

State 6 $[(d + \Delta_1)T_s \leq t \leq T_s]$: When the input voltage is in a negative half-cycle, the switch S_2 is still off and diodes D_1, D_2, D_3, and D_4 are cut off, and the behavior is the same as that of state 3, as shown in Figure 7. Moreover, the corresponding time experienced in this state is $\Delta_2 T_s$.

Based on the fact that the inductor must obey the volt-second balance, Equation (1) can be obtained as

$$\frac{1}{L} \cdot (v_{in} - V_o) \cdot d \cdot T_s + \frac{1}{L} \cdot (-V_o) \cdot \Delta_1 \cdot T_s + \frac{1}{L} \cdot 0 \cdot \Delta_2 \cdot T_s = 0 \quad (1)$$

and

$$d + \Delta_1 + \Delta_2 = 1 \quad (2)$$

By substituting (2) into (1), the voltage conversion ratio can be calculated as

$$\frac{V_o}{v_{in}} = \frac{d}{d + \Delta_1} \quad (3)$$

4. Design Considerations

Table 1 displays the specifications for the proposed rectifier.

Table 1. System Specifications.

Name	Value
Input voltage (v_{in})	90~130 V_{rms}
Nominal input voltage	110 V_{rms}
Output voltage (V_o)	80 V
Rated output current ($I_{o,rated}$)	1.125 A
Rated output power ($P_{o,rated}$)	90 W
Output voltage ripple (Δv_o)	$\Delta v_o = 3\% \cdot V_o$
Switching frequency (f_s)	100 kHz
Rated load efficiency (η)	95%

4.1. Design of Output Inductor

In the design of an inductor, it is necessary to consider the peak input AC current $I_{in,pk}$ when the circuit is operated at the lowest input AC voltage $v_{in,min}$ and under the rated output power $P_{o,rated}$. By assuming that the input AC voltage and the input AC current are ideal sinusoids, the input AC voltage v_{in} and the input AC current i_{in} can be defined as $V_{in,pk}\sin\omega_L t$ and $I_{in,pk}\sin\omega_L t$, respectively, where $V_{in,pk}$ and $I_{in,pk}$ are the peak value of the input AC voltage and the peak value of the input AC current, respectively, and ω_L is the line radian frequency. To simplify the analysis, the phase angle $\omega_L t$ is replaced by the phase angle θ, so the input AC voltage can v_{in} be expressed as follows:

$$v_{in} = V_{in,pk}\sin\theta \tag{4}$$

Similarly, the input AC current i_{in} can be expressed as

$$i_{in} = I_{in,pk}\sin\theta \tag{5}$$

As shown in Figure 9, since there is no input current when the input voltage is lower than the output voltage of the buck-type PFC rectifier, it is necessary to assume that the input AC current i_{in} in (5) should be rewritten into (6).

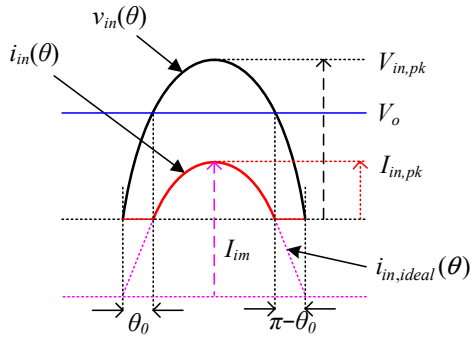

Figure 9. Relationship between input AC voltage and input AC current.

$$i_{in} = I_{in,pk}\sin\theta = I_{im}\cdot(\sin\theta - \sin\theta_0), \theta_0 < \theta < \pi - \theta_0 \tag{6}$$

where

$$\theta_0 = \sin^{-1}\left(\frac{V_o}{V_{in,pk}}\right) \tag{7}$$

I_{im} is the amplitude of the ideal input AC current $i_{in,ideal}(\theta)$.

Substituting the system specifications shown in Table 1 and the lowest input AC voltage $v_{in,min}$ into (7) yields

$$\begin{aligned}\theta_0 &= \sin^{-1}\left(\tfrac{V_o}{V_{in,pk}}\right) = \sin^{-1}(D)\\ &= \sin^{-1}\left(\tfrac{80}{90\sqrt{2}}\right) = \sin^{-1}(0.63) = 0.68\end{aligned} \tag{8}$$

By multiplying the instantaneous value of the input AC voltage and the instantaneous value of the input AC current by the time integral, the average input power can be obtained as follows:

$$P_{in} = \frac{1}{T_L}\cdot\int_{t_0}^{t_0+T_L} p(\theta)d\theta = \frac{1}{\pi/2}\cdot\int_{\theta_0}^{\pi/2} v_{in}(\theta)i_{in}(\theta)d\theta \tag{9}$$

Substituting (4) and (6) into (9) yields

$$\begin{aligned} P_{in} &= \frac{2}{\pi} \cdot \int_{\theta_0}^{\pi/2} V_{in,pk} \sin\theta \cdot I_{im}(\sin\theta - \sin\theta_0) d\theta \\ &= \frac{2V_{in,pk} I_{im}}{\pi} \cdot \int_{\theta_0}^{\pi/2} (\sin^2\theta - \sin\theta \sin\theta_0) d\theta \\ &= \frac{2V_{in,pk} I_{im}}{\pi} \cdot \left(\frac{\pi}{4} - \frac{\cos\theta_0 \sin\theta_0}{2} - \frac{\theta_0}{2}\right) \end{aligned} \tag{10}$$

The amplitude of the ideal input AC current, called I_{im}, is determined by the input power P_{in}, as shown in (11):

$$I_{im} = \frac{\pi P_{in}}{2V_{in,pk}} \cdot \frac{1}{\left(\frac{\pi}{4} - \frac{\cos\theta_0 \sin\theta_0}{2} - \frac{\theta_0}{2}\right)} \tag{11}$$

In addition, the average input power is obtained from the output power, and the prescribed efficiency, i.e., $P_{in} = P_{out}/\eta$, (11) can be rewritten as

$$I_{im} = \frac{\pi \cdot P_{out}/\eta}{2V_{in,pk}} \cdot \frac{1}{\left(\frac{\pi}{4} - \frac{\cos\theta_0 \sin\theta_0}{2} - \frac{\theta_0}{2}\right)} \tag{12}$$

By substituting the rated output load $P_{o,rated}$, the peak value of the minimum input AC voltage $v_{in,min}$, and the results of (8) into (12), the ideal input AC current amplitude I_{im} can be obtained as follows:

$$I_{im} = \frac{\pi \times \frac{90}{0.95}}{2 \times 90\sqrt{2}} \cdot \frac{1}{\left(\frac{\pi}{4} - \frac{0.63 \times 0.78}{2} - \frac{0.68}{2}\right)} = 5.83\text{A} \tag{13}$$

By setting the conduction angle θ in (7) to $\frac{\pi}{2}$, the peak value of the input AC current, called $I_{in,pk}$, can be obtained to be

$$I_{in,pk} = I_{im} \cdot (1 - \sin\theta_0) \tag{14}$$

Substituting the results of (8) and (13) into (14) yields

$$I_{in,pk} = 5.83 \times (1 - 0.63) = 2.16\text{A} \tag{15}$$

The average value of the inductor current i_L, called I_L, is

$$I_L = \langle i_L(t) \rangle_{T_s} = \frac{i_{in}}{D} \tag{16}$$

By substituting $I_{in,pk}$ into (16), the peak value of the average value of the inductor current, called $I_{L,avg,pk}$, can be found as

$$I_{L,avg,pk} = \frac{I_{in,pk}}{D} \tag{17}$$

The ripple current through the inductor L can be expressed as

$$\Delta i_L = \frac{(v_{in} - V_o) D T_s}{L} = \frac{V_o (1 - D) T_s}{L} \tag{18}$$

Therefore, if the inductor L is to be operated in the current discontinuous mode (DCM), the value of inductor L must satisfy the following inequality:

$$\begin{aligned} & I_{L,avg,pk} \leq \frac{\Delta i_L}{2} \\ & \Rightarrow \frac{I_{in,pk}}{D} \leq \frac{V_o(1-D)T_s}{2L} \\ & \Rightarrow L \leq \frac{V_o D(1-D)T_s}{2I_{in,pk}} \end{aligned} \tag{19}$$

Substituting the system specifications shown in Table 1 and the results of (8) and (15) into (19) yields

$$L \leq \frac{80 \times 0.63 \times (1-0.63) \times 10\ \mu}{2 \times 2.16} = 43.2\ \mu\text{H} \tag{20}$$

Accordingly, the MPP powder iron core, manufactured by CSC Co. (Beijing, China) with a model name of CM270125, is used herein and its basic characteristic parameters are shown in Table 2. Therefore, the number of turns can be calculated as below:

$$N = \sqrt{\frac{L}{A_L}} = \sqrt{\frac{43.19\ \mu}{157\text{n}}} = 16.6 \tag{21}$$

Table 2. Characteristic parameters of powder iron core.

Part No.	A_L(nH/N^2)	A_ℓ(cm^2)	B_s(G)
CM270125	157	0.654	7000

In order to ensure that the required inductance value is sufficient for the converter to operate in DCM under any load condition, the number of turns is taken as 16. Therefore, the actual value of the inductor L is

$$L = A_L \cdot N^2 = 157\text{n} \times 16^2 = 40.2\ \mu\text{H} \tag{22}$$

4.2. Design of Output Capacitor

In the following, the current in the output capacitor C_o, called $i_c(t)$, can be expressed as

$$\begin{aligned} i_c(t) &= \frac{V_{in,rms} \cdot I_{in,rms}}{V_o} \cdot (-\cos 2\omega_L t) \\ &= -I_o \cos 2\omega_L t \end{aligned} \tag{23}$$

The relationship between the output current capacitor $i_c(t)$ and the output voltage capacitor $v_c(t)$ can be expressed as

$$v_c(t) = \frac{1}{C_o} \int i_c(t) dt \tag{24}$$

By substituting (23) into (24), the output voltage ripple $\widetilde{v}_o(t)$ can be expressed as

$$\widetilde{v}_o(t) = \frac{-I_o}{2\omega_L C_o} \sin 2\omega_L t \tag{25}$$

When the circuit operates in steady state, it can be seen that from (25), the output voltage ripple varies from $\frac{-I_o}{2\omega_L C_o}$ to $\frac{I_o}{2\omega_L C_o}$ and the frequency is twice the utility frequency.

$$\Delta v_o = \frac{I_o}{\omega_L C_o} \tag{26}$$

As shown in Table 1, the output voltage ripple is 3% of the output voltage. That is, the peak-to-peak value of the output voltage ripple Δv_o is

$$\Delta v_o = 3\% \cdot V_o = 0.03 \times 80 = 2.4\ \text{V} \tag{27}$$

Substituting (27) into (26) yields

$$C_o = \frac{I_o}{\omega_L \Delta v_o} = \frac{1.125}{2\pi \times 60 \times 2.4} = 1243\ \mu\text{F} \tag{28}$$

Since the step-down power factor corrector has an input voltage lower than the output voltage, it is necessary to multiply the value of C_o by the conduction angle $\pi - 2\theta_0$ to obtain the value of $C_{o,new}$.

$$C_{o,new} = C_o(\pi - 2\theta_0) = 1243\ \mu \times 1.78 = 2212\ \mu\text{F} \tag{29}$$

Therefore, a 2200 µF/100 V Nippon Chemi-Con electrolytic capacitor connected in parallel with a 100 µF/450 V United Chemi-Con electrolytic capacitor is used as the output capacitor C_o.

5. Experimental Results

The measured waveforms, THD, PF, and efficiency are shown herein.

5.1. Measured Waveforms under 110 V Input Voltage

Figures 10–33 show the waveforms at nominal input voltage. Figures 10–13 show the waveforms of input AC voltage and input AC current under different output load conditions. From these waveforms, it can be seen that within the range of the conduction angle of the input current, the phase of the input current follows the phase of the input voltage as closely as possible, and the input current is as close as possible to the form of a sinusoidal waveform, so as to achieve the PFC function. From Figures 14–17, it can be seen that the harmonics of the input AC current under different output load conditions comply with the harmonic specification of IEC61000-3-2 Class D. For the positive half-cycle of the input voltage, Figures 18–21 show the waveforms of v_{ds1} under different output loads. From these waveforms, it can be seen that when the switch S_1 is off and the inductor current i_L is zero, the waveform of v_{ds1} displays low-frequency oscillation, which is caused by the resonance between the output inductance and the parasitic capacitance of the switch S_1. For the negative half-cycle of the input voltage, Figures 22–25 show the waveforms of v_{ds2} under different output load conditions. The behavior of the switch S_2 is almost identical to that of S_1. From Figures 26–29, it can be seen that the output inductor current i_L is in DCM under different output load conditions, which is consistent with the design requirement. Figures 30–33 display the waveforms of the output voltage ripple $\widetilde{v}_o$ under different output load conditions. From these waveforms, it can be seen that the output voltage ripple is larger when the output load is heavier.

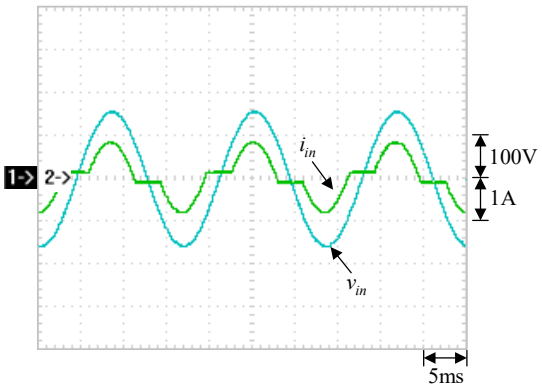

Figure 10. Measured waveforms under 25% load: (1) v_{in}; (2) i_{in}.

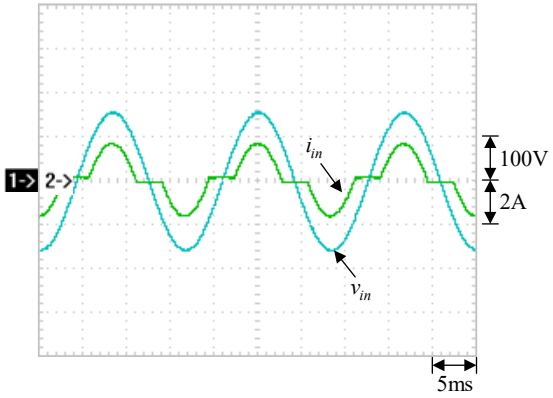

Figure 11. Measured waveforms under 50% load: (1) v_{in}; (2) i_{in}.

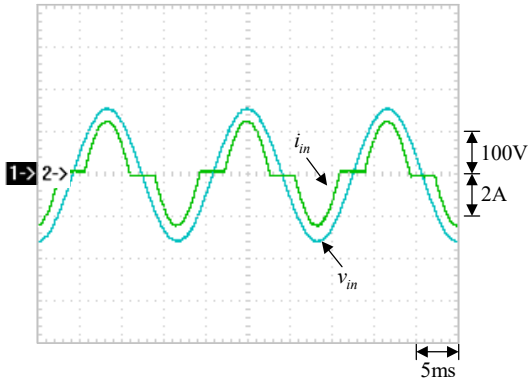

Figure 12. Measured waveforms under 75% load: (1) v_{in}; (2) i_{in}.

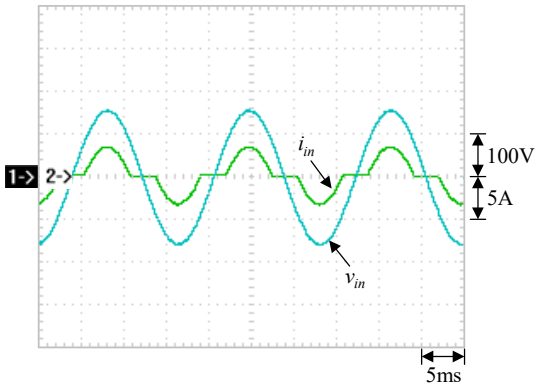

Figure 13. Measured waveforms under 100% load: (1) v_{in}; (2) i_{in}.

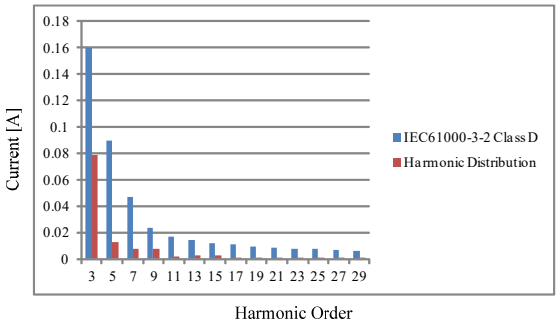

Figure 14. Harmonic distribution of input current under 25% load [1].

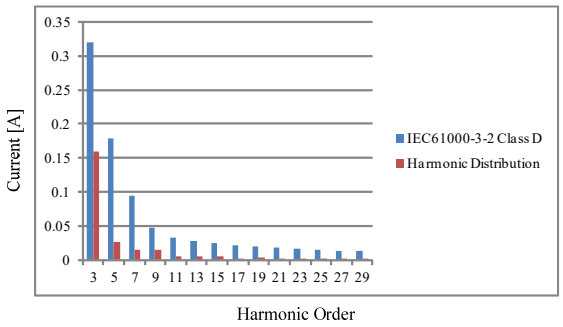

Figure 15. Harmonic distribution of input current under 50% load [1].

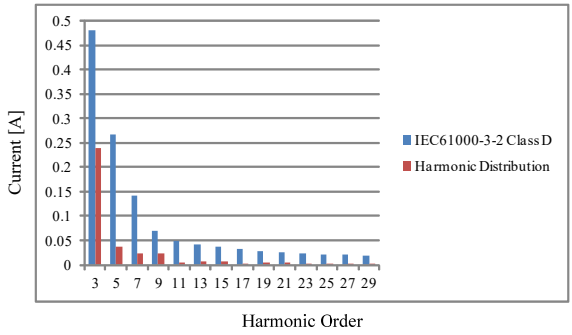

Figure 16. Harmonic distribution of input current under 75% load [1].

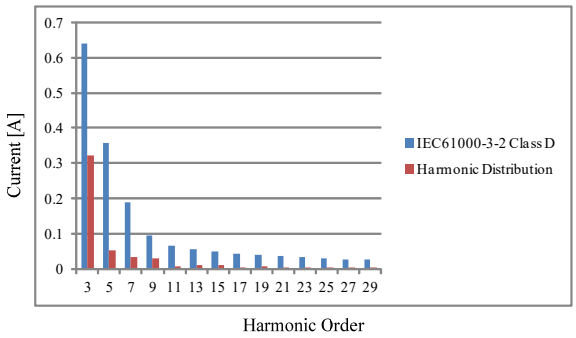

Figure 17. Harmonic distribution of input current under 100% load [1].

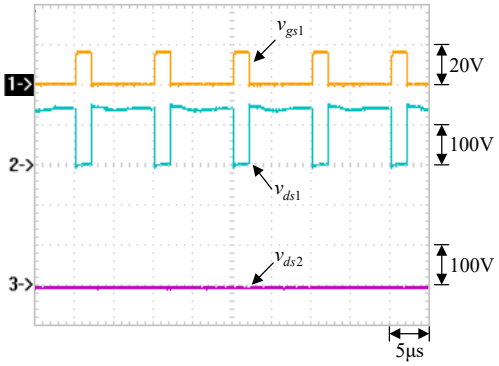

Figure 18. Measured waveforms at the peak of the positive half-cycle under 25% load: (1) v_{gs1}; (2) v_{ds1}; (3) v_{ds2}.

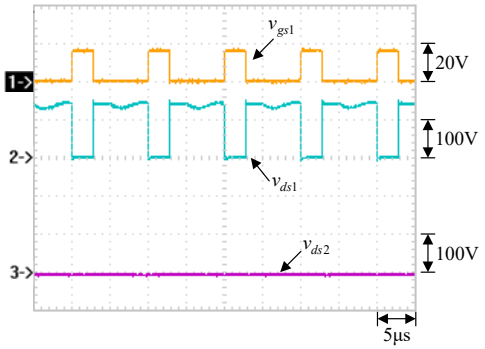

Figure 19. Measured waveforms at the peak of the positive half-cycle under 50% load: (1) v_{gs1}; (2) v_{ds1}; (3) v_{ds2}.

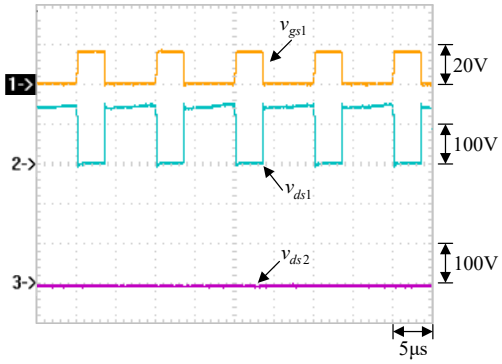

Figure 20. Measured waveforms at the peak of the positive half-cycle under 75% load: (1) v_{gs1}; (2) v_{ds1}; (3) v_{ds2}.

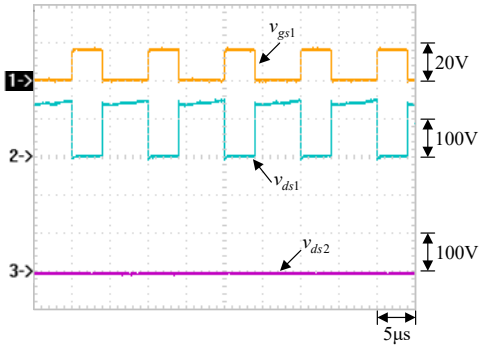

Figure 21. Measured waveforms at the peak of the positive half-cycle under 100% load: (1) v_{gs1}; (2) v_{ds1}; (3) v_{ds2}.

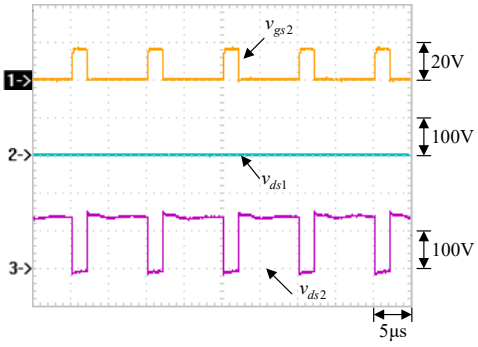

Figure 22. Measured waveforms at the valley of the negative half-cycle under 25% load: (1) v_{gs2}; (2) v_{ds1}; (3) v_{ds2}.

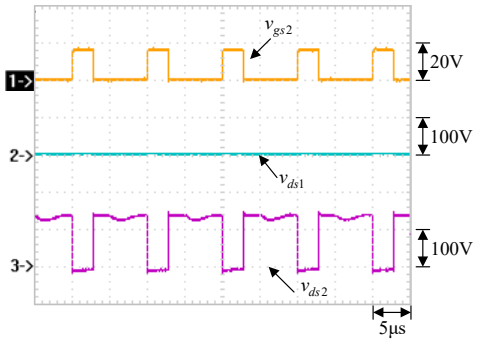

Figure 23. Measured waveforms at the valley of the negative half-cycle under 50% load: (1) v_{gs2}; (2) v_{ds1}; (3) v_{ds2}.

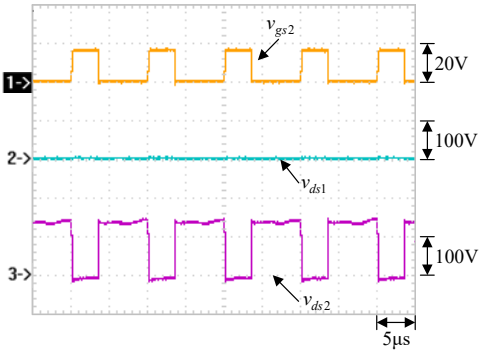

Figure 24. Measured waveforms at the valley of the negative half-cycle under 75% load: (1) v_{gs2}; (2) v_{ds1}; (3) v_{ds2}.

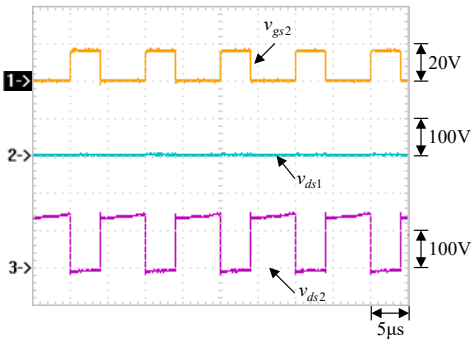

Figure 25. Measured waveforms at the valley of the negative half-cycle under 100% load: (1) v_{gs2}, (2) v_{ds1}, (3) v_{ds2}.

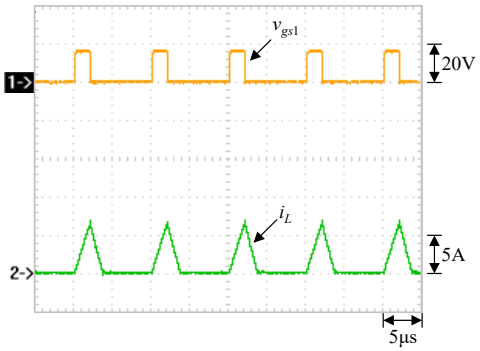

Figure 26. Measured waveforms at the peak of the positive half-cycle under 25% load: (1) v_{gs1}; (2) i_L.

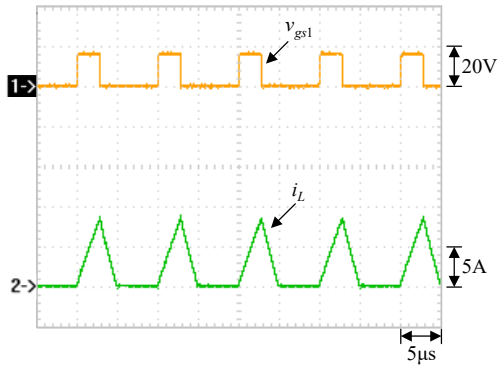

Figure 27. Measured waveforms at the peak of the positive half-cycle under 50% load: (1) v_{gs1}; (2) i_L.

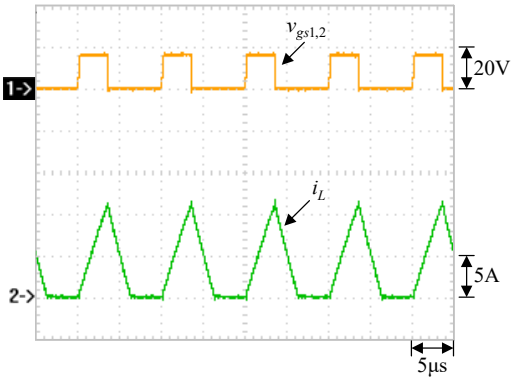

Figure 28. Measured waveforms at the peak of the positive half-cycle under 75% load: (1) $v_{gs1,2}$; (2) i_L.

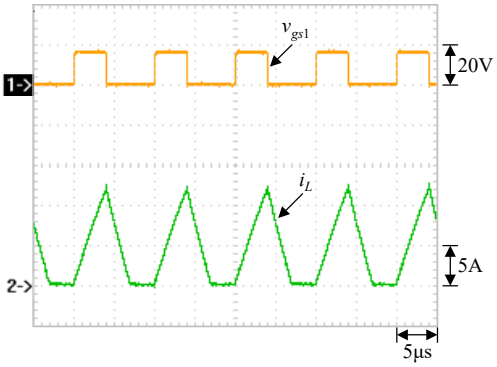

Figure 29. Measured waveforms at the peak of the positive half-cycle under 100% load: (1) v_{gs1}; (2) i_L.

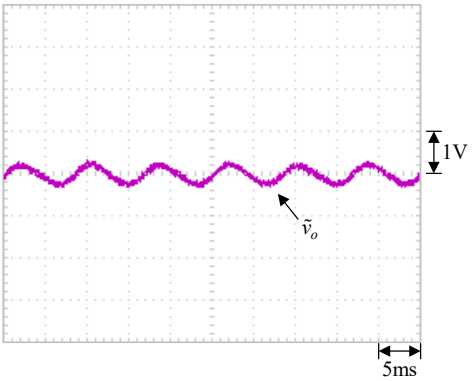

Figure 30. Output voltage ripple $\tilde{v}_o$ under 25% load.

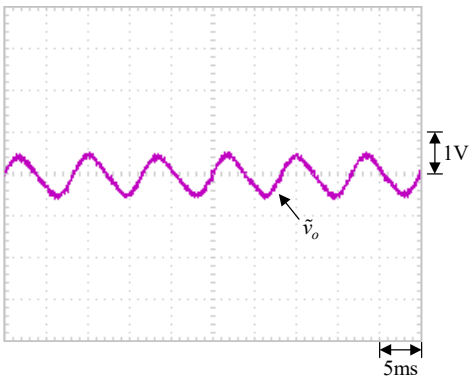

Figure 31. Output voltage ripple $\tilde{v}_o$ under 50% load.

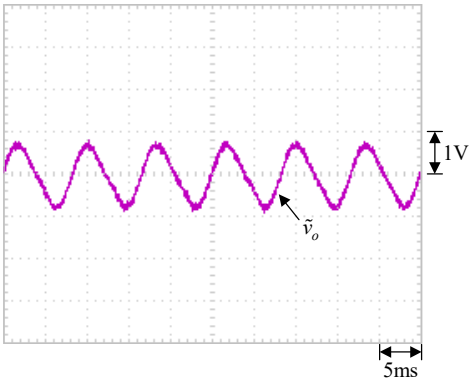

Figure 32. Output voltage ripple $\tilde{v}_o$ under 75% load.

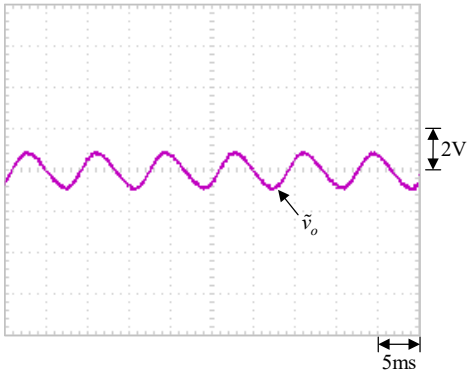

Figure 33. Output voltage ripple of $\tilde{v}_o$ under 100% load.

5.2. Measured Output Voltage Ripple under 100% Load at Different Input Voltages

Figure 34a–c display the waveforms of the output voltage ripple under an output power of 90 W at input voltages of 90 V, 110 V, and 130 V, respectively. The expression of the output voltage ripple can be seen from (25), and the output voltage ripple is only related to the output current and is independent of the input voltage.

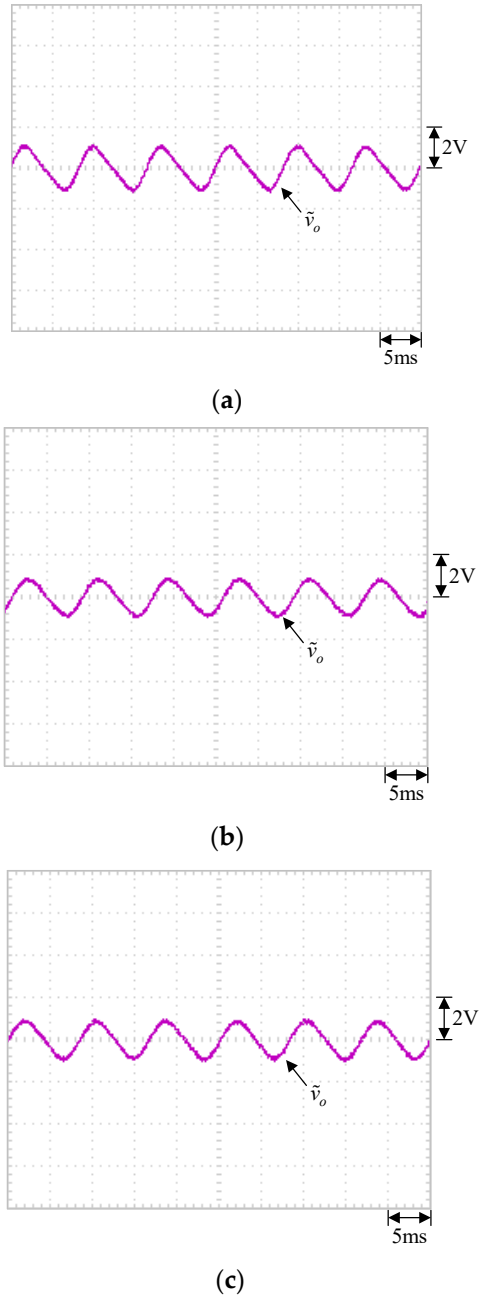

Figure 34. Output voltage ripple under 100% load at input voltages of (**a**) 90 V; (**b**) 110 V; (**c**) 130 V.

5.3. Measured Curves of THD, PF, and Efficiency

Figures 35 and 36 show the curves of THD and PF versus output power at different input voltages, respectively. From Figure 35, it can be seen that under the same output power, the lower the input voltage, the higher the THD. This is because there is more distortion current created from the lower input voltage. From Figure 36, it can be seen that under the same output power, the lower the input voltage, the lower the PF. This is because there is more difference in phase between the input voltage and the fundamental input current. From this figure, it can be seen that the PF can be kept above 0.88. And, the maximum PF is 0.95. Figure 37 shows the curve of efficiency versus output power at different input voltages. From this figure, it can be seen that the efficiency can be maintained above 95%. And, the maximum efficiency is 96.8% and can be achieved at the lowest input voltage under the minimum output power. In addition, the power losses at load under input voltages of 90 V, 110 V, and 130 V are 4.342 W, 4.064 W, and 3.817 W, respectively.

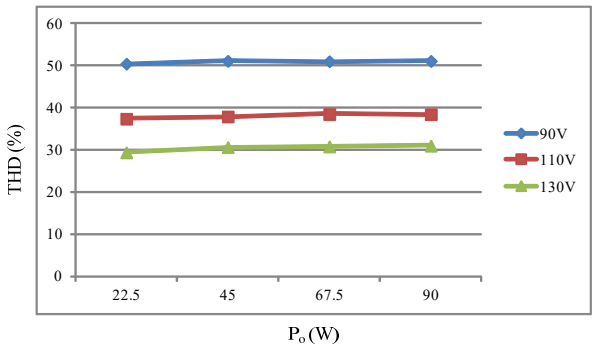

Figure 35. Curves of THD vs. output power at different input voltages.

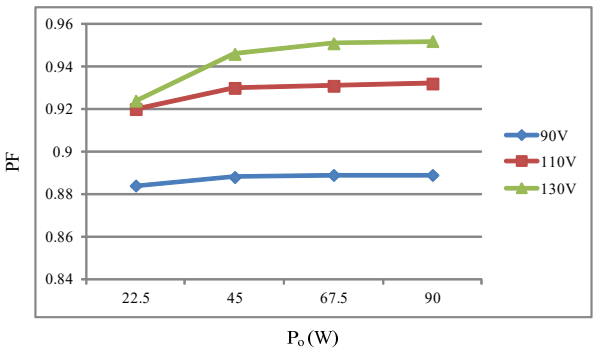

Figure 36. Curves of PF vs. output power at different input voltages.

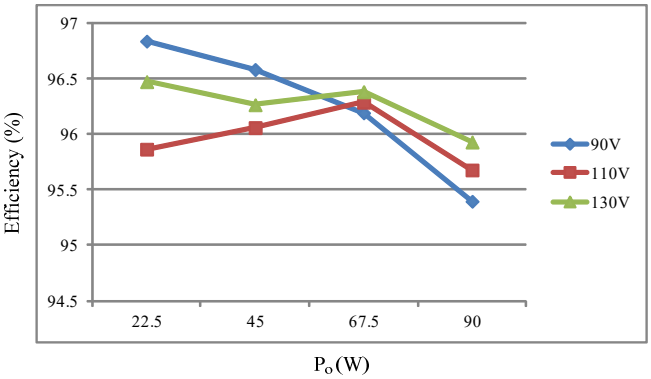

Figure 37. Curves of efficiency vs. output power at different input voltages.

5.4. Comparison between the Proposed and the Existing

There are many other existing papers investigating bridgeless single-stage step-down PFC [22–31] circuit structures, which are summarized in Table 3. From Table 3, it can be seen that the proposed circuit has a lower number of output inductors and capacitors as well as the same number of switches, magnetic elements, and diodes, as compared to the existing bridgeless buck PFC circuits.

Table 3. Comparison of the proposed topology and the existing topologies in [22–31].

Reference Number	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[31]	Proposed
Input Voltage (V_{rms})	230	220	230	110	70.7	100	110	120	110	110	110
Output Voltage (V)	160	160	160	48	50	48	80	85	130	48	80
Power (W)	75	---	75	150	31.3	100	100	120	100	120	90
Switch	2	2	2	2	2	2	3	2	4	3	2
Diode	4	5	4	6	4	3	5	4	4	5	4
Magnetic Element	2	1	2	4	3	3	1	2	2	2	1
Capacitor	2	1	1	4	2	3	1	1	2	2	1
THD (%)	19.6	26.7	50.69	5.1	---	17.7	37.2	---	---	5.3	38.2
Power Factor	0.661	0.966	0.941	0.998	---	0.985	0.924	0.896	0.971	---	0.932
Full-Load Efficiency (%)	89.5	---	---	94.5	96.6	96.3	95.3	86.2	92.1	93.1	95.7
Switching Frequency (kHz)	65	50	65	40	20	50	47	20	50	100	100

6. Conclusions

A single-stage step-down power factor corrector without a full-bridge rectifier is presented. From the experimental results, it can be seen that the proposed circuit can operate in DCM at different input voltages under output load conditions, which is consistent with the design results. Furthermore, this circuit can pass the IEC61000-3-2 Class D harmonic specification under all experimental conditions. In addition, the maximum PF is 0.95 and the maximum efficiency is 96.8%. As compared with the existing circuits, shown in [22–31], the proposed circuit has a lower number of output inductors and capacitors as well as the same number of switches and diodes.

Author Contributions: Conceptualization, K.-I.H. and J.-J.S.; methodology, K.-I.H. and J.-J.S.; software, Y.-P.H.; validation, J.-J.S. and Y.-P.H.; formal analysis, Y.-P.H.; investigation, J.-J.S. and Y.-P.H.; resources, K.-I.H.; data curation, J.-J.S. and Y.-P.H.; writing—original draft preparation, K.-I.H.; writing—review and editing, K.-I.H.; visualization, J.-J.S. and Y.-P.H.; supervision, K.-I.H.; project administration, K.-I.H.; funding acquisition, K.-I.H. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

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