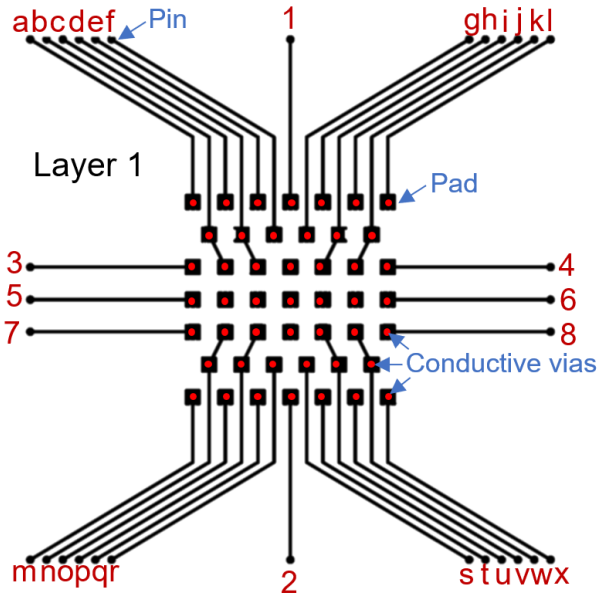


**Figure S1.** Circuit diagram of the first layer.

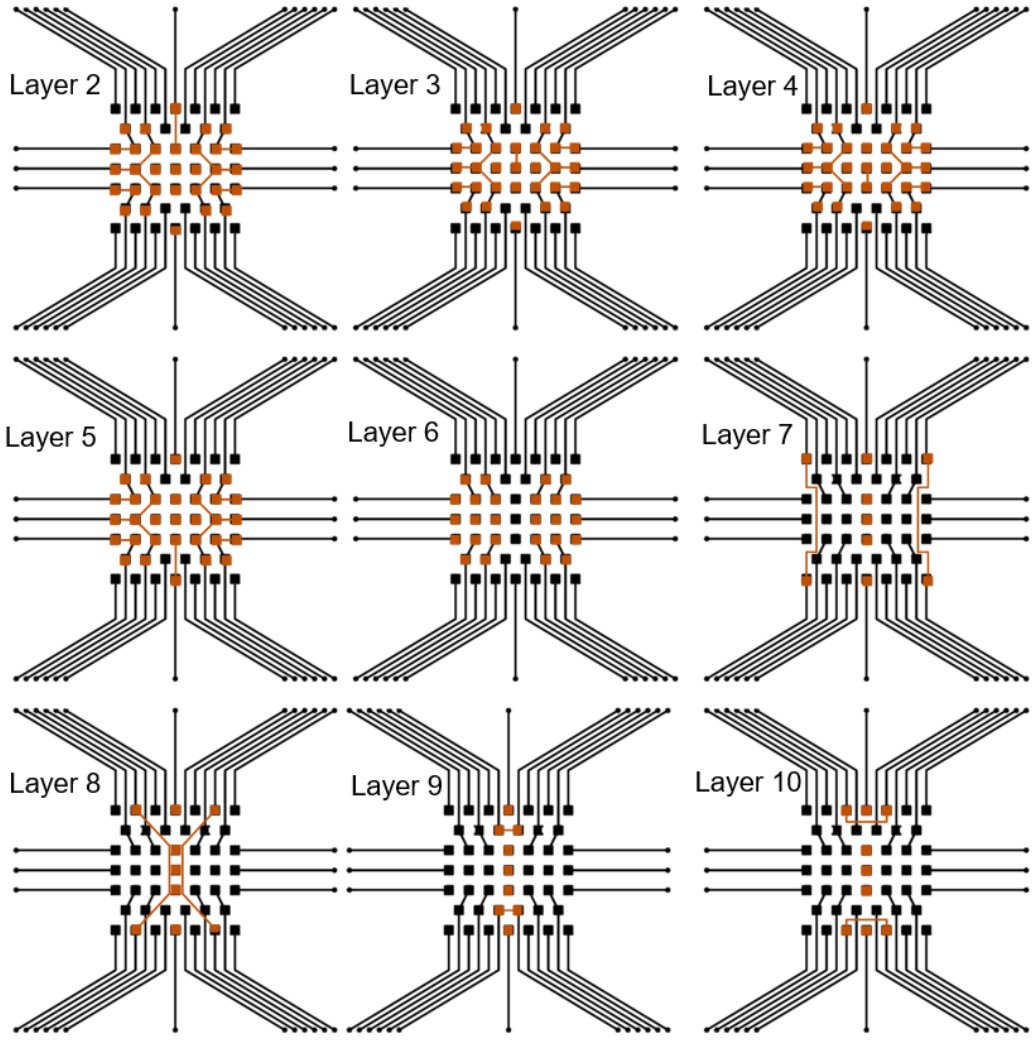


**Figure S2.** Circuit diagram from the second to tenth layers.

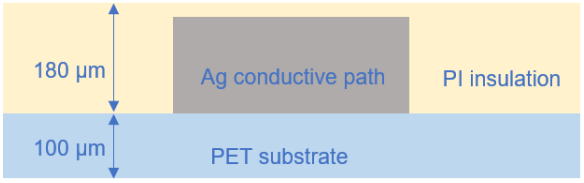


**Figure S3.** Cross-section schematic diagram of the FEA model

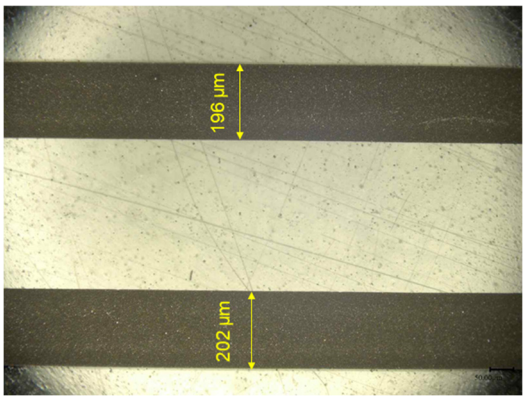


**Figure S4.** The conductive path printed by EHD.