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A Low-Power, Fully Integrated SC DC–DC Step-Up Converter with Phase-Reduced Soft-Charging Technique for Fully Implantable Neural Interfaces

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Abstract: We present a high-power conversion efficiency (PCE) on-chip switched-capacitor (SC) DC–DC step-up converter for a fully implantable neural interface operating with less than a few tens μW from energy harvesting. To improve the PCE in such light loads and wide variations of voltage-conversion ratio (VCR), which is a typical scenario for ultra-low-power fully implantable systems depending on energy harvesting, a phase-reduced soft-charging technique has been implemented in a step-up converter, thereby achieving very low VCR-sensitive PCE variation compared with other state-of-the-art works. The proposed DC–DC converter has been fabricated in a standard 180 nm CMOS 1P6M process. It exhibits high PCE (~80%) for wide input and output ranges from 0.5 V to 1.2 V and from 1.2 V to 1.8 V, respectively, with switching frequencies of 0.3–2 MHz, achieving a peak efficiency of 82.6% at 54 μW loads.

Keywords: DC–DC converter; step-up converter; soft-charging; switched-capacitor (SC); neural interfaces; low-power electronics

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1. Introduction

Among the various system requirements for fully implantable neural interfaces, the energy source and its proper management have been recognized as among the biggest concerns. Since the fully implantable system, as its name indicates, must be implanted inside the body, the energy sources for the operation of the system are scarce and are hard to manage efficiently due to the lack of stability of the energy sources. One solution to resolve this issue is to cause the active circuits for the fully implantable neural interface to operate with as low power as possible, making it less sensitive to the amount of available energy. This approach has resulted in many low-power neural interface architecture and circuit design techniques [1–17]. The other solution is to guarantee enough energy sources even inside the body via efficient energy harvesting and optimal management of them. A few viable energy-harvesting solutions have recently been made available in the community, some of which show promising results for fully implantable systems to be deployed in real application fields [18,19].

However, each energy-harvesting solution still has a few technical hurdles for a fully implantable system to be used practically. One of the most popular and widely adopted solutions is wireless power transfer (WPT) using electromagnetic near fields, i.e., magnetic field coupling. WPT using magnetic fields can transcutaneously transfer enough power (a few mW–a few tens of mW) for the operation of most of the fully implantable neural interfaces with minimal loss when choosing the right operating frequency, i.e., 13.56 MHz industry, scientific, and medical (ISM) band, hence, it is widely adopted in wireless neural recordings and stimulations [19–21]. However, WPT using a magnetic field has some drawbacks; it suffers from high sensitivities for distance, angular alignment, and relative size between primary and secondary coils, complicating in vivo experiments [22,23]. In addition, due to the relatively low frequency chosen for the small loss when the magnetic

field propagates through the body, the coil size (secondary coil to be implanted inside the body) becomes bulky (by a few centimeters), which may result in foreign-body reactions. To tackle this issue, a millimeter-sized coil for implantable devices using ~GHz frequency has been proposed [24]; however, the maximum power it can provide is only a few μW and its energy-transfer sensitivity seems too high, limiting its applications.

Recently, WPT based on ultrasound or light has drawn much attention as an alternative candidate for energy sources suitable for fully implantable neural interface systems. Since the piezoelectric and photovoltaic effects are free of matching limitations imposed by wavelengths, the recipients, such as piezoelectric devices and *p*–*n* junctions, can be implemented in relatively small sizes inside the body [25,26]; moreover, because the amount of energy they can transfer depends on the materials (even though it depends on the size), one can easily design those devices accordingly. One pointed-out drawback of such devices is that the amount of energy they produce is highly affected by environmental factors, such as the presence of obstacles and light or ultrasound intensity, requiring careful power management for reliable operation of the fully implantable systems. Figure 1 shows typical power management for ultrasound or light-energy harvestings. To deal with such environmental variations, the maximum power-point tracking (MPPT) algorithm is commonly employed with energy-harvesting systems to adjust the operating point of the energy source. The MPPT module sensing the condition of input or output according to the type of its algorithm allows the DC–DC converter to operate at a point where it can produce maximum power from an energy source, and, if necessary, a battery is used to store excess energy. In addition, DC–DC converters engaged in those energy harvestings should operate efficiently and reliably despite such fluctuations in the operating points. From the perspective of power management, such changes of the operating point from energy sources can be translated into a large variation of the input voltage in the given impedance; in other words, a DC–DC conversion that is capable of producing a fixed (or controllable) output voltage despite wide input-voltage variation is very necessary for the reliable operation of loads (implantable interfaces).

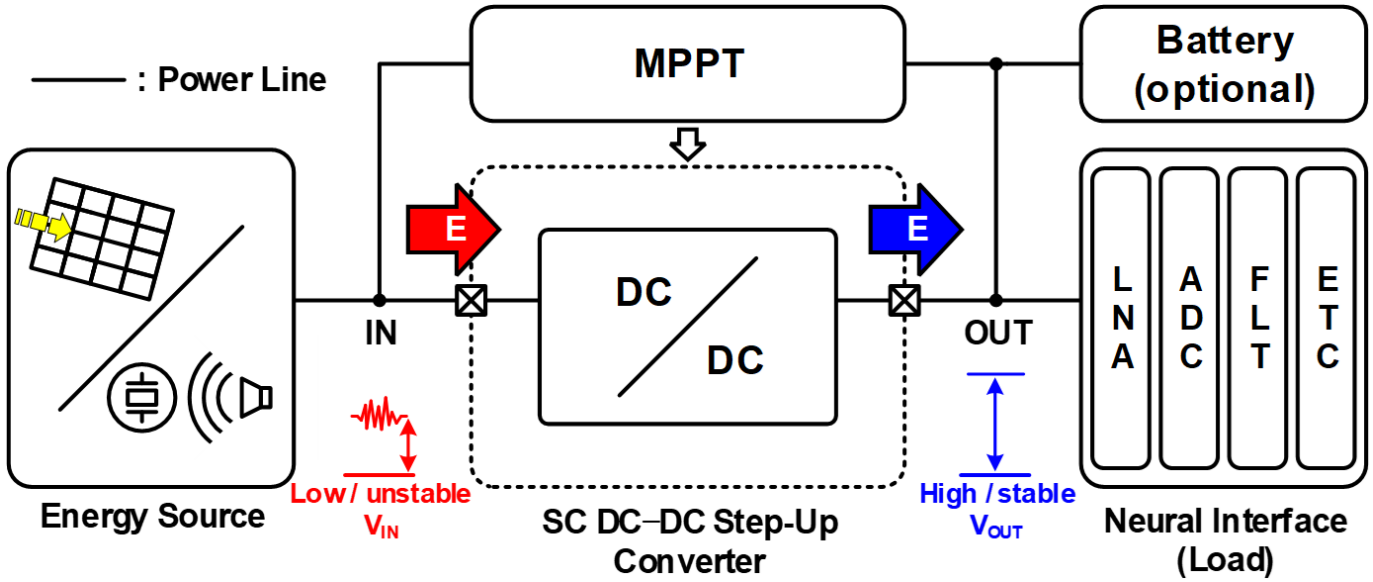


Figure 1. Conceptual operation scenario for a fully implantable neural interface which relies on energy harvesting; the proposed soft-charge-based DC–DC converter plays a central role for reliable operation of the neural interface.

In this paper, we present a switched-capacitor (SC) step-up converter which exhibits very low PCE variation, even though there are large variations of input power, while maintaining high PCE; thus, it is suitable for a fully implantable neural interface that depends on solar, thermoelectric tag [27,28], or ultrasonic (in this case, combined with

a rectifying circuit [29]) energy harvesting. The converter has been implemented by adopting a recently announced soft-charging technique [22] and modifying it by introducing a phase-reduction scheme for better PCE and uniformity. Our modification has provided the implemented DC–DC SC step-up converter with high and flat power conversion efficiency (PCE ~80%) for a wide range of input variations, from 0.5 to 1.2 V, even with the ultralight load of ~μA, thereby achieving >30% smaller variation in PCE. In addition, our DC–DC converter has been fully implemented on-chip; therefore, the energy-harvesting device (*p*–*n* junctions if choosing light as energy sources, in particular near-infrared light for implantable devices, see [30,31]) and the active circuit for neural interface systems, such as low-noise neural recording amplifier, filter, and analog-to-digital converter, can be fully integrated within a single die, possibly increasing the level of integration that is more favorable for fully implantable systems.

2. Soft-Charging Technique

In this section, the soft-charging technique will be briefly explained to provide a better understanding of our proposed phase-reduction scheme. The term "soft-charging" originated from a familiar fundamental phenomenon of charge redistribution when multiple capacitors interact. The soft-charging technique has been widely accepted in the implementation of the fully integrated switched-capacitor DC–DC converter due to its inherent low charge-redistribution loss (CRL) and fine granular voltage-conversion ratio (VCR) [32] when properly engaged [33,34]. Unlike conventional SC converters charging a certain amount of the energy from input to a single capacitor (or a few, but not many) and conveying it to the output capacitor (which is usually a single capacitor as well), in soft-charging DC–DC converters, the energy is divided into N capacitors at the input, and then each capacitor transmits a fraction of the entire energy to the output. In this way, the CRL generated in the charge-transfer process between capacitors can be efficiently reduced according to the dividing factor N [32]. If N can be increased infinitely, the CRL will be approximately zero, thus, the ideal energy-delivery efficiency (or PCE) can reach 1; however, in practical implementations, N would be limited because the number of switches and the control circuit complexity will increase, and thereby the related switching loss, conduction loss, and power consumption in the control circuit will escalate.

2.1. Conventional Soft-Charging Technique

The soft-charging technique can be visualized through the analysis of phase flow for a multi-phase step-up converter consisting of multiple capacitors. Figure 2a shows the voltage level of all flying capacitors in a step-up converter employing the soft-charging technique, denoted as C_1 to $C_{2n+2m+4}$ at the moment of the k^{th} phase. Let us assume that a conventional soft-charging step-up converter forms V_{OUT} by dividing V_{IN} into $(n + 1)$ fractions and stacking it $(m + 1)$ times on V_{IN}, requiring the number of $(2n + 2m + 4)$ capacitors and phases. In every phase, at least one of the top and bottom plates of flying capacitors must be connected to fixed voltage levels, such as V_{IN}, V_{OUT}, and *GND*, and the other plate of the capacitors must be interconnected with other flying capacitors to transmit or receive a certain amount of charge. Via such interconnections, the virtual voltage levels $V_{B[1]}$ to $V_{B[n]}$ and $V_{T[1]}$ to $V_{T[m]}$ are generated and soft-charging can be facilitated. The top and bottom plates' generated virtual voltage levels can be expressed as:

$$\Delta V_B = \frac{V_{IN}}{n+1} = \Delta V_T = \frac{V_{OUT} - V_{IN}}{m+1} \quad (1)$$

The optimal condition to achieve the smallest CRL with the given number of capacitors can be achieved when they each have the same amount of voltage difference; thus, the optimal voltage conversion ratio (VCR_{OPT}) that produces the smallest CRL is expressed as:

$$VCR_{OPT} = \frac{V_{OUT}}{V_{IN}} = \frac{n+m+2}{n+1} \quad (2)$$

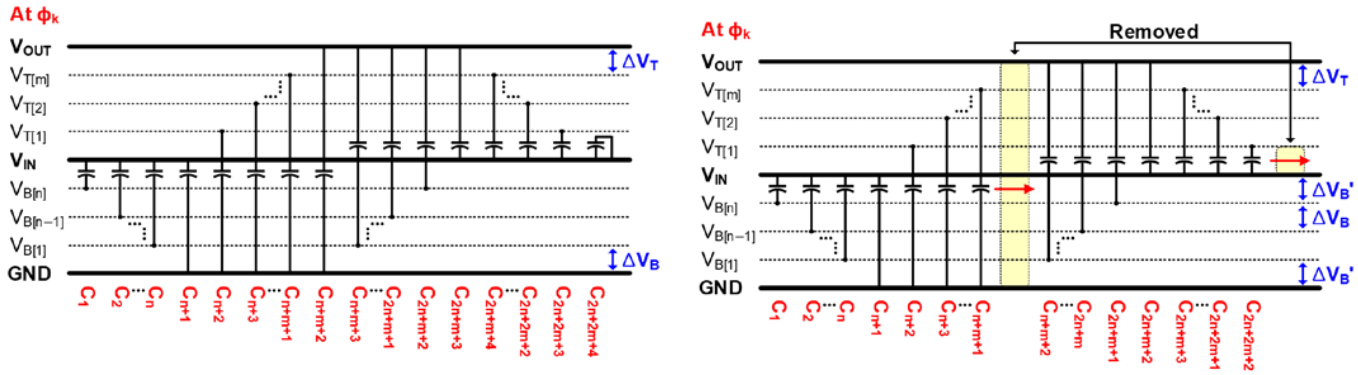


Figure 2. The voltage level of the flying capacitor at a kth phase in (**a**) a conventional structure and in (**b**) a phase-reduced topology.

The amount of charge supplied by the input (Q_{IN}) and transferred to the output (Q_{OUT}) at one phase, and PCE can also be expressed as:

$$Q_{IN} = C_{fly} \cdot [(n+2)\Delta V_B + m\Delta V_T] \quad (3)$$

$$Q_{OUT} = C_{fly} \cdot (n+1-1)\Delta V_B = C_{fly} \cdot n\Delta V_B \quad (4)$$

$$PCE_{conv} = \frac{P_{OUT}}{P_{IN}} = \frac{f_{CLK}(Q_{OUT} \cdot V_{OUT})}{f_{CLK}(Q_{IN} \cdot V_{IN})} = \frac{n}{n+1} \quad (5)$$

where C_{fly} is the capacitance of a unit flying capacitor (C_1~$C_{2n+2m+4}$). As shown in Equation (5), the maximum PCE which the converter can achieve is solely determined by n when considering only the CRL as a loss.

2.2. Phase Reduction in Soft-Charging Technique

According to analysis of the conventional soft-charging technique applied for a step-up DC–DC converter as shown in Figure 2a, one can be sure that the larger n will definitely provide better efficiency, but a question arises: what about the power consumption in the many switches related to each phase and, consequently, the complicated controller? In this section, we will provide the proposed phase-reduction scheme that can achieve higher PCE, even if the same n and m with the conventional soft-charging technique are employed (in other words, the same PCE with the conventional one while requiring lower overhead implementation). Figure 2b shows the phase-reduced soft-charging technique applied for a step-up DC–DC converter where two redundant phases have been removed from the conventional one at ϕ_k. At the following phase (ϕ_{k+1}), one can expect that C_{n+m+1} and $C_{2n+2m+2}$ of Figure 2b have the same voltage level of C_{n+m+2} and C_1, respectively, meaning that they preserve the same amount of charge. At the same time, this phase-reduced topology not only skips the phase but also results in changes in virtual voltage levels lower than V_{IN} ($V_{B[1]}$~$V_{B[n]}$). Figure 3 shows this phenomenon clearly. In the conventional topology, a bottom plate of C_{2n+m+1} and that of discharged $C_{2n+2m+4}$ are connected causing charge redistribution at ϕ_{k+1}, and $C_{2n+2m+4}$ receives a charge of q, but in the phase-reduced topology, as the C_{2n+m} and $C_{2n+2m+2}$ precharged by q are charge-redistributed, $C_{2n+2m+2}$ obtains a charge of q', which causes $V_{B[n]}$ to be lower than before. Under the same principle, $V_{B[1]}$ has increased compared to its conventional topology. As $V_{B[1]}$ and $V_{B[n]}$ are changed, $V_{B[2]}$~$V_{B[n-1]}$ are changed as well but V_T remains at its voltage level and optimal VCR is not changed, i.e., $\Delta V_T = (V_{OUT} - V_{IN})/(m+1) = V_{IN}/(n+1)$ and $VCR_{OPT} = (n+m+2)/(n+1)$. Considering the amount of charge transferred through the interaction of capacitors, $\Delta V_B{}'$ expressing the potential difference ($V_{B[1]} - GND$) and ($V_{IN} - V_{B[n]}$), ΔV_B expressing

the voltage step from $V_{B[1]}$ to $V_{B[n]}$, and $V_{B[k]}$ of phase-reduced topology can be expressed as follows:

$$\Delta V'_B - \Delta V_T = \Delta V_B,\ V_{IN} = 2\Delta V'_B + (n-1)\Delta V_B \tag{6}$$

$$\Delta V_B = \frac{n-1}{(n+1)^2} V_{IN},\ \Delta V'_B = \frac{2n}{(n+1)^2} V_{IN} \tag{7}$$

$$V_{B[k]} = \Delta V'_B + (k-1)\Delta V_B \ \ (1 \le k \le n) \tag{8}$$

According to Equation (7), Q_{IN} and Q_{OUT} at a given phase, and PCE can be expressed as:

$$Q_{IN} = C_{fly} \cdot [(\Delta V'_B - \Delta V_T) + (n-1)\Delta V_B + 2\Delta V'_B + m\Delta V_T] \tag{9}$$

$$Q_{OUT} = C_{fly} \cdot [(\Delta V'_B - \Delta V_T) + (n-1)\Delta V_B + \Delta V'_B] \tag{10}$$

$$PCE_{ph-rd} = \frac{P_{OUT}}{P_{IN}} = \frac{f_{CLK}(Q_{OUT} \cdot V_{OUT})}{f_{CLK}(Q_{IN} \cdot V_{IN})} = \frac{n^2+nm+2n}{n^2+nm+3n+m} = \frac{n+\frac{2}{n+m}}{n+\frac{2}{n+m}+1} \tag{11}$$

Therefore, the proposed phase-reduced topology is always more efficient than the same conventional soft-charging one; in other words, better PCE can be achieved with the same numbers of n and m. A numerical calculation confirms this. Figure 4 compares the calculated PCE in both conventional and proposed phase-reduced soft-charging techniques by varying n and m. As shown, phase-reduced soft-charging provides better PCE than the conventional one and the enhancement is increased when n or m becomes smaller. In addition, the converter with the proposed phase-reduced scheme can result in less PCE variation than the conventional soft-charging converter even though the converter is not operating in optimal VCR conditions. Since the PCE slope of the phase-reduced scheme in Figure 4 is always sluggish compared to the conventional one, it can be deduced that the PCE is insensitive when n or m changes but optimal VCR is maintained, or when n or m is the same but VCR is changed. This result is of particular importance because most energy-harvesting sensors (especially implantable sensors) must be limited in their size, and, thus, it is usually hard to implement a complicated controller for DC–DC conversion; also, large VCR variations due to the instability of the energy-harvesting sources must be compensated for in the DC–DC converter while maintaining high PCE.

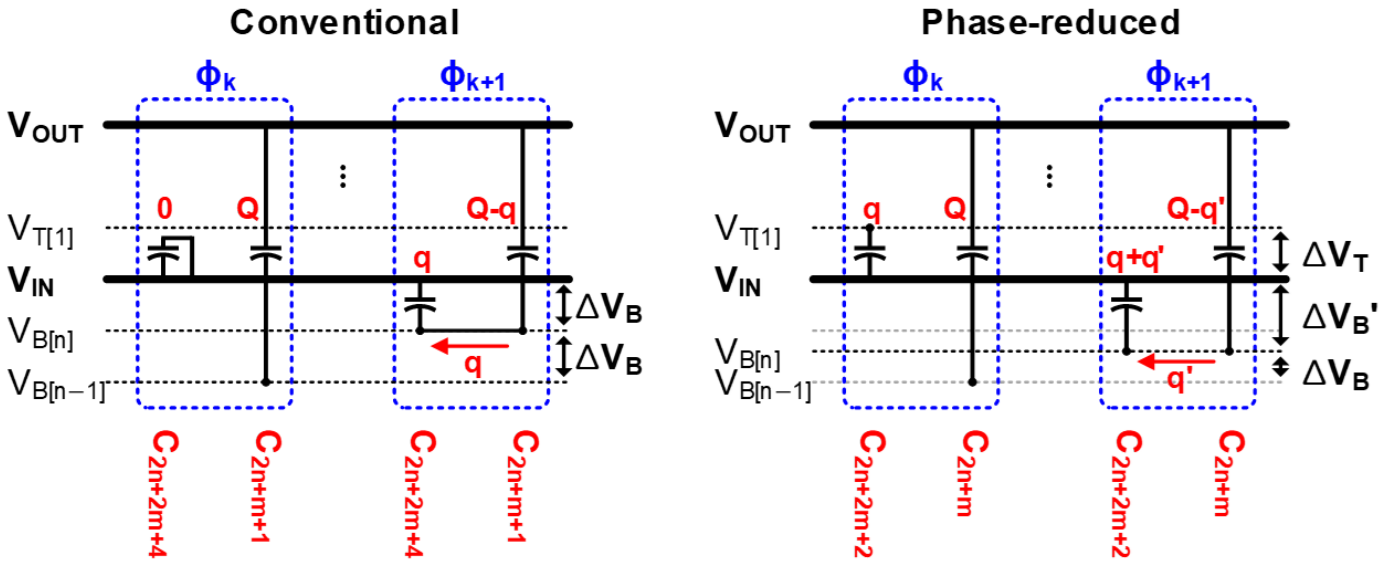


Figure 3. Phase diagram comparing V_B of conventional with that of phase-reduced topology.

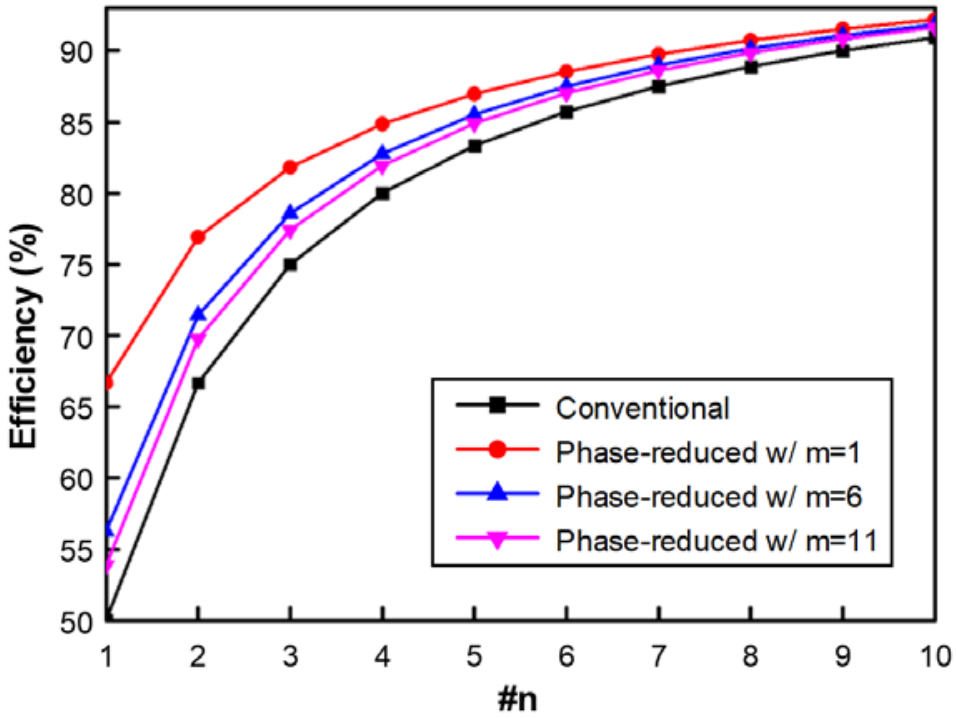


Figure 4. PCE comparison of phase-reduced topology with conventional topology.

3. Overall Circuit Implementation

To check the feasibility of the proposed phase-reduction scheme, we have implemented a soft-charging-based step-up SC DC–DC converter with n = 9 and m = 13 (VCR_{OPT} = 2.4). According to Figure 4, the condition at n = 9 would not provide a large improvement but we chose it because (1) our target is to achieve ~80% flat overall PCE even with large input power variations and (2) in the next run, we are going to integrate this converter with a silicon p–n junction as an energy-harvester, which may generate a quite low output voltage (0.4~0.5 V) while generating high voltage, >1 V. Figure 5 shows the overall circuit implementation. A unit cell consists of one flying capacitor (100 pF), its counter phase (CP) flying capacitor which operates with a π-phase difference, and the related power switches (a total of 52). The two capacitors in the unit cell complementarily share the logic signals for their controls, thus, those consume less logic power (about half) compared to ($2n + 2m + 2$)-cells composed of only one flying capacitor, enabling more efficient energy transfer. The power switches are implemented by using a medium voltage transistor (MVT) because a nominal V_{TH} ~0.55 V in the given 180 nm process cannot completely turn on/off switches. In each plate of the flying capacitor, the switch type (NMOS or PMOS) has been carefully selected for stability of operation. The gate signals for the switches on the bottom side (SB) are connected to the bottom side switches operating *GND* to V_{IN}, and the ones for the switches on the top side (ST) are connected at the top side switches for V_{IN} to V_{OUT}. Each phase control signal is generated by dividing the clock signal (CLK) from the cascaded D-flip-flops and logic gates. The CLK has a 75% duty ratio to provide the capacitors with enough time to completely settle and to guarantee non-overlapping between each phase signal. The supply voltage of all logic circuits comes from V_{IN}, but the level shifter uses both V_{OUT} and V_{IN}.

The start-up process has been achieved via the forward-conducting p–n junctions (body-to-source/drain) and subthreshold leakage of the power switches. For a reliable start-up, the load should not be connected before V_{OUT} rises to a certain voltage (~0.3 V). To guarantee this reliable start-up operation, we implemented a dynamic comparator and a switch at the output. Once V_{OUT} is larger than V_{REF}, the SW_{LOAD} connects the output of the converter to external loads. To regulate V_{OUT} at the desired value, pulse skipping

modulation (PSM) has been employed at the on-chip and pulse frequency modulation (PFM) at the off-chip. When $V_{OUT,f} > V_{REF}$, all phase signals except P_1 are turned off and the charge transferring to the output is stopped. If $V_{OUT,f}$ is reduced below V_{REF}, P_1~$P_{2n+2m+2}$ are generated again to regulate the output properly. The main CLK varies from 0.3 to 2 MHz; those are fast enough to regulate V_{OUT} within 50 mV deviation at a maximum current of 36.4 µA in transience at the output. The comparator has a 40 mV hysteresis to prevent output bouncing due to the noise.

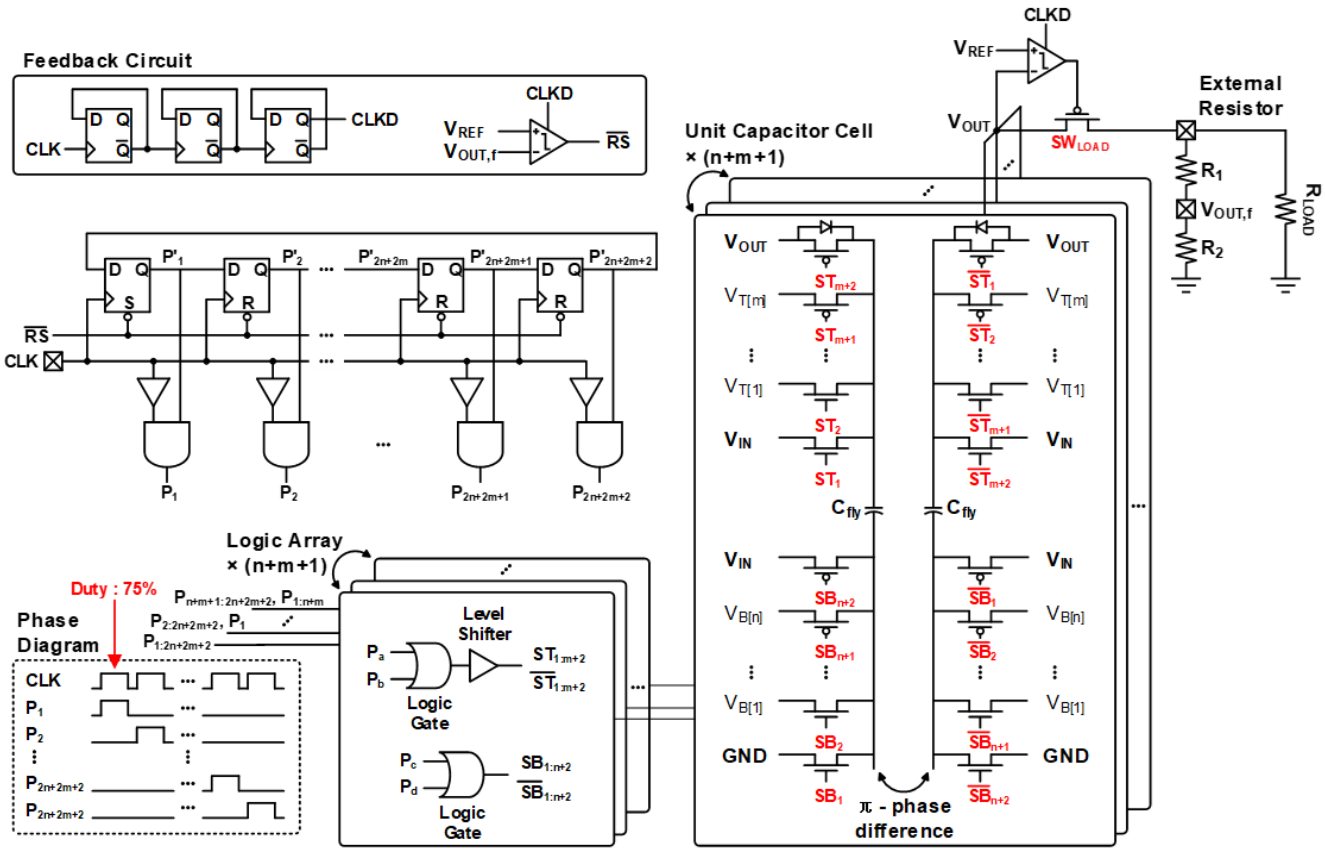


Figure 5. Overall circuit implementation of the step-up DC–DC converter with the phase-reduced soft-charging technique.

4. Measurement Results

The implemented SC step-up DC–DC converter has been fabricated in a standard 180 nm CMOS 1P6M process. Figure 6 shows a microphotograph of the fabricated chip. The active area is 3.5 × 1.4 mm^2, mostly occupied by MIM (metal–insulator–metal) capacitors. The total capacitance is ~4.6 nF. The logic and virtual voltage level wires shared by the two flying capacitors, as described in the previous section, are located between the counter-phase flying capacitors. Since virtual voltage level wires are common connections between all of the capacitors, they are routed in a ring shape, so that charge passes through all cells. In consideration of the long path, we carefully layout that path to connect all cells in parallel with a large width to reduce a series resistance component in the entire course, so we have less affected the overall PCE.

Figure 7 summarizes the transient responses of the fabricated converter. Figure 7a shows V_{OUT} nominally set as 1.2 V while the load current pulse abruptly changes from 0 to 36.4 µA (equivalently $R_L \approx 33$ kΩ). V_{OUT} increases during the soft-charging state, supplying charges to the output. When the output becomes larger than the given reference (V_{REF}), all phase signals except P_1 stop so that the output capacitor (C_{OUT}) solely supplies load current; therefore, V_{OUT} decreases. Depending on the amount of load current, only the speed at which the charge is accumulated in the C_{OUT} varies, i.e., voltage slope, but average

V_{OUT} is maintained. You can notice that there is PSM operation even if there is no load since V_{OUT} must feed the control logic and power switches; however, if the load consumes more than the maximum output current, feedback circuits cannot operate properly, decreasing V_{OUT} as shown in Figure 7b. It can be seen that if the load requires more current than the input can supply, $V_{OUT,f}$ cannot reach V_{REF}, so feedback does not work. Figure 7c depicts V_{OUT} (fixed at 1.2 V) when V_{IN} is abruptly changed between 0.5 and 0.6 V. When V_{IN} = 0.6 V, the output voltage is slightly reduced because an optimized VCR has not been established, but the feedback is still operating normally and supplying the load current. The start-up process is also shown in Figure 7d. As mentioned in Section 3, V_{OUT} slowly increases until it rises to the nominal V_{TH} ~300 mV of the MVT device, and then shows a sharp transition. In the section where the V_{OUT} increases slowly, only a small amount of charge flows through the *p*–*n* junctions and sub-V_{th} channel of the power switch, so that the slope is gradual. After the V_{OUT} becomes ~300 mV, the top-side switches operate properly, and turn on the switches connected to the load. It takes ~50 ms for V_{OUT} to reach the desired level of 1.2 V.

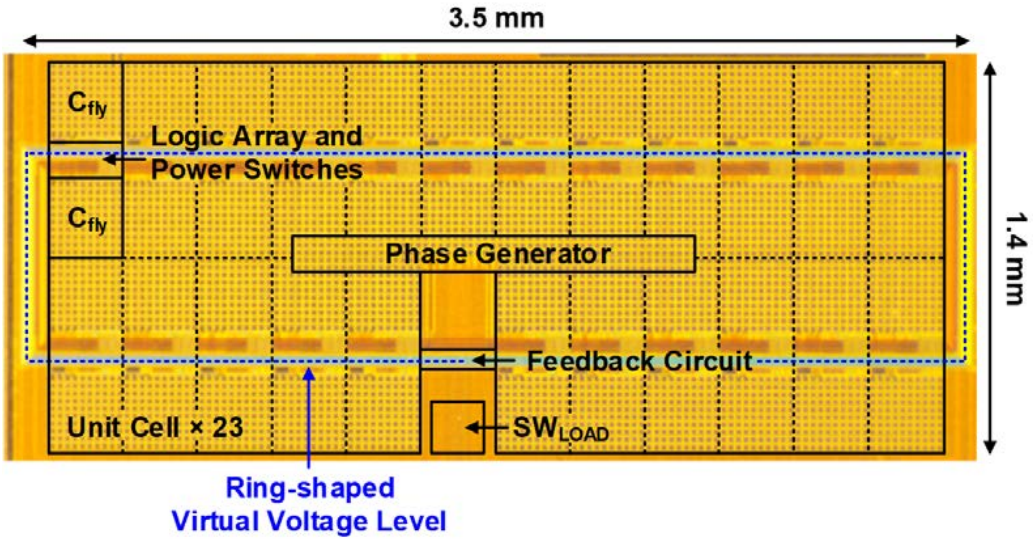


Figure 6. A microphotograph of a fabricated phase-reduced soft-charging step-up converter.

The PCE of the fabricated step-up DC–DC converter has been comprehensively measured. Figure 8a depicts the PCEs by varying the clock frequency (f_{CLK}) and V_{IN} while keeping V_{OUT} as 1.2 V with 60 kΩ load (I_{LOAD} = 20 μA, P_{OUT} = 24 μW) without guaranteeing optimal VCR. As shown, when the clock speed is properly adjusted for the converter it delivers the necessary charge at the output, and the PCE remains flat at ~80% despite the wide variation of V_{IN} from 0.5 V to 0.8 V, i.e., the VCR is far away from the VCR_{OPT}. Figure 8b shows the optimized PCEs of the fabricated converter by adjusting the VCR point by point. As the V_{OUT} (V_{IN} also changed to maintain VCR = 2.4) increases, strong inversion of each FET is ensured, and the charge is delivered better, resulting in higher peak PCE; however, the overall PCE variation is not different to the one without optimization in Figure 8a. Measured virtual voltage levels are also provided in Figure 9. As previously seen in Figure 2b, a flying capacitor is soft-charged while being charged/discharged through a small amount of voltage step, as illustrated in Figure 9a. The virtual voltage levels ($V_{B[1]}$~$V_{B[9]}$ and $V_{T[1]}$~$V_{T[13]}$) generated during the charge-transfer process of several flying capacitors are shown in Figure 9b. At this time, the mid-level of V_B, especially $V_{B[4]}$, tends to ripple because the threshold voltage of the power switches connected to this level is insufficient to ensure adequate settling time regardless of switch type, and this ripple is represented as conduction loss.

The maximum PCE by varying V_{IN} for both 1.2 and 1.8 V V_{OUT} is shown in Figure 10, indicating that the PCE has a flat distribution of around 80% in the wide range of input voltages. This measurement was performed under the 60 kΩ load condition. The peak

PCE was measured as ~82.6% when V_{IN} = 0.95 V, V_{OUT} = 1.8 V, and f_{CLK} = 342 kHz. Table 1 compares the performance of our fabricated converter with other state-of-the-art switched-capacitor DC–DC converters. To highlight the stable and high-power conversion performance of our converter even with wide input-voltage variations, we created a figure of merit termed as VCR sensitivity. VCR sensitivity can be calculated as the ratio of the PCE to VCR variations (VCR sensitivity = ΔPCE/ΔVCR, smaller is better), indicating how much PCE variation of the given converter shows when the VCR changes. Our SC step-up DC–DC converter shows comparable performance with others in terms of the VCR range and PCE, and much better performance in VCR sensitivity; this means a smaller PCE variation in spite of the wide input-voltage fluctuation, which is a desirable characteristic for power management dedicated to energy harvesting along with continuous PCE.

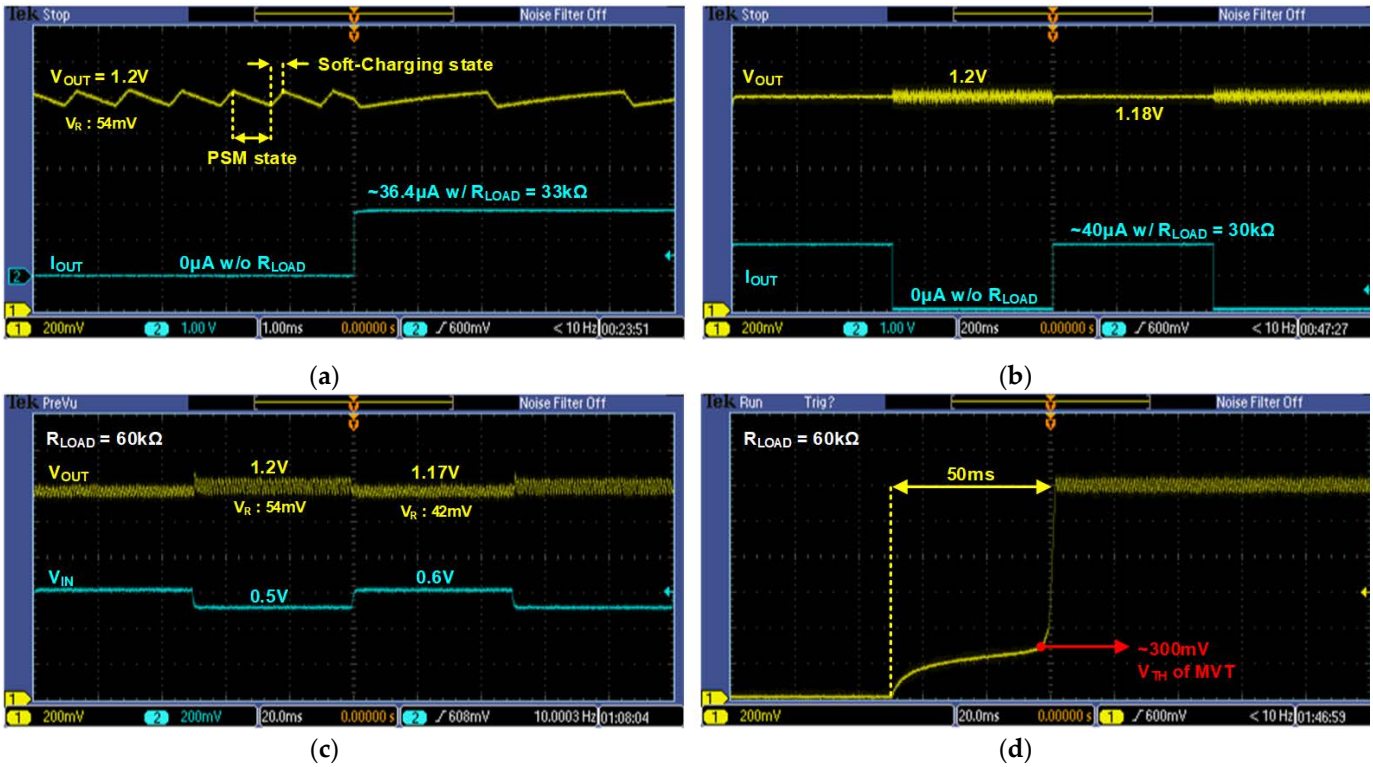


Figure 7. Captured waveform measuring (**a**) load regulation with 33 kΩ, (**b**) load regulation with 30 kΩ, (**c**) line regulation at V_{IN} = 0.5–0.6 V and (**d**) start-up sequence.

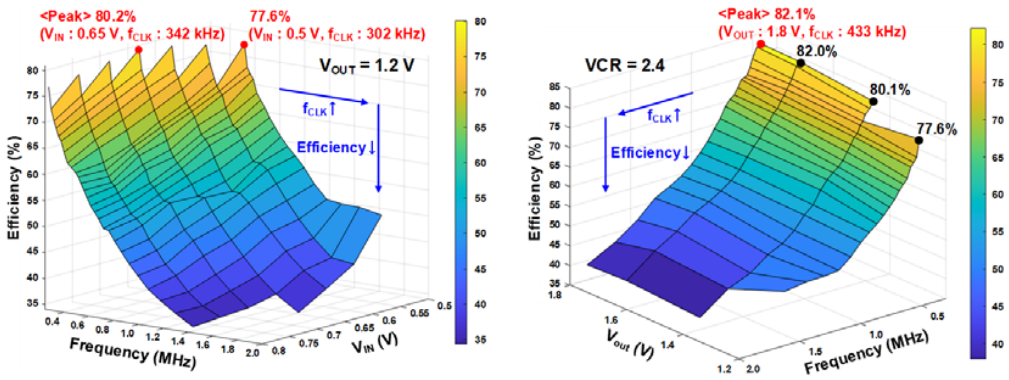
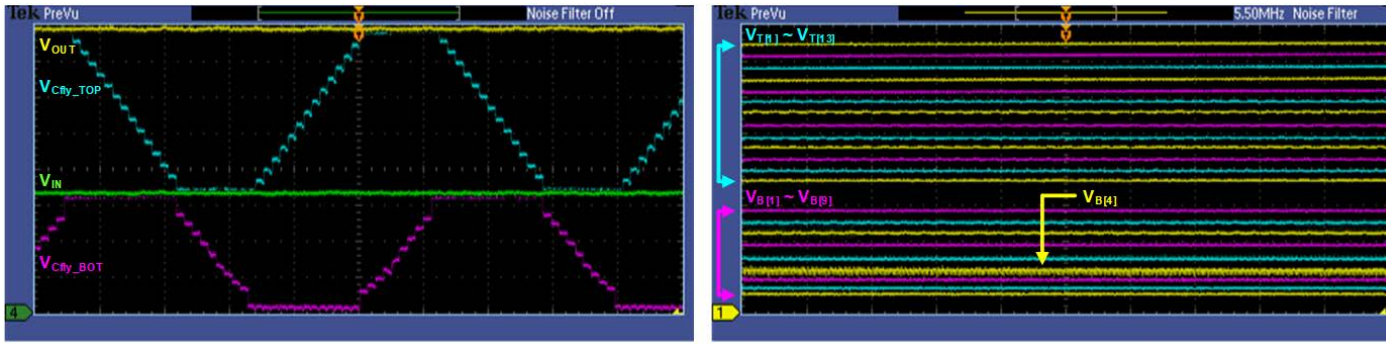


Figure 8. Measured PCE plot (**a**) under fixed V_{OUT} = 1.2 V condition and (**b**) under fixed VCR = 2.4 condition.



(**a**) (**b**)

Figure 9. Measured voltage level of (**a**) V_{IN}, V_{OUT} and each plate voltage of one flying capacitor (V_{Cfly_TOP} and V_{Cfly_BOT}) and (**b**) virtual node ($V_{B[1]}$~$V_{B[9]}$ and $V_{T[1]}$~$V_{T[13]}$), at V_{IN} = 0.75 V and V_{OUT} = 1.8 V.

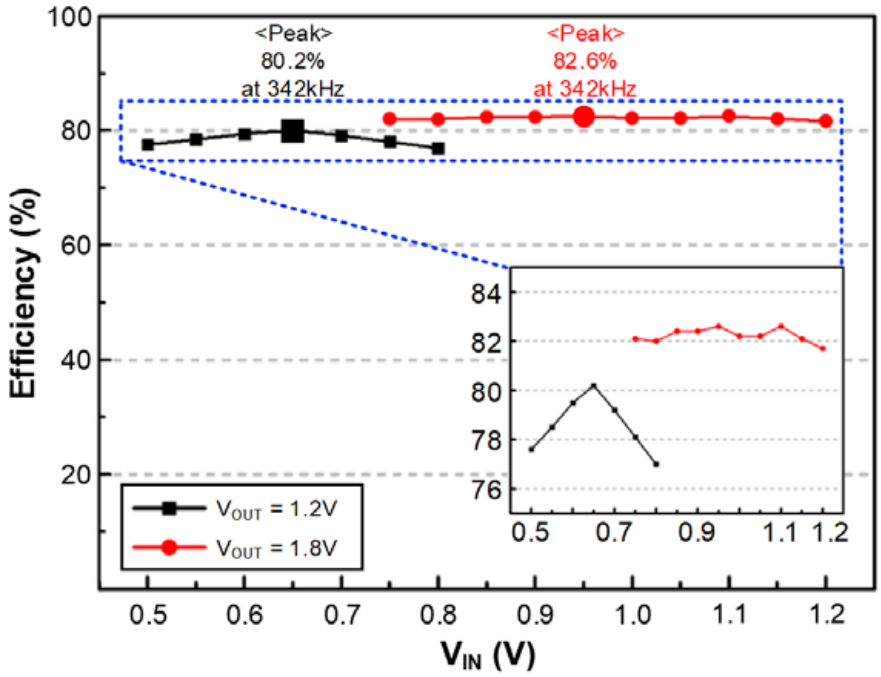


Figure 10. Measured PCE plot with varied V_{IN} and V_{OUT} under optimized frequency conditions.

Table 1. Summary and comparison with recent state-of-the-art works.

	[32]	[33]	[1] [34]	[35]	[36]	**This Work**
Technology	28 nm	180 nm	180 nm	65 nm	65 nm	**180 nm**
Topology	Out-phasing	Soft-Charging	Soft-Charging	Buck + Boost	Buck + BoostSCPC	**Phase-Reduced Soft-Charging**
V_{IN} (V)	3.2	0.1–0.5	0.95–1.8	0.22–2.4	0.25–1	**0.5–1.2**
V_{OUT} (V)	0.95	0.75	1.8	0.85–1.2	0.9–1.5	**1.2–1.8**
VCR	0.33	1.5–7.5	1–1.89	0.5–7 (#24)	0.9–6	**1.5–2.4**
PCE_{peak} (%)	82.0	85.4	85.3	84.1	86.0	**82.6**
[2] VCR Sensitivity (%/VCR)	-	-	3	34.22	20	[3] **1/2.9**
Area (mm^2)	0.117	3.89	1.75	2.4	1.4	**4.9**

[1] Only the power-management unit considered. [2] VCR sensitivity = (PCE_{peak} − PCE_{min})/ΔVCR. [3] 1 at V_{OUT} = 1.2 V and 2.9 at V_{OUT} = 1.8 V.

5. Conclusions

In this paper, we have presented a prototype low-power, fully integrated SC DC–DC step-up converter with the proposed phase-reduced soft-charging scheme for a fully implantable neural interface. For reliable operation of the fully implantable neural interface, the power-management module must guarantee stable power transfer with high PCE despite large variations of energy source due to unexpected environmental changes. Thanks to the proposed phase-reduced soft-charging technique, we achieved high (~80%) and flat PCE (1 VCR sensitivity at V_{OUT} = 1.2 V and 2.9 VCR sensitivity at V_{OUT} = 1.8 V) even with large input-voltage variations (0.5−1.2 V) in the measurement of the prototype chip; also, other performances, such as the peak PCE and VCR range, are comparable with state-of-the-art works.

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