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4H-SiC/SiO_2 Interface Degradation in 1.2 kV 4H-SiC MOSFETs Due to Power Cycling Tests

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Abstract: Power cycling tests (PCTs) assess the reliability of power devices by closely simulating their operating conditions. A PCT was performed on commercially available 1.2 kV 4H-SiC power metal–oxide–semiconductor field-effect transistors to observe its impact on the 4H-SiC/SiO_2 interface. High-resolution transmission electron microscopy and electron energy loss spectroscopy measurements showed variations in the length of the 4H-SiC/SiO_2 transition layer, depending on whether the device was power cycled. Moreover, the total resistance at $V_g \gg V_t$ in $R_{tot} - (V_g\text{-}V_t)^{-1}$ graph increased to 16.5%, while it changed more radically to 47.3% at $V_g \approx V_t$. The threshold voltage shifted negatively. These variations cannot be expected solely through the wearout of the package.

Keywords: power cycling test; 4H-SiC; interface

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1. Introduction

Silicon carbide (SiC) exhibits superior material properties compared to traditional silicon, making it highly suitable for power devices. In terms of thermal conductivity, SiC boasts a high value, enabling efficient heat dissipation and operation at elevated temperatures, crucial for power electronics [1,2]. Additionally, SiC's high critical electric field allows it to handle high voltages with minimal resistance, enhancing device performance and reliability [3,4]. When compared to silicon insulated-gate bipolar transistors (IGBTs), SiC devices offer lower drift region resistance and a higher critical electric field, translating to improved efficiency and reliability in high-power applications [5]. The robustness of 4H-SiC devices makes them well-suited for harsh environments, expanding their utility in diverse fields, from electric vehicles to renewable energy systems [6]. In EVs, the high thermal conductivity of SiC ensures efficient power management and cooling, while the high critical electric field enables the handling of high voltages required for electric propulsion systems. These characteristics make SiC devices ideal for enhancing the performance and efficiency of automotive EVs, contributing to the advancement of sustainable transportation technologies. As the industry seeks solutions for higher power demands and increased energy efficiency, the merit of 4H-SiC power devices lies in their crucial role in advancing the capabilities and reliability of power electronics.

On the other hand, the reliability of 4H-SiC power MOSFETs compared to silicon IGBTs is a topic of ongoing research and development, with several key issues that need to be addressed to ensure their widespread adoption in power electronics applications. Gate oxide reliability, a critical aspect of SiC MOSFET performance, is closely intertwined with high-temperature stress degradation. The gate oxide serves as a crucial interface between the gate electrode and the semiconductor material, playing a pivotal role in device operation. Stress conditions such as extreme high temperatures, voltage bias, and current loads can lead to performance degradation and device failure [7]. Ensuring robust gate oxide capable of withstanding elevated temperatures while switching is essential for adopting 4H-SiC

power MOSFETs. Failure modes in gate oxide include threshold voltage shifts and increased leakage currents [8]. High interface trap density is mentioned as the primary cause of these phenomena [8–11]. Therefore, there was a variety of research performed to overcome the reliability issue at the 4H-SiC/SiO_2 interface. Siqi Zhao et al. optimized the oxidation process of silicon carbide (SiC) to minimize defects at the interface, thereby enhancing the electrical properties of the MOSFETs. Additionally, the paper explores advanced techniques such as nitrogen implantation and wet oxidation processes to passivate near-interface traps and improve the overall electrical quality of the 4H-SiC/SiO_2 interface [12]. These strategies aim to mitigate interface-related challenges and enhance the performance and reliability of 4H-SiC power MOSFETs by addressing critical issues at the SiC/SiO_2 interface [10]. On the other hand, degradation owing to the 4H-SiC/SiO_2 interface becomes more pronounced while the device is operating [7,9].

Reliability assessments provide insights into the longevity, robustness, and failure modes under various operating conditions. As these devices find applications in electric vehicles, solar inverters, and aircraft power systems, understanding their reliability becomes indispensable. Therefore, JEDEC, AEC-A101, and AQG324 guide several tests to evaluate the reliability of power semiconductors. Among the various reliability tests, power cycling tests (PCTs) assess the reliability of power devices by closely simulating their operating conditions [13]. Failure modes commonly mentioned in PCTs include voids and cracks in the package [13,14]. The influence of power cycling-induced stress on the 4H-SiC/SiO_2 interface is often underestimated.

Figure 1 shows a series of resistances within the drain-to-source current path of high-voltage vertically double-implanted 4H-SiC n-type metal–oxide–semiconductor field-effect transistors (VD-MOSFETs). The total internal resistance (R_{tot}) is the sum of the resistance components.

$$R_{tot} = R_{contact} + R_{N+} + R_{channel} + R_{JFET} + R_{Drift} + R_{Substrate} \quad (1)$$

The predominant components contributing to the R_{tot} differ between Si and 4H-SiC. In 4H-SiC VD-MOSFETs, the resistance components related to the 4H-SiC/SiO_2 interface account for 80% of the R_{tot} [15]. The issues related to the 4H-SiC/SiO_2 interface are the accumulation of interfacial carbon [16,17], threefold-coordinated O and C interstitials [17], Si vacancies [18], and dangling Si and C bonds [17]. However, silicon power semiconductors and their interfaces with SiO_2 are yet to be investigated.

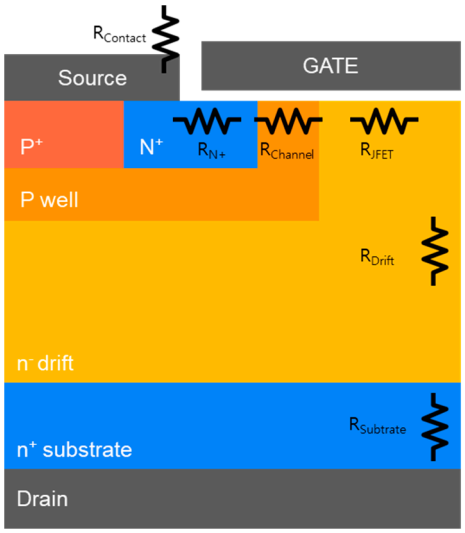


Figure 1. Series resistors of the total resistance (R_{tot}).

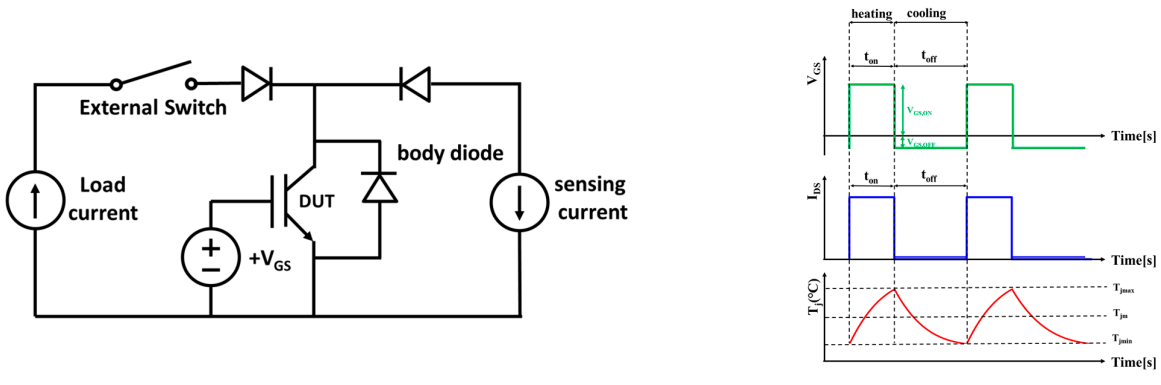
PCTs involve repeated switching of the gate electrode while simultaneously subjecting it to artificially high heating currents. Wearouts in solder voids and wire bonds are closely

related to the coefficient of thermal expansion (CTE). At each junction, the device under test (DUT) has different CTE rates [19]. When a heated current generates a junction temperature swing, the region where the CTE is different receives thermomechanical stress. Finally, the wire bonds are broken, increasing the solder voids.

Another perspective is that the power loss at each resistor in the current path is the origin of the ejected heat. Hence, the region exposed to electrical stress or a high heating current from the PCT is closely related to the resistance. The quality of a 4H-SiC/SiO_2 interface is poor; therefore, the channel resistance (R_{CH}) is a highly resistive element of the R_{tot} in 4H-SiC power MOSFETs. Therefore, the impact of the active chip is questionable. When subjected to stress like elevated temperatures or varying gate bias conditions, the influence of high interface trap density is magnified. Elevated temperatures can accelerate trap-assisted tunneling processes, leading to enhanced trap occupation and subsequent degradation in device characteristics [7]. Similarly, under different gate bias conditions, the interaction between carriers and interface traps can further exacerbate threshold voltage shifts and increase on-state resistance, affecting the overall performance of the MOSFETs [7,9]. Hence, in this paper, we conducted PCTs on 4H-SiC power devices and examined the changes in the devices before and after the tests. We investigated the failure modes and defects originating from the package, which are the primary causes of failure in power cycling tests. Additionally, we explored the internal defects and degradation within the devices. Through HR-TEM/EELS analysis, we examined differences in the 4H-SiC/SiO_2 transition layer depending on the PCTs. We studied the electrical characteristics influenced by the state of the 4H-SiC/SiO_2 interface. By utilizing transfer characteristic graphs measured before and after power cycling tests, we observed a negative shift in the threshold voltage and an increase in the resistance of the channel region. By conducting power cycling tests, which closely simulate the operating environment of 4H-SiC power MOSFETs, we examined the resulting changes not only in the package but also in the 4H-SiC/SiO_2 interface.

2. Materials and Methods

The commercial 4H-SiC MOSFET with a standard TO-247 package featuring a breakdown voltage of 1.2 kV and on-state resistance ($R_{DS,ON}$) of 80 mΩ was chosen for the DUT. A MicReD Industrial Power Tester 1500 A, Siemens imposed power and monitored the DUT's test parameters. For precise experiments, the forward voltage drop of the body diode (V_{on}) serves as a temperature-sensitive electrical parameter (TSEP) [20]. Figure 2a shows the equivalent circuit, and Figure 2b shows the waveforms of the PCT parameters and the output junction temperature cycles. Table 1 lists the test conditions. The test equipment automatically maintains a constant temperature swing (ΔT_j) under a fixed on-time (t_{on}) and off-time (t_{off}) by adjusting the heating current (I_H). A sample is considered failed when V_{on} increases by 120%.



(**a**) (**b**)

Figure 2. Power cycling test conditions: (**a**) equivalent circuit; (**b**) waveforms for power cycling test parameters and output junction temperature swing.

Table 1. Power cycling test setup.

ΔT_j (°C)	T_{jmax} (°C)	t_{on} (s)	t_{off} (s)	$V_{GS,on}$ (V)	$V_{GS,off}$ (V)	I_S (mA)	I_H (A)	V_{on} (%)
110	170	2	4	18	−5	−80	22.3	120%

To determine the failure mode at the 4H-SiC/SiO_2 interface, the DUTs were decapsulated and observed, especially for the stressed cells in the active region, using GEMINI500, an ultrahigh analytical field-emission scanning electron microscope (FE-SEM), and a focused ion beam (FIB). Titan Cubed G2 60-300KV(FEI), High-resolution transmission electron microscopy (HR-TEM), and electron energy loss spectroscopy (EELS) were used to inspect the 4H-SiC/SiO_2 interface of the substantially deteriorated cells in detail. The use of HR-TEM and EELS in observing the 4H-SiC/SiO_2 interface brings about several key advantages in the context of this research. HR-TEM provides the visualization of nanoscale features with precision. This capability is crucial when studying the intricate details of the 4H-SiC/SiO_2 transition layer, as it allows researchers to discern subtle structural changes induced by PCT. EELS, on the other hand, offers valuable insights into the elemental composition of the interface. By mapping the percentages of Si, C, and O along the transition layer, EELS helps quantify compositional variations that might be indicative of degradation or damage. Moreover, the combination of HR-TEM and EELS enables a comprehensive examination of both structural and chemical aspects, providing a holistic understanding of the 4H-SiC/SiO_2 interface's response to PCT-induced stress. This approach enhances the reliability and accuracy of the observations, making HR-TEM and EELS indispensable tools for unraveling the complexities of the SiC/SiO_2 interface and its role in the performance of power devices.

The transfer curves at a fixed, small drain voltage (V_d = 50 mV) were measured using a Keysight B1506a (Santa Rosa, CA, USA),power device curve tracer, before and after the PCT. Figure 3 shows the transfer characteristics, I_d vs. V_g, of the 4H-SiC n-MOSFETs (VD-MOSFETs). The linear extrapolation method employed for extracting the threshold voltage (V_t) involves plotting the device's transfer characteristics, specifically the drain current (I_d) against gate voltage (V_g) at a fixed, small drain voltage. By identifying the linear region in which the drain current increases linearly with the gate voltage, a straight line is extrapolated to intersect with the x-axis, determining the V_t accurately. The maximum transconductance point is chosen for heightened accuracy. The technique is crucial for assessing the impact of power cycling tests on the threshold voltage of 4H-SiC power devices, ensuring a reliable measure of the device's conduction initiation point. Figure 4a plots the total resistance of the transfer graph, R_{tot}, vs. the $(V_g\text{-}V_t)^{-1}$ value. The calculated resistance values from the transfer graph are plotted on the y-axis, while the corresponding $(V_g\text{-}V_t)^{-1}$ values are plotted on the x-axis. This results in the R_{tot} vs. $(V_g\text{-}V_t)^{-1}$ graph, providing a visual representation of the relationship between total resistance and the inverse of the gate overdrive voltage. This graph allows for a detailed analysis of how different resistance components contribute to the overall behavior of the device under varying gate conditions. At large $(V_g\text{-}V_t)^{-1}$ values, where V_g closes to V_t, the channel resistance dominates the total drain-source current [21–23]. The intersection with the ordinate y-axis in Figure 4b yields the residual resistance R_s [21–23].

All series resistances, except R_{CH}, in Equation (1) comprise R_s. There are other resistances. The resistance of the source wire to the source metal contact, $R_{Wirebond}$, and the resistance of the solder, R_{Solder}, originate from the package to an active chip connection. We assumed that $R_{Wirebond}$ and R_{Solder} were practical reasons for the increase in R_s after PCT because regions in the n-drift are seldom weakened by ΔT_j. By comparing the changed parameters in the R_{tot} vs. $(V_g\text{-}V_t)^{-1}$ graph, we can determine which regions, such as R_s or R_{ch}, become more resistive.

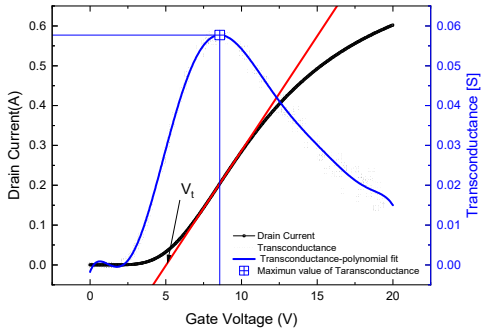
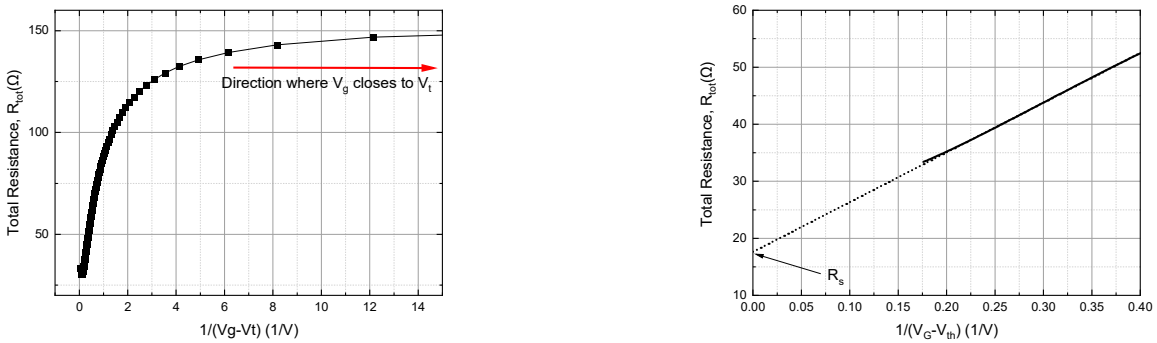


Figure 3. Transfer curve and transconductance of commercial high-voltage vertically double implanted 4H-SiC n-MOSFETs (VD-MOSFETs). The linear extrapolation method is applied to extract V_t.



(**a**) (**b**)

Figure 4. R_{tot} vs. $(V_g\text{-}V_t)^{-1}$ graph when (**a**) $V_G \rightarrow V_{TH}$, R_{CH} is the dominant component of R_{tot} and (**b**) $\frac{1}{V_G - V_{TH}} \rightarrow 0$. The y-intercept represents the residual resistance R_S.

3. Results and Discussion

When the on-state voltage drop (V_{on}) reached the predefined test stop condition mentioned in Table 1, the sample experiments were stopped. Figure 5 shows the value of V_{on} measured at each cycle, and the thermal resistance (R_{th}) was checked every 500th cycle. It was observed that V_{on} underwent dynamic variations after the 2300th cycle.

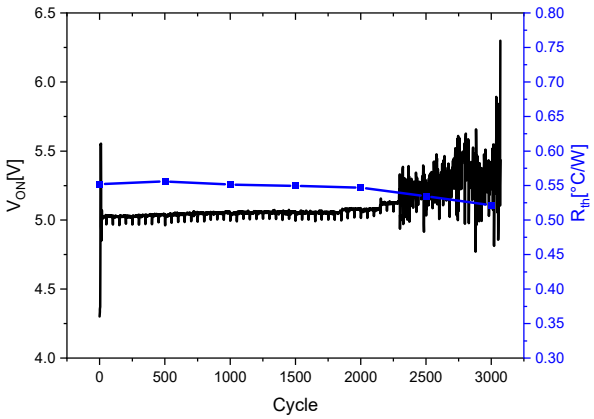
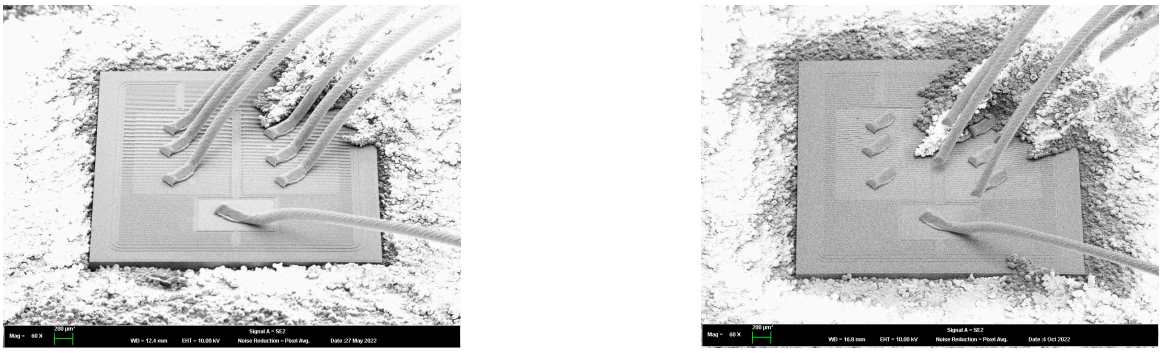


Figure 5. On-state voltage drop at every cycle and thermal resistance at every 500th power cycle.

3.1. Stress Symptoms of the Surroundings

The primary reason for the increase in V_{on} in the TO-247-3L discrete device is usually defects in/on the wire bonds [13,24]. Although solder fatigue is another potential problem, neither a 5% increase nor a decrease in R_{th} was observed in this experiment. An increase in thermal resistance in the thermal path is occasionally attributed to solder fatigue [13,25].

Therefore, it is hard to expect solder-void-related critical degradation. Figure 6 shows the partially decapsulated DUT images of the intrinsic and power-cycled samples. After power cycling, cracks were observed in the wire-bond heels, which led to separation. The resistance of the wire increases when the bond between the wire and the active device is weak. Overall, V_{on} varied aggressively with wire bond deterioration.



(**a**) (**b**)

Figure 6. Partially decapsulated DUT images of (**a**) an intrinsic device and (**b**) a power-cycled device, whose V_{on} was increased to 120%.

3.2. Pattern of Degradation at a 4H-SiC/SiO$_2$ Interface

This research investigates the impact of power cycling tests (PCT) on the 4H-SiC/SiO_2 interface in commercial 1.2 kV 4H-SiC VD-MOSFETs. Employing advanced microscopy and spectroscopy techniques, this study reveals changes in the length of the 4H-SiC/SiO_2 transition layer, which is critical for device reliability. The analysis of electrical parameters, including threshold voltage shifts and resistance variations, will be addressed in this chapter to demonstrate potential damage at the SiC/SiO_2 interface post-PCT. The cracks and delamination on the inter-layer dielectric (ILD) were sporadically detected in the active region of each sample. Figure 7 shows cells from the DUT where the ILD was slightly delaminated. The HRTEM image in Figure 8 was obtained from the cross-section along the red and green dotted line in Figure 7.

To monitor the degradation at the 4H-SiC/SiO_2 interface, Figure 8a,b shows the comparison of the HR-TEM images of the intrinsic and power-cycled DUTs. The DUT undergoing PCT (or power-cycled DUT) exhibited a different lattice structure, especially near the 4H-SiC/SiO_2 interface, as indicated by the red bidirectional arrows. To quantitatively analyze the transition layer, EELS was conducted along the green line, as shown in Figure 9a, at the 4H-SiC/SiO_2 interface in the junction field-effect transistor (JFET) region. The composition percentages of Si, C, and O were collected at 48 different positions, from the gate dielectric SiO_2 to the semiconductor 4H-SiC. Figure 9b illustrates the percentage composition changes in the Si L-edge, O K-edge, and C K-edge collected near the 4H-SiC/SiO_2 interface for each sample. The percentage composition of each element reached saturation at both ends, that is, SiO_2 and SiC, except in the transition layer. The slope of each element in the transition layer also varied during PCT. The 4H-SiC/SiO_2 transition layer of the power-cycled DUT was longer than that of the intrinsic sample. It is essential for maintaining a sharp and well-defined interface between the SiC and SiO_2 layers to ensure proper device operation. Electrically, the transition layer influences charge carrier mobility, interface trap density, and overall device performance. A high-quality transition layer helps in reducing defects, interface traps, and charge carrier scattering, which are essential for maintaining consistent device operation over time [11,26,27].

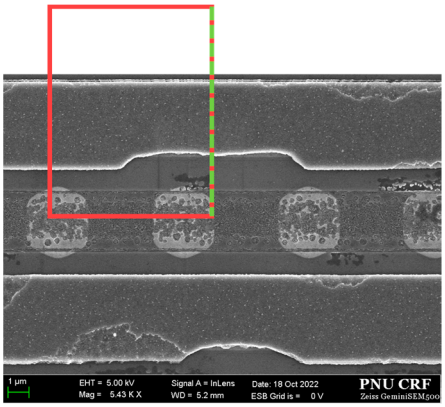
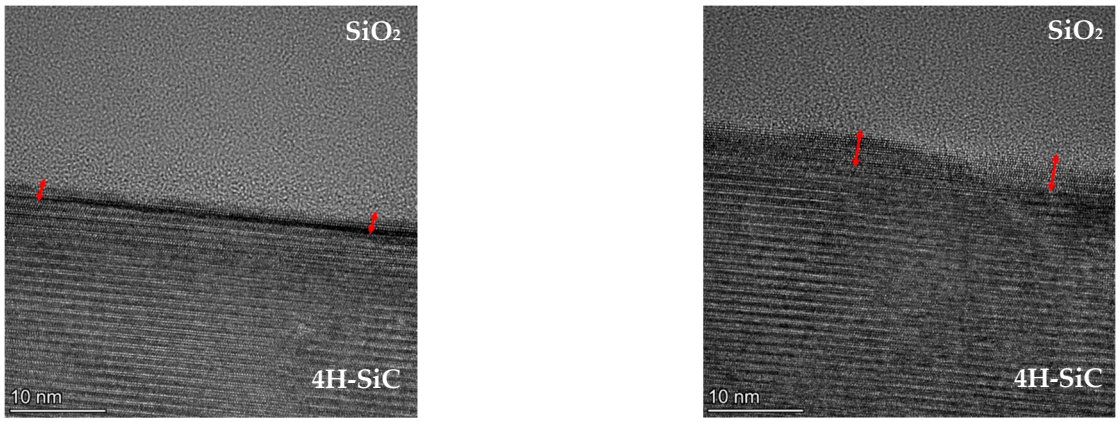
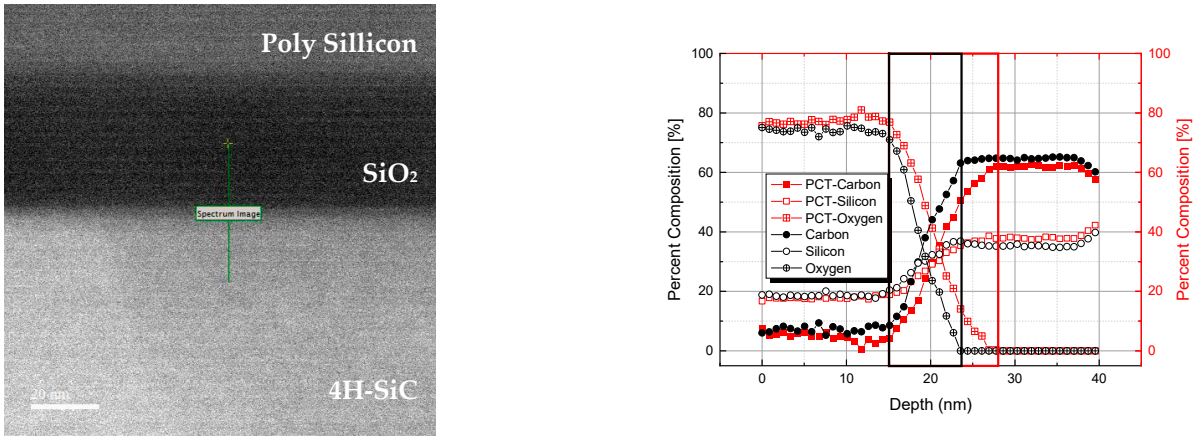


Figure 7. FE-SEM image of the deteriorated cells in DUTs HR-TEM was measured along a red and green dotted line.



(**a**) (**b**)

Figure 8. HR-TEM images of (**a**) an intrinsic device and (**b**) a power-cycled device, whose V_{on} was increased to 120%.

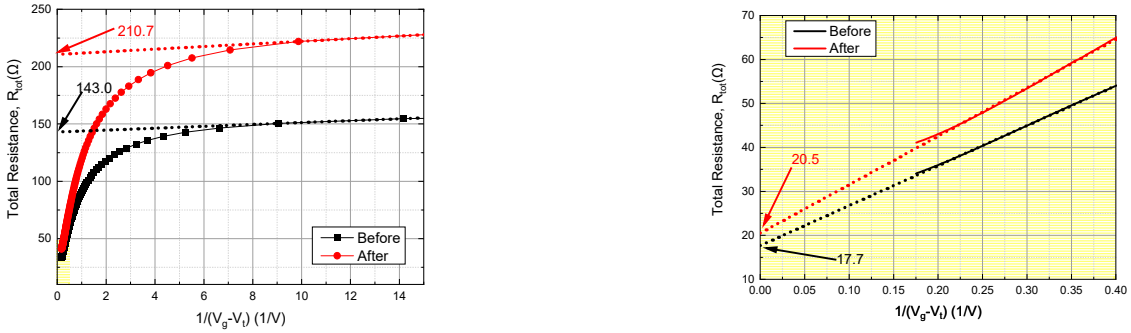


(**a**) (**b**)

Figure 9. EELS results: (**a**) SEM image for EELS percent composition mapping line (green); (**b**) EELS percent composition vs. depth.

When the length of the 4H-SiC/SiO_2 transition layer was short, the surface roughness between the 4H-SiC semiconductor and SiO_2 gate dielectric was low [28,29]. As the surface roughness increased, the mobility decreased, increasing the channel resistance [30,31]. To compare the results from the HR-TEM and EELS regarding the channel resistance, an R_{tot} vs. $(V_g\text{-}V_t)^{-1}$ graph was plotted in Figure 10. Figure 10 shows the change in the overall

resistance R_{tot} calculated using a transfer graph (V_d = 50 mV). In this graph, as the x-axis increases, V_g approaches V_t, and channel resistance R_{CH} dominates R_{tot} [21]. It can be observed that the resistance of the channel increased significantly after PCT. The resistance extrapolated from the $V_g \approx V_t$ increased by 47.3%, while $V_g \gg V_t$, $(V_g\text{-}V_t)^{-1} \rightarrow 0$, increased by 16.5% after power cycling. In the $V_g \approx V_t$ range, a relatively low drain current flows, and it is less affected by the gate-to-source electrode feedback (G-S feedback) owing to the wire bond. The change in resistance in the $V_g \approx V_t$ range was more dramatic than in the case of $V_g \gg V_t$. These results indicate that R_{CH} has increased. This corresponds to the findings of prior research that the channel resistance is very high when the transition layer is distinguishable.



(**a**) (**b**)

Figure 10. R_{tot} vs. $(V_g\text{-}V_t)^{-1}$ graph. The y-intercept for each graph indicates the total resistance when (**a**) $V_g \approx V_t$ and (**b**) $V_g \gg V_t$. The yellow region in (**a**) is magnified into (**b**).

Fiorenza et al. successfully showed that an interface with a low near-interface trap and oxide trap density has a shorter length than the 4H-SiC/SiO_2 transition layer [32]. Zhang et al. conducted theoretical research on the relationship between near-interface oxide traps and Si interstitials in substoichiometric SiO_x in the transition layer and found the presence of dangling bonds, including SiC_yO_x and SiO_xN_y compounds [33]. Likewise, complex flaws that induce a negative V_t shift exist within the 4H-SiC/SiO_2 transition layer. Figure 11 shows the V_t values extracted from the measured transfer and transconductance graphs. The threshold voltage exhibited a negative shift. If the defects in the wire bond had degraded the G-S feedback, the threshold voltage would have increased. It is reasonable to assume that as the transition area with various defects expands, the influence of traps that lead to a negative V_t shift becomes more significant.

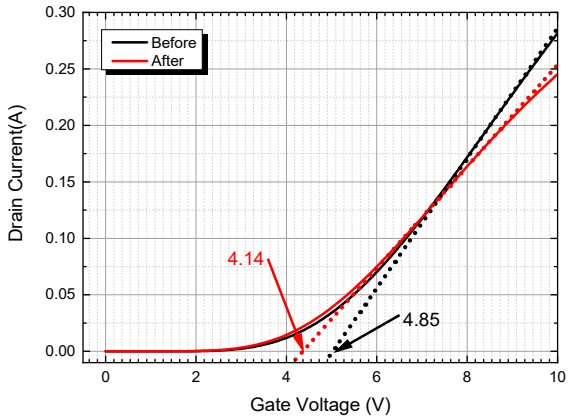


Figure 11. The transfer curves at a fixed, small drain voltage (Vd = 50 mV). The x-intercepts is the threshold voltage before/after power cycling test.

The negative threshold voltage (Vt) shift observed in the 4H-SiC MOSFETs after PCT poses significant concerns for device performance. A negative V_t shift typically indicates a degradation in the transistor's characteristics, impacting its switching behavior and overall functionality. This shift can lead to increased power losses, reduced efficiency, and compromised reliability [34]. Moreover, negative Vt shifts are often associated with the presence of defects or traps in the semiconductor material, indicating potential structural and electrical damage. Addressing and mitigating this adverse effect is crucial for maintaining the long-term stability and functionality of 4H-SiC power devices in practical applications.

4. Conclusions

This study shows the impact of power cycling tests (PCTs) on the 4H-SiC/SiO_2 interface in commercial 1.2 kV 4H-SiC VD-MOSFETs, which is crucial for evaluating power device reliability. Traditionally, PCTs focus on package-related issues, but this research emphasizes the underestimated influence of power cycling-induced stress on the 4H-SiC/SiO_2 interface. The internal resistance components in 4H-SiC VD-MOSFETs significantly differ from silicon, with the 4H-SiC/SiO_2 interface accounting for a substantial portion of the total resistance (R_{tot}).

Power cycling tests involve repeated gate electrode switching with high heating currents, causing wearout in solder voids and wire bonds. Power loss in each resistor in the current path is considered the source of ejected heat. Regions exposed to electrical stress or high heating currents, closely related to resistance, are crucial in 4H-SiC power MOSFETs. Experimental results showed dynamic variations in the on-state voltage drop (V_{on}) attributed to defects in wire bonds. Thorough decapsulation and observation of devices revealed a correlation between V_{on} variations and wire bond deterioration. Inspection of the 4H-SiC/SiO_2 interface using HR-TEM and EELS demonstrated changes in lattice structure and composition percentages after power cycling.

A critical aspect involved plotting R_{tot} vs. $(V_g\text{-}V_t)^{-1}$ graphs, indicating significant resistance increases after power cycling, particularly in the $V_g \approx V_t$ range. Findings emphasize the intricate relationship between power cycling, interface degradation, and changes in electrical parameters. In conclusion, this research contributes valuable insights into the effects of power cycling on 4H-SiC power devices, emphasizing the need for a deeper understanding of interface dynamics for enhanced device reliability and performance.

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Conflicts of Interest: Author MiJin Kim was employed by the company Samsung Electronics. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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