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Graphical Design Approach for UWB Stacked CG LNA Using Inversion Coefficient

Ahmed Hamed [1,*] and Ayman Ismail [2,*]

[1] MEMS-Vision LLC, Cairo 11375, Egypt
[2] Integrated Circuits Laboratory, ECE Department, Faculty of Engineering, Ain Shams University, Cairo 11566, Egypt
* Correspondence: ahmed.hamed@mems-vision.com (A.H.); ayman.hassan@eng.asu.edu.eg (A.I.); Tel.: +20-1158710638

Abstract: The design of ultra-wide-band (UWB) low-noise amplifiers (LNAs) entails a large number of design challenges and tradeoffs, which include sustaining good input matching over a wide bandwidth along with finding a proper compromise between various LNA performance metrics, such as gain, bandwidth, noise figure, power, and linearity. This paper presents a design approach for UWB LNAs based on the inversion coefficient (IC). The proposed approach is a graphical design approach where the proper operating point is chosen based on predefined constraints. A complete systematic solution is presented for the problem of UWB input matching with a high degree of analytical accuracy. The design approach is illustrated through the design of two UWB stacked common-gate LNAs in 65 nm technology. The post-layout simulation results show very good agreement with analytical expectations. The first LNA achieves an S_{11} better than −8.2 dB over a 27.6 GHz frequency range, a gain of 12.4 dB over a 16.5 GHz bandwidth, a minimum noise-figure, NF, of 4.5 dB, and an IIP_3 of −5.2 dBm while consuming only 530 µW. The second LNA achieves an S_{11} better than −15 dB over an 8.8 GHz frequency range, a gain of 12.5 dB over a 6.8 GHz bandwidth, a minimum NF of 4 dB, and an IIP_3 of −4.3 dBm while consuming only 550 µW.

Keywords: design methodology; inversion coefficient; LNA; low power; UWB

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1. Introduction

UWB communication has been a growing field of research since the Federal Communications Commission (FCC) changed its regulations to allow the unlicensed usage of UWB signals in 2002. UWB signals are defined by the FCC as those having −10 dB bandwidths greater than 500 MHz with a transmitted power mask limited to −41.3 dBm/MHz within the 3.1–10.6 GHz band [1]. The most popular implementation of UWB systems is the impulse radio technique (IR-UWB), where each symbol is represented by a short pulse of signal followed by a long time off with no power transmitted, thus saving power. This is the key difference between IR-UWB and NB communications, where for the latter, a modulated RF carrier is continuously transmitted throughout the whole symbol period [2]. The inherent power-saving property of the IR-UWB transceivers, along with their high data rate capability, make them an attractive choice for high-accuracy ultra-low-power wireless body area networks (WBANs) powered by a tiny battery or even an energy harvesting system [3]. Moreover, IR-UWB transceivers have become a strong candidate for indoor localization and ranging applications due to the utilization of very short data pulses. High-bandwidth, very short pulses are used to accurately estimate time of flight (TOF) and time of arrival (TOA) metrics, thus achieving high-precision ranging with minimal distance errors [4]. In addition, UWB technology has found its path towards other various applications, such as smart car keys, RFIDs, personal area networks (PANs), and even modern implementations of synthetic aperture radars (SARs).

One of the most vital building blocks of UWB systems is the LNA. The design of UWB LNAs entails a large number of challenges and trade-offs, such as maintaining good input matching over the wide amplifier bandwidth and achieving a high gain, low noise, and high IIP_3 while maintaining a compact area and low power dissipation. Achieving these seemingly contradictory specifications requires a lot of design iterations, which if not properly managed, may lead to suboptimal designs that limit the performance of the whole system. Thus, a systematic design approach is recommended in order to maximize the LNA figure of merit, FoM, and to understand the potential and limitations of different topologies and technology nodes while minimizing design time and effort. There are a lot of research efforts aiming to standardize the design process and offering different design methodologies. The work in [5] is an LNA design methodology where g_m/I_D is used as a benchmark for the transistor operating point. Device parameters are extracted by simulation in terms of g_m/I_D and represented as a table dataset or a lookup table (LUT). The specifications of the target circuit topology are then represented analytically in terms of the small-signal device parameters, where the optimum g_m/I_D is chosen to achieve pre-defined target specifications and optimize the circuit performance. The main drawback of this approach is that it requires the user to perform a full characterization of the MOSFET under all size and bias conditions to build LUTs for each device parameter. Another LUT-based methodology is found in [6], where the gate-source voltage is chosen to maximize linearity while the transistors' widths are chosen to maximize other LNA specifications. This method also requires full MOSFET characterization prior to the design phase. The aforementioned limitations imply the need for a simple transistor device model that clearly describes transistor physics and accurately describes transistor parameters in all regions of interest (namely, weak inversion, moderate inversion, and strong inversion), and this is what the charge-based EKV model does [7]. The simplified EKV model in [7] represents the transistor operating region by the inversion coefficient term, IC, which is a normalization of the drain current I_D to a technology parameter called the specific current I_{spec}. The IC divides the transistor regions of operation depending on the level of channel inversion as follows:

$$\begin{aligned} IC &< 0.1 : \text{weak inversion (WI)} \\ 0.1 < IC &< 10 : \text{moderate inversion (MI)} \\ IC &> 10 : \text{strong inversion (SI)} \end{aligned}$$

It is worth noting that having a design approach that considers weak inversion and moderate inversion in addition to strong inversion (rather than the square law that considers strong inversion only) is crucial, especially for designs conducted in modern advanced technologies, where technologies' f_t have risen considerably but the low-power standards, such as the Internet of Things' (IoT) standards, still define relatively low carrier frequencies. In such cases, operating at weak or moderate inversions leads to low-power operation and can still satisfy the operating frequency.

The IC is adopted in [8,9] as the basis of their design methodology. The design methodology adopted in [8] starts by characterizing the MOSFET in the target technology to extract the technology parameters forming the device parameters' expressions. This step is performed once for each technology. After that, a circuit analysis is performed to derive the design equations for the target topology. This step is unique and has to be performed for each circuit topology. The final step is to write a MATLAB script that optimizes the circuit equations based on a defined FoM to find the optimum biasing and sizing point. One main missed part in this methodology is that the choice of transistor lengths is made arbitrarily without specific reasoning behind it and thus is not optimized. A two-step approach is adopted in [9], namely active and passive, where the active step is used to meet the performance specifications and the passive step is used to meet the required matching. In the active step, the gain and the NF metrics are set as an initial condition, and then an optimum transistor bias point, IC_{opt}, at a fixed transistor width and length is found based

on maximizing a pre-defined FoM. After that, a loop iterates on the sizing variables W and L until all performance specifications are achieved. In the passive step, input matching specifications are calculated in terms of the device passives, parasitic capacitances, and resistances. Then, a loop iterates on the circuit passives until the required matching is achieved. The automation script then tests again against performance specifications, and if they are met, the design is complete; if not, the whole process is repeated again. During the device parameter extraction step, the gate-source capacitance is assumed to be independent of the IC, which is not accurate due to the intrinsic part of it. This leads to inaccurate results, especially for matching metrics (passive step). The methodology in [10] adopts the Advanced Compact MOSFET model (ACM) for optimizing resistive-feedback LNAs and describes all the circuit equations in terms of seven transistor parameters. However, the assumption of too many arbitrarily chosen constraints using only one variable (IIP3) for optimization and suboptimal matching procedures necessitates a design loop of many iterations while reaching suboptimal design points and very small matching bandwidth.

The remaining part of this paper is organized as follows. Section 2 gives a glimpse into the design approach used. Section 3 describes the EKV charge-based transistor model used to describe transistor parameters. Section 4 presents the analysis of the LNA topology used in this paper, which is the stacked common-gate LNA. Section 5 describes the design flow and discusses the results. And finally, the work is concluded in Section 6.

2. Design Methodology

A UWB LNA design approach based on IC and LNA FoM is presented in this paper. As shown in Figure 1, the design approach consists of four main steps. First, all device parameters of interest are derived in terms of IC, W, and L, where W and L are the transistor channel width and length, respectively. The second step is to represent different performance metrics in terms of device parameters and hence in terms of IC, W, and L. The third step is to define the design constraints imposed on the design and define the FoM to be maximized in terms of IC, W, and L to generate the design graphs. The final step is to choose the proper bias point and sizing, IC_o, W_o, and L_o, using the design graphs. So, basically, the optimization process is conducted graphically by selecting the most appropriate IC that satisfies all the design constraints and maximizes FoM.

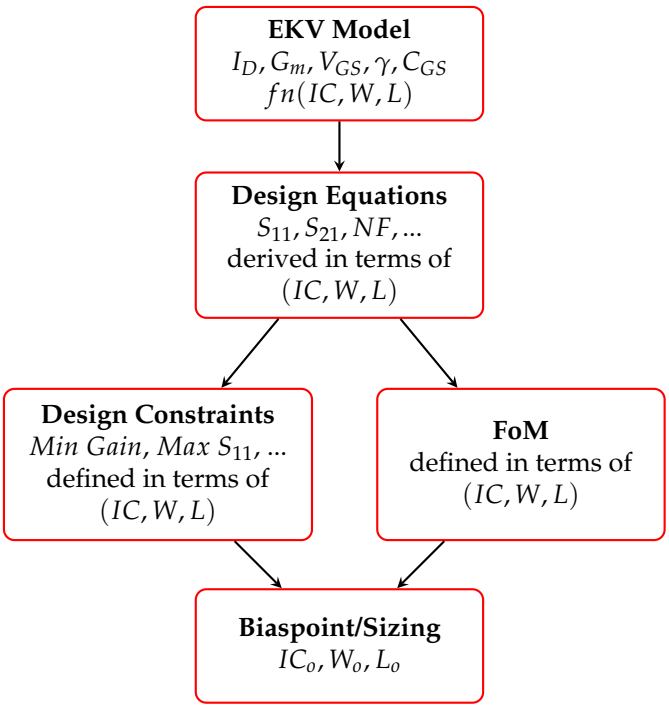

Figure 1. Design methodology.

It is worth noting that unlike the methodologies in [5,6], the adopted approach offers a complete analytical solution where every device parameter as well as the transistor biasing point and sizing can be predicted analytically. Moreover, the design steps do not require lengthy iterations and trials, like in the cases of [10] or [11]. The choice of the transistor length is made to maximize the input matching bandwidth, as discussed in Section 5, giving the proposed approach an edge on the one in [8]. A multi-variable *FoM* covering all the important circuit specifications is used for optimization rather than the use of only one variable, as in the case of [10]. Finally, both the intrinsic and extrinsic parts of the gate-source capacitance are modeled as outlined in Section 3, thus more accurate results for input matching are achieved in contrast to the methodology in [9].

3. Charge-Based Transistor Model

The EKV charge-based model was first introduced by C. Enz, F. Krummenacher and E.A. Vittoz [8]. The transistor operating point is described in terms of the inversion coefficient,

$$IC = \frac{I_D}{I_{spec}}, \tag{1}$$

$$I_{spec} = \frac{W}{L} I_{spec_\square}, \tag{2}$$

$$I_{spec_\square} = 2n\mu_n C_{ox} U_T^2, \tag{3}$$

where I_D is the transistor drain current, I_{spec} is the transistor-specific current, $I_{spec_\square}$ is the specific current per square, W is the transistor gate width, L is the transistor gate length, n is the nonideality factor, μ_n is the low-field mobility, C_{ox} is the oxide capacitance per unit area, and $U_T = {}^{KT}/_{q}$ is the thermal voltage.

The inversion coefficient parameter can be related to the normalized channel charge using [12]:

$$IC \equiv i_{dsat} = q_s^2 + q_s - q_{dsat}^2 - q_{dsat}, \tag{4}$$

$$q_{dsat} = \frac{\lambda_c i_{dsat}}{2}, \tag{5}$$

where i_{dsat} is the normalized drain saturation current, q_s is the normalized source charge, q_{dsat} is the normalized drain saturation charge, and $\lambda_c = {}^{L_{sat}}/_{L}$ is the velocity saturation parameter, which represents the percentage of the channel length in which the carrier's velocity is saturated. From (4) and (5), q_s can be represented as [7]

$$q_s = \frac{\sqrt{(\lambda_c IC + 1)^2 + 4IC} - 1}{2}, \tag{6}$$

The normalized gate transconductance, g_m, is expressed as [8]

$$g_m = \frac{G_m}{G_{spec}} = \frac{1}{n} \frac{2q_s}{\lambda_c(\lambda_c IC + 1) + 2}, \tag{7}$$

where G_m is the transistor transconductance and $G_{spec} = {}^{I_{spec}}/_{U_T}$ is the transconductance normalization factor.

Considering the gate-source voltage V_{GS}, an analytical expression in terms of IC can be deduced from the general solution of the compact charge-based model found in [7]:

$$2q_i + ln(q_i) = v_p - v, \tag{8}$$

where q_i, v, and v_p are the normalized channel charge, normalized channel voltage, and normalized pinch-off voltage, respectively. At the source end of the channel, this becomes [7]

$$2q_s + ln(q_s) = v_p - v_s. \tag{9}$$

But, from [7],

$$v_p = \frac{V_p}{U_T} = \frac{V_G - V_{T0}}{nU_T}, \tag{10}$$

$$v_s = \frac{V_s}{U_T}, \tag{11}$$

where V_G and V_{T0} are the transistor gate voltage and threshold voltage in equilibrium, respectively, where the latter is a technology parameter. Substituting (10) and (11) in (9)

$$\frac{V_G - nV_s - V_{T0}}{nU_T} = 2q_s + ln(q_s). \tag{12}$$

Assuming zero source voltage ($V_s = 0$),

$$V_{GS} = V_{T0} + nU_T(2q_s + ln(q_s)). \tag{13}$$

For a non-zero bulk-source voltage ($V_{BS} > 0$), an additional term is added to (13) to model the body effect.

The gate-source capacitance per unit area, C_{GS0} is expressed in terms of IC using the following relations [13]:

$$C_{GS0} = X_1 + X_2 C_{int0}, \tag{14}$$

$$C_{int0} = \frac{n - (1 + x)/3}{n}, \tag{15}$$

$$x = \frac{(\sqrt{IC + 0.25} + 0.5) + 1}{(\sqrt{IC + 0.25} + 0.5)^2}, \tag{16}$$

where X_1 and X_2 are technology-dependent constants.

The gate-drain capacitance, C_{GD} is expressed as

$$C_{GD} = WC_{GD0}, \tag{17}$$

where W is the transistor width and C_{GD0} is a technology-dependent parameter.

The thermal excess noise factor γ_n is also a function of IC, where

$$\gamma_n = \gamma_w + \alpha_n IC, \tag{18}$$

where γ_w and α_n are the weak inversion values of γ_n and the inversion level dependency factor, respectively. Both are technology-dependent parameters.

The aforementioned device parameters (g_m, V_{GS}, C_{GS}, and γ_n) are plotted in Figure 2 against IC, with g_m and V_{GS} shown for different λ_c values for 65 nm technology. According to [8], velocity saturation has a minor effect at lengths greater than or equal to 200 nm and can be neglected even for shorter lengths without much effect on the results' accuracy, knowing that at lengths as small as 65 nm, λ_c is about 0.3. The target application in this paper is the UWB LNA operating at frequencies of up to 10.6 GHz, while this technology's f_t is 200 GHz; thus, there is no need to utilize small transistor lengths and compromise the transistor gain and drain-source isolation. Also, as will be shown later, the moderate inversion region always offers the best compromise for the transistor bias point that maximizes the circuit FoM while achieving the design constraints. For all these reasons, λ_c will be neglected in all the forthcoming analyses.

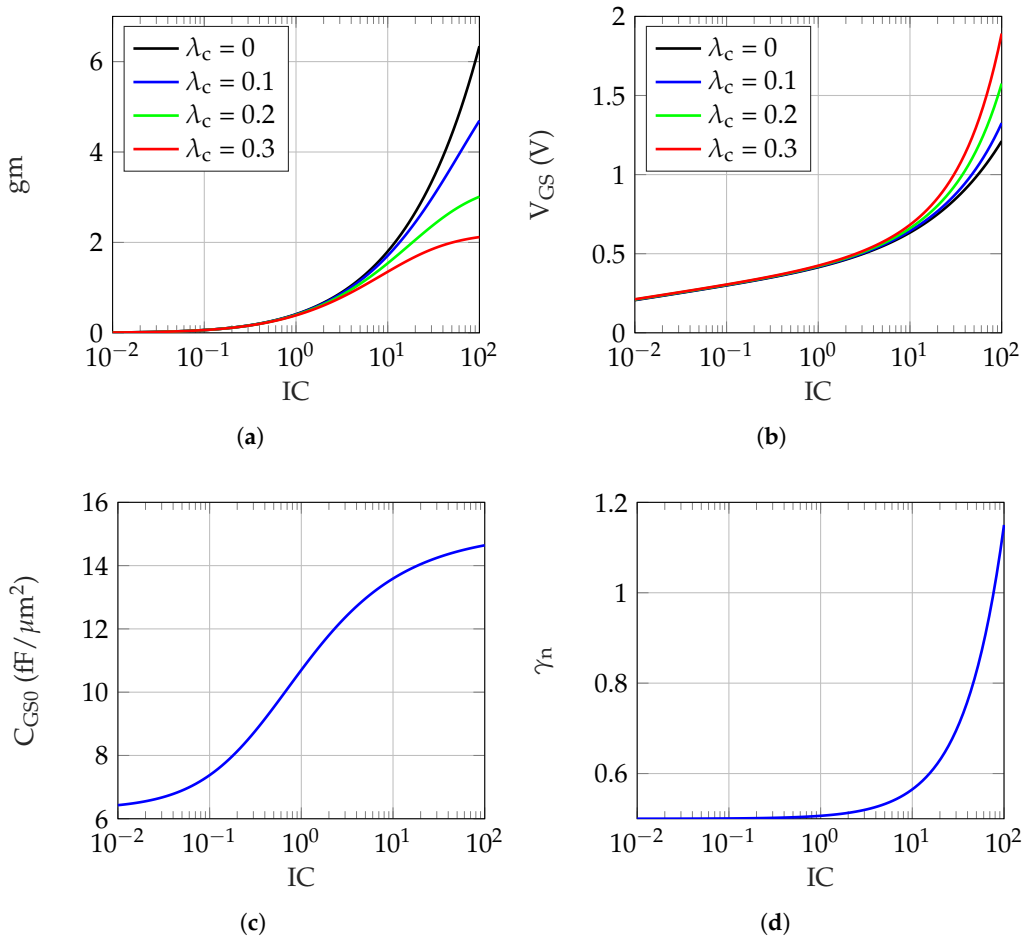

Figure 2. (**a**) g_m at different λ_c values, (**b**) V_{GS} at different λ_c values, (**c**) C_{GS0}, and (**d**) γ_n.

The accurate extraction of the model parameters is a very important step for accurate analytical predictions. This task has to be performed once for every technology node in order to be able to use the model. There has already been extensive research conducted in this domain, as can be found in [14], where the bottom line in the extraction process is performing curve-fitting to simulation data. This was performed in this work for the TSMC 65 nm process using DC and noise characterization for the NMOS and PMOS transistors by fitting the simulation data.

Table 1 summarizes the different model parameters for NMOS and PMOS transistors in the adopted technology. Simulation data for G_m, V_{GS}, C_{GS}, C_{GD}, and the output noise current are used for the proper extraction of the addressed model parameters.

Table 1. EKV model parameters for TSMC 65 nm process.

Parameter Name	Value for NMOS	Value for PMOS
$I_{spec_\square}$	1.5 µA	0.5 µA
n	1.5	1.5
V_{T0}	380 mV	390 mV
X_1	−0.3 m	−0.3 m
X_2	19.8 m	19.8 m
C_{GD0}	0.4 fF/µm	0.4 fF/µm
γ_w	0.5	0.5
α_n	10 m	3 m

4. Analysis of the Stacked CG Topology

The stacked common-gate amplifier topology (Figure 3) is adopted for the UWB LNA of this work. In the stacked common-gate amplifier, the supply current is reused such that both the NMOS and the PMOS transistors act as active devices to boost the amplifier's total transconductance ($G_{m_{tot}}$). The main advantage of the stacked common-gate over the standard common-gate topology is that the former uses the available headroom more efficiently. As demonstrated in Figure 4, the stacked common-gate actively uses the headroom that is normally used on the biasing device in the standard common-gate.

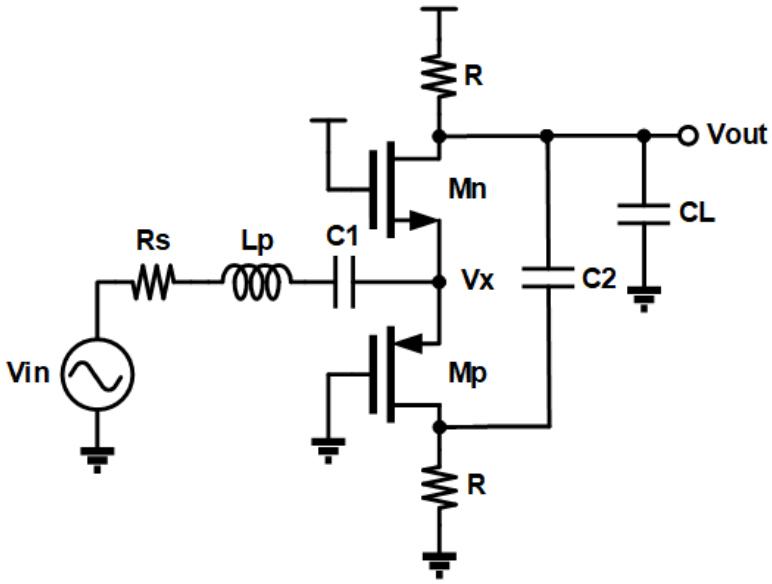

Figure 3. The stacked common-gate topology.

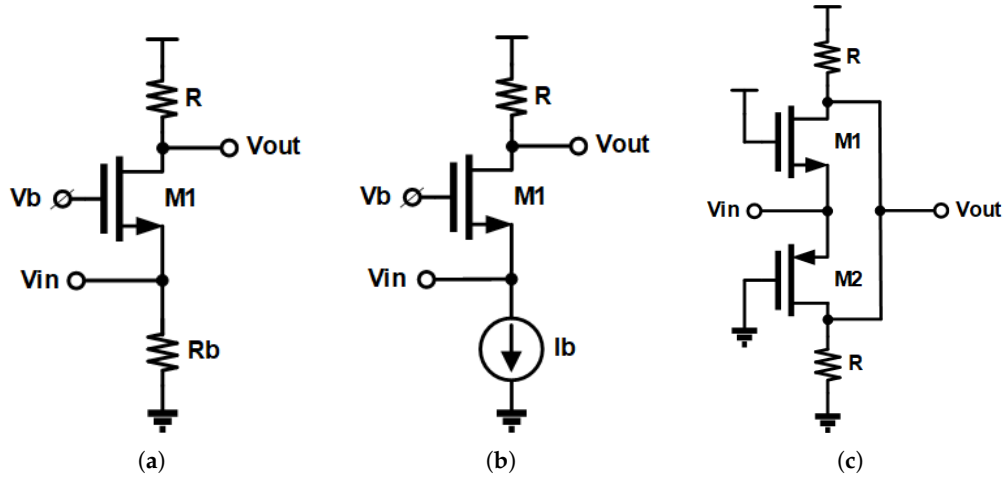

Figure 4. Common-gate amplifier with (**a**) biasing resistor, (**b**) biasing current source, and (**c**) current reuse.

4.1. PMOS-to-NMOS Sizing Ratio

The total transconductance of the amplifier equals the summation of NMOS and PMOS transconductances, G_{m_n} and G_{m_p}, respectively; however, for the same current, there are endless combinations of G_{m_n} and G_{m_p} that are determined by the PMOS to NMOS sizing ratio $\frac{(W/L)_p}{(W/L)_n}$, which is equal to W_p/W_n, assuming equal transistor lengths. Finding the sizing ratio (W_p/W_n) that maximizes $G_{m_{tot}}$ is crucial for obtaining a better design. Neglecting

the λ_c-parameter, the overdrive voltages and transconductances of NMOS and PMOS transistors can be written as (ignoring body effect)

$$V_{od_{n,p}} = nU_T[2q_{s_{n,p}} + ln(q_{s_{n,p}})], \tag{19a}$$

$$G_{m_{n,p}} = \frac{I_{spec_{n,p}} q_{s_{n,p}}}{nU_T}, \tag{19b}$$

where

$$q_{s_{n,p}} = \frac{\sqrt{4IC_{n,p}+1}-1}{2}, \tag{20}$$

where V_{od}, G_m, and q_s are the overdrive voltage, the transconductance, and the normalized channel charge at the source end of the transistor, respectively. Assuming that $V_{od_n} + V_{od_p} = V$, where $V = V_{DD} - (V_{T0_n} + V_{T0_p})$, where the body effect is neglected for simplicity and without much effect on the results' accuracy, this can be restated as follows:

$$V_{od_n} + V_{od_p} = XV + (1-X)V = V, \tag{21}$$

where X is the ratio of V_{od_n} to the voltage headroom V and its value ranges from 0 to 1. Knowing that

$$G_{m_{tot}} = G_{m_n} + G_{m_p}, \tag{22}$$

the set of equations from Equation (19) through to Equation (22) have to be solved analytically. However, no closed-form expression can be obtained because these equations cannot be solved analytically, thus an approximation has to be made in order to find an analytical solution.

4.1.1. Strong Inversion Approximation

In strong inversion, $IC \geq 10$, thus $q_{s_{n,p}} \approx \sqrt{IC_{n,p}}$, and as a result, Equation (19) can be approximated to

$$V_{od_{n,p}} = 2nU_T\sqrt{IC_{n,p}}, \tag{23a}$$

$$G_{m_{n,p}} = \frac{I_{spec_{n,p}}\sqrt{IC_{n,p}}}{nU_T}. \tag{23b}$$

From (23a) and the definition of X,

$$\frac{V_{od_n}}{V_{od_p}} = \sqrt{\frac{IC_n}{IC_p}} = \left(\frac{X}{1-X}\right). \tag{24}$$

But from (1) and due to current reuse,

$$\frac{IC_n}{IC_p} = \frac{I_{spec_p}}{I_{spec_n}} = \left(\frac{X}{1-X}\right)^2, \tag{25}$$

This can be rewritten as follows:

$$IC_n = X^2 IC, \tag{26a}$$

$$IC_p = (1-X)^2 IC, \tag{26b}$$

$$I_{spec_n} = (1-X)^2 I_{spec}, \tag{26c}$$

$$I_{spec_p} = X^2 I_{spec}, \tag{26d}$$

where IC and I_{spec} are arbitrary constants. Substituting (23b) and (26) in (22)

$$G_{m_{tot}} = \frac{I_{spec}\sqrt{IC}}{nU_T}[(1-X)^2 X + X^2(1-X)]. \tag{27}$$

To find X for maximum $G_{m_{tot}}$, then

$$\frac{\partial G_{m_{tot}}}{\partial X} = \frac{I_{spec}\sqrt{IC}}{nU_T}[1-2X] = 0. \tag{28}$$

Equation (28) yields $X = 0.5$. This result along with (1), (2), (19), and (26) yield

$$V_{od_n} = V_{od_p} = V_{od}, \tag{29a}$$
$$IC_n = IC_p = IC, \tag{29b}$$
$$I_{spec_n} = I_{spec_p} = I_{spec}, \tag{29c}$$
$$G_{m_n} = G_{m_p} = G_m, \tag{29d}$$
$$\frac{W_p}{W_n} = \frac{I_{spec_{\square_n}}}{I_{spec_{\square_p}}}, \tag{29e}$$

4.1.2. Weak Inversion Approximation

In weak inversion, $IC \leq 0.1$, thus (19) can be approximated to

$$V_{od_{n,p}} = nU_T ln(q_{s_{n,p}}), \tag{30a}$$
$$G_{m_{n,p}} = \frac{I_{spec_{n,p}} q_{s_{n,p}}}{2nU_T}. \tag{30b}$$

From (30a) and the definition of X,

$$q_{s_n} = exp\left(\frac{XV}{nU_T}\right), \tag{31a}$$
$$q_{s_p} = exp\left(\frac{(1-X)V}{nU_T}\right). \tag{31b}$$

From (20) and (31),

$$IC_n = exp\left(\frac{2XV}{nU_T}\right) + exp\left(\frac{XV}{nU_T}\right), \tag{32a}$$
$$IC_p = exp\left(\frac{2(1-X)V}{nU_T}\right) + exp\left(\frac{(1-X)V}{nU_T}\right), \tag{32b}$$

But, due to current reuse and from (1), $\frac{I_{spec_n}}{I_{spec_p}} = \frac{IC_p}{IC_n}$, thus

$$I_{spec_n} = I_{spec} IC_p, \tag{33a}$$
$$I_{spec_p} = I_{spec} IC_n, \tag{33b}$$

where I_{spec} is an arbitrary constant. Substituting (30b), (31), (32), and (33) in (22)

$$G_{m_{tot}} = \frac{I_{spec}}{nU_T} f(X), \tag{34}$$

where

$$f(X) = [exp\left(\frac{(2-X)V}{nU_T}\right) + exp\left(\frac{(1+X)V}{nU_T}\right) + 2exp\left(\frac{V}{nU_T}\right)]. \tag{35}$$

To find X for maximum G_{m_tot},

$$\frac{\partial G_{m_{tot}}}{\partial X} = \frac{I_{spec} V}{(nU_T)^2}[exp\left(\frac{(1+X)V}{nU_T}\right) - exp\left(\frac{(2-X)V}{nU_T}\right)] = 0, \tag{36}$$

hence $X = 0.5$. This makes (29) also valid in weak inversion.

Therefore, it can be concluded that for the maximum G_{m_tot} for stacked PMOS and NMOS transistors, a $(W/L)_p$ to $(W/L)_n$ ratio should be chosen such that $V_x = \frac{1}{2}(V_{DD} - V_{T_n} - V_{T_p}) + V_{T_p} = \frac{V_{DD}}{2} - \frac{V_{T_n}}{2} + \frac{V_{T_p}}{2}$.

4.2. Input Matching

The input impedance of the stacked common-gate stage can be deduced from the small signal model shown in Figure 5, where the AC coupling capacitance C_1 in Figure 3 is selected to be effectively a short circuit in the mid-band frequency range of interest.

$$Z_{in}(s) = \frac{R_{in} + sL_p + s^2 L_p R_{in} C_{in}}{1 + sR_{in}C_{in}}, \tag{37}$$

where R_{in} ($R_{in} = \frac{R/2 + r_o/2}{1 + 2G_m r_o/2} \approx \frac{1}{2G_m}$ for $R << r_o$, where r_o is the transistor output impedance) is the mid-band input impedance, L_p is the bond wire inductance, and $C_{in} = C_{GS_n} + C_{GS_p} + C_{SB_n} + C_{SB_p} \approx C_{GS_n} + C_{GS_p}$. This result is accurate for frequencies far greater than the C_1 corner frequency. Computing S_{11},

$$S_{11}(\omega) = \frac{Z_{in}(\omega) - R_s}{Z_{in}(\omega) + R_s}, \tag{38}$$

$$|S_{11}(\omega)|_{dB} = 10log\left(\frac{[(R_{in} - R_s) - \omega^2 L_p \tau_{in}]^2 + \omega^2 (L_p - R_s \tau_{in})^2}{[(R_{in} + R_s) - \omega^2 L_p \tau_{in}]^2 + \omega^2 (L_p + R_s \tau_{in})^2}\right), \tag{39}$$

where $\tau_{in} = R_{in} C_{in}$.

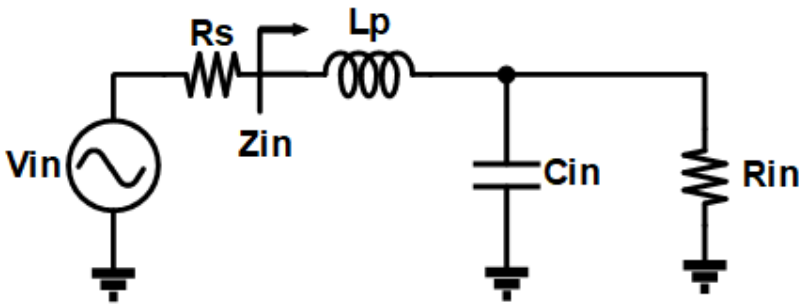

Figure 5. The small signal model of the stacked common-gate amplifier for input-impedance calculation.

4.3. Gain

From Figure 4c, the amplifier voltage gain at the mid-band frequency range can be formulated as

$$A_v = \frac{V_{out}}{V_x} = \frac{(1 + 2G_m r_o/2)R/2}{r_o/2 + R/2} \approx G_m R, \tag{40}$$

for $R << r_o$ and $G_m r_o >> 1$. These assumptions become inaccurate if the minimum feature length is used or at large currents; both extremes are avoided so as not to deteriorate amplifier gain or power consumption.

4.4. Bandwidth

The low-frequency corner of the signal bandwidth is determined by the AC coupling corner frequency as

$$f_{low} = \frac{1}{2\pi(R_s + R_{in})C_1}, \tag{41}$$

while the high-frequency corner is determined by the output pole and can be expressed as

$$f_{high} = \frac{1}{\pi R C_L}, \tag{42}$$

where the output impedance is equal to ½, $C_L = C_{GD_n} + C_{GD_p} + C_{DB_n} + C_{DB_p} \approx C_{GD_n} + C_{GD_p}$. f_{low} is typically in the range of a few hundred megahertz for an AC coupling cap in the range of a few picofarads, where f_{high} is in the range of a few to tens of gigahertz, thus f_{high} can be considered the amplifier bandwidth.

4.5. Noise

There are three sources of noise in the circuit in Figure 3, namely M_n, M_p, and R, where, at the mid-band and high frequency, the first two can be lumped into one device with double the transconductance, as shown in Figure 6. From Figure 6, it can be shown that the gain from the combined transistor gate to the output is

$$|A_{v_n}| = \frac{G_m R}{1 + 2G_m R_s}. \tag{43}$$

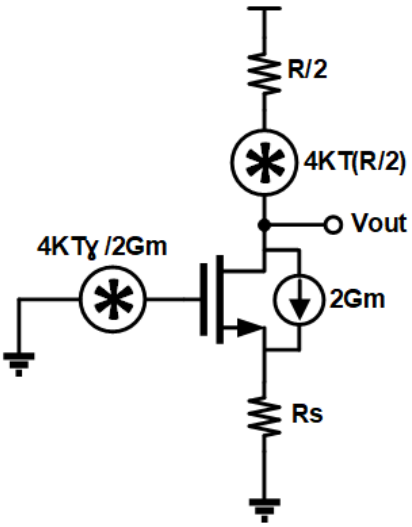

Figure 6. Equivalent noise circuit for the stacked common-gate amplifier.

Also, the signal gain (Figure 3) is

$$|A_{v,0}| = \frac{V_{out}}{V_{in}} = \frac{R_{in}}{R_s + R_{in}} G_m R = \frac{G_m R}{1 + 2G_m R_s}. \tag{44}$$

The generated output noise power from the lumped transistor and the output resistors have the following power densities:

$$\overline{V^2_{n,out,M_{n,p}}} = \frac{4KT\gamma}{2G_m} \frac{G_m^2 R^2}{(1 + 2G_m R_s)^2} = \frac{2KT\gamma G_m R^2}{(1 + 2G_m R_s)^2}, \tag{45a}$$

$$\overline{V^2_{n,out,R}} = 4KT\frac{R}{2} = 2KTR, \tag{45b}$$

where $\gamma = (\gamma_n + \gamma_p)/2$ is the average noise excess factor for NMOS and PMOS transistors, K is the Boltzmann constant, and T is the absolute temperature in Kelvin. The noise figure of the circuit can be deduced from (43) and (45) and is equal to

$$NF = 1 + \frac{\overline{V_{n,out,M_{n,p}}^2} + \overline{V_{n,out,R}^2}}{4KTR_sA_{v,0}^2}, \tag{46a}$$

$$NF = 1 + \frac{G_mR\gamma + (1 + 2G_mR_s)^2}{2G_m^2R_sR}, \tag{46b}$$

$$NF_{excess} = \frac{G_mR\gamma + (1 + 2G_mR_s)^2}{2G_m^2R_sR}, \tag{46c}$$

where NF_{excess} is the excess noise figure.

5. Graph-Based Design

The previous two sections represent the first two steps in the design approach, where the MOSFET parameters were defined in terms of the EKV model parameters and the circuit performance metrics were defined in terms of the MOSFET parameters. In this section, the remaining two steps are performed to complete the LNA design. The third step entails defining the design constraints that have to be met and the FoM to be maximized. Finally, the last step entails a bias point and size selection based on the data from the preceding step.

5.1. Design Constraints

The following constraints are used in this context; however, any other set of constraints can be used to fit other applications.

5.1.1. Minimum Gain Constraint

The LNA gain is one of its most critical performance metrics, thus it is reasonable to put a constraint on it

$$A_v \geq A_{min}, \tag{47}$$

where A_{min} is the minimum gain constraint. From (40), it follows that

$$R \geq A_{min}/G_m, \tag{48}$$

5.1.2. Maximum NF Constraint

The NF is one of the crucial LNA performance metrics. A constraint on it can be driven as follows:

$$NF \leq NF_{max}, \tag{49}$$

where NF_{max} is the maximum NF constraint. From (46b), it follows that

$$R \geq \frac{(1 + 2G_mR_s)^2}{(2NF_{max}G_mR_s - \gamma)G_m}, \tag{50}$$

5.1.3. Input Matching Constraint

This imposes a constraint on the max S_{11} value and a constraint on input capacitance, C_{in}, which maximizes the S_{11} bandwidth within which this value is not exceeded. The low-frequency S_{11} value can be deduced from (39) by substituting ω with zero; this leads to

$$S_{11,low-freq} = 20log|\frac{R_{in} - R_s}{R_{in} + R_s}|. \tag{51}$$

By targeting an S_{11} ($S_{11,targ}$) that is lower than $S_{11,low-freq}$ ($S_{11,targ} \leq S_{11,low-freq}$) and re-arranging it, it imposes a constraint on R_{in}

$$\left(\frac{1-10^{\frac{S_{11,targ}}{20}}}{1+10^{\frac{S_{11,targ}}{20}}}\right)R_s \leq R_{in} \leq \left(\frac{1+10^{\frac{S_{11,targ}}{20}}}{1-10^{\frac{S_{11,targ}}{20}}}\right)R_s. \tag{52}$$

By performing Equations (39) to (51), the frequency value at which S_{11} is equal to its low-frequency counterpart, $S_{11,low-freq}$, is computed to be

$$\omega_{S_{11}} = \sqrt{\frac{L_p(2R_{in}^2C_{in} - L_p) - R_s^2R_{in}^2C_{in}^2}{L_p^2R_{in}^2C_{in}^2}}. \tag{53}$$

Hence, $\omega_{S_{11}}$ represents the bandwidth where S_{11} is lower than its low-frequency value. For a certain R_{in} value and parasitic inductance value L_p, C_{in} is the only degree of freedom to set the S_{11} bandwidth. The C_{in} value that achieves the highest possible $\omega_{S_{11}}$ can be computed by taking the derivative of (53) with respect to C_{in} and equating the result to zero. This gives the C_{in} value that maximizes the S_{11} bandwidth,

$$C_{in,o} = L_p/R_{in}^2. \tag{54}$$

This result is generic and can be applied to any LNA circuit that can be described using the small signal model in Figure 5.

The S_{11} values derived in (39) and (51) neglect the AC coupling cap, C_1, effect. As shown in Figure 7, adding C_1 raises the DC value of S_{11} to 0 dB while the two curves (the actual S_{11} curve and the simplified S_{11} curve without C_1) approach each other at higher frequencies.

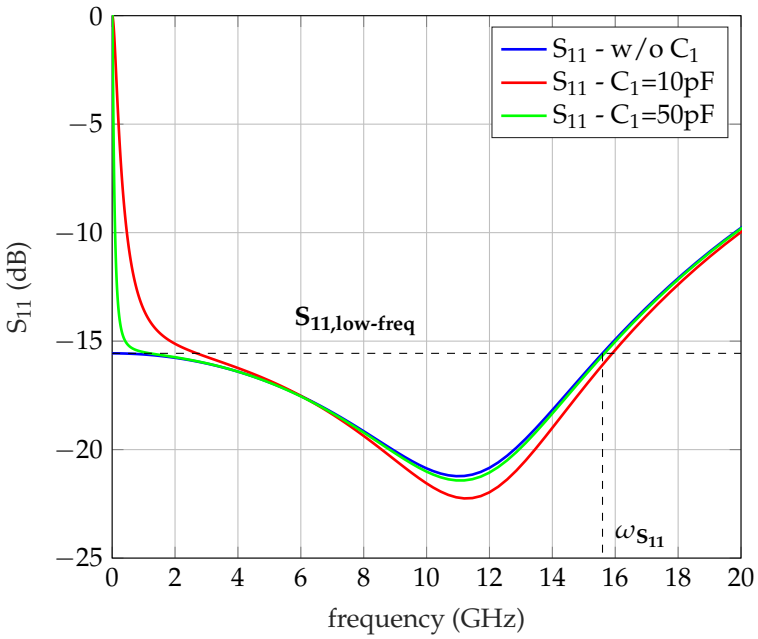

Figure 7. S_{11} versus frequency with no C_1 (blue), with C_1 = 10 pF (red), and with C_1 = 50 pF (green) (from Figure 5 after including C_1).

5.1.4. Headroom Constraint

This constraint is used to guarantee that the transistors are well into saturation and avoid operating near the triode region, deteriorating linearity. To achieve this, the maximum headroom on any of the output resistors is set by

$$HR = \frac{I_D R}{V_{DD}} \leq HR_{max}, \tag{55a}$$

$$HR = \frac{I_{spec_n} ICR}{V_{DD}} \leq HR_{max}, \tag{55b}$$

where I_D is the transistors' drain current, V_{DD} is the supply voltage, and HR_{max} is the maximum allowable headroom on one resistor.

An extra constraint for the accuracy of the design flow and to avoid the short channel issues discussed before is the minimum transistor channel length allowed.

5.2. Figure of Merit

Defining the FoM for the LNA is the core of the design process. An adopted FoM has to be balanced and take all the important LNA specifications into consideration while targeting UWB applications. There are multiple FoMs reported in the literature, and the one in [15] is considered to be the most basic,

$$FoM_1 = \frac{A_v \cdot BW(\text{GHz})}{NF_{excess} \cdot P_D(\text{mW})} \quad (\text{GHz/mW}), \tag{56}$$

where P_D is the power dissipation in mW.

Adding the circuit area to the FoM is crucial for the LNA design; thus, the adopted FoM in this work is extended to FoM_1 by adding the transistor area in μm^2 to minimize the total circuit area [16].

$$FoM_2 = \frac{A_v \cdot BW(\text{GHz})}{NF_{excess} \cdot P_D(\text{mW}) \cdot Area(\mu m^2)} (\frac{\text{GHz}}{\text{mW} \cdot \mu m^2}), \tag{57}$$

5.3. Sizing/Bias Point Selection

The last step in the design process is to choose the IC for the transistors and their sizing (W/L) that meet all the design constraints and offer the best FoM for the circuit. This last step is demonstrated through two different designs: the design of a high-bandwidth LNA with a target gain and the design of a low-noise LNA.

5.3.1. High-Bandwidth LNA

Table 2 summarizes the design inputs and constraints used for the design. The IC and (W/L) can be chosen graphically by plotting both the design parameters and the FoM. Figure 8 shows these parameters versus the IC, while Figure 9 shows the FoM for different $(W/L)_n$ values, where $(W/L)_p$ can then be deduced using (29e). The parameters in Figure 8 along with the FoM in Figure 9 are uniquely used for the choice of the transistors' IC and the NMOS aspect ratio $(W/L)_n$. The first parameter is R_{in}, which is computed using $R_{in} = 1/2G_m$, where G_m is given by (19b) and (20). The minimum and maximum constraints on R_{in} are given by the relation in (52). The second parameter is the transistors' lengths, which satisfies the relation $L = \frac{C_{GS_n}}{W_n C_{GS0}}$, where $C_{GS_n} = \frac{C_{in}}{(1+W_p/W_n)}$, C_{in} is set as in (54), and C_{GS0} is given by (14), (15), and (16). The third parameter is the HR_{max}, which can be computed from (55) while substituting R in (48). The fourth parameter is the bandwidth found in (42).

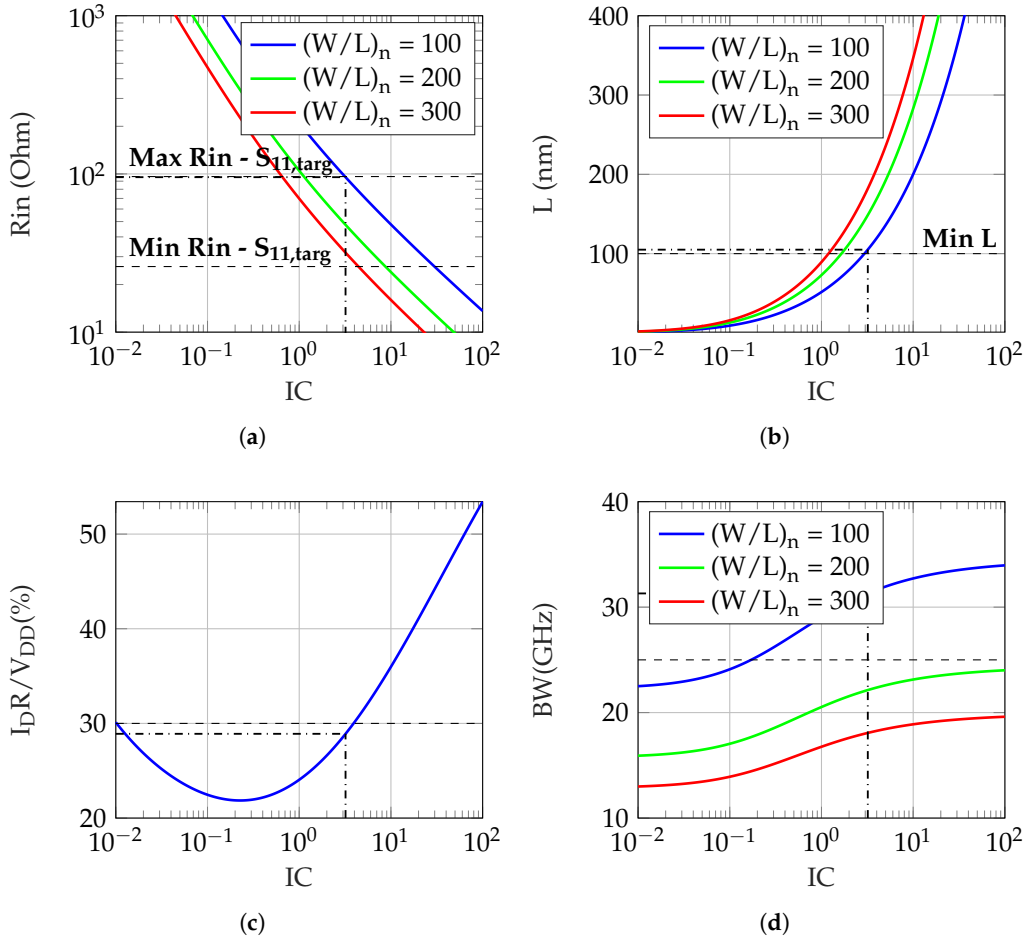

Figure 8. (**a**) Low-frequency input impedance, (**b**) transistors' lengths, (**c**) voltage headroom on the load resistor, and (**d**) bandwidth vs. *IC* for the high-bandwidth LNA.

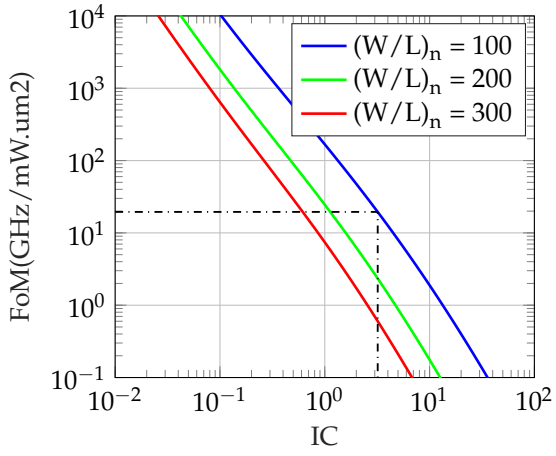

Figure 9. *FoM* vs. *IC* for the high-bandwidth LNA.

Table 2. Design inputs and constraints of the high-bandwidth LNA.

	Circuit Components		**Transistor Constraints**		**Specifications**		
Parameter	R_s	L_p	HR_{max}	L_{min}	A_v	S_{11}	Bandwidth
Value	50 Ω	0.5 nH	30%	100 nm	10 dB	−10 dB	25 GHz

As noticed from Figures 8 and 9, the IC that fulfills all the design constraints and achieves the best FoM is 3.2, which corresponds to the transistors' operation in moderate inversion with a $(W/L)_n$ of 100. This corresponds to a FoM of 19.6 $\frac{\text{GHz}}{\text{mW}\cdot\mu\text{m}^2}$, an L of 105 nm, a headroom of 28.9%, and a low-frequency input impedance of 95.4 Ω, which lies between the minimum value and the maximum value needed for a low-frequency S_{11} of less than −10 dB, as stated in (52). The next step is to find the values of the load resistor, R, and the supply voltage, V_{DD}, that correspond to an IC equal to 3.2. The load resistor value can be found by substituting A_{min} in (48) with 3.17 (equivalent to 10 dB), while the G_m can be computed from (19b) and (20) using an IC equal to 3.2 and a $(W/L)_n$ equal to 100. The resultant R value is about 605 Ω. The supply voltage, V_{DD}, can be computed from the equation $V_{DD} = V_{T0_n} + V_{T0_p} + 2V_{od}$, assuming no body effect, and the source and the bulk of each transistor are tied together, where V_{od} corresponds to the NMOS or the PMOS overdrive voltage, as deduced in (29a), which can be computed using (19a). The resultant V_{DD} value is around 1 V. All the circuit performance parameters can also be calculated using the relationships deduced in Sections 4 and 5. An actual circuit is built and verified using the TSMC 65 nm process based on the design outputs. In the first iteration of the design, the transistors' bulk and source terminals are tied together, and the body effect is ignored. The body effect is considered afterwards (transistors' bulks are tied to supply rails). The higher resulting transistor threshold voltages impose a higher supply voltage at the same IC. The physical layout of this LNA is shown in Figure 10. The shown layout was used in the post-layout simulations to examine the effect of added parasitics on the LNA performance, as reported in Table 3.

Table 3. Design results of the high-bandwidth LNA.

		Analytical Value	Schematics (No Body Effect)	Schematics (Body Effect)	Post-Layout (Body Effect)
Transistor Parameters	IC	3.2	3.26	3.21	3.18
	I_D (μA)	480	489	482	478
	L (nm)	105	105	105	105
	$(W/L)_n$	100	100	100	100
	$(W/L)_p$	300	300	300	300
Circuit Parameters	$R(\Omega)$	605	606	606	606
	V_{DD} (V)	1	0.98	1.1	1.12
	C_{in} (fF)	55	60.3	58.7	N/A
	C_{load} (fF)	16.8	20.2	19.2	N/A
	R_{in} (Ω)	95.4	127.2	106.7	111.9
Circuit Performance Metrics	A_v (dB)	10	10.8	11.9	12.4
	BW (GHz)	31.3	32.9	25.6	16.5
	HR (%)	28.9	30.4	26.7	27.6
	S_{11} (dB)	≤−10	−7.1	−8.6	−8.2
	S_{11} BW (GHz)	N/A	34.7	27.2	27.6
	P_{DC} (mW)	0.48	0.48	0.53	0.53
	NF (dB)	5.3	4.5→6.2	4.3→6	4.5→5.8
	IIP_3 (dBm)	N/A	−5.5	−4.3	−5.2
	FoM ($\frac{\text{GHz}}{\text{mW}\cdot\mu\text{m}^2}$)	19.6	29.6	25.5	16.2

Figure 11 shows the results of the high-bandwidth LNA, and Figure 11a shows the S_{21} across frequencies, and the low-frequency and high-frequency 3 dB corners are 50 MHz and 25.6 GHz, respectively, where the high-frequency corner reduces to 16.5 GHz post-layout. As shown in Figure 11b, the S_{11} schematic simulation result is better than −8.6 dB across the frequency range of 0.6 GHz to 27.8 GHz, and the post-layout value is better than −8.2 dB across the frequency range of 0.7 GHz to 28.3 GHz. The NF is shown in Figure 11c, where it ranges from 4.3 dB to 11.8 dB for schematic simulations. The NF value is confined between 4.3 dB and 6 dB for the major portion of the frequency range; however, it deteriorates at

very low frequencies, where the matching behavior is not ideal due to the DC-blocking cap effect. The *NF* post-layout result is more similar in ranges from 4.5 dB to 11.6 dB, and when it is confined between 4.5 dB and 5.8 dB for most of the spectrum.

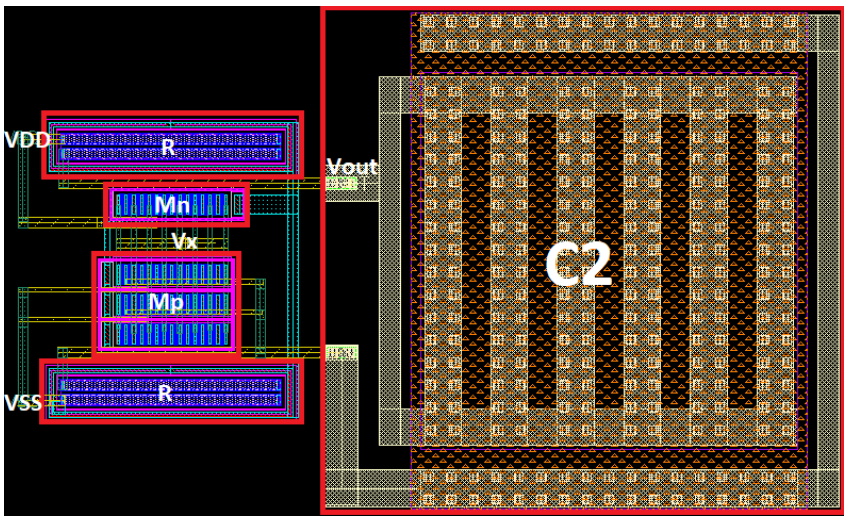

Figure 10. Physical layout of the high-bandwidth LNA.

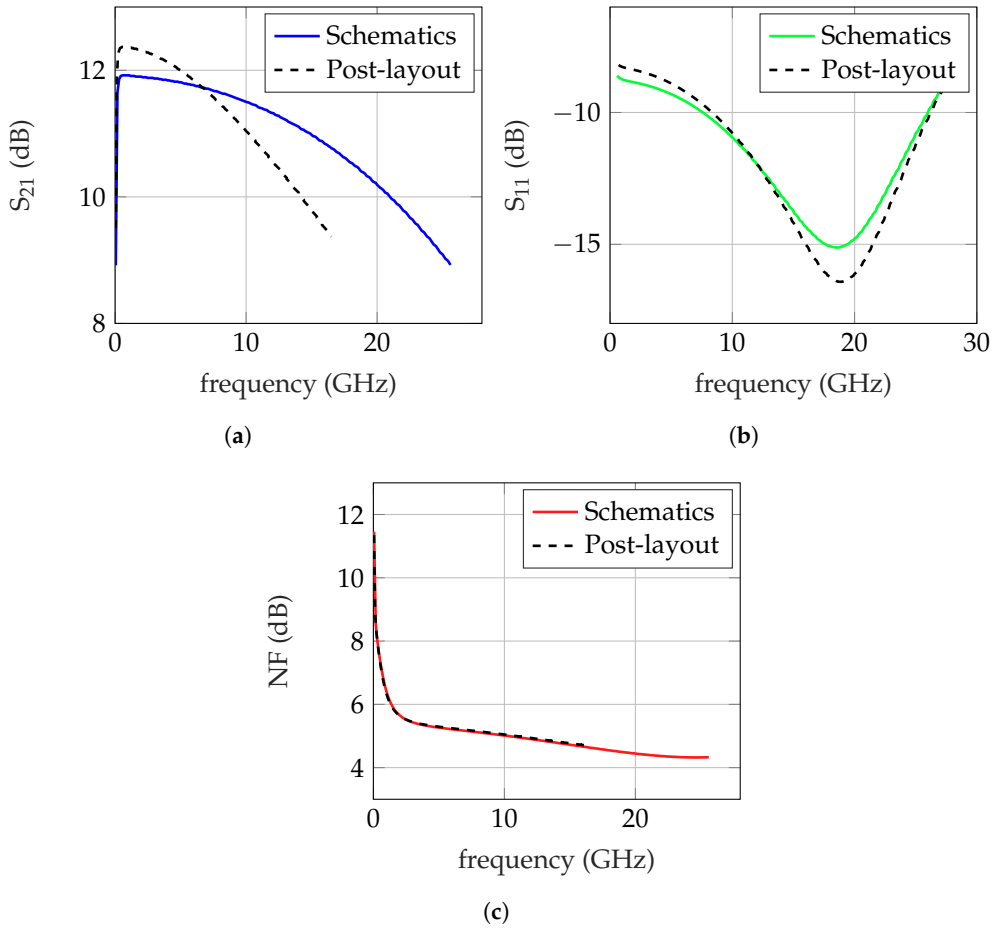

Figure 11. Schematic (solid) and post-layout (dashed) results of the high-bandwidth LNA: (**a**) S_{21}, (**b**) S_{11}, and (**c**) *NF*.

5.3.2. Low-Noise LNA

Table 4 summarizes the design inputs and constraints used for the design. A similar approach is adopted in the design process as in the first LNA, but with different design constraints. Figure 12 shows the design parameters versus the IC, while Figure 13 shows the FoM for different $(W/L)_n$ values. As noticed from Figures 12 and 13, the IC that fulfills all the design constraints and achieves the best FoM is 0.9, which corresponds to the transistors' operation in moderate inversion with a $(W/L)_n$ of 450. This corresponds to a FoM of 3.1 $\frac{\text{GHz}}{\text{mW}\cdot\mu\text{m}^2}$, an L of 102 nm, a headroom of 29.9%, a gain (A_v) of 12 dB, and a low-frequency input impedance (R_{in}) of 50 Ω, which lies between the minimum value and the maximum value needed for a low-frequency S_{11} of less than −15 dB, as stated in (52). The next step is to find the values of the load resistor, R, and the supply voltage, V_{DD}, that correspond to an IC equal to 0.9. The load resistor value can be found by substituting NF_{max} in (50) with 2.51 (equivalent to 4 dB), while G_m can be computed from (19b) using an IC equal to 0.9 and $(W/L)_n$ equal to 450. The resultant R value is about 400 Ω. The supply voltage, V_{DD}, can be computed from the equation $V_{DD} = V_{T0_n} + V_{T0_p} + 2V_{od}$, assuming no body effect, and the source and the bulk of each transistor are tied together, where V_{od} corresponds to the NMOS or the PMOS overdrive voltage, as deduced in (29a), which can be computed using (19a). The resultant V_{DD} value is around 0.82 V. An actual circuit is built and verified using the TSMC 65 nm process based on the design outputs, and the results are summarized in Table 5. Figure 14 shows the physical layout of this LNA.

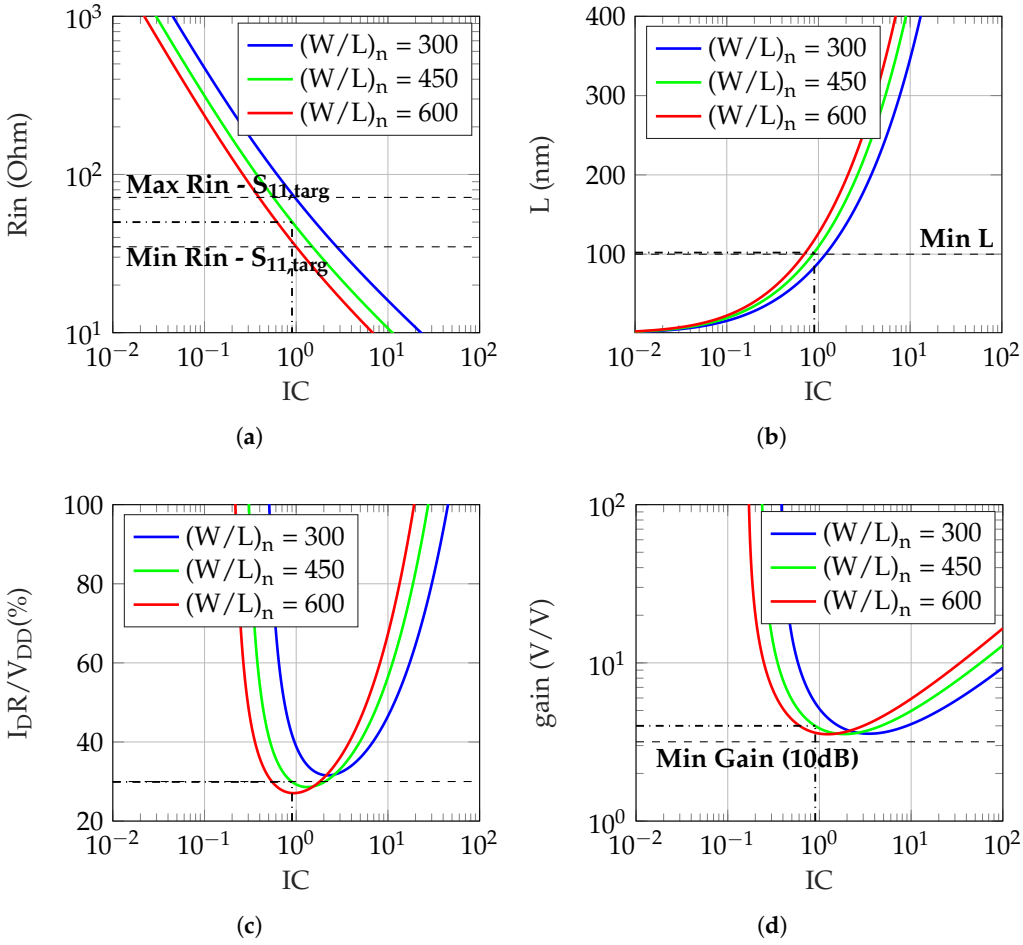

Figure 12. (**a**) Low-frequency input impedance, (**b**) transistors' lengths, (**c**) voltage headroom on the load resistor, and (**d**) gain vs. IC for the low-noise LNA.

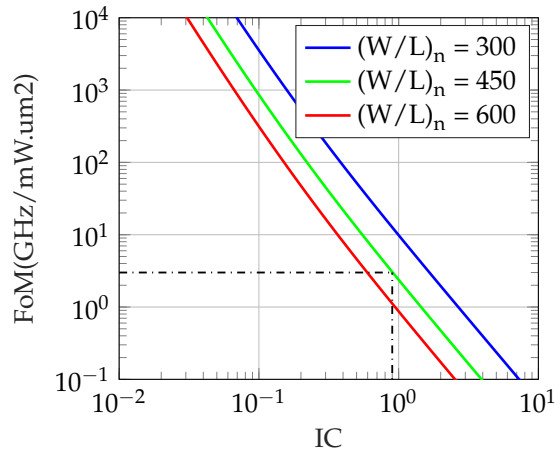

Figure 13. *FoM* vs. *IC* for the low-noise LNA.

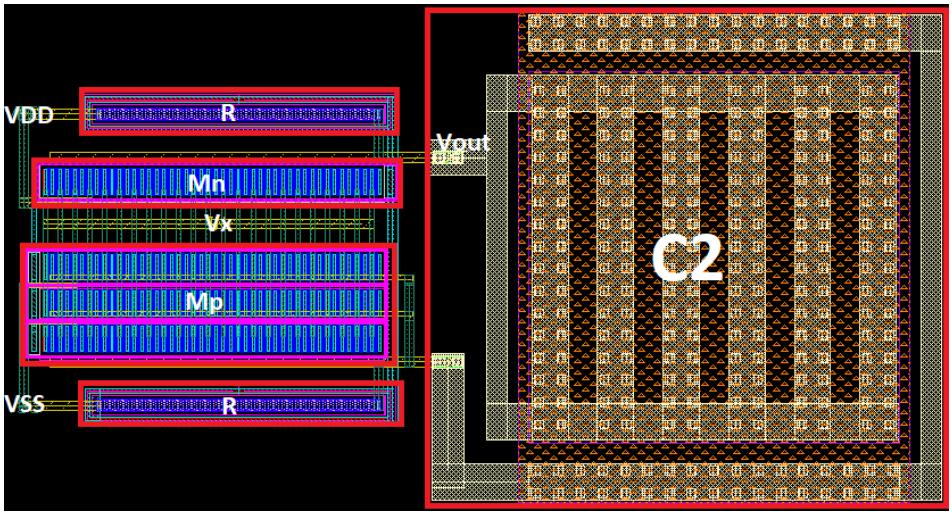

Figure 14. Physical layout of the low-noise LNA.

Table 4. Design inputs and constraints of the low-noise LNA.

	Circuit Components		**Transistor Constraints**		**Specifications**		
Parameter	R_s	L_p	HR_{max}	L_{min}	A_v	S_{11}	NF
Value	50 Ω	0.5 nH	30%	100 nm	10 dB	−15 dB	4 dB

Figure 15 shows the results of the low-noise LNA, and Figure 15a shows the S_{21} across frequencies, and the low-frequency and high-frequency 3 dB corners are 80 MHz and 9.9 GHz, respectively, and the high-frequency corner reduces to 6.9 GHz post-layout. As shown in Figure 15b, the S_{11} schematic simulation result is better than −13 dB across the frequency range of 0.35 MHz to 9.9 GHz, and the post-layout value is better than −15 dB across the frequency range of 0.47 MHz to 9.2 GHz. The *NF* is shown in Figure 15c, and it ranges from 3.7 dB to 9.2 dB. The *NF* value is confined between 3.7 dB and 7 dB for the major portion of the frequency range; however, it deteriorates at very low frequencies. The *NF* post-layout result ranges from 4 dB to 9.3 dB and is confined between 4 dB and 7 dB for most of the spectrum.

Table 5. Design results of the low-noise LNA.

		Analytical Value	Schematics (No Body Effect)	Schematics (Body Effect)	Post-Layout (Body Effect)
Transistor Parameters	IC	0.9	0.9	0.92	0.92
	I_D (µA)	608	607	618	605
	L (nm)	102	100	100	100
	$(W/L)_n$	450	450	450	450
	$(W/L)_p$	1350	1350	1350	1350
Circuit Parameters	$R(\Omega)$	400	400	400	400
	V_{DD} (V)	0.82	0.79	0.9	0.91
	C_{in} (fF)	197.8	214.7	210.3	N/A
	C_{load} (fF)	73.6	83.5	81	N/A
	R_{in} (Ω)	50	64.6	54.4	57
Circuit Performance Metrics	A_v(dB)	12	11.1	12.1	12.5
	BW (GHz)	10.8	13.8	9.9	6.8
	HR (%)	29.9	30.9	27.6	27.6
	S_{11} (dB)	≤ -15	-15	-13	-15
	S_{11} BW (GHz)	N/A	13.4	9.6	8.8
	P_{DC} (mW)	0.5	0.48	0.56	0.55
	NF (dB)	4	4→7.8	3.7→7	4→7
	IIP_3 (dBm)	N/A	-7	-4.1	-4.3
	FoM ($\frac{\text{GHz}}{\text{mW}\cdot\mu\text{m}^2}$)	3.1	3.8	3	1.9

The implemented circuits are compared with the state-of-the-art designs, as shown in Table 6, where the FoM used for the comparison is $FoM = \frac{A_v \cdot BW(\text{GHz}) \cdot IIP_3(\text{mW})}{NF_{excess} \cdot P_D(\text{mW})}$, which considers IIP_3. The voltage gain and noise figure used in the FoM are the maximum and minimum across the frequencies, respectively. The implemented LNAs achieve better performance than most of the state-of-the-art designs. Exceptions to this are the designs in [8,10,17], which achieve better FoM. The high FoM of the LNA in [8] is possible due to the exceptional linearity of its design. However, this is achieved by utilizing a negative feedback loop, which increases design complexity and raises stability concerns. The matching bandwidth of the design in [10] is too small compared to the 3 dB bandwidth of the gain; thus, the real bandwidth is smaller than the reported one, deteriorating the achieved FoM. The LNA in [17] achieves a very wide bandwidth but at the cost of a higher power. Special techniques are used for noise and nonlinearity cancelation that result in increased complexity. Moreover, the very high power consumption makes the design unpreferable for use in low-power IoT applications. In [15], a three-stage amplifier with a second-order resonance circuit is used for controlled matching performance. This comes at the cost of relatively high power consumption and deteriorated linearity, thus compromising its FoM. The LNA in [18] utilizes an active notch filter for blocker suppression and linearity enhancement. The overall design uses a large number of bulky passives and multiple-stage topology compromising its area and power. The enhanced noise performance is a result of using a load resonant tank circuit. This is opposed to the use of two load resistors in our current reuse design to avoid the use of bulky inductors. The use of a feedback loop for input matching enhancement and a feedforward path for noise cancelation in the design in [19] results in an overall high power dissipation while not reducing the NF much. Multiple feedforward noise-canceling paths are used in [20] that result in low NF. However, the achieved bandwidth is relatively low due to the use of three transistors and an inductor in the output branch, increasing the parasitic capacitance at the output node. Finally, the use of a two-stage inverter-based amplifier in [21] increases the power consumption, significantly deteriorating the overall FoM despite achieving good linearity and noise performance.

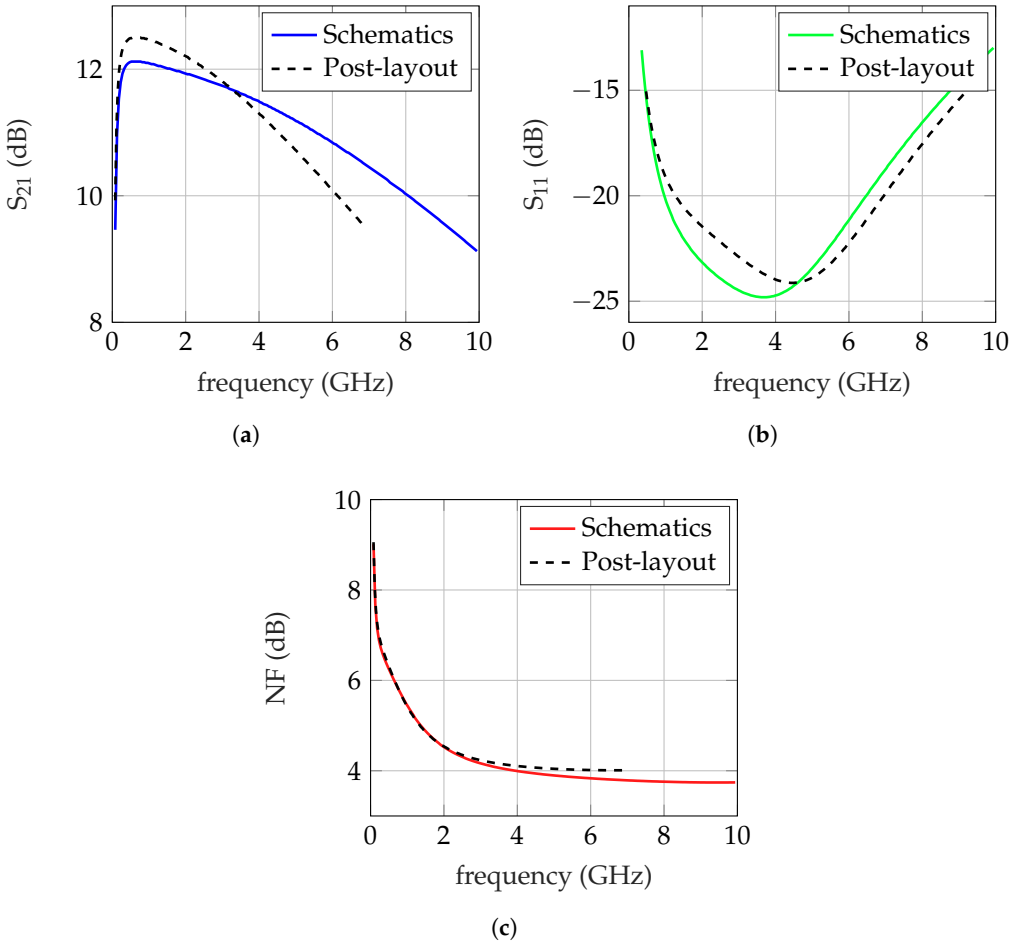

Figure 15. Schematic (solid) and post-layout (dashed) results of the low-noise LNA. (**a**) S_{21}, (**b**) S_{11}, and (**c**) NF.

Table 6. Performance metrics comparison for the proposed LNAs and the state-of-the-art LNAs.

Design	Tech (nm)	S_{11} (dB)	Gain (dB)	Bandwidth (GHz)	IIP_3 (dBm)	P_{DC} (mW)	NF (dB)	FoM (GHz)
[6]	65	<-11.6	17	7	0.7	5.5	3.7	7.9
[8]	28	<-10	17	5.8	7.9	3.7	3	68.8
[10]	28	<-10	25	3	-9.6	0.9	1.5	15.8
[15]	130	<-11	15	9.3	-7	8.5	4	0.8
[17]	65	<-10	12.8	19	5.8	20.3	3.3	13.6
[18]	130	<-11.5	16.1	6.8	2.7	10.2	2.1	12.7
[19]	40	<-10	17	10	-2.8	9	3.5	3.3
[20]	28	<-10	15.2	4.5	-4.6	4.5	2.1	3.2
[21]	180	<-10.7	15.2	11.5	-0.2	18	2.2	5.3
High-BW LNA *	**65**	$<$**−8.2**	**12.4**	**16.5**	**−5.2**	**0.53**	**4.5**	**21.5**
Low-Noise LNA *	**65**	$<$**−15**	**12.5**	**6.8**	**−4.3**	**0.55**	**4**	**12.8**

* Simulated performance.

It is worth noting that the objective of this work is not to report the best FoM but to present a graphical design approach that is guided by pre-defined constraints. Also, the comparison table with the state-of-the-art is intended only to show how the obtained performance by simulations fits with respect to previous work. However, it is understood that a real comparison can only be made if the design is fabricated and measured on silicon. In general, to increase the chances that simulations match the measurements after fabrication, all parasitics need to be included in simulations (which was performed in

this work). However, it is understood that fabrications and measurements should still be conducted to validate that the inclusion of parasitics was conducted properly in the design phase. Nevertheless, this is beyond the objectives of this work.

6. Conclusions

A design approach for a UWB LNA based on an IC is proposed. The proposed approach is not limited to the transistor-strong inversion region, as in the case of adopting the square law. The design approach utilizes the EKV model to derive expressions for different circuit performance metrics as a function of transistor parameters. Since the EKV model is valid in weak, moderate, and strong inversion, the derived expressions can be used to choose the bias point of the circuit transistors while navigating through different operation regions. A number of design constraints are defined to set boundries to the design space, and the value of IC is used as a knob to maximize the FoM that combines relevant performance metrics. The design approach is applied to the design of two UWB stacked common-gate LNAs, and the design values and specifications obtained from the design approach were compared to simulation results, showing high agreement, indicating the effectiveness of the approach in reaching the target specifications with no iterations.

The designed high-bandwidth LNA achieves S_{11} better than -8.2 dB over a 27.6 GHz frequency range, a gain of 12.4 dB over a 16.5 GHz bandwidth, a minimum NF of 4.5 dB, and an IIP_3 of -5.2 dBm while consuming only 530 μW. The designed low-noise LNA achieves a S_{11} of better than -15 dB over an 8.8 GHz frequency range, a gain of 12.5 dB over a 6.8 GHz bandwidth, a minimum NF of 4 dB, and an IIP_3 of -4.3 dBm while consuming only 550 μW.

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Abbreviations

The following abbreviations are used in this manuscript:

ACM	Advanced Compact MOSFET
BW	Bandwidth
FCC	Federal Communications Commission
IC	Inversion Coefficient
IoT	Internet of Things
IR	Impulse radio
LNA	Low-noise amplifier
LUT	Lookup table
MOSFET	Metal–oxide–semiconductor field-effect transistor
NF	Noise figure
PAN	Personal area network
SAR	Synthetic aperture radar
TOA	Time of arrival
TOF	Time of flight
UWB	Ultra-wide band
WBAN	Wireless body area network

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