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SiC Fin-Channel MOSFET for Enhanced Gate Shielding Effect

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Abstract: A SiC fin-channel MOSFET structure (Fin-MOS) is proposed for an enhanced gate shielding effect. The gates are placed on each side of the narrow fin-channel region, while grounded p-shield regions below the gates provide a strong shielding effect. The device is investigated using Sentaurus TCAD. For a narrow fin-channel region, there is difficulty in forming an Ohmic contact to the p-base; a floating p-base might potentially store negative charges upon high drain voltage, and, thus, causes threshold voltage instabilities. The simulation reveals that, for a fin-width of 0.2 µm, the p-shield regions provide a stringent shielding effect against high drain voltage, and the dynamic threshold voltage shift (ΔV_{th}) is negligible. Compared to conventional trench MOSFET (Trench-MOS) and asymmetric trench MOSFET (Asym-MOS), the proposed Fin-MOS boasts the lowest OFF-state oxide field and reverse transfer capacitance (C_{rss}), while maintaining a similar low ON-resistance.

Keywords: SiC MOSFET; fin-channel; gate shielding effect; dynamic threshold voltage

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1. Introduction

With the increasing energy demand and growing environmental concerns, the application of power electronics in the energy sector is becoming increasingly important. Modern power electronics continues to evolve towards a high power, high efficiency, and integration [1]. Power semiconductor devices play a crucial role in this development.

Over the past few decades, the rapid progress of power semiconductor devices has primarily relied on the advancement of silicon-based devices [2]. Silicon, with its ability to undergo thermal oxidation and form silicon dioxide, is an excellent insulator suitable for producing stable metal-oxide-semiconductor (MOS) devices [3]. However, traditional silicon-based power MOSFETs face challenges in effectively operating in high-temperature, high-power, and high-frequency applications due to the inherent limitations of silicon's physical properties. In contrast, wide-bandgap semiconductor materials like gallium nitride (GaN) and silicon carbide (SiC) exhibit superior physical characteristics, including a high breakdown field and high electron mobility, making them ideal for future power devices [4].

Among the wide-bandgap materials, the commercial application of SiC materials is the most mature. SiC MOSFETs emerge as an excellent candidate for replacing silicon-based MOSFETs in the next generation of power electronic systems. The carbonization of silicon carbide enables it to undergo thermal oxidation, similar to silicon, which are considered as a promising approach to enhance the performance of the next-generation power conversion systems [5,6].

The development of SiC MOSFETs is hindered by its low channel mobility which leads to a large channel resistance [7,8]. There are many techniques being reported for the reduction of the channel resistance, such as the adoption of a shorter channel, MOS interface treatment for a higher channel mobility, etc. [9–13]. Among the efforts, the trench MOSFET structure is widely recognized as a promising approach for realizing a low-resistance SiC power transistor, since it allows a more compact cell design, and, thus, lowers the channel resistance by increasing the channel density [14,15]. Moreover, the trench MOSFET structure presents the flexibility to exploit the higher channel mobility on non-basic faces [16–18].

For conventional trench MOSFETs, there is no shielding region, and, for this reason, the devices may face many problems upon high drain voltage. One of the problems is the high OFF-state oxide field at the trench corner. Although the breakdown field of oxide in SiC MOSFETs (typically more than 10 MV/cm [19]) is significantly higher than that of SiC, it is supposed to keep the maximum oxide electric field ($E_{\text{OX-M}}$) below 3 MV/cm for long-term reliability [20,21]. Furthermore, the presence of a large reverse transfer capacitance significantly hampers the switching performance of conventional trench MOSFETs, resulting in an unsatisfactory operation [13]. To solve these problems, in 1998, J. Tan et al. proposed the use of a p-shield region beneath the trench gate as a means of oxide protection. This device demonstrated a breakdown voltage (BV) of 1400 V at an oxide field of 3.1 MV/cm. However, the potential dynamic issues associated with the floating p-type shielding region were overlooked. In a subsequent study conducted by J. Wei et al. from the Hong Kong University of Science and Technology, it was discovered that the p-shield region needs to be properly grounded in order to fully exploit the dynamic characteristics of the devices [22]. In 2017, Dethard Peters et al. described an asymmetric SiC trench MOSFET concept (Asym-MOS), with a well-grounded p-shield region on one side and the bottom of the gate in a cell to shield the gate oxide [23]. The most favorable orientation was chosen for improving the channel mobility and the results show that the channel mobility for the selected crystal plane is twice as large as the traditional crystal plane [24,25]. However, the implementation of this structure entails stringent fabrication requirements for the trenches. In 2020, T. Yang et al. from Tsinghua University introduced a novel SiC trench MOSFET design featuring deep p+ shielded regions and current spreading layers (CSLs) (referred to as DPCSL-MOS) [26]. The findings demonstrate that incorporating CSLs with a higher doping concentration than the drift layer effectively mitigates the JFET effect and reduces the resulting device ON-resistance (R_{ON}). The device shows a BV of 1560 V with a R_{ON} of 1.72 mΩ·cm^2 because of the high channel mobility of 50 cm^2/V-s being adopted. However, the complexity of the device fabrication process, which includes secondary epitaxial growth, poses challenges for its current commercialization. In 2023, J. Gao et al. described a recessed source trench silicon carbide MOSFET with integrated MOS-channel diode (MCD) [27]. The MCD utilizes a short channel with adjustable length by varying the recessed depth. This design eliminates the bipolar degradation of the parasitic body p-i-n diode by creating a low potential barrier for the electron flow through the JFET region. The recessed source trench introduces an additional depletion region, resulting in a more uniform distribution of the OFF-state electric field. As a result, the proposed SiC MOSFET achieves a significant reduction in the gate-to-drain capacitance and an improvement in thebreakdown voltage compared to the SiC trench MOSFET with an integrated self-assembled three-level protection Schottky barrier diode. However, the current process still involves multiple etching and implantation steps, suggesting that further technological advancements are needed.

In this work, a SiC fin-channel MOSFET (Fin-MOS) is proposed to enhanced the gate shielding effect, and is comprehensively investigated using TCAD simulations. Grounded p-shield regions are placed under the gates to reduce the gate-to-drain electrical coupling. The manufacturing process of the proposed Fin-MOS is compatible with the traditional trench MOSFET. However, the ohmic contact to the p-base is removed because of the narrow fin-channel region. As reported in the literature [22], a floating p-region may result in instabilities due to the charge storage effect. In this work, we proposed a Fin-MOS structure model with the parasitic n-p-n structure to investigate the threshold voltage instability of the Fin-MOS. It is found that, in the proposed Fin-MOS, as a result of the enhanced shielding effect, the charge-storage-induced instability is negligible. Compared to the conventional trench MOSFET and asymmetric trench MOSFET, the proposed Fin-MOS exhibits the lowest $E_{OX\text{-}M}$ to 0.77 MV/cm while maintaining a low ON-resistance (R_{ON}). Moreover, the Fin-MOS boasts the lowest reverse transfer capacitance (C_{rss}), gate charge (Q_G), gate-to-drain charge (Q_{GD}), and saturation current (I_{sat}) among these three structures. As a result, the adoption of the Fin-MOS structure holds significant promise in the development of high-performance SiC power switching transistors. By utilizing the Fin-MOS design, the dynamic stability of devices in high-voltage switch applications can be improved. This advancement offers a potential solution to enhance the overall performance and reliability of SiC-based power switches.

2. Device Structure and Parameter Optimization

2.1. Simulation Models

This study employs numerical simulations using Sentaurus TCAD to investigate the topic under consideration. The electron/hole continuity equations and Poisson equation are solved self-consistently, incorporating various factors, including the Shockley–Read–Hall recombination, Auger recombination, incomplete dopant ionization, doping-dependent transport, band narrowing, anisotropic material properties, and impact ionization [28]. The electron and hole impact ionization coefficients described in [10] are implemented in this study. The simulation parameters for the Trench-MOS are formulated based on the methodology outlined in Reference [9], while those for the Asym-MOS are derived from Reference [23]. It is important to note that specific parameters for the Asym-MOS have not been publicly disclosed by Infineon, which may result in deviations between the simulated Asym-MOS devices and their real commercial counterparts. Nevertheless, all parameters, except those discussed in the paper that require optimization, remain consistent with the Trench-MOS to facilitate meaningful comparisons.

2.2. Structure

Figure 1 shows the cross-sectional structures of the Trench-MOS, the Asym-MOS, and the proposed Fin-MOS. The devices studied in this letter are designed to work below 1200 V. For all of the devices, the doping concentration of the drift region is 8×10^{15} cm^{-3} and the thickness (from the bottom of the gate to the backside n+ region) is 11 µm. The depth of the gate trench is set to 1.5 µm. For both the sidewall and the bottom, the thickness of the gate oxide is 50 nm. The length of the channels is 0.5 µm. The channel mobility of the Trench-MOS and the Fin-MOS is set to 20 cm^2/V-s [29–33]; the channel mobility of the Asym-MOS will be discussed later. For the Fin-MOS, the fin-width is W_{fin}. The cell-width (W_{cell}) of the Trench-MOS, the Asym-MOS, and the Fin-MOS are, respectively, 3 µm, 2.7 µm, and 3 µm + W_{fin}.

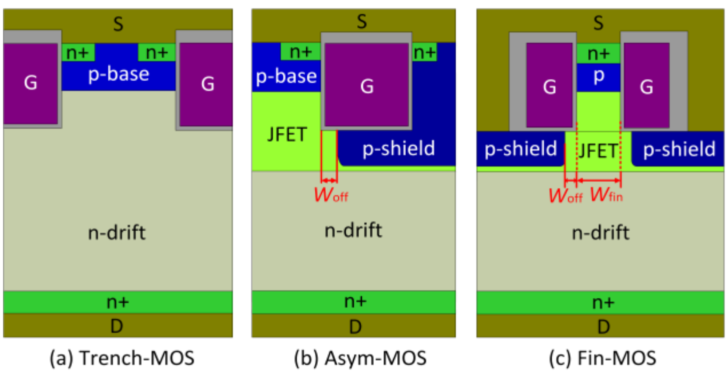

Figure 1. Schematic cross-sectional structures of (**a**) the conventional trench MOSFET (Trench-MOS), (**b**) the asymmetric trench MOSFET (Asym-MOS), and (**c**) the proposed fin-channel MOSFET (FinMOS).

2.3. Fabrication

For the Trench-MOS and the Asym-MOS, the fabrication technologies are well-established. For the proposed Fin-MOS, the fabrication process is shown in Figure 2. As shown in Figure 2a, the epitaxial structure consists of the n+ substrate, a 10.8 µm n-drift region with a doping concentration of 8×10^{15} cm^{-3}, and a 1.8 µm n-type JFET region (in this region, while the p-type shielding regions on both sides and the n-type region in the middle form a structure similar to the Junction Field-Effect Transistor (hence the name JFET region), with a doping concentration of N_{JFET}, and, at the top, is a 0.7 µm p-type layer with a doping concentration of N_{PB} used as the base region. The device fabrication commented with multiple nitrogen implantations to form the n+ source region as shown in Figure 2b. Then, the inductively coupled plasma reactive ion etching (RIE) is used to form the gate trench, as illustrated in Figure 2c. Then, multiple implantations are utilized to form the p+ shield region, as shown in Figure 2d. The self-aligned process is recommended to simplify the fabrication process. The offset distance between the p-shield and trench corner (W_{off}) is 0.2 µm. As shown in Figure 2e, Spacer-gate technology can be used to form the gates. The final process included the deposition of the gate oxide and the metal overlay process, which are shown in Figure 2f.

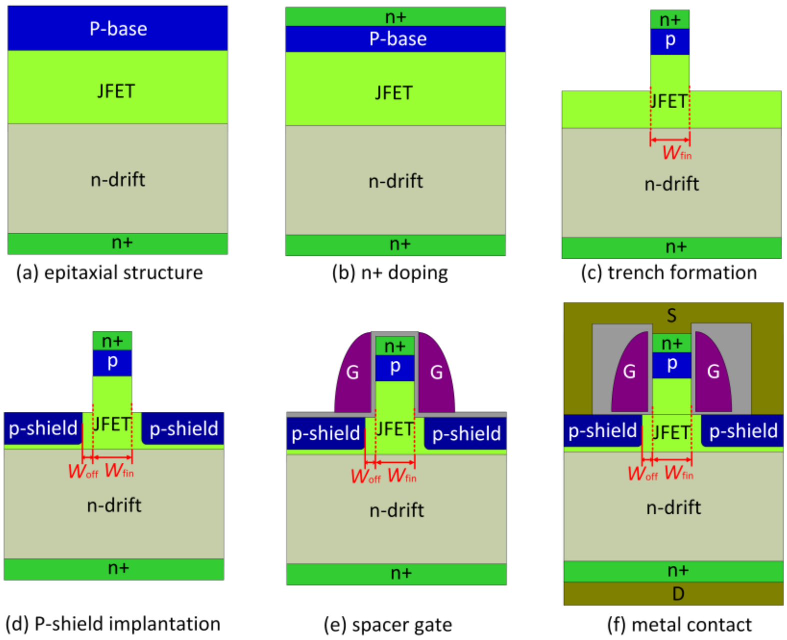

Figure 2. The fabrication process for the Fin-MOS. (**a**) Forming the first epi layer. (**b**) Forming the n+ source region. (**c**) Forming the gate trench. (**d**) Forming the p-shield region. (**e**) Spacer-gate technology is used to form the gates. (**f**) Forming the gate oxide and metal overlay.

2.4. Parameter Optimization

All three devices have different structural configurations, resulting in inconsistent cell widths. For the Trench-MOS, all the parameters are constant. For the proposed Fin-MOS, W_{fin} is a key factor affecting device performance, and it is also the first parameter we need to determine. On this basis, it is necessary to further determine the doping concentration in the base region. For the Asym-MOS and Fin-MOS devices, which feature shielded regions, the doping concentrations in the JFET regions will be optimized. Furthermore, in terms of channel mobility in the simulation, we did not set the mobility of the Asym-MOS the same as the other two types of MOSFETs, as previous studies have reported that a channel along the (11–20) face exhibits approximately twice the channel mobility (μ_{ch}) compared to that along the (−1–120) face [24,25].

Figure 3a presents the influence of W_{fin} upon BV in the proposed Fin-MOS. For the conventional SiC MOSFET, the p-base typically has a doping level of ~10^{17} cm^{-3}. Using a narrow fin-structure, junction-less MOSFETs without p-base doping (N_{PB}) are proven to be possible [34,35]. However, for N_{PB} = 0 cm^{-3}, BV is very sensitive to W_{fin}, and drops quickly at a relatively small W_{fin} because the p-base is easily punched through. With N_{PB} = 10^{17} cm^{-3}, BV is more robust, and drops more gently with W_{fin}. In this work, W_{fin} = 0.2 μm is adopted for a robust BV.

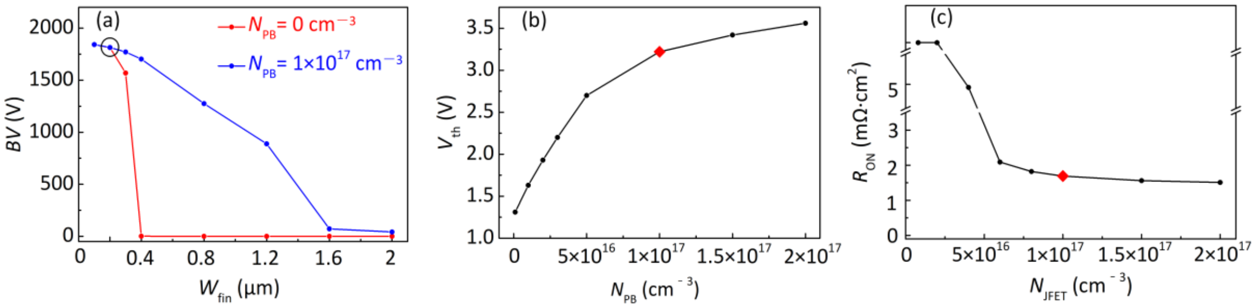

Figure 3. (**a**) The influence of W_{fin} upon BV for different N_{PB} (N_{JFET} = 1 × 10^{17} cm^{-3}) in Fin-MOS. W_{fin} = 0.2 μm is chosen as the optimized value. (**b**) The influence of N_{PB} upon V_{th} (N_{JFET} = 1 × 10^{17} cm^{-3}) in Fin-MOS (V_{DS} = 1 V). N_{PB} = 1 × 10^{17} cm^{-3} is chosen as the optimized value. (**c**) The influence of N_{JFET} upon R_{ON} for different N_{PB} (V_{GS} = 15 V). N_{JFET} = 1 × 10^{17} cm^{-3} is chosen as the optimized value.

The doping of the p-base may influence the devices' threshold voltage [14,36]. As shown in Figure 3b, the devices' threshold voltage (V_{th}) increases with the increase in N_{PB}, and gradually saturates for N_{PB} beyond 10^{17} cm^{-3}. In this work, N_{PB} = 1 × 10^{17} cm^{-3} is adopted.

For the proposed Fin-MOS, the JFET region between the adjacent p-shield regions may result in a large resistance if improperly designed. Figure 3c presents R_{ON} of the Fin-MOS as a function of N_{JFET}. R_{ON} decreases with N_{JFET}, and becomes insensitive for N_{JFET} beyond 10^{17} cm^{-3}. Therefore, N_{JFET} = 1 × 10^{17} cm^{-3} is adopted in the remaining part of the paper.

For the Asym-MOS, N_{JFET} is to be optimized. With the increasing of N_{JFET}, the depletion regions around the p-shields gradually shrink and results in a lower R_{ON}, but the shielding effect becomes weaker, which leads to a higher $E_{OX\text{-}M}$. Figure 4a shows the effects of N_{JFET} on R_{ON} and $E_{OX\text{-}M}$. R_{ON} is obtained at V_{GS} = 15 V. $E_{OX\text{-}M}$ is obtained at V_{GS} = 0 V and V_{DS} = 1200 V. In this work, N_{JFET} = 5 × 10^{16} cm^{-3} is adopted. For the Asym-MOS, the orientation of the trench channel can be adjusted in the etching process. It is reported a channel along the (11–20) face results in a channel mobility (μ_{ch}) around twice of that along the (−1–120) face [24,25]. Figure 4b shows the influence of μ_{ch} upon R_{ON}. With μ_{ch} increasing from 20 cm^2/V-s to 40 cm^2/V-s, the R_{ON} of Asym-MOS decreases from 1.98 mΩ·cm^2 to 1.72 mΩ·cm^2. In the remaining part of the paper, the μ_{ch} of Trench-MOS and Fin-MOS is set to 20 cm^2/V-s, while the μ_{ch} of Asym-MOS is set to 40 cm^2/V-s.

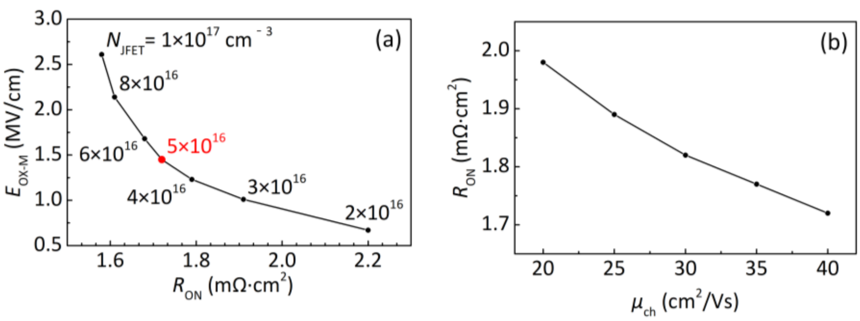

Figure 4. (**a**) The trade-off between R_{ON} and $E_{OX\text{-}M}$ (μ_{ch} = 40 cm^2/Vs) in Asym-MOS. N_{JFET} = 5 × 10^{16} cm^{-3} is chosen as the optimized value for the study in the remaining part of the letter. (**b**) The influence of μ_{ch} upon R_{ON} in Asym-MOS.

3. Investigation of Threshold Voltage Instability

As reported in the literature, a floating p-region inside a SiC MOSFET might store negative charges upon high drain voltage stress, resulting in dynamic performance instabilities [22]. As shown in Figure 5a, for the proposed Fin-MOS, the p-base is a floating p-region, and the potential negative charge storage upon high drain voltage might lead to a positive threshold voltage shift (ΔV_{th}), as observed in GaN power transistors with a floating p-region [37,38]. However, the Fin-MOS with a small W_{fin} may not face this problem because the narrow JFET region is supposed to provide a strong shielding effect to the floating p-base. To prove this, for devices with a different W_{fin}, dynamic *I*–*V* simulation is carried out using the testing waveforms in Figure 5b. A high drain voltage pulse is applied to the device to mimic the OFF-state stress in switching applications. Then, 1 µs after the drain pulse, the V_{GS} sweeps from 0 to 15 V for the dynamic transfer measurement, and the dynamic V_{th} is extracted. Figure 5c shows the influence of W_{fin} upon ΔV_{th}. When the W_{fin} is larger than 1 µm, ΔV_{th} increases sharply.

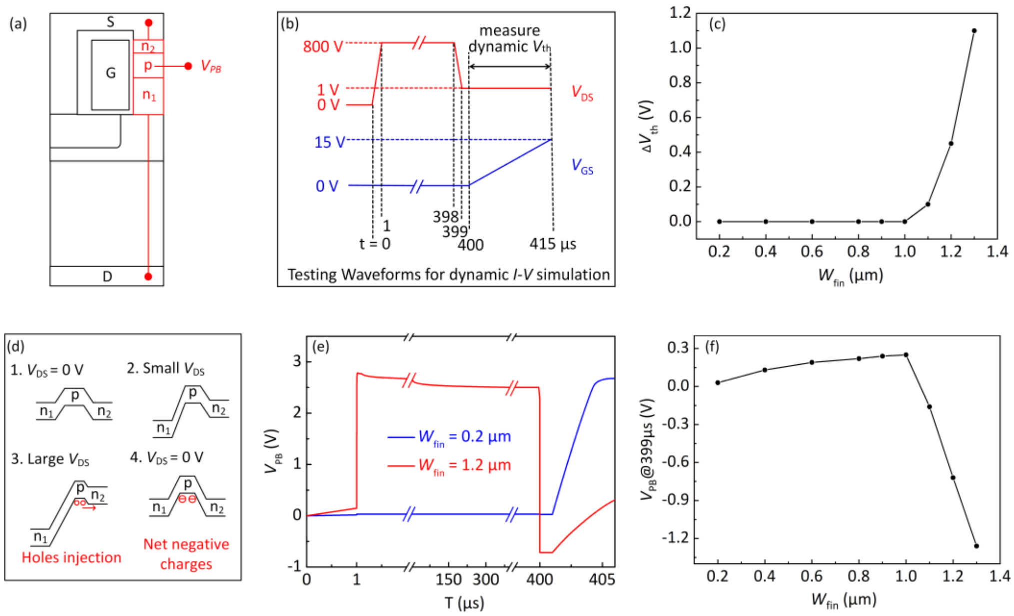

Figure 5. Investigation of threshold voltage instability of the Fin-MOS. (**a**) The Fin-MOS structure with the parasitic n-p-n structure highlighted. (**b**) Testing waveforms for the dynamic *I*–*V* simulations. (**c**) The simulated ΔV_{th} (V_{th} after 800 V drain pulse minus V_{th} after 0 V drain pulse) as a function of W_{fin}. (**d**) Illustration of the charge storage effect in floating p-base. (**e**) V_{PB} waveforms for Fin-MOS with W_{fin} = 1.2 µm and Fin-MOS with W_{fin} = 0.2 µm. (**f**) The influence of W_{fin} upon V_{PB}.

Figure 5d illustrates the charge storage process in the floating p-base of the Fin-MOS. Upon high V_{DS}, the p-n junction formed by the p-base and its upper n-region turns on, and holes will be injected into the upper n-region. After the high V_{DS} is removed, the holes cannot flow back to the p-base, leaving net negative charges, and causing a dynamic threshold voltage drift.

The above analysis can be further reflected and proven by the changes in the voltage of the floating p-region (V_{PB}). Figure 5e shows the simulated waveforms of V_{PB} of two devices with W_{fin} = 1.2 µm and 0.2 µm. When W_{fin} = 1.2 µm, V_{PB} rises to 2.8 V as V_{DS} is swept from 0 V to 800 V, which turns on the p-n junction; therefore, holes are injected out of the p-base. After the drain pulse, V_{PB} drop to −0.72 V, which proves the storage of net negative charges in the p-base. However, the charge storage effect is not observed for the device with W_{fin} = 0.2 µm, since the p-base is well-shielded. Figure 5f plots V_{PB} at 399 µs (immediately after drain pulse) as a function of W_{fin}. When W_{fin} is larger than 1 µm, V_{PB} becomes negative. The result agrees with Figure 5c. Therefore, for the Fin-MOS with

W_{fin} = 0.2 μm, the charge storage effect and the consequent dynamic threshold voltage shift are negligible.

4. Device Characteristics

Figure 6 shows the *I*–*V* characteristics of the three SiC MOSFETs. The Trench-MOS boasts the lowest R_{ON} of 1.61 mΩ·cm^2 because of the high channel density. The Asym-MOS has a much lower channel density than the Trench-MOS, and it still has a low R_{ON} of 1.72 mΩ·cm^2 because of the high channel mobility of 40 cm^2/V-s being adopted. Though a low channel mobility of 20 cm^2/V-s is being adopted, the Fin-MOS has a low R_{ON} of 1.71 mΩ·cm^2, owing to the high channel density. The slight increase in R_{ON} compared to the Trench-MOS is caused by the JFET resistance when the current passes though the aperture between p-shields. All the studied MOSFETs present a breakdown voltage beyond 1500 V. The Fin-MOS boasts the highest breakdown voltage because the distances beyond p-shield regions are reduced, which smooths the electric field distribution. Furthermore, though with a higher channel density than the Asym-MOS, the saturation current of the Fin-MOS is the lowest among the three, as a result of its narrow JFET region.

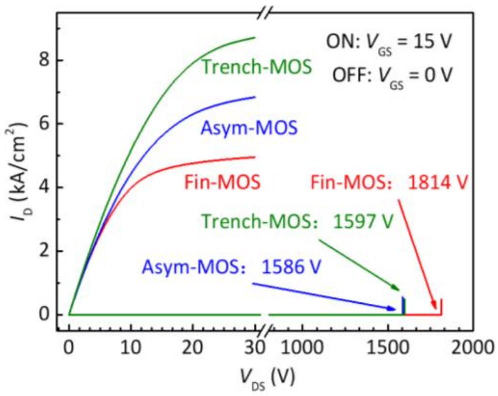

Figure 6. The *I*–*V* characteristics of the three SiC MOSFETs.

Figure 7 shows the OFF-state electric field distributions at V_{DS} = 1200 V in a half-cell of the studied MOSFETs. For the Trench-MOS, $E_{OX\text{-}M}$ at the trench corner is as high as 7.43 MV/cm, which puts a severe threat to the device's long-term reliability. For the Asym-MOS, $E_{OX\text{-}M}$ drops down to 1.45 MV/cm with the shielding effect by the grounded p-shield regions. For the proposed Fin-MOS, because of its narrow JFET region, the gate shielding effect is strengthened so that the E_{OX} of 0.77 MV/cm is lower than that in the Asym-MOS.

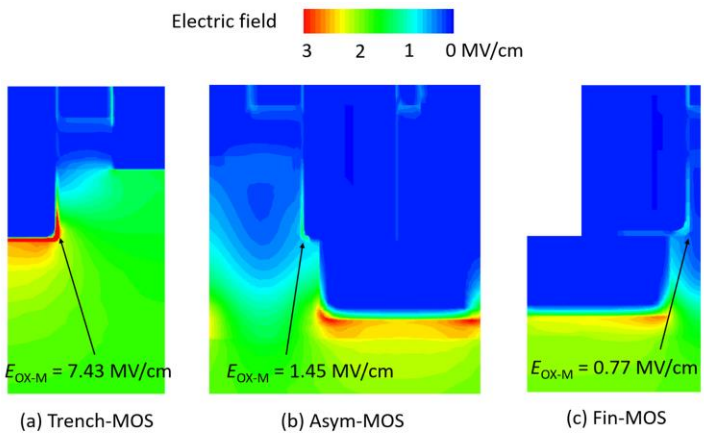

Figure 7. The OFF-state electric field distributions at V_{DS} = 1200 V in a half-cell of (**a**) the Trench-MOS, a cell of (**b**) the Asym-MOS, and a half cell of (**c**) the Fin-MOS.

Reverse transfer capacitance (C_{rss}) is one of the important dynamic characteristics of the power devices [39,40]. Figure 8 shows the C_{rss} of the three SiC MOSFETs. The Trench-MOS suffers the largest C_{rss}. For the Asym-MOS, the p-shield regions provide a shield to the gate, resulting in a lower C_{rss}. For the proposed Fin-MOS with W_{fin} = 0.2 µm, the p-shield provides the strongest shield to the gate, leading to the lowest C_{rss} among the studied MOSFETs.

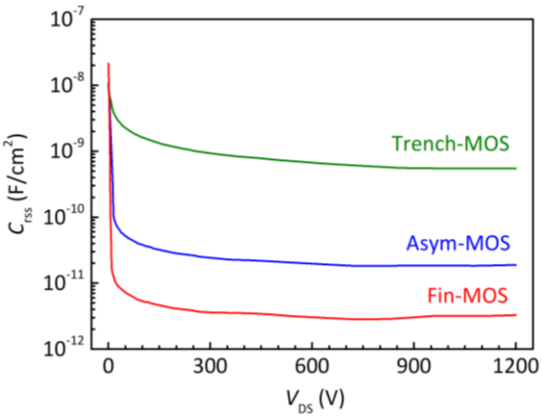

Figure 8. Reverse transfer capacitance (C_{rss}) of the studied MOSFETs.

Figure 9 shows the V_{GS}–Q_G curves of the three SiC MOSFETs. The test circuit is shown in Figure 9b. For 1200 V devices, the operating range of V_{DS} typically falls within 0–800 V [9,16]; for the Trench-MOS, it is Q_G = 2093 nC/cm^2 and Q_{GD} = 1063 nC/cm^2; for the Asym-MOS, it is Q_G = 1424 nC/cm^2 and Q_{GD} = 107 nC/cm^2; while, for the Fin-MOS, it is Q_G = 1282 nC/cm^2 and Q_{GD} = 62 nC/cm^2. For comparison, the main characteristics of the three SiC MOSFETs are listed in Table 1. The Fin-MOS boasts the highest breakdown voltage and the lowest $E_{OX\text{-}M}$, C_{rss}, Q_G, Q_{GD}, and I_{sat}. At the same time, the Fin-MOS achieves a comparable low R_{ON}.

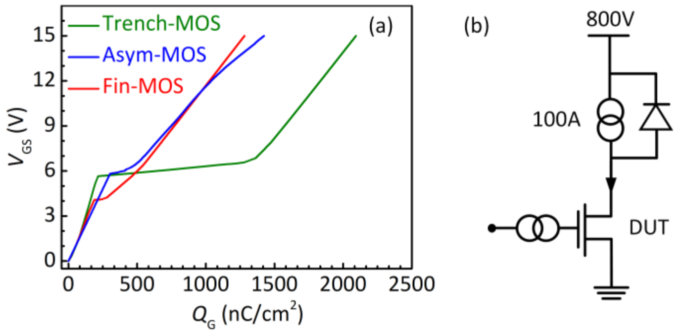

Figure 9. (**a**) V_{GS}–Q_G curves of the studied MOSFETs. (**b**) The test circuit for the gate charge characteristics. For the Trench-MOS, Q_G = 2093 nC/cm^2 and Q_{GD} = 1063 nC/cm^2, for the Asym-MOS, Q_G = 1424 nC/cm^2 and Q_{GD} = 107 nC/cm^2, while, for the Fin-MOS, Q_G = 1282 nC/cm^2 and Q_{GD} = 62 nC/cm^2.

Additionally, to demonstrate the advantages of the proposed SiC fin-channel MOSFET, the dynamic and static figures of merit (FOMs) for the three devices are shown in Table 1. It is found that the proposed Fin-MOS exhibits the highest static FOM and the lowest dynamic FOM, further highlighting its favorable characteristics.

Table 1. Characteristic of the Trench-MOS, the Asym-MOS, and the Fin-MOS.

	Trench-MOS	Asym-MOS	Fin-MOS	Unit
μ_{ch}	20	40	20	cm^2/Vs
R_{ON} [a]	1.61	1.72	1.71	$m\Omega \cdot cm^2$
BV	1597	1586	1814	V
Static FOM [b]	1584	1462	1924	MW/cm^2
$E_{OX\text{-}M}$ [c]	7.43	1.45	0.77	MV/cm
V_{th}	5.17	5.13	3.22	V
I_{sat} [d]	14.09	8.25	6.56	KA/cm^2
C_{rss} [e]	678	19.8	3.1	pF/cm^2
Q_G	2093	1424	1282	nC/cm^2
Q_{GD}	1063	107	62	nC/cm^2
Dynamic FOM [f]	1711	184	106	$m\Omega \cdot nC$

[a] R_{ON} at V_{GS} = 15 V. [b] BV^2/R_{ON}. [c] $E_{OX\text{-}M}$ at V_{DS} = 1200 V. [d] I_{sat} at V_{DS} = 800 V. [e] C_{rss} at V_{DS} = 600 V. [f] $Q_{GD} \cdot R_{ON}$.

5. Conclusions

For conventional trench MOSFETs, there is no shielding region and, for this reason, the devices may face many problems upon high drain voltage. In this work, a SiC fin-channel MOSFET (Fin-MOS) is proposed for an enhanced gate shielding effect. The gates are placed on each side of the narrow fin-channel region, while grounded p-shield regions below the gates provide a strong shielding effect. Sentaurus TCAD simulations are carried out to optimize the parameters. For the Fin-MOS, W_{fin} = 0.2 μm is adopted for a robust *BV*. Then, $N_{PB} = 1 \times 10^{17}$ cm^{-3} is adopted because V_{th} increases with the increase in N_{PB}, and gradually saturates for N_{PB} beyond 10^{17} cm^{-3}. Finally, $N_{JFET} = 1 \times 10^{17}$ cm^{-3} is adopted because R_{ON} decreases with N_{JFET}, and becomes insensitive for N_{JFET} beyond 10^{17} cm^{-3}. For the Asym-MOS, $N_{JFET} = 5 \times 10^{16}$ cm^{-3} is adopted and μ_{ch} is set to 40 cm^2/V-s.

For a narrow fin-channel region, there is difficulty in forming an Ohmic contact to the p-base. However, a floating p-base might potentially store negative charges upon high drain voltage and, thus, causes threshold voltage instabilities. In this work, we proposed a Fin-MOS structure model with the parasitic n-p-n structure to investigate the threshold voltage instability of the Fin-MOS. With the help of a simulation, we revealed, in the proposed Fin-MOS with W_{fin} = 0.2 μm, as a result of the enhanced shielding effect, the charge storage induced instability is negligible. However, when W_{fin} is larger than 1 μm, devices will still face the problem of threshold voltage instabilities.

Finally, the static and dynamic characteristics of the three devices were characterized. Compared to the conventional trench MOSFET (Trench-MOS) and the asymmetric trench MOSFET (Asym-MOS), the Fin-MOS boasts the best OFF-state characteristic, and the lowest reverse transfer capacitance and saturation current. Moreover, the Fin-MOS keeps a similar low ON-resistance. Therefore, the Fin-MOS is a promising approach to realize high-performance and SiC power-switching transistors and help to improve the dynamic stability of devices in high-voltage switch applications.

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