

Article

# CMOS Design of Chaotic Systems Using Biquadratic OTA-C Filters

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**Abstract:** This manuscript shows the CMOS design of Lorenz systems using operational transconductance amplifiers (OTAs). Two Lorenz systems are then synchronized in a master–slave topology and used to implement a CMOS secure communication system. The contribution is devoted to the correct design of first- and second-order OTA-C filters, using 180 nm CMOS technology, to guarantee chaotic behavior. First, Simulink is used to simulate a secure communication system using two Lorenz systems connected in a master–slave topology, which is tested using sinusoidal signals that are masked by chaotic signals. Second, the Lorenz systems are scaled to have amplitudes of the state variables below 1 Volt, to allow for CMOS design using OTA-C filters. The transconductances of the OTAs are tuned to accomplish a Laplace transfer function. In this manner, this work highlights the design of a second-order CMOS OTA-C filter, whose damping factor is tuned to generate appropriate chaotic behavior. Finally, chaotic masking is performed by designing a whole CMOS secure communication system by using OTA-C based Lorenz systems, and its SPICE simulation results show its appropriateness for hardware security applications.

**Keywords:** chaos; Lorenz system; secure communication system; OTA-C filter; biquadratic filter; damping factor; SPICE



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## 1. Introduction

Chaos is a complex and seemingly disordered phenomenon that was introduced by meteorologist Edward Lorenz in proposing a mathematical model consisting of three ordinary differential equations (ODEs) [1]. Up to now, researchers know that a chaotic system is highly sensitive to slight variations in the initial conditions, which can lead the solutions of ODEs to have completely different trajectories over time. In this manner, despite its apparent disorder, chaos has at least three remarkable characteristics, i.e., high sensitivity to initial conditions, lack of periodicity, and deterministic behavior, which means that its time evolution is completely determined by its mathematical model. In the continuous-time domain, a chaotic system must have at least three ODEs, as for the case of the Lorenz system [2], which is one of the most famous examples of chaotic systems.

Chaotic systems have proven to be useful in the design of secure communications. For instance, the authors in [3] detail the development of chaos-based digital communication systems, including coherent and non-coherent systems. In this work, a secure communication system is designed by applying the synchronization technique introduced by Pecora and Carroll [4], where two chaotic systems, such as Lorenz systems, can be synchronized to perform a chaotic masking of information. This work uses two Lorenz systems that are synchronized in a master–slave topology to mask data. Additionally, one can use other chaotic systems, for example, the autonomous electronic chaos generator, which comprises a bipolar junction transistor, a resistor, two inductors, and one capacitor [5]; chaotic maps designed with four transistors [6,7]; or other chaotic systems

designed with different building blocks using CMOS technology. Examples of the latter include the work in [8], which uses a modified voltage differencing voltage transconductance amplifier; ref. [9], which uses a voltage differencing inverted buffered amplifier; refs. [10,11], which use a modified voltage differencing current conveyor; ref. [12], which uses a current-controlled current conveyor feedback amplifier; ref. [13], which uses a single extra-X current-controlled current conveyor; ref. [14], which uses a voltage differencing gain amplifier; ref. [15], which uses cross-coupled inverter rings; and [16], which uses operational amplifiers and multipliers. Despite the huge number of active devices, this work shows the suitability of operational transconductance amplifiers (OTAs) to design biquadratic filters that are tuned to implement CMOS chaos generators.

The CMOS design of OTAs is not a trivial task, especially when the target is to develop low-voltage and low-power circuit applications. In designing chaos generators, another important device is the CMOS multiplier, for which a good tutorial was introduced by Han and Sanchez-Sinencio [17], where the authors highlight that the multiplier is used not only as a computational building block but also as a programming element in systems such as filters and neural networks, and as a mixer/modulator in communication systems. Regarding OTA design, recent works emphasize its CMOS implementation, as in [18], where an OTA-based meminductor simulator circuit is introduced, or in [19], where a simple realization of the meminductor emulator using two OTAs and two capacitors is presented. In designing chaotic systems, active filters and those implemented with OTAs could be required. Some related works on OTA-C filters are the following: the authors in [20] show two new first-order universal active filter configurations employing OTAs and grounded capacitors; in [21], the authors present a biquadratic filter using one dual-output OTA, three single-output OTAs, and two grounded capacitors to derive a new quadrature oscillator with independent control of the oscillation frequency and the oscillation condition; the authors in [22] present an independently tunable five-input and three-output biquadratic filter using five single-ended output OTAs and two grounded capacitors; and the authors in [23] present an OTA-C filter for biomedical applications that consists of a cascade of biquadratic sections, each configured via a serial-peripheral-interface circuit embedded with nonvolatile memories to provide low-pass or bandpass response. An implementation of an OTA-C filter using commercially available discrete components was given in [24]; an OTA-based filter with low sensitivity operating at high frequency was given in [25]; OTA-based biquadratic filters with electronically reconfigurable transfer functions were given in [26]; and biquadratic OTA-C and universal filters with tunable pole-Q were introduced in [27]. One can find more works related to OTA-C filters, but in all cases, the topologies are quite similar to the ones given in the tutorial [28]. The outstanding challenge is the design of integrated circuits for low-voltage and low-power applications, as in the case studies given in [29–31].

The remaining sections are organized as follows: Section 2 shows the mathematical model and analysis of Lorenz systems and synchronization in a master–slave topology using Simulink to appreciate an application in the chaotic masking of sinusoidal signals. Section 3 shows the scaling of the Lorenz system to obtain amplitudes of the state variables within  $\pm 1$  Volt to allow for CMOS design using 180 nm integrated circuit technology; it also shows the macro-modeling of the OTA-C blocks that implement first- and second-order active filters. Section 4 pays special attention to the design of the OTAs, detailing the tuning of the transconductances, and the design of the OTA-C biquad filters, the damping factor of which is tuned to generate chaotic behavior. Section 5 shows the design of a CMOS secure communication system that synchronizes two CMOS Lorenz systems and masks a sinusoidal signal, which is recovered after having been encrypted by chaotic signals. Finally, the conclusions are provided in Section 6.

## 2. Chaotic Masking Using Lorenz Systems

In his seminal work [1], Lorenz introduced a mathematical model to describe how the air behaves and evolves in the atmosphere under small changes. This model helped him

to discover that chaotic behavior can be modeled by three ODEs and that their solutions highly depend and are highly sensitive to the initial conditions. Since then, such a model has been well known as Lorenz system and its attractor is said to have a butterfly effect. Equation (1) shows the mathematical model of the Lorenz system, which generates chaotic behavior by setting the coefficients as [1]  $\sigma = 10$ ,  $\rho = 28$ , and  $\beta = 8/3$  and by using the initial conditions of  $(x_0, y_0, z_0) = (0.1, 0.1, 0.1)$ .

$$\begin{aligned} \dot{x} &= \sigma(y - x), \\ \dot{y} &= x(\rho - z) - y, \\ \dot{z} &= xy - \beta z. \end{aligned} \tag{1}$$

The high-level simulation of the chaotic Lorenz system can be performed by using Simulink, whose equations in the frequency domain are given in (2). The block description is sketched in Figure 1, where it can be appreciated that the equations are synthesized using addition, subtraction, multiplication, and gain blocks, while three  $1/s$  integrator blocks are used to obtain each state variable,  $x$ ,  $y$ , and  $z$ . The simulated times series for each state variable can be appreciated in Figure 2, while the chaotic attractor in a 3D space is shown in Figure 3.

$$\begin{aligned} X(s) &= \frac{1}{s}(\sigma(Y(s) - X(s))), \\ Y(s) &= \frac{1}{s}(X(s)(\rho - Z(s)) - Y(s)), \\ Z(s) &= \frac{1}{s}(X(s) * Y(s) - \beta Z(s)). \end{aligned} \tag{2}$$

Simulink is a useful software application to test the synchronization of two identical chaotic systems. Let us consider two Lorenz systems to perform their synchronization by applying the Pecora and Carroll technique. In this case, a master–slave topology can be synthesized from (3) (denoting the master system) and (4) (denoting the slave system), where it can be appreciated that one of the variables, e.g.,  $x_m$ , of the master system is used as a coupling signal to control and synchronize the slave system, so that  $x_s = x_m$ . This coupling signal is adjusted over time to make both systems evolve similarly, thus achieving the synchronization of their chaotic behaviors.

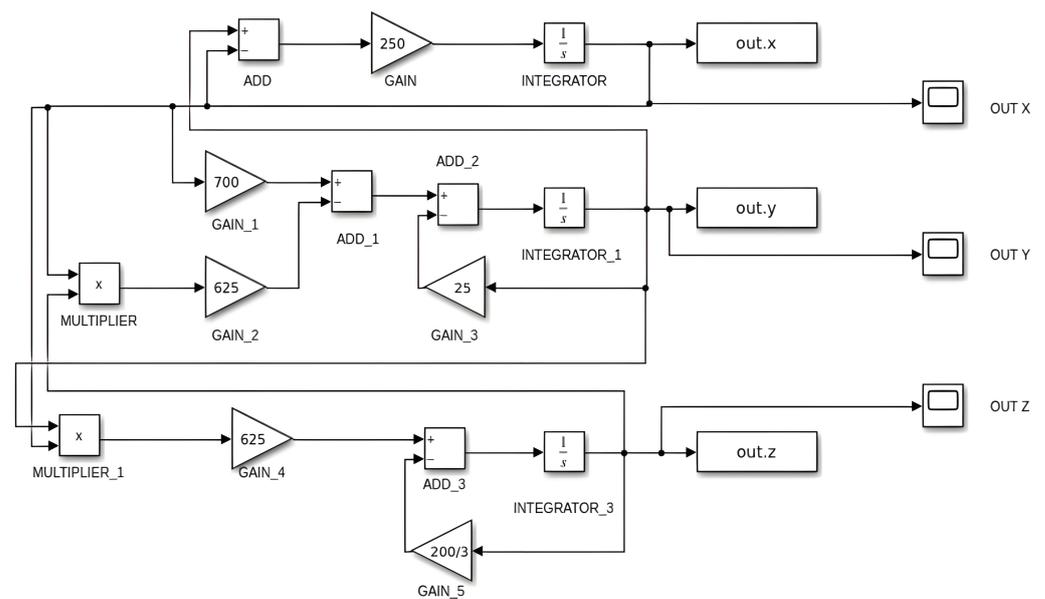


Figure 1. Implementation of the Lorenz oscillator in Matlab/Simulink from (2).

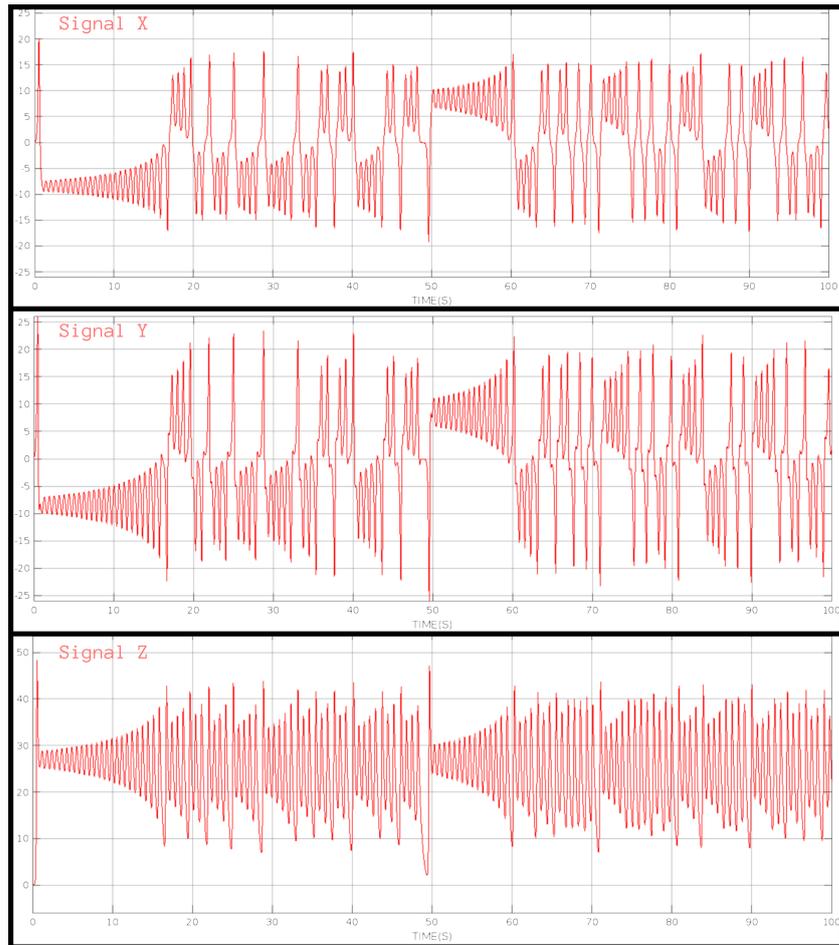


Figure 2. Time series of x, y, and z of the Lorenz system.

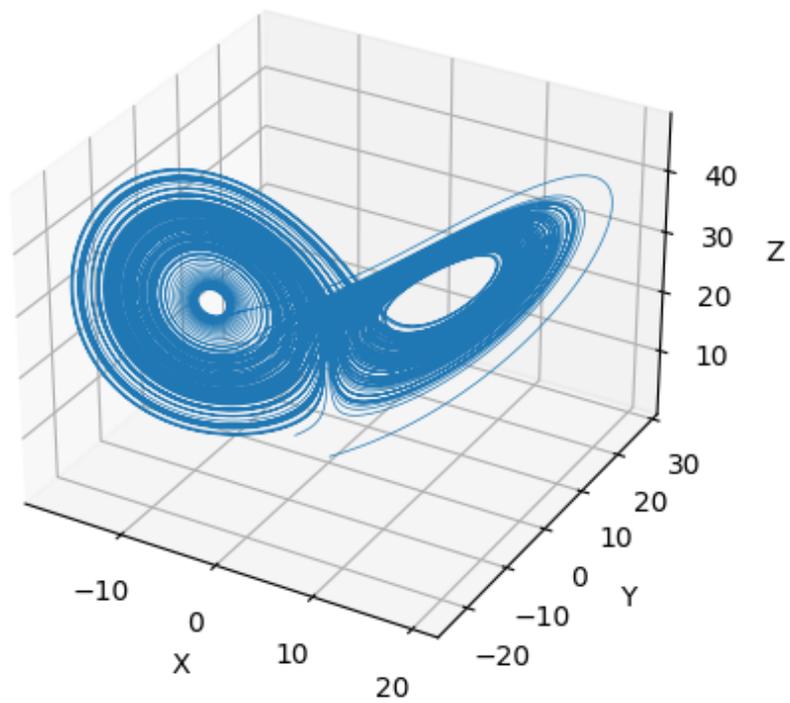


Figure 3. Lorenz attractor in 3D space.

$$\begin{aligned} \dot{x}_m &= \sigma(y_m - x_m), \\ \dot{y}_m &= x_m(\rho - z_m) - y_m, \\ \dot{z}_m &= x_m y_m - \beta z_m, \end{aligned} \tag{3}$$

$$\begin{aligned} \dot{y}_s &= x_m(\rho - z_s) - y_s, \\ \dot{z}_s &= x_m y_s - \beta z_s. \end{aligned} \tag{4}$$

As one can infer, Equations (3) and (4) can be described in Simulink, as shown in Figure 4. The blocks of the master system (*m*) are distinguished from those of the synchronized slave system (*s*), but according to (3) and (4), state variable  $x_s$  must be taken from the master block, i.e.,  $x_m = x_s$ . As the synchronization is ideal, i.e., using the mathematical equations given in (3) and (4), the phase plots between the state variables of the master and slave systems form a line with a 45° slope. This synchronized scheme can be used to implement a secure communication system, as the one shown in Figure 5.

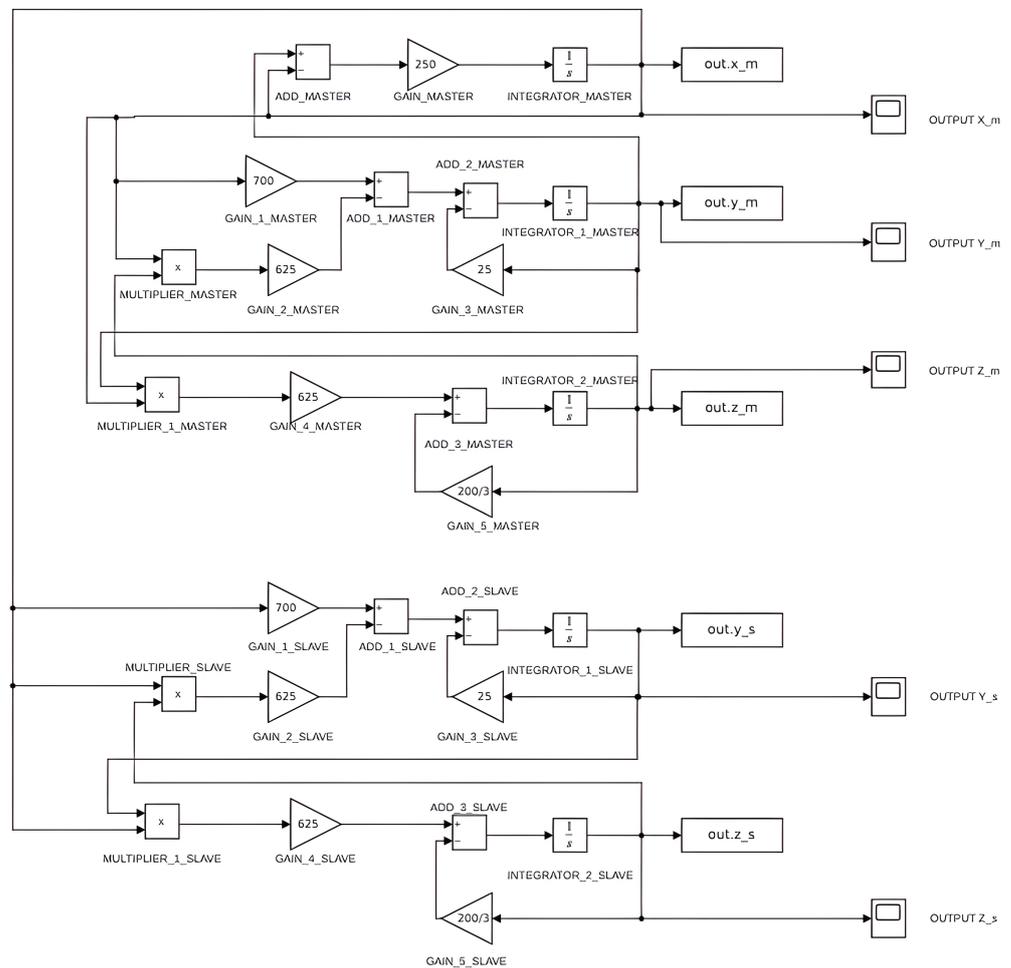


Figure 4. Implementation of the synchronization technique in Matlab/Simulink.

Chaotic masking by using two synchronized systems in a master–slave topology can be performed as shown in Figure 5. The upper blocks describe the masking of chaos ( $Y_m$ ) with the transmitted signal and the recovery of the original signal by subtracting the chaotic time series ( $Y_s$ ). In this case, channel  $B(t)$  encrypts the transmitted signal ( $A(t)$ ), and the recovered one ( $C(t)$ ) must be the same, i.e.,  $C(t) = A(t)$ . Let us consider a test signal as the sum of three sine waves, as given in (5), to which the chaos of the master system ( $Y_m$ ) is added, as given in (6). In this case, channel  $B(t)$  encrypts the information being

transmitted; afterwards, the latter can be recovered by subtracting the chaotic signal in the slave system, with  $Y_s$  behaving as  $Y_m$ , thus generating the equation given in (7). In the end, as the master and slave systems are synchronized,  $Y_m = Y_s$ , and finally,  $C(t) = A(t)$ .

$$A(t) = 0.1\sin(100t) + 0.1\sin(500t) + 0.1\sin(500t) \tag{5}$$

$$B(t) = 0.1\sin(100t) + 0.1\sin(500t) + 0.1\sin(500t) + Y_m \tag{6}$$

$$C(t) = (0.1\sin(100t) + 0.1\sin(500t) + 0.1\sin(500t) + Y_m) - Y_s \tag{7}$$

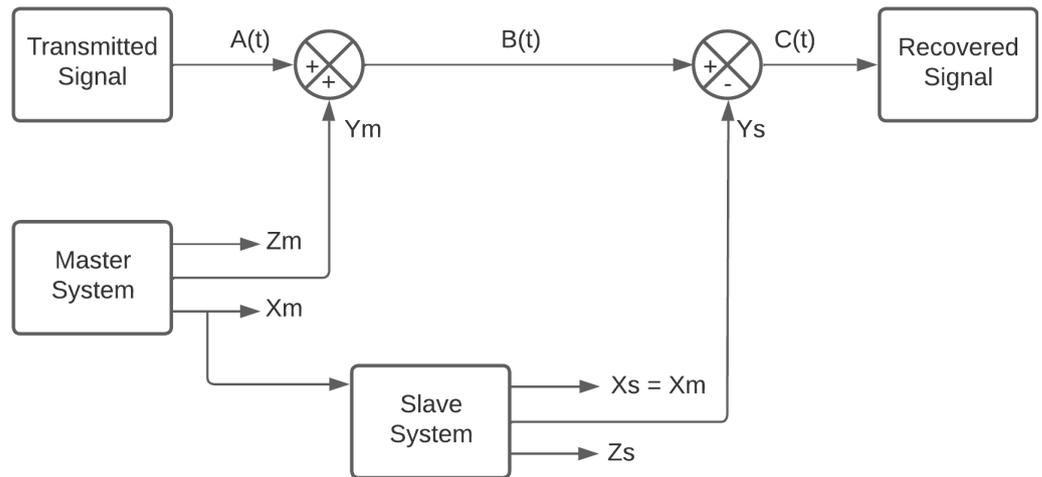


Figure 5. Chaotic masking by using two synchronized systems in a master–slave topology.

The test signal given in (5), consisting of the sum of three sine signals of different frequencies and equal amplitude, is shown in Figure 6. This signal is masked with chaos, so that the channel is described by (6), as shown in Figure 7. If the slave follows the master system with zero error, then the recovered signal can be expressed by (7), as shown in Figure 8.

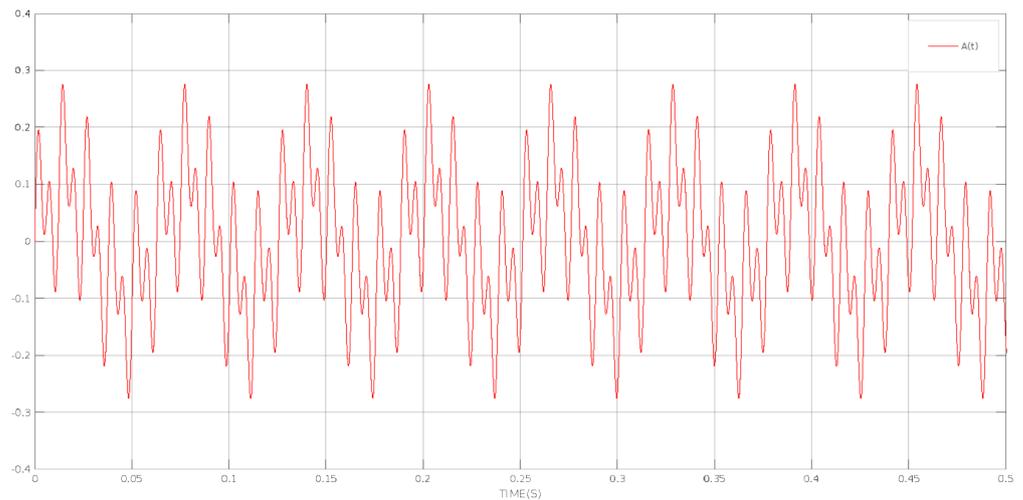


Figure 6. Test signal given in (5), consisting of the sum of three sine signals of different frequency and equal amplitude.

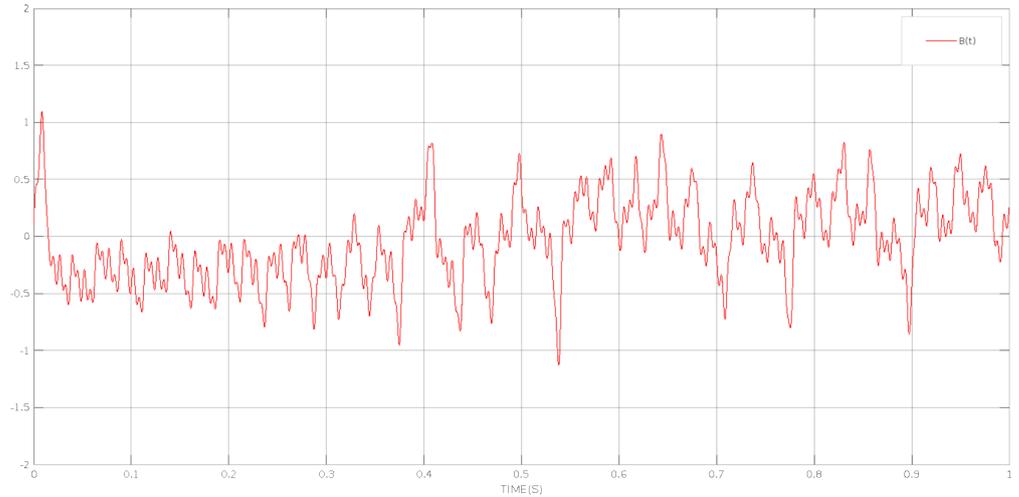


Figure 7. Chaotic masking described by (6).

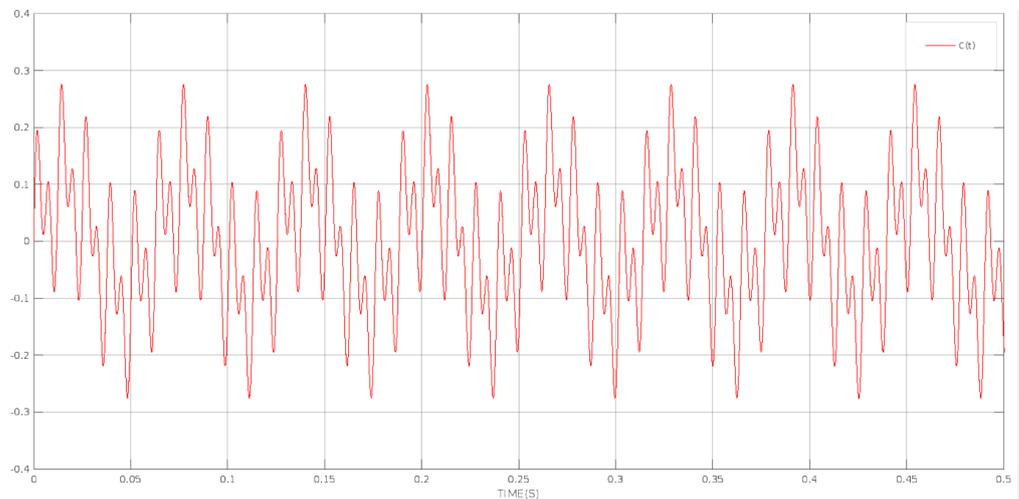


Figure 8. Recovered signal described by (7).

### 3. Scaling of Lorenz System and Simulation Using OTA-C Filters

The CMOS design using integrated circuit technology imposes restrictions on the amplitudes of the signals. In this work, Lorenz systems are designed using 180 nm integrated circuit technology from UMC. Both MOSFET models of the P- and N-channels are nm180\_reg\_18\_V124 of level 49. In this manner, the mathematical model is scaled to have amplitudes of the state variables within a range of  $\pm 1$  Volt. In principle, the scaling process is performed by a variable change for each state variable, until one finds the updated coefficient values that allow for CMOS design. In this work, the scaled system of equations for Lorenz systems in the Laplace domain is given in (8). One can see that the Laplace transform of the multiplication of two variables in the time domain produces the convolution of those variables; in this case, the two products are described by  $X(s) * Z(s)$  and  $X(s) * Y(s)$ .

$$\begin{aligned}
 sX(s) &= 10Y(s) - 10X(s), \\
 sY(s) &= 28X(s) - 400X(s) * Z(s) - Y(s), \\
 sZ(s) &= 400X(s) * Y(s) - \frac{8}{3}Z(s).
 \end{aligned}
 \tag{8}$$

From this system of equations, the manipulation of each state variable can lead to associate transfer functions to first- and second-order (biquadratic) active filters. For the

case of state variable  $X(s)$ , it can be associated to a first-order low-pass filter, as shown in (9).

$$X(s) = \left( \frac{10}{s+10} \right) Y(s). \tag{9}$$

For the case of  $Y(s)$ , it also results in associating low-pass filters that multiply one state variable or the convolution of two of them, as shown in (10).

$$Y(s) = \left( \frac{28}{s+1} \right) X(s) - \left( \frac{400}{s+1} \right) X(s) * Z(s). \tag{10}$$

For the case of  $Z(s)$ , one can associate (11). However, as  $X(s)$  is given in (9), one can derive an equation that includes a transfer function equivalent to a biquadratic active filter, as given in (12), which also performs the convolution  $Y(s) * Y(s)$ .

$$Z(s) = \left( \frac{400}{s+8/3} \right) X(s) * Y(s), \tag{11}$$

$$Z(s) = \left( \frac{4000}{s^2 + \frac{38}{3}s + \frac{80}{3}} \right) Y(s) * Y(s). \tag{12}$$

Equations (9), (10), and (12) can be simulated as the block description shown in Figure 9, which shows the labels of the three state variables and the first- and second-order (biquadratic) transfer functions, which are designed with OTA-C filters herein.

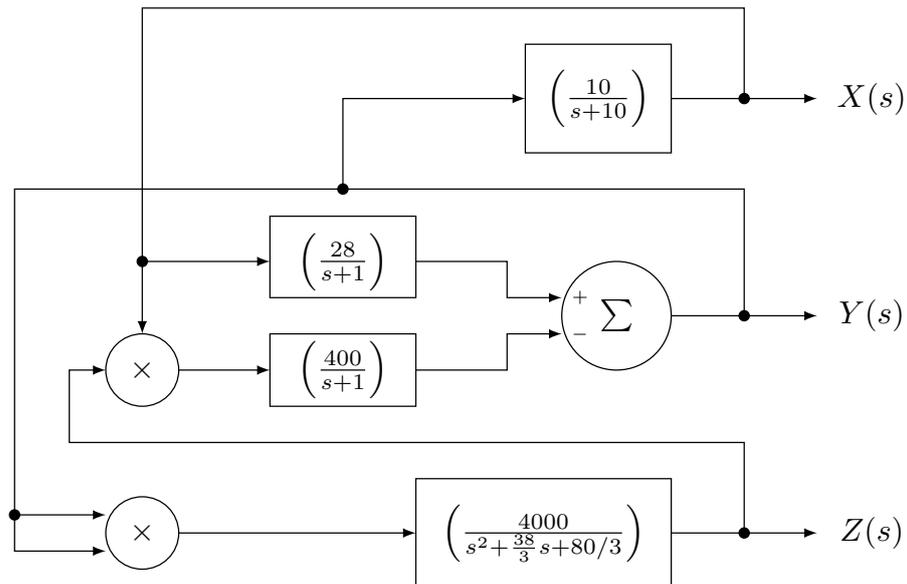


Figure 9. Block diagram description associated to Equations (9), (10), and (12).

As shown in Figure 9, the convolution operations can be performed using a multiplier circuit, which can be designed with CMOS technology, as already shown in the tutorial given in [17]. In the same manner, the transfer functions can be associated to active filters that can be designed with OTA-C topologies, as shown in the tutorial [28]. The integrator based on OTA-C is shown in Figure 10. In this case, the transconductance of the OTAs and capacitance values can be calculated from the transfer function in voltage mode given at the bottom of the figure.

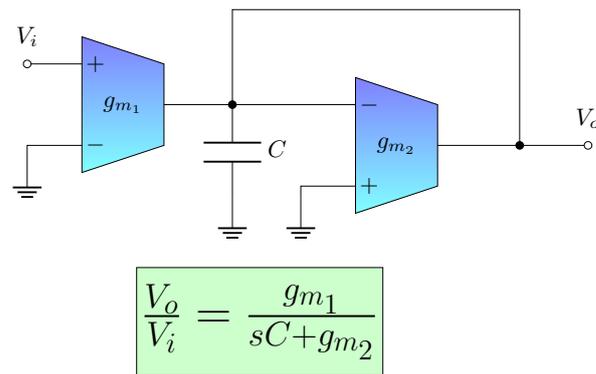


Figure 10. Structure of an adjustable integrator OTA-C circuit in voltage-mode operation.

The block diagram shown in Figure 9 can be macro-modeled using integrators, multipliers, and OTA-C active filter topologies to generate the design shown in Figure 11. It can be appreciated that Figure 9 embeds four transfer functions whose OTA-C topologies require the values of transconductances ( $g_m$ ) and capacitances that must be suitable for CMOS design. Table 1 lists the values of the transconductances and capacitances associated to CMOS first- and second-order active filters.

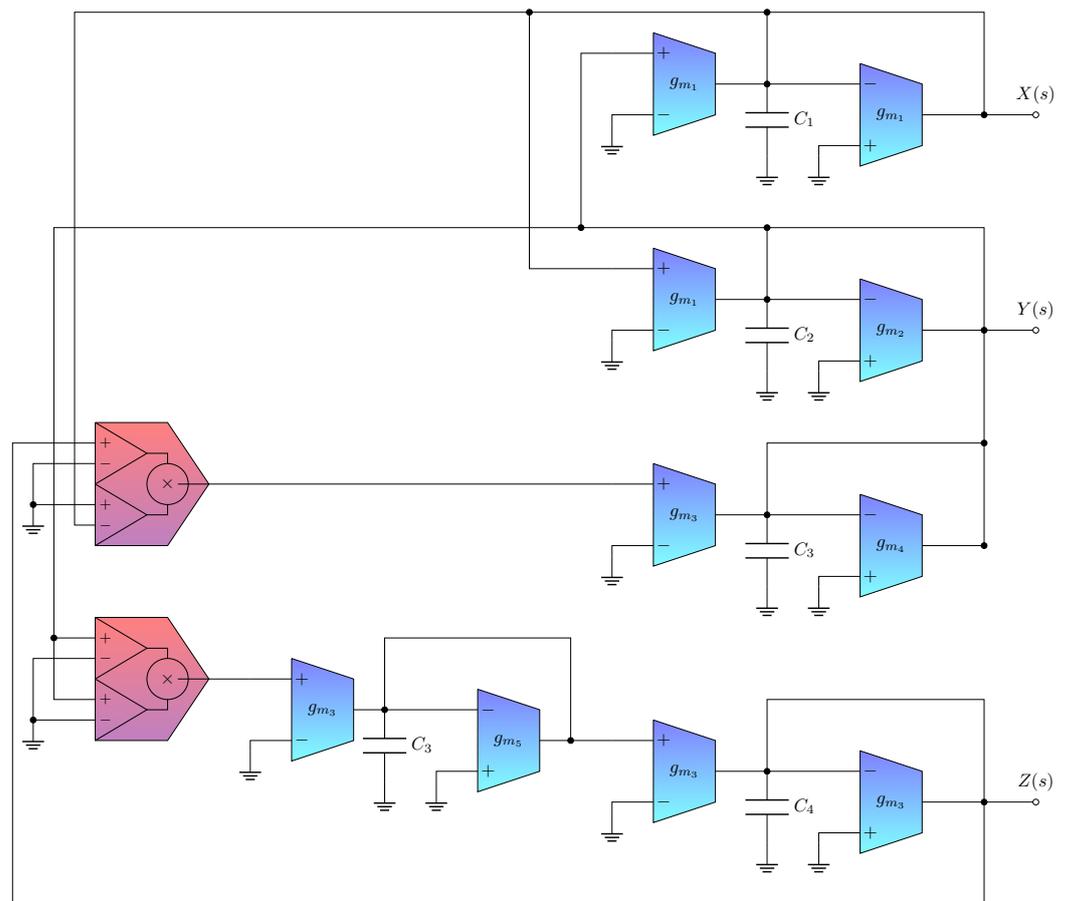


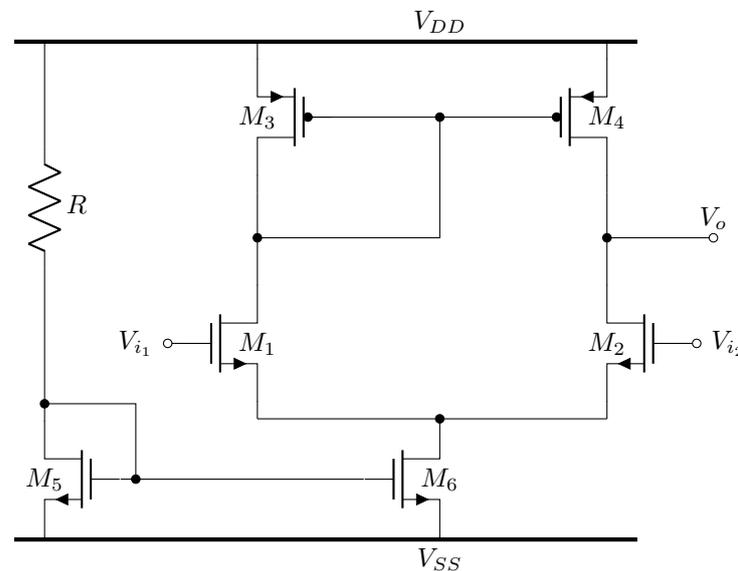
Figure 11. Macro-modeling the block description shown in Figure 9 by using multipliers, integrators, and OTA-C active filter topologies.

**Table 1.** Transconductance ( $g_m$ ) and capacitance values to accomplish each transfer function shown in Figure 9, which are designed with OTA-C topologies as shown in Figure 11.

Active Filter	$g_m$ [ $\mu\text{S}$ ]	Capacitance [ $\mu\text{F}$ ]
$\frac{10}{s+10}$	$g_{m1} = 164.44$	$C_1 = 16.44$
$\frac{28}{s+1}$	$g_{m1} = 164.44, g_{m2} = 5.87$	$C_2 = 5.87$
$\frac{400}{s+1}$	$g_{m3} = 500, g_{m4} = 1.25$	$C_3 = 1.25$
$\frac{4000}{s+1}$	$g_{m3} = 500, g_{m5} = 3.32$	$C_4 = 50$
$\frac{10}{s^2+38/3s+80/3}$		

#### 4. Design of OTA-C Biquad Filters

To accomplish each of the macro-modeling specifications of the OTA-C topologies, it is necessary to design five different transconductance ( $g_m$ ) values. These  $g_m$  must be suitable for the four active OTA-C filters listed in Table 1. For instance, the first of the OTAs will have the schematic structure shown in Figure 12, which is taken from [32], in order to achieve  $g_m \approx 164.44 \mu\text{S}$ . After sizing the MOSFETs, the width (W) and length (L) of the channel of each transistor and the resistor value are listed in Table 2.



**Figure 12.** Design of an OTA to obtain  $g_m \approx 164.44 \mu\text{S}$ .

**Table 2.** W/L values of each MOSFET for the OTA shown in Figure 12, in order to obtain  $g_m \approx 164.44 \mu\text{S}$ .

MOSFET	W/L Dimensions [ $\mu\text{m}$ ]	Value [ $\text{k}\Omega$ ]
$M_1, M_2$	6/0.54	-
$M_3, M_4$	24/0.54	-
$M_5, M_6$	12/0.54	-
R	-	75

For the case of obtaining  $g_{m2}$ ,  $g_{m4}$ , and  $g_{m5}$ , one can use a variant of the OTA shown in Figure 12. Briefly, the updated topology includes source degeneration using resistors, as detailed in [33] and shown in Figure 13, where  $R_1 = R_2$ , which can be varied to tune the desired  $g_m$  value. Some authors just vary the current bias, as shown in [34]; however, the transconductance may become nonlinear, so the best solution herein is the use of source degeneration topologies.

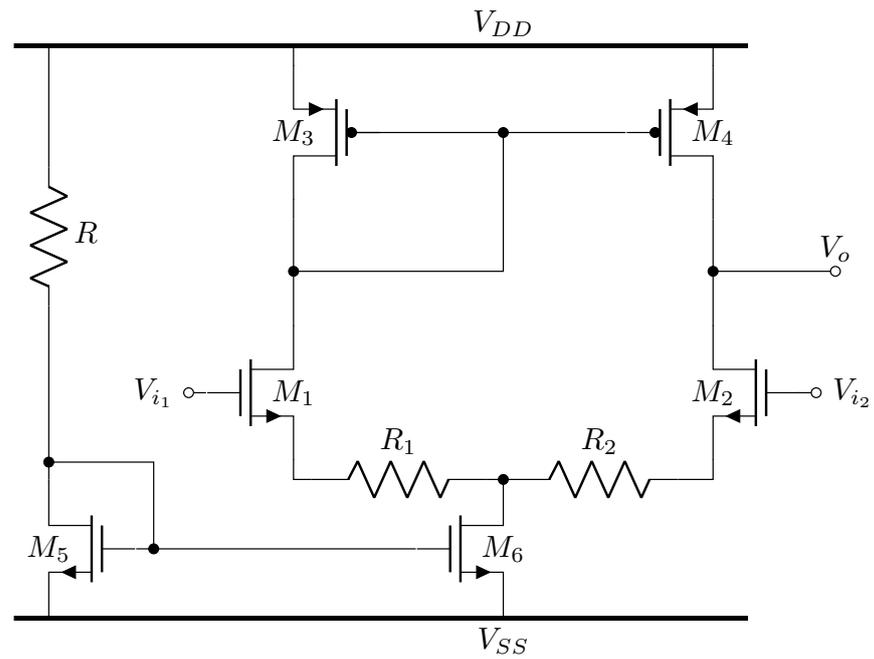


Figure 13. Source degeneration-based OTA design.

Finally, for the implementation of the OTA whose transconductance value should be  $g_{m3} = 500 \mu\text{S}$ , the two-stage Miller topology shown in Figure 14, which is taken from [32], is implemented with its respective compensation stage composed of  $R_c$  and  $C_c$ . Table 3 shows the W/L dimensions of each MOSFET, as well as the passive circuit element values.

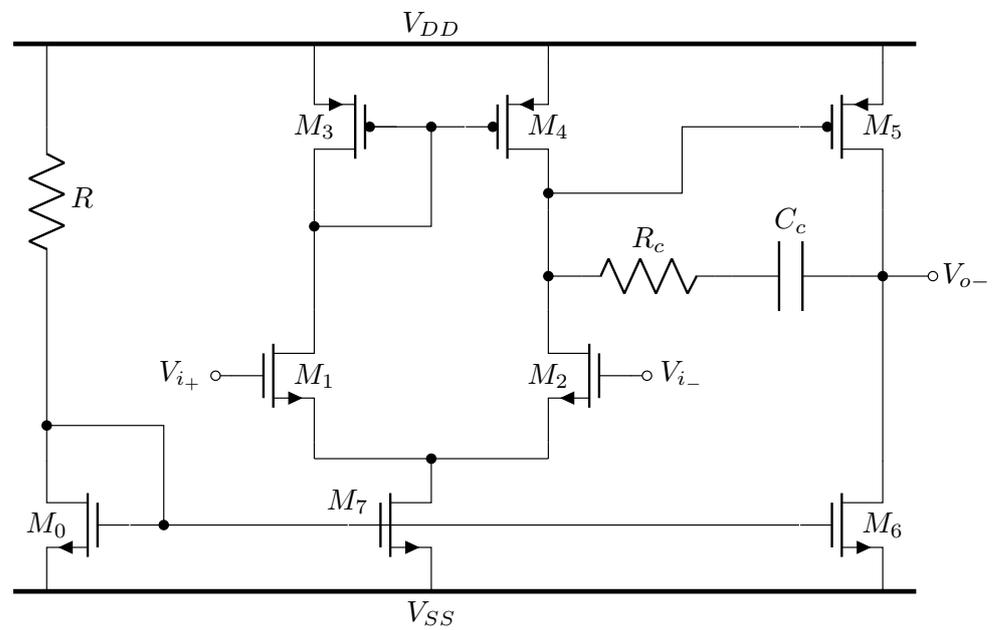


Figure 14. Two-stage OTA to obtain  $g_{m3} = 500 \mu\text{S}$ .

**Table 3.** W/L dimensions of the MOSFETs and circuit element values of the two-stage OTA shown in Figure 14.

MOSFET	W/L [ $\mu\text{m}$ ]	k $\Omega$	pF
$M_1, M_2$	6/0.54	-	-
$M_3, M_4$	24/0.54	-	-
$M_0, M_6$	12/0.54	-	-
$M_5$	48/0.54	-	-
$R_c$	-	1.25	-
$R$	-	20	-
$C_c, C_L$	-	-	0.5

The direct CMOS design from Figure 11 mitigates chaotic behavior due to the fact that the biquadratic filter requires finding the right place for the poles, which is established as follows: The mathematical description of a second-order or biquadratic filter that satisfies (12) is given in (13).

$$H(s) = \frac{k\omega_n^2}{s^2 + 2\delta\omega_n + \omega_n^2}, \tag{13}$$

where  $\delta$  is the relative damping factor and  $\omega_n$  is the undamped natural frequency. In this manner, (12) can be re-ordered as given in (14).

$$Z(s) = \frac{400\sigma}{s^2 + (\beta + \sigma)s + (\beta\sigma)} Y(s) * Y(s), \tag{14}$$

where it can be seen that  $\omega_n = \sqrt{\beta\sigma}$  and  $2\delta\omega_n = (\beta + \sigma)$ , so that at the end, the damping factor can be described by (15).

$$\delta = \frac{(\beta + \sigma)}{2\sqrt{\beta\sigma}}. \tag{15}$$

The damping factor can be tuned to generate the desired behavior, which, in this case, is chaotic behavior. Therefore, the damping factor depends on the values of  $\sigma$  and  $\beta$ , as shown in (15), so depending on the value of  $\delta$ , a system behaves as follows:

- If  $\delta > 1$ , the system is overdamped.
- If  $\delta = 1$ , the system is critically damped.
- If  $\delta < 1$ , the system is underdamped.
- If  $\delta = 0$ , the system is not damped, and it tends to oscillate.

By setting  $\sigma = 10$ , then the damping factor depends on  $\beta$ , as given in (16).

$$\delta = \frac{(\beta + 10)}{2\sqrt{10}\sqrt{\beta}} = \frac{(10 + \beta)}{2\sqrt{10}} \cdot \frac{1}{\sqrt{\beta}}, \tag{16}$$

and plotting this function can help to visualize how  $\delta$  depends on the values assigned to  $\beta$ . Thus, by plotting the function given in (16), as shown in Figure 15, one can appreciate how the system behaves for values  $\beta \neq 8/3$ . In addition, one can see that point A on the graph represents the value of  $\beta = 8/3$ . In order to guarantee that the CMOS design of Lorenz systems based on biquadratic filters remains oscillating with chaotic behavior, a value of  $\beta = 15$  is chosen in order to modify its behavior over time. As a result, the SPICE simulations of the CMOS and OTA-C-based Lorenz systems are shown in Figures 16 and 17.

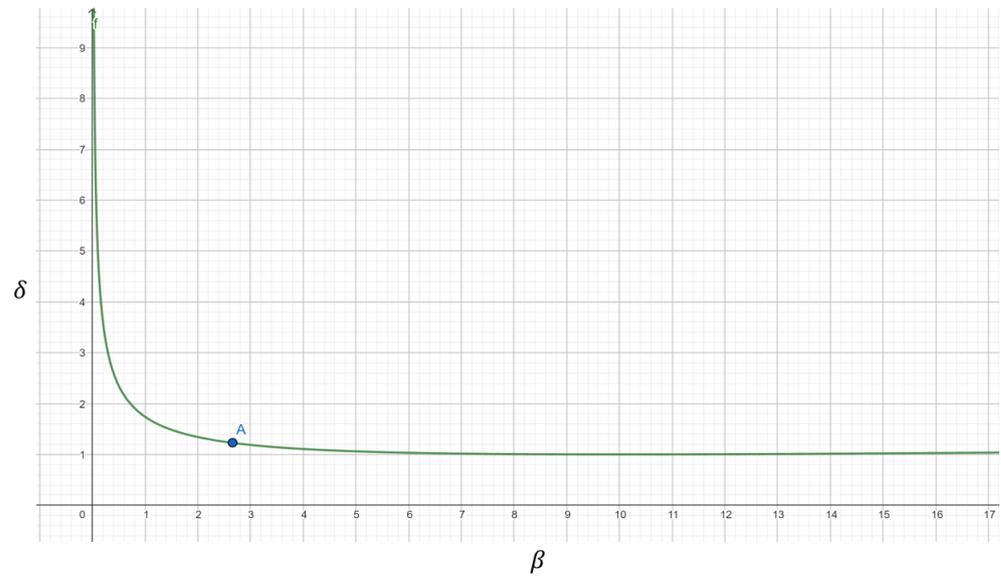


Figure 15. Plot of  $\delta$  given in (16) as a function of  $\beta$ .

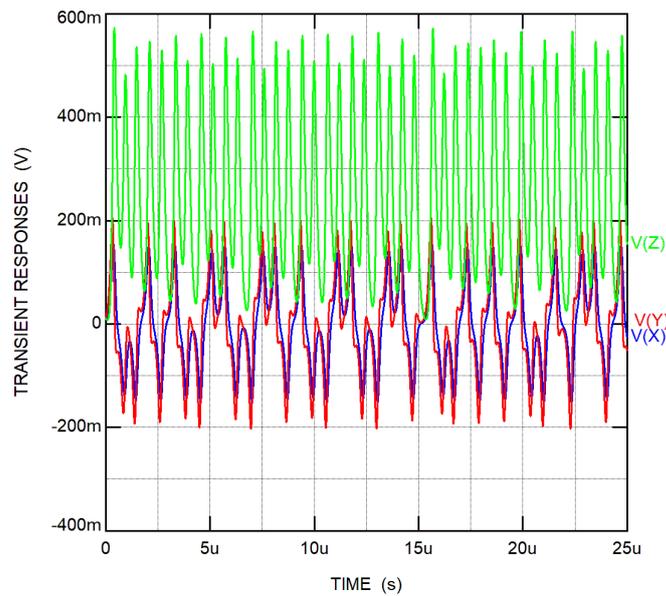


Figure 16. Time series of Lorenz system designed with 180 nm CMOS integrated circuit technology from the OTA-C-based design shown in Figure 11.

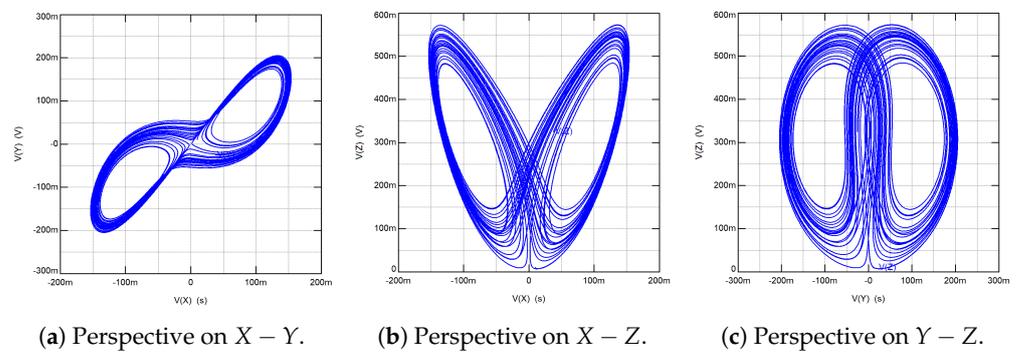


Figure 17. Phase portraits of Lorenz system designed with OTA-C topologies, in which the damping factor of the biquadratic filter is tuned by setting  $\beta = 15$ .

### 5. Chaotic Masking Using OTA-C Filters

As described above, chaotic masking based on two synchronized systems in a master–slave topology can be performed as shown in Figure 5, where it can be appreciated that state variable  $Y$  is used to mask a signal. First, the simulation results of synchronizing two CMOS Lorenz systems using the Pecora and Carroll technique are shown in Figure 18a for state variable  $Y$ , whose are lower than 300 mV, and in Figure 18b for state variable  $Z$ , whose amplitudes are lower than 800 mV. The synchronization results can also be appreciated by plotting both state variables of the master and slave systems. So, Figure 19a shows the synchronization result for state variables  $Y$ , and Figure 19b shows the synchronization result for state variables  $Z$ . A good related work on synchronizing a numerical solution in a computer with an analog circuit can be found in [35]; other authors show how to reconstruct a system from data estimating additional members in resulting equations [36]. In this work, the original equations are scaled to allow the amplitudes of the state variables to be within  $\pm 1$ ; then, they are synthesized by OTA-C topologies. Figure 20 shows the synchronization errors of the CMOS designs for state variables  $Y$  and  $Z$  of the master and slave systems. In each case, the root mean squared errors (RMSEs) are  $RMSE_Y = 67.94 \times 10^{-6}$  and  $RMSE_Z = 101.68 \times 10^{-6}$ .

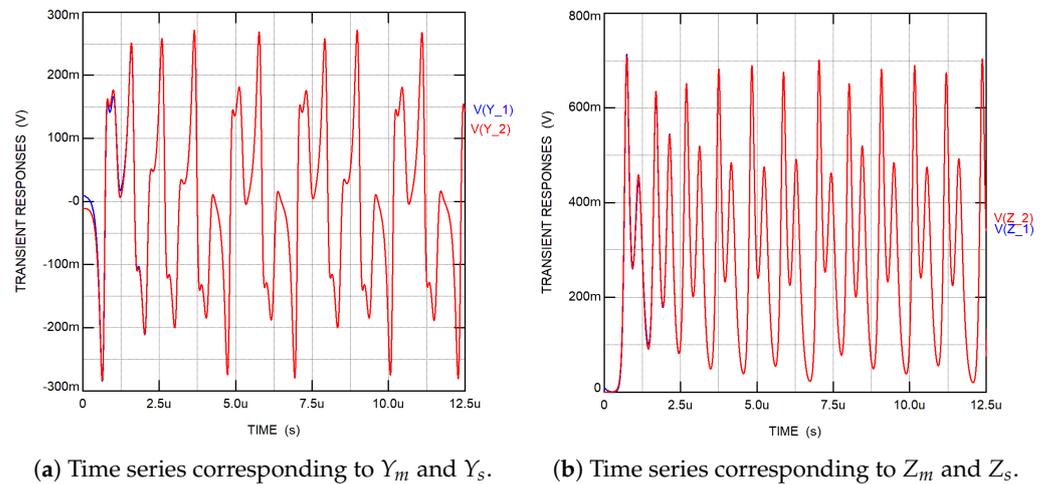


Figure 18. Time-series results of two CMOS Lorenz systems designed with OTA-C active filters.

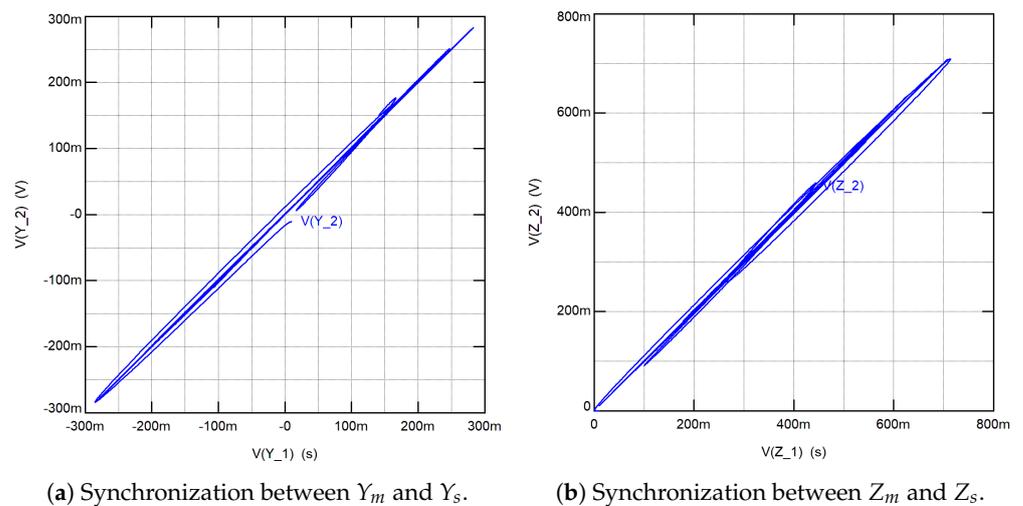
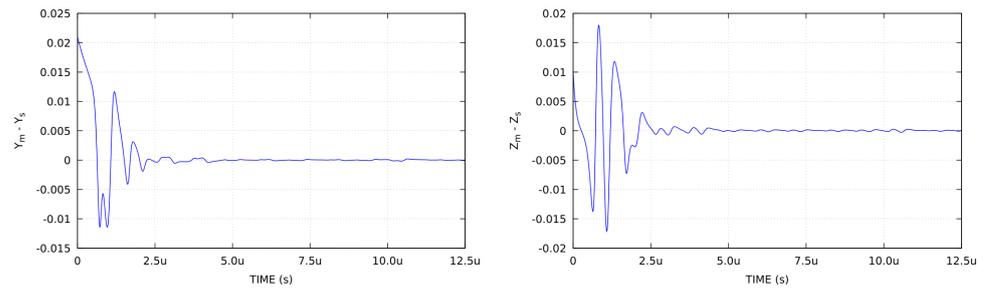


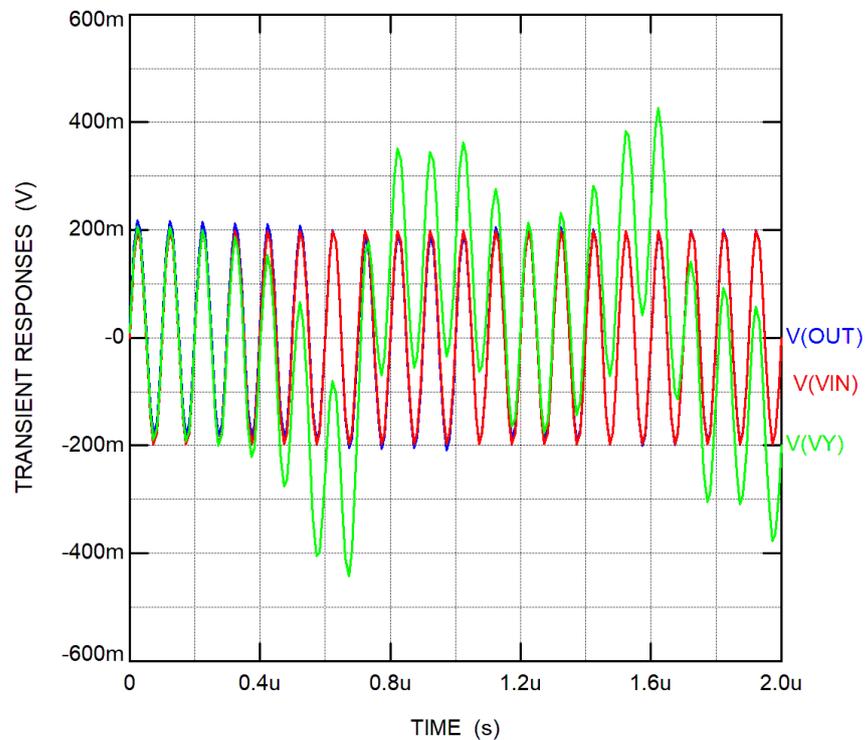
Figure 19. Synchronization results of two CMOS Lorenz systems designed with OTA-C active filters.



(a) Synchronization error between  $Y_m$  and  $Y_s$ . (b) Synchronization error between  $Z_m$  and  $Z_s$ .

**Figure 20.** Errors of the synchronization of two CMOS Lorenz systems designed with OTA-C active filters.

By designing two CMOS Lorenz systems with OTA-C topologies, as detailed in Section 4, a whole CMOS secure communication system is developed from Figure 11. The master and slave systems provide chaotic time series taken from their state variables  $Y_m$  and  $Y_s$ , respectively. In the case of the CMOS design proposed herein, the transmitted signal  $A(t)$  is a sinusoidal one and is masked with  $Y_m$  to generate signal  $B(t)$ , i.e., the channel that encrypts the input signal. As the slave system is well synchronized with the master one, the original signal can be recovered by subtracting the chaotic time series, obtaining  $C(t) = B(t) - Y_s = (A(t) - Y_m) - Y_s$ . Finally, as  $Y_s = Y_m$ ,  $C(t) = A(t)$ . This can be appreciated in Figure 21, where  $A(t) = V(VIN)$ ,  $B(t) = V(VY)$ , and  $C(t) = V(OUT)$ . It can be seen that during the transient behavior, one can see a pretty small difference between  $V(VIN)$  and  $V(OUT)$ , but after about  $0.6 \mu s$ , the error is almost zero, indicating that the recovered signal is the same as the transmitted one, while the encrypted one is masked in the chaotic time series.



**Figure 21.** Chaotic masking of a sinusoidal signal with chaotic time series by using the scheme shown in Figure 5 and designing the whole system with 180 nm CMOS integrated circuit technology.

Further research can be performed considering the secrecy analysis of the proposed communication system, as done in the recent works [37–39], showing resistance to various attacks.

## 6. Conclusions

We here show the design of Lorenz systems using OTA-C active filters implemented with 180 nm CMOS integrated circuit technology. As a particular case, the CMOS design consists of implementing three first-order low-pass filters and one biquadratic filter, whose damping factor is tuned to guarantee chaotic behavior, so that coefficient  $\beta$  in the original Lorenz system is updated from 8/3 to 15, as detailed in Section 4.

A secure communication system is simulated by using the original values of the Lorenz systems that are simulated in Simulink. Afterwards, the mathematical model is scaled to allow for CMOS design that requires the amplitudes of the state variables to be bounded between  $\pm 1$  Volt. The chaotic masking achieved by using two Lorenz systems synchronized in a master–slave topology and designed with CMOS OTA-C blocks shows its appropriateness for real applications in secure communications that require low-voltage supply, instead of using embedded systems as field-programmable gate arrays, which require higher voltage levels and power supply.

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