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CMOS Wireless Hybrid Transceiver Powered by Integrated Photodiodes for Ultra-Low-Power IoT Applications

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Abstract: In this article, a communication platform for a self-powered integrated light energy harvester based on a wireless hybrid transceiver is proposed. It consists of an optical receiver and a reconfigurable radio frequency (RF) transmitter. The hybrid optical/RF communication approach improves load balancing, energy efficiency, security, and interference reduction. A light beam for communication in the downlink, coupled with a 1 MHz radio frequency signal for the uplink, offers a small area and ultra-low-power consumption design for Smart Dust/IoT applications. The optical receiver employs a new charge-pump-based technique for the automatic acquisition of a reference voltage, enabling compensation for comparator offset errors and variations in DC-level illumination. On the uplink side, the reconfigurable transmitter supports OOK/FSK/BPSK data modulation. Electronic components and the energy harvester, including integrated photodiodes, have been designed, fabricated, and experimentally tested in a 0.18 µm triple-well CMOS technology in a 1.5 × 1.3 mm^2 chip area. Experiments show the correct system behavior for general and pseudo-random stream input data, with a minimum pulse width of 50 µs and a data transmission rate of 20 kb/s for the optical receiver and 1 MHz carrier frequency. The maximum measured power of the signal received from the transmitter is approximately −18.65 dBm when using a light-harvested power supply.

Keywords: solar/optical harvesting; ultra-low-power circuit; hybrid transceiver; IoT; Smart Dust

Citation: Nikseresht, S.; Fernández, D.; Cosp-Vilella, J.; Selin-Lorenzo, I.; Madrenas, J. CMOS Wireless Hybrid Transceiver Powered by Integrated Photodiodes for Ultra-Low-Power IoT Applications. *Electronics* **2024**, *13*, 28. https://doi.org/10.3390/electronics13010028

Academic Editor: Alireza Saberkari

Received: 29 November 2023
Revised: 14 December 2023
Accepted: 18 December 2023
Published: 20 December 2023

1. Introduction

Over the past few years, there has been a remarkable surge in the adoption of Internet of Things (IoT) applications, driven by the rapid advancements in low-power and miniature electronics. These IoT solutions have found their way into various domains, including but not limited to smart homes, consumer electronics, wearable devices, and industrial monitoring [1,2]. The momentum of this phenomenon remains steadfast, and in accordance with forecasts, a staggering 34.7 billion IoT devices are expected to be in operation worldwide by the year 2032 [3].

There is a notable shift toward Smart Dust Motes (SDMs) in the evolution of IoT devices. These tiny millimeter-scale packages incorporate self-contained sensors, computing capabilities, and communication modules [4,5]. Typically, SDMs rely on on-device batteries for power. The main issue with battery reliance in the IoT is their limited energy capacity, which necessitates inconvenient and costly recharging or replacement. Reducing device activity to extend battery life sacrifices functionality, and in some cases, batteries pose safety risks and environmental concerns due to disposal. Powering a large number of IoT sensors is a significant challenge, which gets worse by the remote and hard-to-reach locations where sensors are often deployed, thereby increasing maintenance costs [6,7].

To overcome these challenges, the development of ultra-low-power and small-sized integrated devices coupled with the harvesting of ambient energy sources presents a promis-

ing solution for powering Wireless Smart Dust Networks (WSDNs), thereby eliminating or reducing batteries [8,9].

Another critical challenge for WSDNs is the design of a communication architecture. This part, as the power-hungry component, should be designed in an efficient way in terms of cost, area, and power for the SDM's purpose. Conventional communication relies on radio frequency (RF) signals, which are desired for IoT due to their higher mobility and performance in non-line-of-sight capability. SDMs that employ RF communication links constrained by their limited antenna space encounter power consumption issues due to the high-frequency transmission requirements. However, for specific applications such as short-distance and contactless sensing, where high-frequency limitations become less restrictive, the potential to develop short-range, low-frequency, and low-power communication channels is feasible [8,10–12].

On the other hand, RF networks face overloading, resulting in growing congestion within the RF band and subsequent increases in interference and data transfer errors for wireless devices. The fact that over 70% of wireless data communication currently occurs in indoor environments complicates this issue, a trend that is expected to continue. Regarding these challenges, Optical Wireless Communication (OWC) can serve as a supplementary solution to RF communication for IoT applications [13,14].

OWC presents a range of desirable communication factors, including electromagnetic interference-free, better security, higher energy efficiency, license-free spectrum, and cost-effectiveness. Despite the numerous advantages of OWC systems, certain limitations must be highlighted. These constraints include a significant dependency on line-of-sight conditions, restricted coverage area, susceptibility to unexpected connection blocking, potential interference from various light sources, and limited transmitted power output [15,16]. The issues of network connection blocking and its optimization for accurate data acquisition in optical communications were discussed in [17,18].

To overcome the drawbacks and to take advantage of both RF and OWC, a hybrid optical/RF communication approach can integrate both methods within a single chip, specifically for indoor applications. This integration provides their coexistence without interference with each other. Hybrid wireless communication enhances the system performance, including productivity, reliability, and energy efficiency, and plays a crucial role in load balancing and security in IoT applications [16,19–21].

This work focuses on a wireless hybrid transceiver communication circuit which is simultaneously powered by integrated photodiodes through the received modulated light for SDM-purpose applications. Some other works have explored this topic and some parts of it. In [21], a 10.6 mm^3; smart dust device was proposed, featuring an eight-layer chip stack including solar cells, an energy harvester, a processor with an optical receiver, an RF transmitter, a temperature sensor, decoupling capacitors, a thin-film lithium battery, and a small external antenna. It uses wireless optical communication at a rate of 91 bps for SRAM programming and an 8 GHz RF transmitter for data transmission, with an active power consumption of 36 µW. However, the system's complexity is an issue, especially in the context of IoT, where network coverage depends on the implementation of numerous low-cost sensor nodes. In [5], an ultra-low-power optical wireless transceiver powered by an on-chip solar cell for SDM applications was proposed. However, due to the use of light for both data reception and transmission, it can encounter limitations, such as light interference and a limited coverage area. In [22], the optical receiver used two branches: one for data and another for energy harvesting, with an inductor in the latter for signal filtering. However, the inductor's large size limits its integration into system-in-package solutions. In [23], a solar cell-based optical receiver and harvester for indoor wireless communication was proposed. A limitation of this study is that it requires discrete components, and it is not monolithic.

The feasibility of an optical receiver has been recently reported [24]. The remainder of this article is organized as follows: Section 2 presents an overview of the SDM system, which includes an energy harvesting, wireless optical receiver circuit, and a wireless recon-

figurable transmitter circuit. Section 3 discusses the full system, including its measurement and characterization. Section 4 concludes the article.

2. Smart Dust/IoT Overview

Figure 1 shows the comprehensive architecture of an SDM, which, highlighted in dotted lines, consists of an Energy Harvesting Unit (EHU), and the information processing unit. This unit contains an embedded communication system, including an optical receiver, a transmitter, and a Digitally Controlled Oscillator (DCO), as well as a sensing block and a Digital Control and Processing Unit (DCPU). The EHU collects energy from the received light and converts it to a suitable voltage level to supply other blocks of the SDM. The DCPU controls the entire system for detecting, sending, and processing data. The sensing block obtains data from the environment and sends them to the DCPU for processing. The receiver detects the incident-modulated light through the photodetector and then sends the recovered data to the DCPU for decoding and processing. The transmitter sends the modulated data from the DCPU to an external processor unit for the subsequent processing.

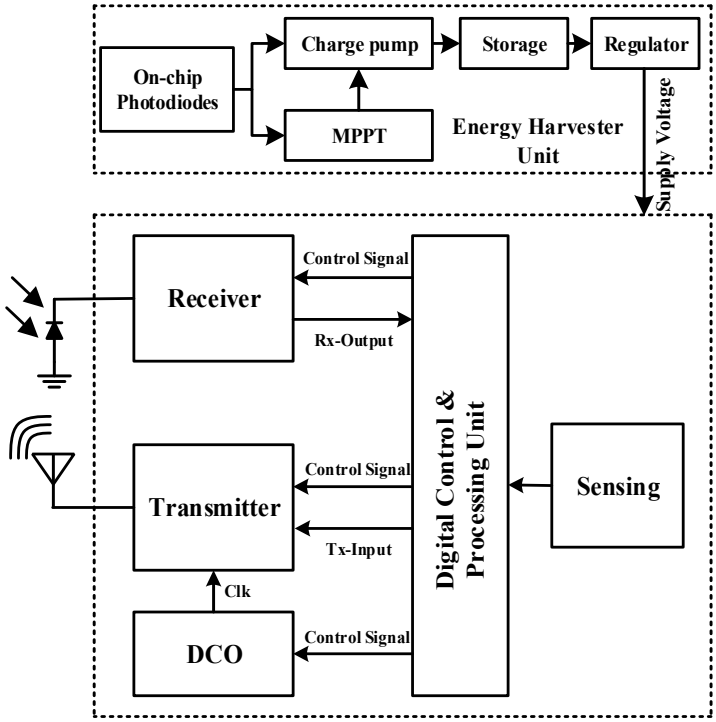


Figure 1. SDM System Overview.

This work focuses on the communications platform; thus, the EHU has been simplified as a set of on-chip parallel positive voltage photodiodes that directly connect to the antenna driver or power amplifier, the system's power-hungry part. The system is configured as a simple transceiver to demonstrate the correct behavior of the communication blocks; the output of the optical receiver directly drives the transmitter, which generates an output signal at two carrier frequencies: 1 MHz and 1.1 MHz. The DCPU configures the receiver to recognize data from different on/off-chip photodetectors, sets the DCO for two different clock frequencies, and adjusts the transmitter for three different signal modulations.

The transceiver structure presented here could be expanded into a comprehensive system block containing a DCPU with a processing unit, sensors, and an advanced EHU featuring Maximum Power Point Tracking (MPPT) as well as a voltage regulator. Potential applications for the sensing block include temperature, humidity, MEMS sensors, etc.

2.1. Energy Harvester

Integrated photodiodes are the preferred choice for energy harvesting, mainly because they can be integrated into a single chip along with electronic circuits. This integration not only simplifies the design but also leads to cost savings in standard bulk CMOS technology during manufacturing [25].

Several pn-junctions are available in modern triple-well standard CMOS processes. Figure 2a depicts a cross-section view of two efficient photodiodes in the standard bulk CMOS technology [26]: PWell/Deep NWell (D1) and Deep NWell/PSub (D2). In most scenarios, the substrate (PSub) must be connected to a ground connection. This ensures that there is no forward biasing of any pn-junction formed between the bulk and the N-type diffusion.

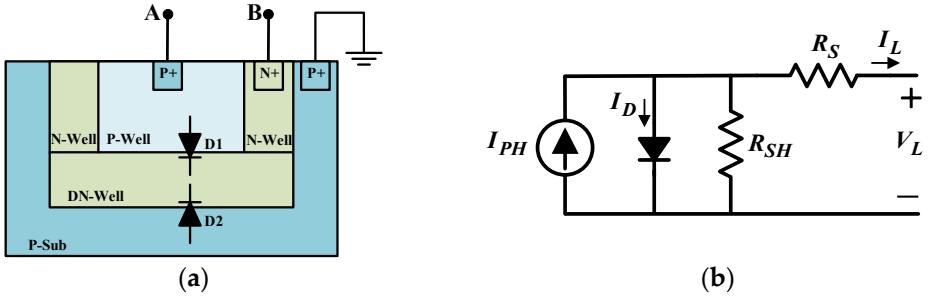


Figure 2. (**a**) Cross-sectional view of two efficient available photodiodes and (**b**) DC model of a photodiode.

To generate a positive voltage, D1 is employed, whereas D2 is short-circuited. This ensures that the supply connects to node A, while node B connects to the ground. For generating a negative voltage, PWell (node A) is connected to the ground, and the supply is connected to node B. Compared to the positive photodiode, the negative one has a higher efficiency due to its deeper junction. However, converting a negative voltage to a positive voltage requires an additional circuit for inversion. According to Figure 2b, the electrical DC model of a photodiode can be expressed as [9]:

$$I_L = I_{PH} - I_D - \left(\frac{V_L + R_S I_L}{R_{SH}}\right) \quad (1)$$

where I_D refers to the forward current flowing through the diode, R_{SH} characterizes the leakage current of the diode, and R_S represents the internal voltage loss due to the interconnecting elements. Figure 3 shows the measured I-V and P-V characteristics of 4 × 4 parallel positive and negative photodiodes matrix for a 240 × 240 μm^2 area under various laser intensity currents, where the laser source is at a vertical distance of 2 cm from the chip, manufactured in a 0.18 µm TSMC technology. According to this figure, the maximum output power densities of the positive and the negative photodiodes are 12.8 $pW/\mu m^2$ and 76.3 $pW/\mu m^2$, respectively, at 0.42 V of the photodiodes' voltage. The results show that the efficiency of the negative photodiode is higher than that of the positive one by a factor of 5.9.

Depending on the illumination level, these photodiodes exhibit a low open-circuit voltage ranging from 0.3 V to 0.5 V. Although it is possible to increase the voltage by stacking several photodiodes, this method suffers from important losses associated with unwanted parasitics. An integrated boost converter to increase the photodiode voltage level can solve this problem at the expense of complicating the design. In this work, to test the energy harvesting module, a matrix of parallel positive photodiodes is employed to generate a positive voltage to directly supply the power amplifier, where node B is connected to the ground. The maximum output power measured in the implemented 13 parallel blocks of the positive photodiode matrix is about 9.6 µW.

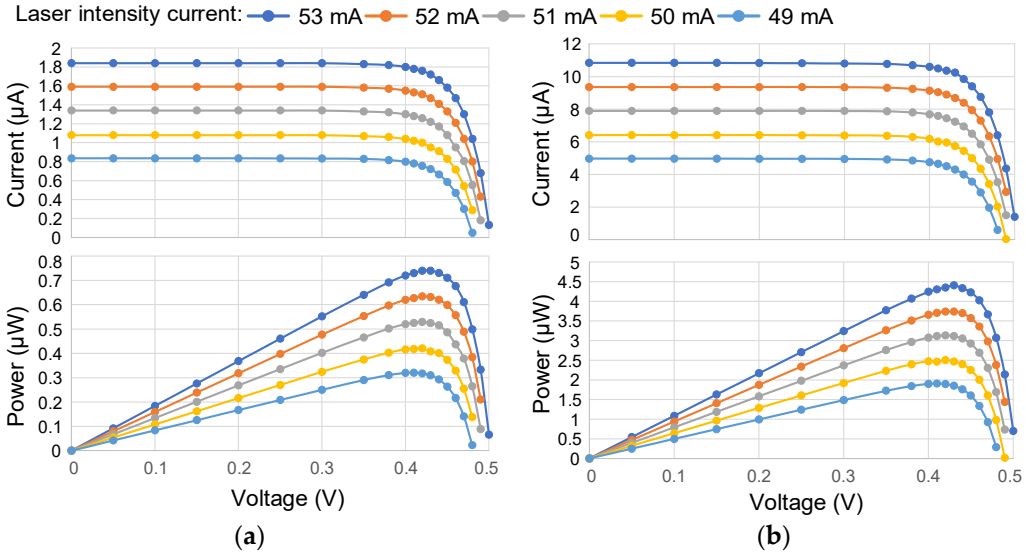


Figure 3. Characteristics of the (**a**) positive and (**b**) negative photodiodes for various laser intensity currents.

2.2. Optical Receiver

Figure 4 illustrates the schematic of the ultra-low-power optical receiver. The design integrates multiple components: a Photodiode (PD), a logarithmic Transimpedance Amplifier (log-TIA), an Operational Transconductance Amplifier (OTA)-based comparator for DC adaptation, a Single Input Charge Pump (SICP), and a Schmitt trigger comparator. The operational flow begins with the PD, which is responsible for sensing the modulated light signal and converting it into an electrical current. It is reverse-biased to improve detection speed. Subsequently, the current is transduced into a voltage signal and amplified by the log-TIA. The output signal is further processed in the comparison block, where it is adapted to DC variations, thus standardizing the input into a readable binary format. Finally, the Schmitt trigger comparator refines the comparison block output, ensuring a clean binary signal, which is essential for obtaining reliable data for subsequent processing. The optical receiver design has been reported in [24], and its performance is evaluated here when linked with the other system elements.

A 20 × 20 µm^2 N-Well/PSub-type PD detects the illumination light data. The structure of the PD is shown in the dashed-circle inset of Figure 4. Signal fading and intensity variations are the challenges that arise from different transmission distances, which are considered while designing the receiver. Adopting a high dynamic range log-TIA as a photoreceiver and the SICP circuit described below alleviates this issue. Log-TIA's high dynamic range enables it to remain sensitive and responsive to these variations in light intensity, guaranteeing that the integrity of the transmitted data is preserved, even under diverse and fluctuating environmental conditions. The log-TIA performance is affected by factors such as the modulation depth, incident light DC level, and capacitance ratio, which improves its ability to adapt to fluctuations in the light intensity. Figure 4 illustrates the circuit and functionality of the log-TIA. Its details have been previously discussed in [27,28]. C_1 and C_2 are MIMCAP-integrated capacitors, with values of 100 fF and 50 fF, respectively. Equation (2) presents the mid-band gain of the log-TIA [28].

$$G_{detector} = \frac{v_{out}/U_T}{i_{pd}/I_{pd}} = \frac{1}{k} \times \frac{C_1 + C_2}{C_2} \approx 4 \quad (2)$$

i_{pd} and v_{out} denote the small-signal input and output components, respectively. I_{pd} is the DC component of the photocurrent, U_T represents the thermal voltage, and k, which is 0.74 in 0.18 µm CMOS technology, indicates the capacitive coupling ratio from the gate to the

channel of the NMOS transistor [29]. Considering a modulation depth of 20% for i_{pd}/I_{pd}, the resulting small-signal output is as follows:

$$v_{out} = U_T \times \frac{i_{pd}}{I_{pd}} \times G_{detector} \approx 20.8 \text{ mV} \quad (3)$$

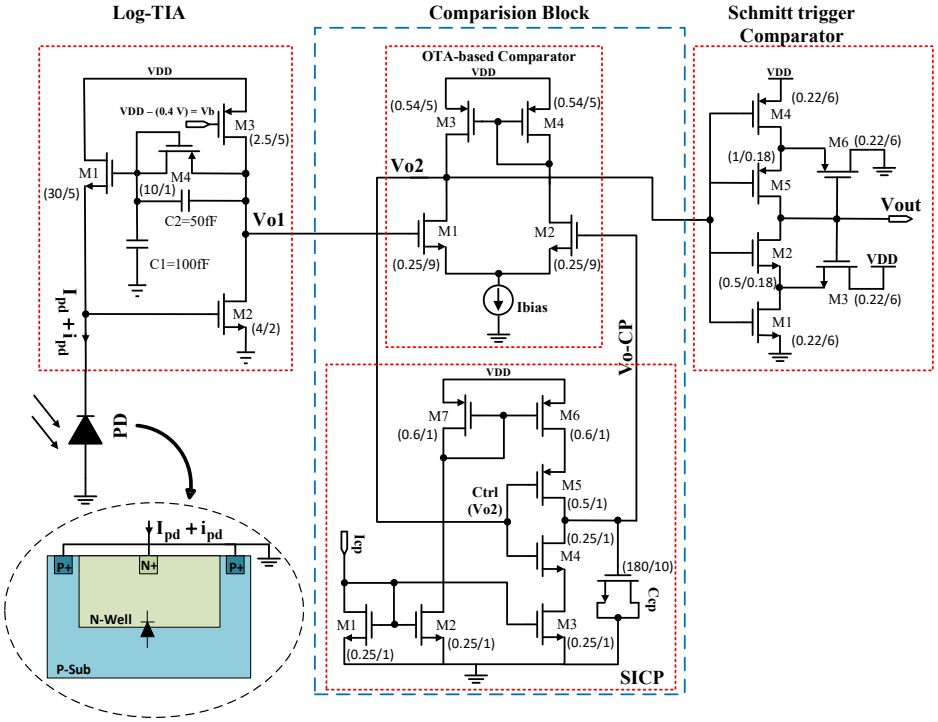


Figure 4. Schematic of the wireless optical receiver.

Furthermore, the log-TIA exhibits passband gain characteristics within a frequency range of 500 Hz to 170 kHz, effectively filtering out undesirable optical interferences that fall outside this passband range. This range excludes unwanted light disturbances, particularly those in the 50–100 Hz range commonly associated with electrical lines and fluorescent tubes.

Comparison Block

Signal DC variations and comparator offset errors are the most common cause of receiver inaccuracy. These issues can significantly impact the performance of Smart Dust/IoT applications, where precision is important. To address this, the design of the comparator in the receiver must incorporate mechanisms that can automatically adjust to these variations. The design ensures that the reference signal is continuously aligned with the fluctuating input signals by implementing a dynamic reference-level generation system within the comparator circuit. This internal adaptation is critical, particularly in complicated situations where external adjustments of the reference signal are impractical or impossible.

Designing a symmetrical layout and using larger devices can reduce random mismatch, but not fully eliminate it. Thus, the receiver performance can be improved, but challenges in minimizing offset accuracy persist [30]. To efficiently improve matching, a new method in the DC adapting comparison block is proposed, as shown by the blue dashed rectangle in Figure 4. This novel technique for obtaining the reference voltage corrects DC variations and offset errors in an OTA-based comparator. Our approach ensures that the receiver can effectively cope with different light intensities and background illuminations, thereby improving its robustness and reliability.

As shown in Figure 4, the closed-loop simple OTA-based comparator and the SICP serve as two essential components in the design of the comparison block. This configuration enables the comparison block to dynamically generate an accurate reference voltage in response to the light conditions detected at the photodetector and ensures that the design can adapt to average illumination levels. Compared with conventional high-order integrators, the proposed SICP requires less power and area, thus presenting a more optimized solution for a receiver. This efficiency is crucial because typical high-order integrators [31] require several amplifiers and capacitors to generate a reference voltage, which leads to increased power consumption and area. Streamlining this process with SICP improves the overall performance of the optical receiver, supporting more efficient and accurate operation.

In this configuration, the log-TIA's output is connected to the first differential input of the initial comparator, while the comparator's output, "Vo2", is linked to the control terminal, "Ctrl", of the SICP. This configuration enables the SICP to recognize the pulse-width output of the comparator. Subsequently, the SICP current source, I_{cp}, which has been set to 10 nA for low power consumption, is responsible for adjusting the charging and discharging of the capacitor C_{cp} based on the detected pulse width. This ensures that the comparator accurately operates, with C_{cp} maintaining the correct DC level, which is then fed into the other differential input of the comparator. Capacitor C_{cp} is estimated by (4) to control the input pulses at different frequencies for the worst case.

$$C_{cp} = \frac{I_{cp} \cdot \Delta t}{V_{ripple}} = \frac{I_{cp}}{2 \cdot f \cdot V_{ripple}} \approx 12.5 \text{ pF} \quad (4)$$

where V_{ripple} is the SICP's output ripple voltage, Δt is the maximum charge and discharge time of C_{cp}, and $\Delta t = 1/2\,f$. In the worst case, V_{ripple} must be equivalent to the minimum peak-to-peak amplitude of log-TIA output. According to Figure 4, Vo1 represents the output of the log-TIA and also serves as one of the inputs to the OTA-based comparator, while Vo-CP is the output of the SICP and another input of the comparator and the reference voltage. To ensure an accurate comparison, the maximum peak-to-peak ripple amplitude of the Vo-CP must be within the peak-to-peak amplitude range of Vo1. The amplitude of Vo1 varies with the photocurrent level; a higher photocurrent yields a greater amplitude. Referring to (4), C_{cp} is inversely related to the frequency (f) and V_{ripple}, with an I_{cp} of 10 nA. For accurate reference voltage generation, the minimum input frequency and peak-to-peak amplitude of Vo1 must be considered. At 5 kHz and a 10 nA photocurrent, the peak-to-peak amplitude of Vo1 is 80.3 mV, leading to a maximum C_{cp} of 12.5 pF. At 170 kHz and a 500 nA photocurrent, it is 112.5 mV, resulting in a minimum C_{cp} of 0.26 pF. These values are derived from the analysis of the signals shown in Figure 5.

The design approach employs a larger C_{cp} capacitor with a value of 15 pF to account for any possible variations in the log-TIA peak-to-peak output amplitude due to the fabrication process. Because capacitor accuracy is not critical in this application, an area-efficient and properly biased MOSCAP with a zero-threshold voltage NMOS transistor is used. To complete the design, a Schmitt trigger comparator, as shown in Figure 4, is employed to ensure the digital output edges are fast.

Because some internal nodes are unavailable for measurement, simulation results are employed to provide a clearer view of them. Figure 5 illustrates a simulated performance of the optical receiver for a 20 nA pseudo-random photocurrent with a 20% modulation depth. To emulate real-world optical communication scenarios, this photocurrent amplitude is controlled with an 8-bit Linear Feedback Shift Register (LFSR), which generates a 255-long pseudo-random bit sequence. It is designed to produce a pulse width of at least 50 µs. Signal Vo-CP, the output of the SICP, shows that it properly controls the charging and discharging of the capacitor C_{cp} in response to the DC component of the input signal. This validates that the DC adapting comparison block automatically generates a reference voltage and compensates for any DC fluctuations or offset deviations.

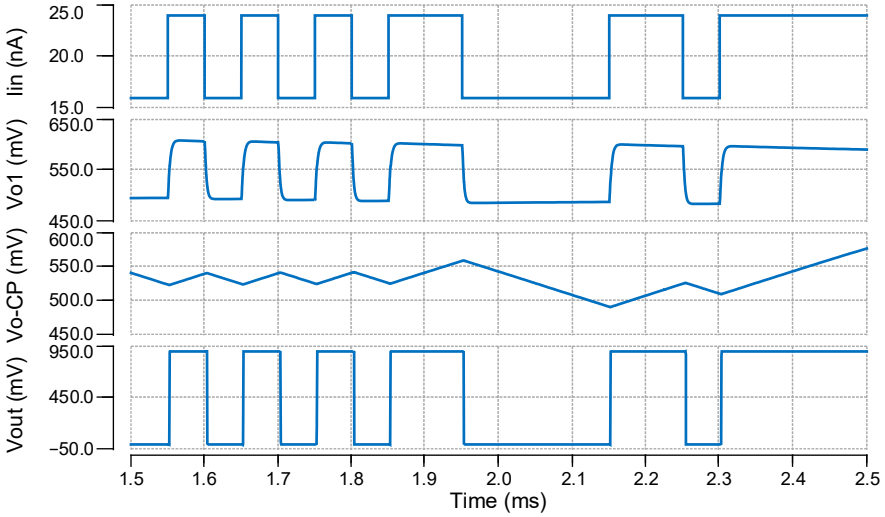


Figure 5. Simulation results of the optical receiver for a 20 nA photocurrent with a 20% modulation depth intensity. Iin is a modulated data current input, Vo1 is the Log-TIA output, Vo-Cp is the output of the SICP, and Vout is the optical receiver output.

2.3. Transmitter

Transmitter adaptability and efficiency are paramount in today's overloaded RF communication environments. To address the multiple demands of different communication patterns, an ultra-low-power reconfigurable transmitter capable of managing OOK, BPSK, and FSK modulation is presented, which works in the medium RF range. Figure 6 shows the block diagram of the reconfigurable transmitter. The system is characterized by several digital blocks, a DCO to generate 1 MHz and 1.1 MHz clock frequencies, and a power amplifier responsible for deriving the small external antenna. It is worth mentioning that such low-frequency operation responds to the low-speed requirements of ultra-low-power systems and to the relatively low bandwidth demand of distributed sensors.

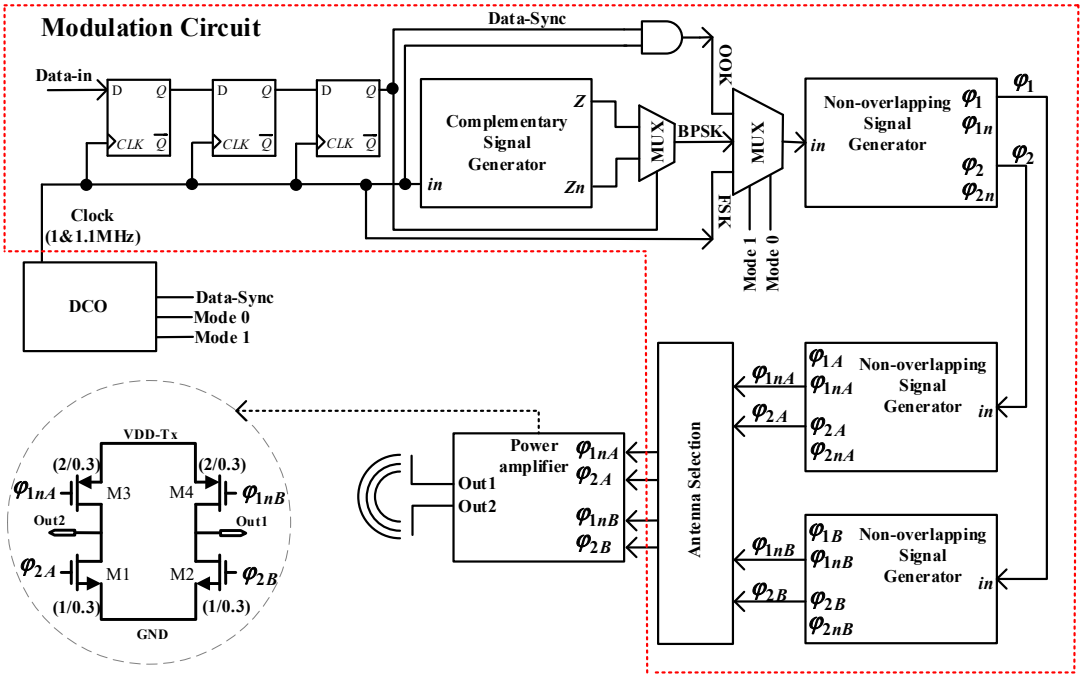


Figure 6. Transmitter block diagram.

2.3.1. Modulation Circuit

At the core of the transmitter lies a cascade of digital blocks, highlighted by the red dotted lines in the inset of Figure 6, which process the binary input data and prepare them for different data modulations. The data are entered via the "Data-in" node, subsequently processed and synchronized through a set of flip-flops to ensure data integrity and timing precision. The complementary signal generator and the first multiplexer (MUX) generate the phase and anti-phase output for BPSK modulation. The AND gate mixes the data signal with the clock signal and prepares the required signal for the OOK modulation. The second MUX along with digital control signals, "Mode 1", "Mode 0", and "Data-Sync", controls the DCO to generate two different frequencies, depending on the binary state of the data signal for FSK modulation. The non-overlapping signal generators enhance the system's accuracy by distinctly separating the signal phases and ensuring that the two signal states never simultaneously overlap. Such careful organization of the digital components guarantees that data are processed and appropriately directed to the following stages. At the end of the system, an antenna selection block is used to enable or disable one or both power amplifier branches, subject to data transmission requirements and energy saving goals, thereby increasing the overall energy efficiency of the system.

The second multiplexer in the block diagram selects a modulation technique. Its mode control signals, "Mode 1" and "Mode 0", switch between various modulation schemes. When set to '00', it selects OOK modulation, a form of Amplitude-shift keying (ASK) where the carrier is transmitted when data is high and goes idle when data is low to reduce the power consumption. The '01' setting activates BPSK, where the carrier's phase shifts by 180 degrees with each binary state change in the input data, essentially inverting the signal based on the transmitted bit. Lastly, with '10', the transmitter employs the FSK. Here, changes in the binary state of the input data lead to frequency adjustments by the DCO: 1.1 MHz for the high state and 1 MHz for the low state. As a result, the transmitter is adaptable and can fit different kinds of communication demands. Figure 7 illustrates an example of the signals generated by the modulation circuit for OOK modulation. As depicted, when the input state is high, the circuit generates appropriate signals. However, during the low input state, the signals remain inactive, ensuring that the power amplifier is not operating. It should be mentioned that the modulation circuit of the design, depicted in Figure 6, is integrated into the chip.

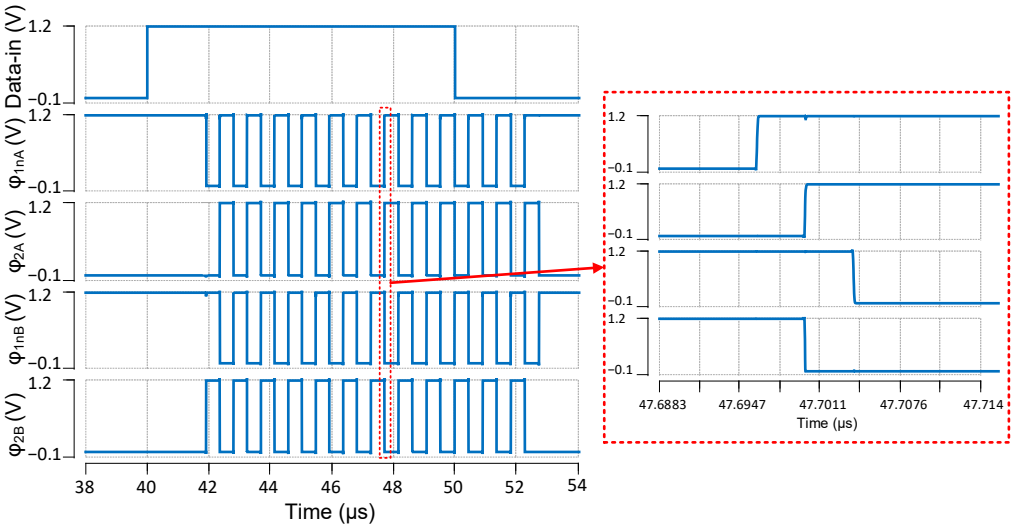


Figure 7. OOK modulated signals sample.

2.3.2. DCO

The schematic of the proposed DCO is depicted in Figure 8. It consists of four primary circuits: start-up, Beta Multiplier (BM)-based current reference, core oscillator, and a Schmitt trigger comparator. The main role of the start-up block is to prevent the BM-based current reference circuit from locking in the zero-current state. Consisting of PMOS transistors and a capacitor, it is based on the RC time constant principle. After initiating the BM-based current reference circuit, it automatically turns off to save energy. The BM-based current reference circuit works in the subthreshold region. It employs cascaded transistors to ensure a steady voltage at the output of the current mirror and improve linearity. This arrangement enhances the output resistance, resulting in better linear current regulation. Equation (5) [32] shows the output reference current.

$$I_{ref} \approx \frac{nU_T((W/L)_1/(W/L)_2)}{R_1 + R_2} \quad (5)$$

where n is the subthreshold factor, W/L represents the width-to-length ratio of a transistor, and R_1 and R_2 are resistors for determining the switching frequency. According to (5), I_{ref} is directly proportional to the thermal voltage (U_T) and indirectly proportional to the N-Well resistor. Since both are Proportional To Absolute Temperature (PTAT), their deviations cancel in the output current and make it almost independent of temperature variation [33]. In addition, it is independent of power supply fluctuations.

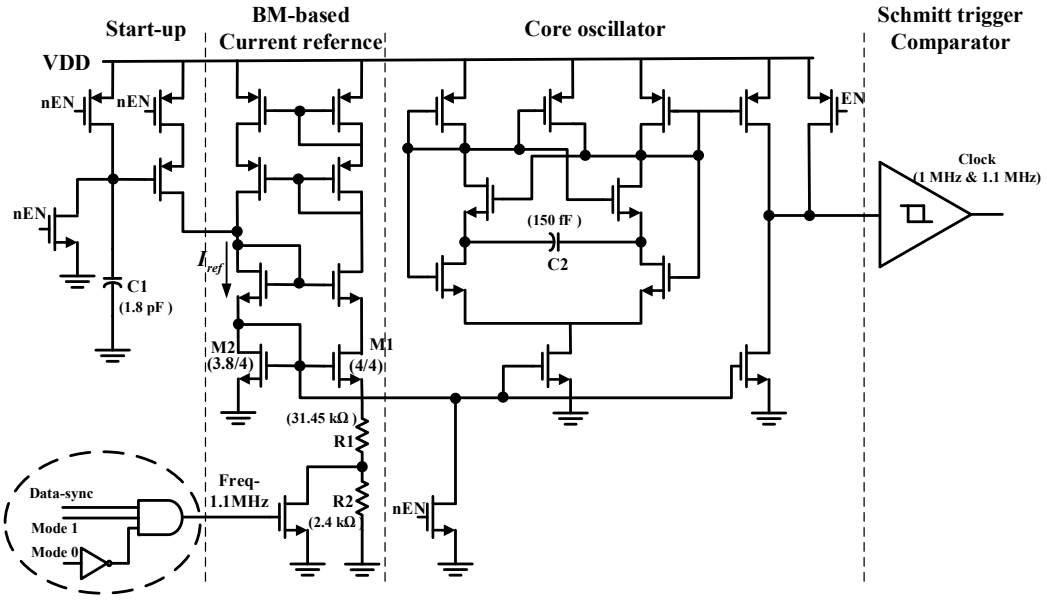


Figure 8. Circuit schematic of the DCO.

At the center of the DCO is the core oscillator, which is a relaxation oscillator that generates two clock frequencies: 1 MHz and 1.1 MHz. It provides high-frequency output waveforms with low power consumption [34]. In Figure 8, a digital block in the black dashed circle inset configures the reference current for the two different DCO frequencies according to the modulation modes used. Finally, a Schmitt trigger comparator is used after the core oscillator to create a clean pulse wave clock with a 50% duty cycle. The power dissipation of the DCO is 800 nW for a 1.2 V power supply.

2.3.3. Power Amplifier and Antenna

A power amplifier, which provides the required amount of output power, is an important component of RF transmitters. The proposed transmitter feeds a small antenna by using an inverter-based amplifier. Figure 6 shows a schematic diagram of the antenna and power amplifier used in the proposed transmitter in the black dashed circle. The proposed inverter-based amplifier is distinguished by its use of a non-overlapping signal generator. This design effectively eliminates the crossbar current, a common issue in conventional inverter-based amplifiers that often leads to increased power losses and thermal stress due to simultaneous conduction. Compared to traditional designs, this approach provides improved energy efficiency and operational stability, especially in applications where these factors are important. Although it is slightly more complex, it offers long-term benefits, including lower maintenance costs and improved overall system performance.

To achieve resonance in the antenna design at a carrier frequency of 1 MHz, the antenna's linear dimensions must be equal to half the wavelength of the operating frequency. A dipole antenna at this frequency should be 150 m long to achieve the resonance criteria for optimal antenna performance; however, such an antenna is obviously not an option in this design. The SDM demands for small size limit the applicable antenna length and prevents ideal resonance conditions. The power amplifier can natively support either unbalanced (monopole) or balanced (dipole) antennas. For this, two output antenna ports are available on the chip, and either of them can be used to feed a monopole or both in the counterphase can be used to differentially feed a dipole. In the experiments, a simple, short-length monopole of approximately 2-cm-long wire was used on "Out1". Therefore, the antenna was driven by M2 and M4 transistors with the driving signals φ_{1nB} and φ_{2B}, and transistors M1 and M3 remained off. This setup allows the monopole antenna to operate in the voltage mode, resulting in lower power consumption.

At an operating frequency of 1 MHz, this antenna presents a radiation resistance of about 1.8 μΩ and, for attaining resonance, a series inductor of approximately 15 mH would be needed [35], which gives a total impedance of 1.8 μΩ–j 94.25 kΩ. The estimated gain of the antenna is about 5 dB, but due to this small radiation resistance, the antenna is extremely inefficient when compared with the inductor series resistance and the resistive losses of the antenna interconnection ports. The inductance value is limited for a miniaturized system; therefore, to simplify it, it was decided not to use any inductor and to directly connect the antenna to the chip pads using a small wire to minimize losses.

3. Experimental Results

The proposed communication platform powered by energy harvesting was implemented with CMOS 0.18 μm TSMC technology on a 1.5 × 1.3 mm^2 chip area. The microphotograph in Figure 9 shows the fabricated photodiodes, which take up the most area, being the optical wireless receiver and the transmitter inside the red line box. The two insets show the transmitter and receiver layouts. Except for the photodiodes, the other blocks are covered by the top metal to protect them from illumination, which significantly changes the transistor characteristics. Figure 10 shows the test setup, which consists of a laser driver (CLD1011LP, Thorlabs GmbH, Bergkirchen, Germany), a test board, a Field Programmable Gate Array development board (FPGA, Xilinx PYNQ-Z2, TUL Corporation, New Taipei City, Taiwan), an external receiver board, and electronic test equipment such as a power supply, spectrum analyzer, oscilloscope, and source meter. Experimental results for the SDM containing the on-chip photodiodes energy harvester and optical/RF transceiver are described below. The core electronic circuits of the receiver and transmitter areas are 127 × 85 μm^2 and 135 × 98 μm^2, respectively.

First, we show the experimental results that describe the optical receiver's performance characteristics. Then, we describe the integrated system's experimental results, which includes the transmitter, the optical receiver, and the energy harvester.

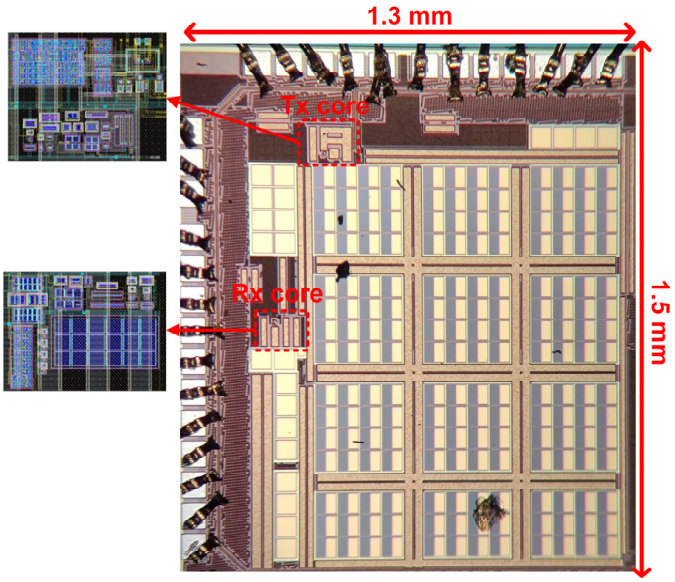


Figure 9. Microphotograph of the fabricated chip.

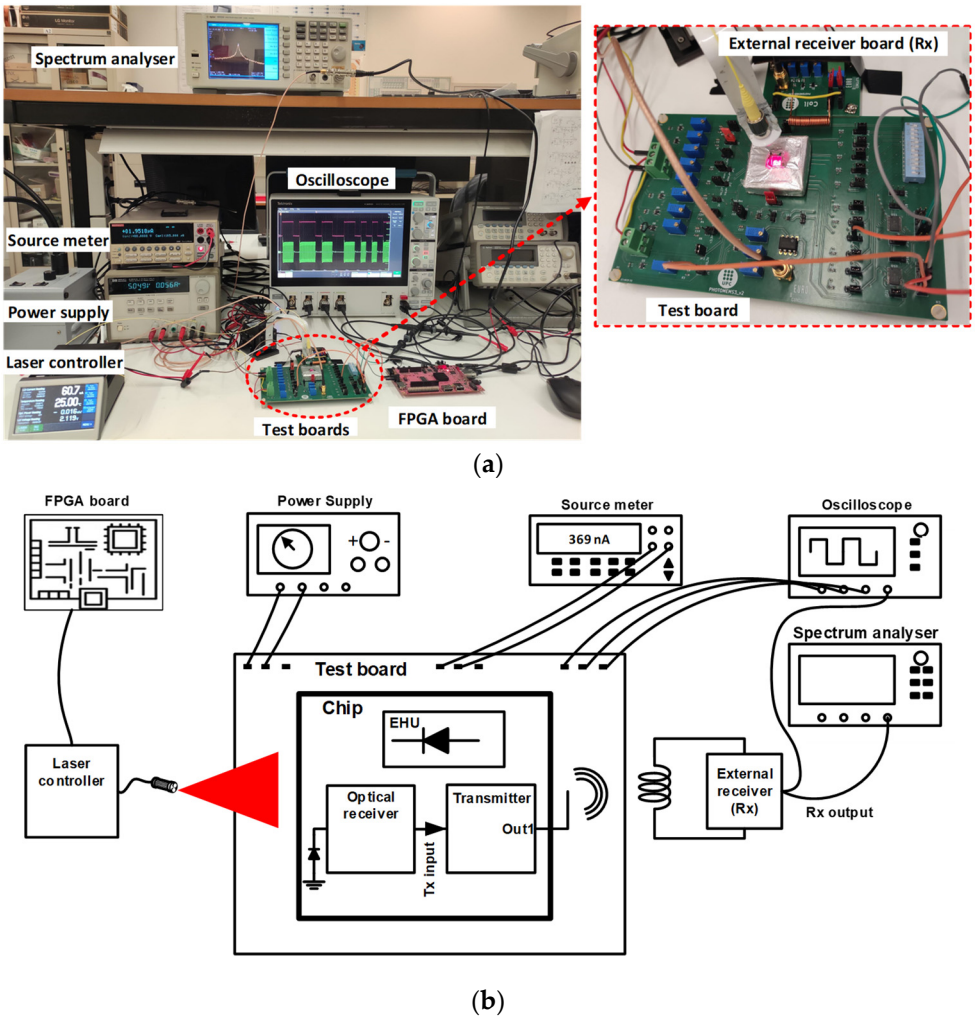


Figure 10. Test setup. (**a**) photograph and (**b**) block diagram.

3.1. Optical Receiver Performance

The optical receiver effectively operates within a supply voltage range of 0.9 V to 1.8 V. Throughout the measurement procedures, the chip is placed at a 2 cm distance from the laser source. It is important to note that the intensity of the laser light is a determining factor in the receiver's data capture capability. Therefore, the laser intensity can be adjusted according to the distance to provide sufficient power and signal intensity.

The experiment begins by applying a laser light modulated with a 255-long pseudo-random bit sequence encoded to prevent more than four consecutive identical bits, zeroes, or ones, to ensure a DC balance for the SICP. The bit pulse width is 50 µs, i.e., a data transmission rate of 20 kb/s. This sequence is fed into the laser controller to modulate the light for transmission. Figure 11 shows the FPGA pseudo-code used to measure the BER. Subsequently, the modulated light is focused on the chip through an optical fiber. It is important to mention that the modulation depth is defined by the ratio of the peak amplitude of this modulated waveform to its average DC level, and the standby DC level defines the maximum light intensity.

```
reset cnt // counts processed bits
reset BER // counts bit errors
generate and encode pseudo-random sequence t(254..0)
while (cnt <= 10^6 + 1)

    transmit bit t(cnt mod 255)
    receive bit r((cnt-1) mod 255) // The Tx-Rx analog system has a 50us delay, i.e. 1 bit
    if (cnt>1)
        if r((cnt-1) mod 255) != t((cnt-1) mod 255) then
            BER = BER + 1 // increase BER when an error occurs
    cnt = cnt + 1
end while
```

Figure 11. FPGA pseudo-code for the BER measurement.

Figure 12a shows the input waveform driving the laser controller and the corresponding output from the receiver, Vout. The driving signal is characterized by a 45 mV average DC level and a 35 mV peak amplitude corresponding to a modulation depth of approximately 80%. The observed delay of 40 µs between the modulated input signal and the output from the receiver is due to the electronic components of the laser controller. Across all the measurements, this delay is approximately 40 µs. The delay has been eliminated from subsequent figures for clarity in the comparison analysis. Figure 12b shows the receiver response to the same bit sequence waveform used in the previous plots but modulated to 10% depth. The results of these experiments validate the receiver's operational reliability throughout a modulation depth range from 10% to 80% with the same standby DC level.

Further tests were performed to evaluate the optical receiver's functionality at different standby DC levels, while the modulation depth remained at 18%. Figure 13 exhibits the comparison between the receiver response, depicted in blue waveforms, and the laser input signals, in red waveforms, for standby DC levels of 80 mV, 90 mV, and 100 mV in subplots (a), (b), and (c), respectively. This plot indicates that the receiver can effectively manage the variations in the current generated by the integrated photodiode and accordingly adjust for DC fluctuations. For a standby DC level of 80 mV and 18% modulation depth, the core of the optical receiver consumes 220 nW or 11 pJ/bit. However, the total power consumption of the optical receiver increases to 369 nW when including the pad ring, along with the additional current mirrors stage required for I_{bias} and I_{cp}, which are integrated by external current injection into the chip.

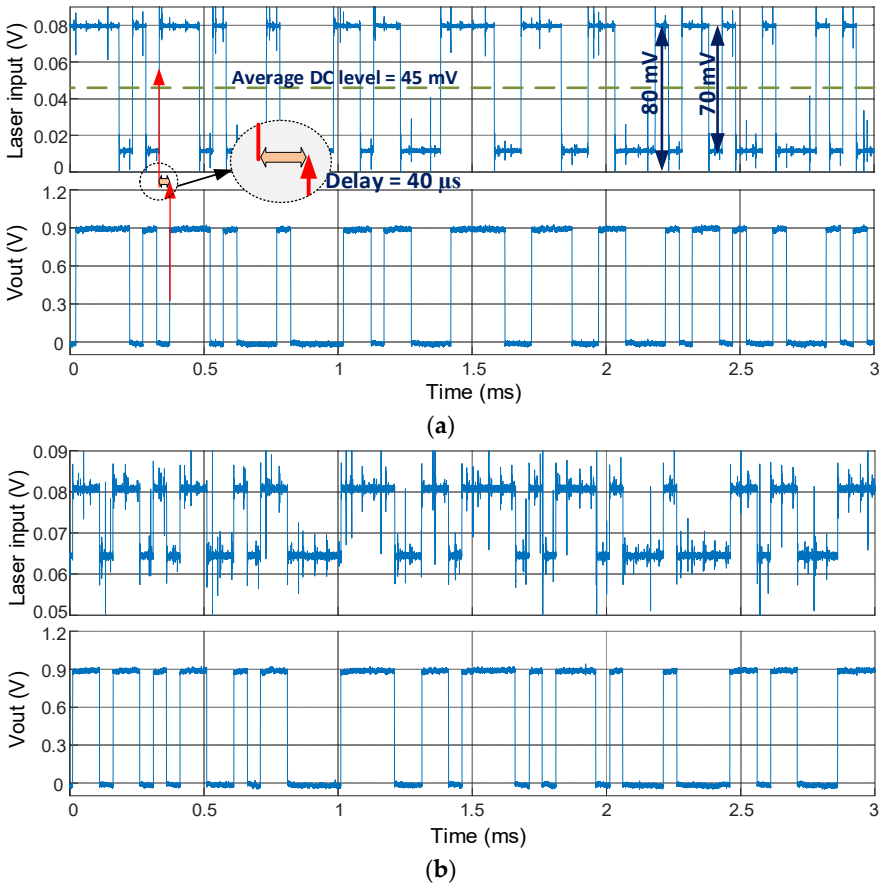


Figure 12. Measurement results of the optical receiver output, Vout, for modulated inputs, laser input, (**a**) with 80% and (**b**) 10% modulation depths and an 80 mV standby DC level.

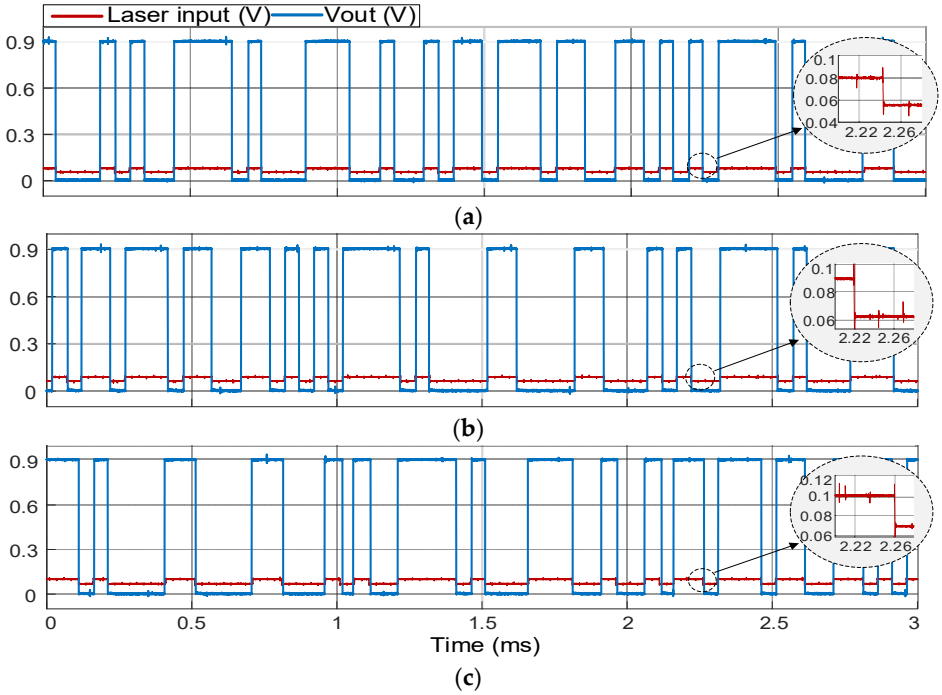


Figure 13. Measurement results of the optical receiver for the same pattern of the emitted data with 18% modulation depth and various standby DC levels: (**a**) 80 mV, (**b**) 90 mV, and (**c**) 100 mV.

The measured Bit Error Rate (BER) of the optical receiver analyzed for 10^6 transmitted bits across different values of modulation depth and laser intensity currents at a standby DC level of 80 mV are shown in Table 1 and Figure 14. The result indicates that lower laser intensity currents and lower modulation depths increase BER. Although the figure cannot display a BER of zero, as the scale used is logarithmic, the experimental results show that a modulation depth of 50% results in a BER of zero for laser intensity currents higher than 41 mA and for the run-length sequence. Additionally, by increasing the laser intensity current from 42 mA to 53 mA, the BER remained at zero for both modulation depths, highlighting a range of error-free operations. This interaction between the modulation depth and BER, which is affected by the laser intensity current, is critical for optimizing the optical communication system. Table 2 summarizes the results of the optical receiver in comparison to previous works.

Table 1. Measured BER for 30% and 50% modulation depths and various laser intensity currents.

Laser Intensity Current (mA)		**43**	**42**	**41**	**40**	**39**	**38**	**37**
BER	30%	0	0.0004	0.042	0.167	0.314	0.360	0.384
	50%	0	0	0.038	0.115	0.276	0.302	0.363

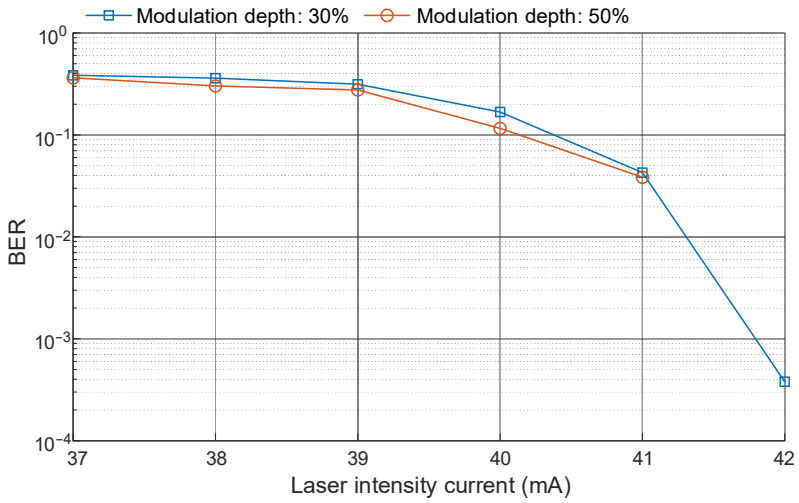


Figure 14. Measured BER, on a logarithmic scale, for different values of modulation depth and laser intensity currents. For both 50% and 30% modulation depths, the BER is zero at higher laser intensity currents, 41 mA and 42 mA, respectively.

Table 2. Optical receiver performance comparison with previous works.

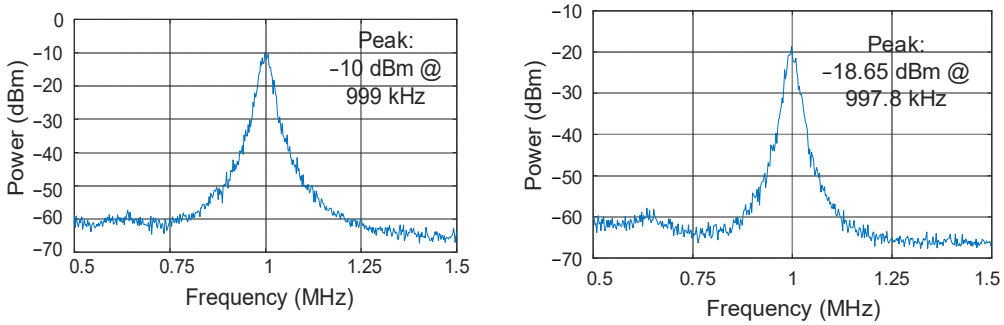
Parameter	**[5]**	**[23]**	**This Work**
Technology (nm)	180	-	180
Supply Voltage (V)	0.5–0.8	3	0.9–1.8
Modulation depth (%)	20	50	10–80
Data rate (b/s)	1 k	2.5 k	20 k
Power consumption (W) @ (J/bit)	20.3 n @ 20.3 p	174 µ @ 70 n	220 n @ 11 p
Fully integrated	Yes	No	Yes
Optical harvesting	Yes	Yes	Yes
Area (μm^2)	-	-	127 × 85

3.2. Transceiver Performance

In this subsection, we detail the experimental results of the SDM, which includes integrated photodiodes for energy harvesting and an optical/RF transceiver for communication. An external 1.2 V supply powers the modulator circuit and the DCO employed in the transmitter block. To validate the feasibility of supplying the power amplifier with the harvesting power source, two power source scenarios are used to provide a better view of their capabilities. The first scenario used an external power source set at 1.2 V, whereas the second employed an integrated power source derived from embedded light harvesters, 0.5 V. This experiment demonstrates that the SDM can properly operate using harvested light energy, thereby reducing its dependence on external power supplies.

Since the circuit is configured as a transceiver, the receiver's output is directly connected to the transmitter's input, "Data-in", as shown in Figure 6. A level shifter is then used to adjust the output signal level of the receiver from 0.9 V to 1.2 V, which is suitable for the operation of the transmitter.

The RF performance of the transmitter is evaluated by analyzing the signal received by an active antenna amplifier working as an external receiver (Rx) connected to a spectrum analyzer, where the transmitter antenna is positioned in the direction and inside the Rx coil. As a first evaluation of the transmitter's performance, an unmodulated 1 MHz signal is fed into the transmitter, ensuring a stable comparison between the externally power supplied circuit versus the harvested one. The power outputs corresponding the two power source scenarios are depicted in Figure 15a for the external supply and Figure 15b for the harvested supply. According to the figure, the difference is 8.65 dB, indicating that with the external power source, the emitted signal is 7.4 times stronger than the emitted signal with the harvesting source. This discrepancy is due to the different DC levels of the two power supplies.



(**a**) (**b**)

Figure 15. Experimental results of the received power from the transmitter (**a**) with 1.2 V and (**b**) with the generated power by the integrated photodiodes, 0.5 V.

Finally, modulated light was applied for concurrently transmitting data to the optical receiver and energy harvesting with the integrated photodiodes. At the same time, the optical receiver output was connected to the transmitter's modulation input. It should be noted that the modulated light used in the initial measurement step within the optical receiver is the same, but with a modulation depth of 30% and a standby DC level of 80 mV. Figure 16a–c depicts the signal received from the transmitter, which shows three distinct modulation schemes: OOK, BPSK, and FSK. Here, 'Tx input' refers to the input of the integrated transmitter, and 'Rx output' denotes the output of the external receiver. The measured results demonstrate that the transmitter effectively works for three different modulations, while harvesting power from modulated light. Figure 17 shows the measured power of the received signal for three different modulations. According to Figure 17c, the detected peaks of received power for an FSK modulation are at 995.6 kHz and 1.087 MHz, which are close to the designed carrier frequencies. Table 3 shows the power consumption of the transmitter for different modulations, for the same setup as in the previous experiment.

Based on the data presented in Table 3 and the power measurements detailed in Section 2.1, the harvested power by the integrated photodiodes is sufficient to continuously sustain the entire system's operations.

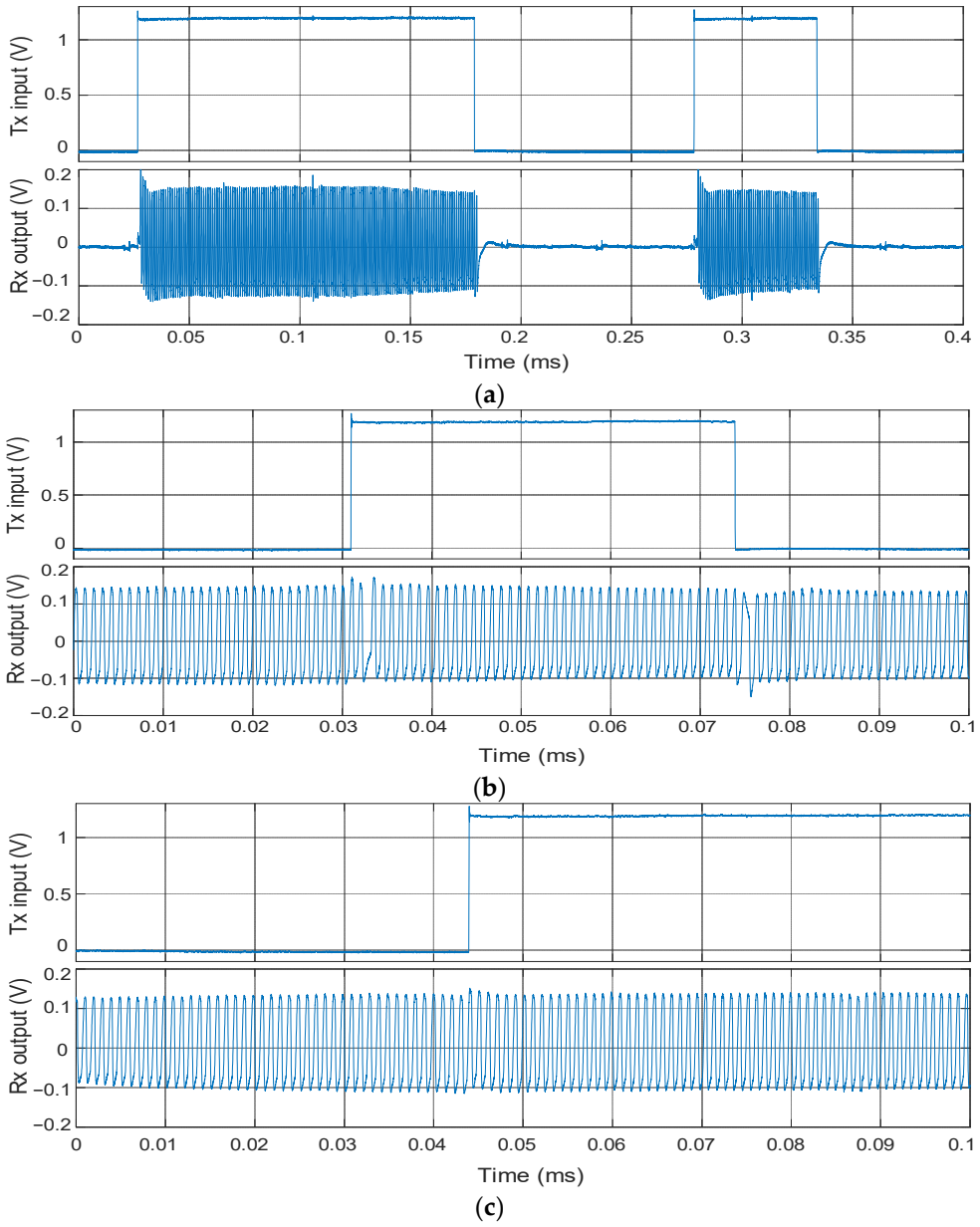


Figure 16. Experimental results of the received signal from the transmitter for different modulations: (**a**) OOK, (**b**) BPSK, and (**c**) FSK.

The measurements indicate that the external receiver can detect the radio signal when the antenna is located 3 cm from the coil. At this distance, there is an attenuation of approximately 34 dB in the received power from the transmitter for both the external and internal power supplies.

It should be noted that there is a trade-off between the harvested power and the modulation depth of the irradiated light. An increase in the modulation depth leads to a reduction in the average power that is harvested by the integrated photodiodes. Table 4 and Figure 18 illustrate the measured harvested power at various modulation depths for the same positive photodiodes discussed in Section 2.1, that is, a positive photodiodes matrix for a 240 $\times$ 240 μm^2 area. For the experiment, a square pulse wave with a pulse width of 50 µs and a standby DC level of 80 mV is applied to the laser driver. The maximum

measured power corresponded to a photodiode voltage of 0.42 V. According to Table 4 and Figure 18, there is a direct relationship between the harvested power and the average DC level of the signal applied to the laser driver. For example, the reduction in the harvested power between 10% and 80% modulation depths is approximately 35%, which is close to the proportion of their average DC levels, which is 37%.

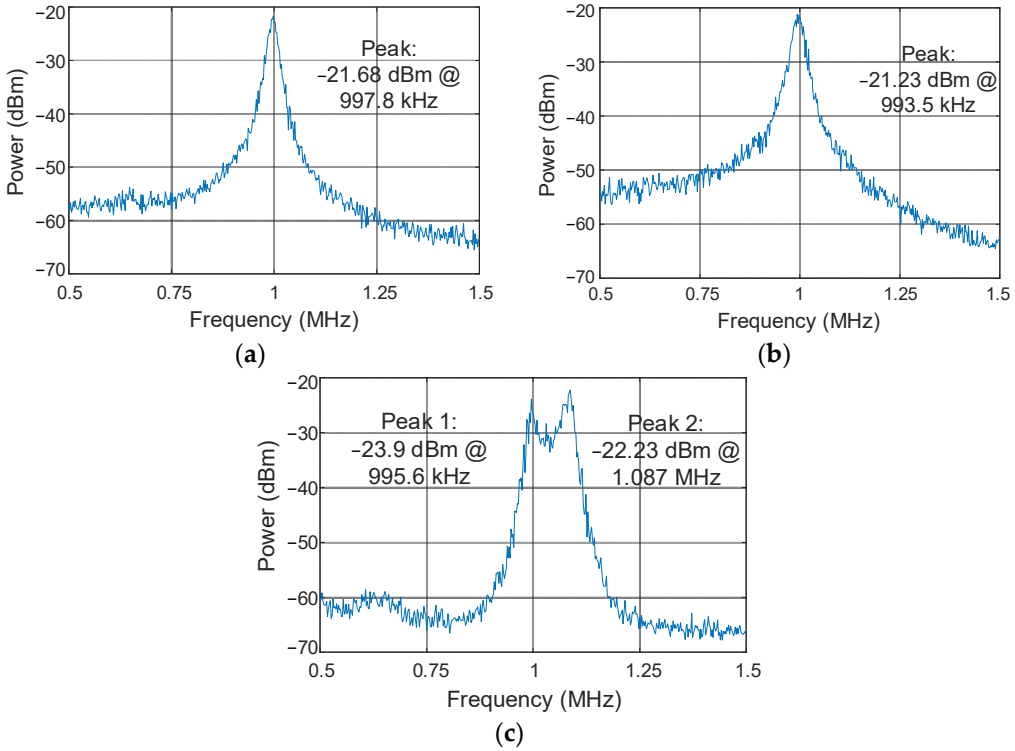


Figure 17. Experimental results of the received signal power from the transmitter for different modulations: (**a**) OOK, (**b**) BPSK, and (**c**) FSK.

Table 3. Transmitter power consumption for different modulations.

Modulation	OOK	BPSK	FSK
Power Consumption (μW)	2.34	3	3.24

Table 4. Trade-off between the measured harvested power and modulation depth. Direct relationship with the average DC level.

Modulation Depth (%)	10	30	60	80
Harvested power (μW)	0.63	0.517	0.439	0.405
Average DC level (mV)	72.5	60	50	45

Finally, the measured results presented in Figures 14 and 18 highlight a critical trade-off between modulation depth, BER, and harvested power. The results show that lower modulation depths lead to higher harvested power at the expense of increased BER and vice versa. Consequently, optimal system performance can be achieved by adjusting the modulation depth to balance both the BER and harvested power. For instance, a modulation depth of 30% is determined as the optimal point, where the system achieves a BER of zero and a maximum harvesting power of 6.7 μW.

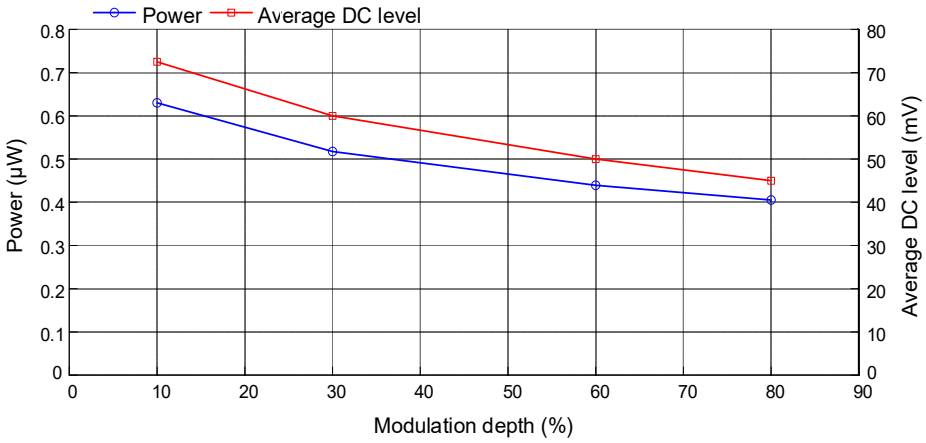


Figure 18. Illustration of the trade-off between the measured maximum harvested power and the modulation depth.

4. Conclusions

In this article, we propose a wireless hybrid transceiver communication circuit simultaneously powered by integrated photodiodes designed for SDM/IoT applications. Hybrid wireless communication enhances system performance by improving efficiency, reliability, and energy saving. Using a novel comparison method, the optical receiver operates at various modulation depths and standby DC levels, enhancing the correction of DC variations and offset of the comparator without the need for external tuning. The reconfigurable transmitter can manage OOK, BPSK, and FSK modulations. The experimental results demonstrate that the hybrid transceiver successfully operates with modulated data at a 20 kb/s data transfer rate and carrier frequencies of 1 MHz and 1.1 MHz. The measured results indicate that there is an interaction between the modulation depth, BER, and harvested power, which must be considered for the optimal operation of the system. The optimal point is at a 30% modulation depth, which yields a BER of zero and a harvested power of approximately 6.7 μW. This power is sufficient to simultaneously supply the full chip, including the wireless receiver and transmitter, which require 220 nW and 3.24 μW, respectively. The reported results open the way for proposing self-powered sensing chips operating as smart dust motes for future applications. The next phase of our research aims to integrate the reported circuits into a comprehensive system embedding payload applications. This system will include a DCPU, an advanced EHU, and a range of sensors, namely temperature, humidity, and various MEMS types. Potential applications include a wide range of areas, such as implantable biomedical devices, environmental monitoring, and robots, among others.

Author Contributions: Conceptualization, S.N., D.F. and J.C.-V.; methodology, S.N. and D.F.; software, S.N., J.C.-V., D.F. and I.S.-L.; validation, S.N., J.C.-V. and D.F.; formal analysis, S.N. and D.F.; investigation, S.N. and D.F.; resources, J.M.; data curation, S.N. and D.F.; writing—original draft preparation, S.N.; writing—review and editing, J.C.-V., J.M. and D.F.; visualization, S.N. and D.F.; supervision, J.C.-V., D.F. and J.M.; project administration, J.M.; funding acquisition, J.M. All authors have read and agreed to the published version of the manuscript.

Funding: Research funded by MCIN/AEI/10.13039/501100011033, grant number PID2021-123535OB-I00 and by ERDF A way of making Europe. In addition, funded by FPI scholarship from the Spanish Ministry of Science and Innovation, grant number PRE2019-088125.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: Author Daniel Fernández was employed by the company Wiyo Technologies. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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