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A 0.5-V Four-Stage Amplifier Using Cross-Feedforward Positive Feedback Frequency Compensation

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Abstract: This paper presents a low-voltage CMOS four-stage amplifier operating in the subthreshold region. The first design technique includes the cross-feedforward positive feedback frequency compensation (CFPFC) for obtaining better bandwidth efficiency in a low-voltage multi-stage amplifier. The second design technique incorporates both the bulk-drain-driven input stage topology in conjunction with a low-voltage attenuator to permit operation at a low voltage, and improves the input common-mode range (ICMR). The proposed circuit is implemented using TSMC-40 nm process technology. It consumes 0.866 µW at a supply voltage of 0.5 V. With a capacitive load of 50 pF, this four-stage amplifier can achieve 84.59 dB in gain, 161.00 kHz in unity-gain bandwidth, 96 deg in phase margin, and 5.7 dB in gain margin whilst offering an input-referred noise of 213.63 nV/$\sqrt{\text{Hz}}$ @1 kHz, small-signal power-bandwidth FoM_{ss} of 9.31 (MHz·pF/µW), and noise-power per bandwidth-based FoM_{npb} of 1.15 × 10^{-6} ((µV/$\sqrt{\text{Hz}}$)·µW/Hz). Compared to the conventional bulk-driven input stage design technique, it offers improved multi-parameter performance metrics in terms of noise, power, and bandwidth at a compromising tradeoff on ICMR with respect to bulk-driven amplifier design. Compared with conventional gate-source input stage design, it offers improved ICMR. The amplifier is useful for low-voltage analog signal-processing applications.

Keywords: multi-stage amplifier; positive frequency compensation; feedforward compensation; low power; low noise; subthreshold; bulk-drain-driven; rail-to-rail amplifier

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1. Introduction

With the trend of integration as well as low-voltage low-power implementations, high-gain, high-swing circuits are important building blocks in integrated circuits and systems. These are particularly useful for applications in the Internet-of-Things [1–3] or energy-harvesting circuits [4] that produce the usual low-voltage supply sources. Not only do these high-gain and high-swing circuits enhance weak signals in the amplification process under low-voltage environment, they also provide compatibility with other low-voltage circuit blocks. As such, good quality analog signal processing is maintained.

The bulk-driven configuration is frequently employed as the input stage in rail-to-rail circuits due to its ability to enhance the common mode range under very-low-voltage designs. However, the bulk-driven approach exhibits a reduced transconductance (g_m), narrower bandwidth, and higher level of leakage current and noise, which may degrade the circuit's performance as the design tradeoff.

For low-voltage design, many multi-stage amplifier topologies [5–9] are well reported. However, in the context of amplifiers realized by advanced technology nodes, the usual gain factor in an amplification stage becomes ineffective due to the problem of output resistance encountered by MOS devices. As such, the increase in the number of stages is unavoidable to meet high gain purposes. This leads to increased complexity in frequency compensation. The price paid for this may be a large tradeoff in the performance metrics pertaining to power consumption and gain bandwidth. The first motivation of this work

is to devise the frequency compensation that supports high-gain multi-stage design for precision advantages whilst offering reasonably good power–bandwidth performance metrics under the category of very-low-voltage rail-to-rail amplifier design, with a ≤0.5 V supply as an example. The second motivation of this work is to devise a rail-to-rail circuit topology that supports high-swing properties under very-low-voltage operation whilst simultaneously providing improved performance metrics in terms of noise, power, and bandwidth. Such performance metrics are crucial factors that indicate the analog signal processing quality being handled by the amplifier under very-low-voltage operation environments.

2. Review of Frequency Compensation and Low-Voltage Amplifier Topologies

2.1. Review of Frequency Compensation in Three-Stage Amplifier Topologies

Nested Miller compensation (*NMC*) [6,8] is a popular scheme for high gain amplifier design with good stability with respect to single Miller compensation (*SMC*) [6]. Figure 1 depicts the *NMC* configuration for a three-stage amplifier. In principle, *NMC* can be expanded to an infinite number of stages. However, with more than three stages, the bandwidth is significantly jeopardized.

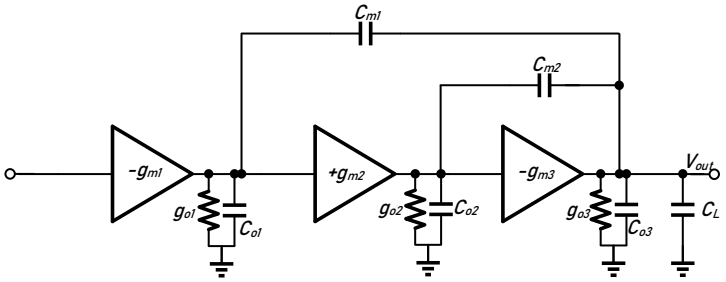

Figure 1. Topology of a three-stage *NMC* amplifier.

Referring to Figure 1, $g_{m1\text{-}3}$ are the transconductance of the three-stage amplifier. $g_{o1\text{-}3}$ are the output conductance of the amplifier. $C_{o1\text{-}3}$ are the output capacitance of the amplifier, and C_{m1} and C_{m2} are the two compensation capacitors of the *NMC* amplifier. Assuming $g_{m3} >> g_{m1}$,g_{m2}, the transfer function for a three-stage *NMC* amplifier is obtained as

$$A_{NMC}(s) = \frac{A_o\left(1 - s\frac{C_{m2}}{g_{m3}} - s^2\frac{C_{m1}(C_{m2}+C_{o2})}{g_{m2}g_{m3}}\right)}{\left(1 + \frac{sC_{m1}g_{m2}g_{m3}}{g_{o1}g_{o2}g_{o3}}\right)\left(1 + s\frac{C_{m2}}{g_{m2}} + s^2\frac{C_L C_{m2}}{g_{m2}g_{m3}}\right)} \tag{1}$$

In order to eliminate the peak effect of high-order complex poles, the polynomial is approximated by the Butterworth expression [9]. This is given as follows:

$$\begin{aligned} H_{butterworth}(s) &= \frac{A_{butterworth}(s)}{1+A_{butterworth}(s)} = \frac{1}{1+s\left(\frac{2}{w_0}\right)+s^2\left(\frac{2}{w_0^2}\right)+s^3\left(\frac{1}{w_0^3}\right)} \\ A_{butterworth}(s) &= \frac{1}{s\frac{2}{w_0}\left[1+s\left(\frac{1}{w_0}\right)+s^2\left(\frac{1}{2w_0^2}\right)\right]} \end{aligned} \tag{2}$$

Relating the *Butterworth* expression $A_{butterworth}(s)$ and the *NMC* expression $A_{NMC}(s)$, we obtain

$$C_{m1} = 4\left(\frac{g_{m1}}{g_{m3}}\right)C_L \tag{3}$$

$$C_{m2} = 2\left(\frac{g_{m2}}{g_{m3}}\right)C_L \tag{4}$$

Then the unity-gain bandwidth (*UGB*) and phase margin *PM* become

$$GBW_{NMC}(s) = \frac{1}{4}\left(\frac{g_{m3}}{C_L}\right) \tag{5}$$

$$PM_{NMC} \approx 60^{\circ} \tag{6}$$

Alternatively, Positive Feedback Compensation (*PFC*) [10] can be used to provide control of the damping ratio of the complex poles, which is achieved through capacitor C_{m2}. This capacitor, considerably smaller than C_{m1}, does not cause the significant slew rate (SR) reduction associated with the first stage whilst additionally generating a LHP zero to enhance the *PM*. The *PFC* topology is depicted in Figure 2. Of particular note, $g_{m1\text{-}3}$ are the transconductance of the three-stage amplifier. $g_{o1\text{-}3}$ are the output conductance of the amplifier. $C_{o1\text{-}3}$ are the output capacitance of the amplifier, and C_{m1} and C_{m2} are the two compensation capacitors of the *PFC* amplifier.

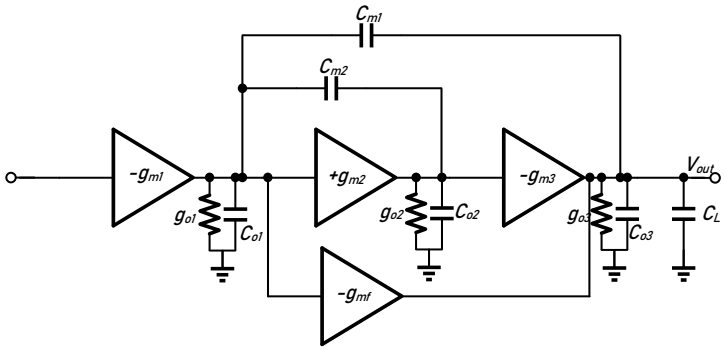

Figure 2. Topology of a three-stage *PFC* amplifier.

The transfer function of the *PFC* amplifier is given as follows:

$$H_{PFC}(s) = \frac{g_{m1}g_{m2}g_{m3}R_1R_2R_L\left(1 + \frac{2C_{m2}}{g_{m2}}s - \frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}s^2\right)}{(1 + sC_{m1}g_{m2}g_{m3}R_1R_2R_L)\left(1 + \frac{C_{m2}(2g_{m3}C_{m1} - g_{m2}C_L)}{g_{m2}g_{m3}C_{m1}}s + \frac{C_L(C_{m2} - c_{o2})}{g_{m2}g_{m3}}s^2\right)} \tag{7}$$

In order for all poles to be located in the left half plane, each term in the denominator must be greater than 0. This leads to the following design relationship:

$$2g_{m3}C_{m1} - g_{m2}C_L > 0 \rightarrow C_{m1} > \frac{g_{m2}}{2g_{m3}}C_L \tag{8}$$

$$C_{m2} - c_{o2} > 0 \rightarrow C_{m2} > c_{o2} \tag{9}$$

Thus, the *GBW* is obtained as follows:

$$GBW_{PFC}(s) = \frac{1}{4}\left(\frac{g_{m3}}{C_L}\right) \cdot \frac{7}{2}\sqrt{\left(\frac{g_{m2}}{g_{m3}}\right)\left(\frac{C_L}{C_{m2} - c_{o2}}\right)} \tag{10}$$

and the *PM* becomes

$$PM_{PFC} = 60^{\circ} + \tan^{-1}\left(\frac{GBW}{|Z_1|}\right) - \tan^{-1}\left(\frac{GBW}{|Z_2|}\right) > 60^{\circ} \tag{11}$$

Another *ASMIHF* compensation topology [11] is depicted in Figure 3. It employs an active single-Miller capacitor and an inner half-feedforward stage so that it facilitates the stabilization of a three-stage amplifier that is able to drive substantial capacitive loads. This is accomplished through the incorporation of a small feedback compensation capacitor and the utilization of two left LHP zeros. *ASMIHF* contributes to reduced silicon die

area occupation, streamlined design complexity, and enhanced small and large signal performance metrics. In addition, two supplementary and cost-effective feedforward stages, with transconductances g_{mf1} and g_{mf2}, are employed to enhance stability and achieve a dual-active push–pull operation. g_{mc1} is the active feedback stage. In conjunction with the gain A_{v2} of the second stage, it relates ω_o and Q in the complex equation. This may affect the circuit stability if not properly designed.

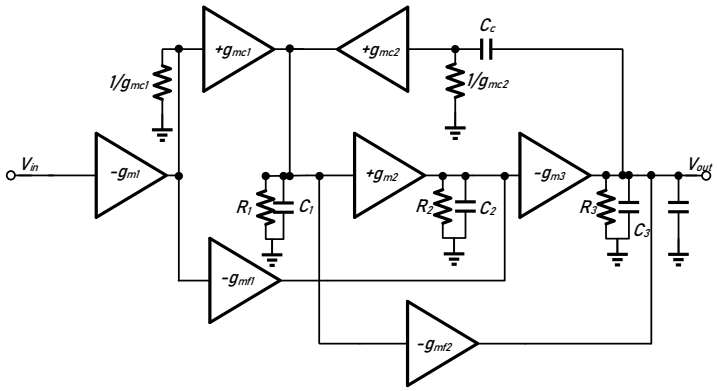

Figure 3. Topology of a three-stage *ASMIHF* amplifier.

The transfer function of the *ASMIHF* amplifier is given as follows:

$$H_{ASMIHF}(s) = \frac{-g_{m1}R_1g_{m2}R_2g_{m3}R_3}{(1+R_1g_{m2}R_2g_{m3}C_Cs)} \cdot \frac{\left(1+\frac{C_C}{g_{mc1}}s\right)\left(1+\frac{g_{mf1}C_1}{2g_{m2}g_{mc1}}s\right)\left(1+\frac{g_{mf2}g_{mc2}C_2}{g_{mf1}g_{m1}g_{m3}}s\right)}{\left(1+\frac{s}{\omega_n \cdot Q}+\frac{s^2}{{\omega_n}^2}\right)(1+R_2C_2s)} \tag{12}$$

where $\omega_n = \sqrt{\frac{g_{m3}g_{mc1}A_2}{C_LC_1}}$ and $Q = C_C\sqrt{\frac{g_{m3}A_2}{g_{mc1}C_LC_1}}$. To obtain a smooth characteristic curve similar to Butterworth's third-order response, Q is assumed to be $\frac{\sqrt{3}}{2}$ as an example. This gives $g_{mc1} = 2g_{m1}$, $g_{mc2} = \frac{3}{2}g_{m1}\frac{g_{mf1}C_1}{g_{mc2}C_c}$, and $C_C = \sqrt{\frac{3}{2}\frac{g_{m1}C_LC_1}{g_{m3}A_2}}$, respectively, and the *GBW* is $\frac{g_{m1}}{C_C}$. Due to the existence of g_{mc1} and g_{mc2}, this combination with the load transistor will inevitably form a cascode structure. Therefore, the structure is not suitable for working at a low supply voltage.

2.2. Review of Frequency Compensation in Four-Stage Amplifier Topologies

Similar to the three-stage op-amp topology, multiple nested Miller compensation [12] is a traditional frequency compensation method in four-stage op-amp design. The multiple nested Miller compensation topology is depicted in Figure 4.

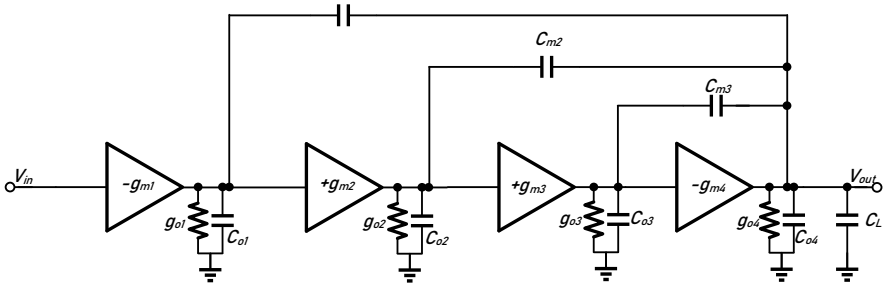

Figure 4. Topology of a four-stage multiple nested Miller compensation amplifier.

Regarding the topology, $g_{m1\text{-}4}$ are the transconductances of the four-stage amplifier. $g_{o1\text{-}4}$ are the output conductances of the amplifier, $C_{o1\text{-}4}$ are the output capacitances of the amplifier, and C_{m1}, C_{m2} and C_{m3} are the three compensation capacitors of the multiple *NMC*

amplifier. When dealing with a multi-stage operational amplifier, determining the precise location of nondominant poles can be tedious calculation. Without specific precautions, these poles may interact. Thus, they lead to complex pairs which cause stability issues. The basic rules for this amplifier design are given as follows:

$$\frac{G_{mi}}{C_i} \leq \frac{1}{2}\frac{G_{mi+1}}{C_{i+1}} \tag{13}$$

$$G_{mN} \gg G_{mi},\ i = 1,\ N-1 \tag{14}$$

where G_{mi} and C_i are the transconductance and compensation capacitor of the ith stage, respectively. The first stability condition, expressed in (14), requires that each nondominant pole be positioned at a frequency at least two times of the preceding one. The output of the first stage is assumed to contribute the dominant pole, while the outputs of the subsequent n – 1 stages produce the nondominant poles. Nevertheless, the fulfillment of (14) requires considerable constraint on the overall bandwidth of an amplifier when the number of stages increases. In the design of power operational amplifiers, (15) is readily fulfilled. This is attributed to the condition that the transconductance of the final stage must be larger than that of the preceding stages to effectively drive substantial loads.

Alternatively, the hybrid nested Miller compensation (*HNMC*) structure [13] or the hybrid cascode frequency compensation structure [14] can be used to further improve the achievable bandwidth of a four-stage op-amp. The hybrid nested Miller compensation (*HNMC*) structure, which is illustrated in Figure 5, has the feedback capacitors across their respective local inverting stages as well as across inverting multi-stages.

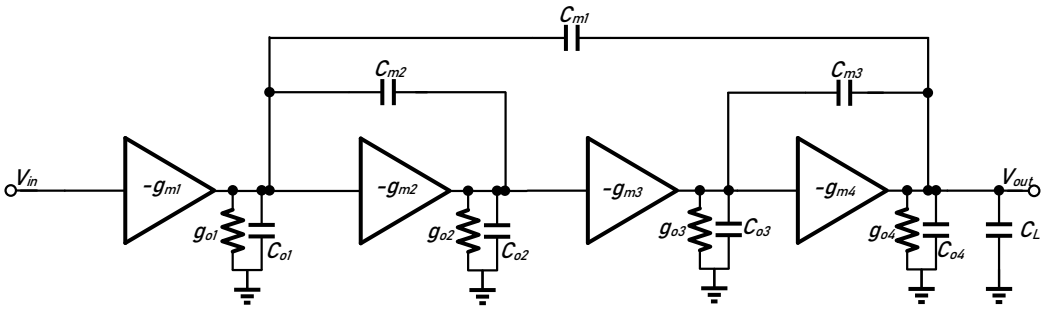

Figure 5. Topology of a four-stage *HNMC* amplifier.

As can be seen in Figure 5, two Miller loops involving C_{m2} and C_{m3} operate on the same nesting level. C_{m1} is also a compensation capacitor within the negative feedback loop. $g_{m1\text{-}4}$ are the transconductances of the four-stage amplifier. $g_{o1\text{-}4}$ are the output conductances of the amplifier. $C_{o1\text{-}4}$ are the output capacitances of the amplifier. An exemplary frequency compensation condition is achieved as follows:

$$\frac{g_{m3}C_{m1}}{C_{m1}C_{m2}} = \frac{1}{2}\frac{g_{m4}}{C_L} \tag{15}$$

where C_L is the load capacitor. At this juncture, according to (14), the unity-gain frequency of the op-amp can be obtained as follows:

$$\omega_t = \frac{g_{m1}}{C_{m1}} \leq \frac{1}{4}\frac{g_{m4}}{C_L} \tag{16}$$

where ω_t is the unity-gain frequency of op-amp. Compared with the $\omega_t = \frac{1}{2}\frac{g_{m4}}{C_L}$ of single Miller compensation (*SMC*), *HNMC* has only two nested levels, and thus the bandwidth is reduced by half. If multiple nested Miller compensation is used, since it has three nested levels, its bandwidth will be reduced to a quarter of *SMC*.

Another typology, nested transconductance-capacitance compensation (*NGCC*) [15], is another way to improve the bandwidth of a four-stage op-amp. The *NGCC* is depicted in Figure 6.

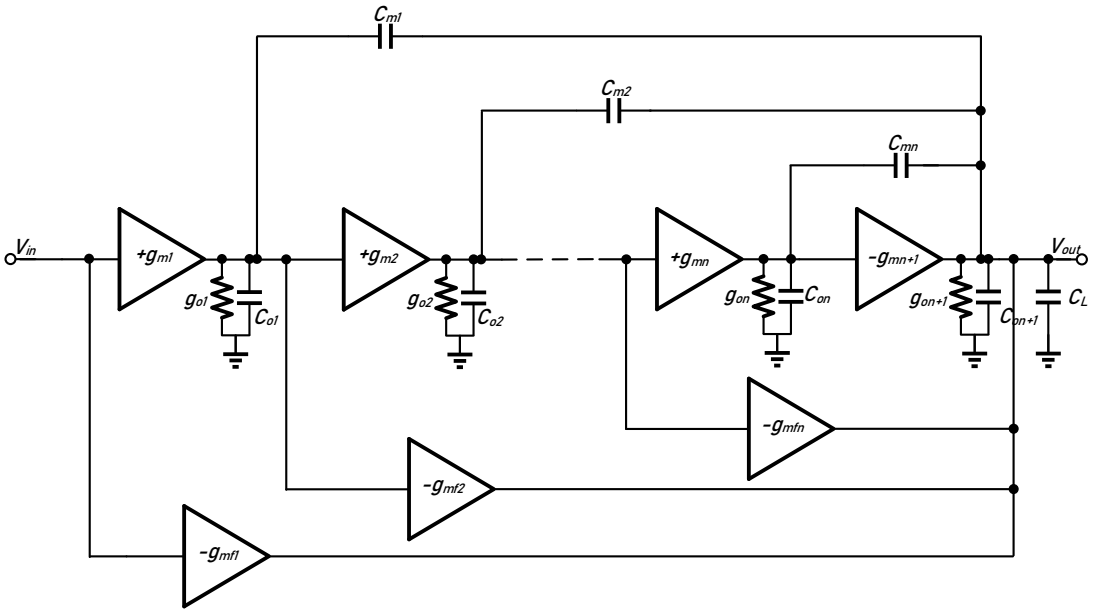

Figure 6. Topology of a four-stage *NGCC* amplifier.

In general, the *i*-th module comprises a transconductor g_{mi}, a feed-forward transconductor g_{mfi}, an output conductance g_{oi}, and a compensation capacitor C_{oi}. The DC voltage gain of the amplifier, as shown in Figure 6, is governed by the combined gain of the $n+1$ cascaded stages ($g_{m1}, g_{m2}, \ldots, g_{mn}, g_{mn+1}$). At high frequencies, when the gain of these stages decreases, the feed-forward transconductance g_{mf} bypasses all stages from $(i+1)$ to n, effectively extending the overall amplifier bandwidth. When $g_{mi} = g_{mfi}$, the transfer function of the *NGCC* amplifier can be obtained as follows:

$$\frac{V_o(s)}{V_i(s)} = \frac{-A_0}{(1 + A_0 \frac{s}{f_1})(1 + \frac{s}{f_2} + \frac{s^2}{f_2 f_3} + \ldots + \frac{s^{n-1}}{\prod_{i=2}^{n} f_i})} \tag{17}$$

where $A_0 = \prod_{j=2}^{n} \frac{g_{mj}}{g_{oj}}$ and $f_i = \frac{g_{mi}}{C_{mi}}$. The stability conditions for the *NGCC*-based topology are determined by applying the Routh stability criterion to the unity-gain closed-loop transfer function. This yields the following stability criteria:

$$f_4 > f_2 \frac{1}{(1 - \frac{f_1}{f_3})} \tag{18}$$

On the contrary, the stability conditions for multistage *NMC* amplifiers introduces complexity to the design process. On the other hand, when designing a stable multistage *NGCC* amplifier, it is more straightforward.

By comparing the bandwidth of a four-stage *NGCC* amplifier with that of an *NMC* amplifier and taking frequency normalization with respect to the gain bandwidth (*GBW*), the following can be obtained:

$$\frac{f_4}{GBW} = \frac{f_4'}{GBW'} - \frac{f_2' + f_3'}{GBW'} \tag{19}$$

where f_4 and *GBW* are the cut-off frequency and gain-bandwidth product of final stage of *NGCC* amplifier, respectively, whereas f_2', f_3', f_4' and GBW' are the cut-off frequencies of

the 2, 3, 4 stages and gain-bandwidth product of the final stage of the four-stage *NGCC* amplifier, respectively. Equation (20) implies that $\frac{f_4}{GBW} < \frac{f_4'}{GBW'}$, which means the *GBW* of *NGCC*, is greater than that of *NMC* for the same power ($f_4 = f_4'$). However, all feedforward paths of *NGCC* are connected to the output of the last stage, which leads to an increase in power consumption.

To achieve higher power efficiency, separate Miller compensation [16], alternative modified topology [17], or active parallel compensation (*APC*) [18] have been used. Figure 7 shows the separating Miller compensation with feedforward path (*SMF*) [16].

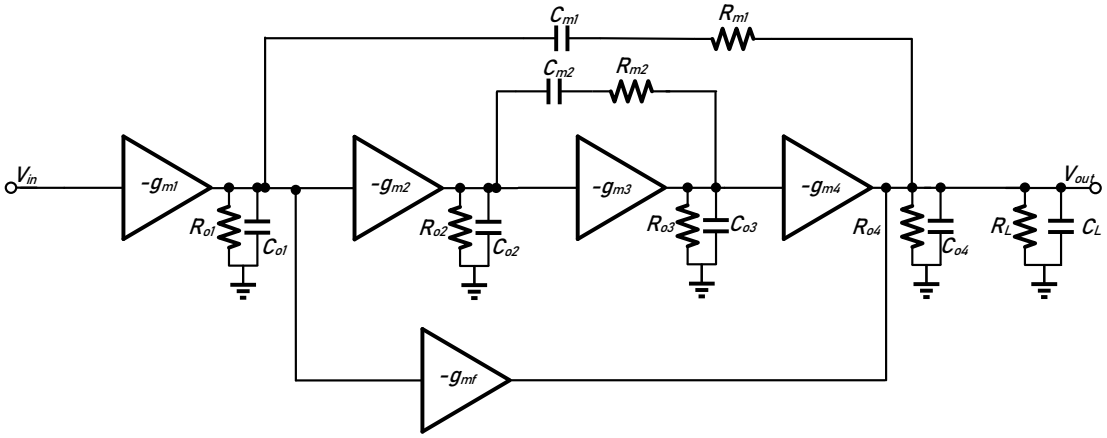

Figure 7. Topology of a four-stage *SMF* amplifier.

It is noted that g_{mi}, R_{oi}, and C_{oi} represent the transconductance, output resistance, and capacitance of the nth stage, respectively. The feedforward stage is denoted by g_{mf}. R_L and C_L indicate the load resistance and capacitance, including the output resistance and capacitance of the final stage. The compensation capacitors are C_{m1} and C_{m2}, while the nulling resistors are R_{m1} and R_{m2}. C_{m1} and R_{m1} together form the primary Miller compensation signal path for the entire amplifier. A secondary Miller compensation signal path is established by C_{m2} and R_{m2}. The transfer function of the four-Stage SMF amplifier is obtained as follows:

$$A_v(s) = A_{DC} \cdot \frac{1 + N_1 s + N_2 s^2 + N_3 s^3}{(1 + \frac{s}{p_0})(1 + D_1 s + D_2 s^2 + D_3 s^3)} \tag{20}$$

where

$$A_{DC} = g_{m1} g_{m2} g_{m3} g_{m4} R_{o1} R_{o2} R_{o3} R_L \tag{21}$$

$$N_1 = R_{m1} C_{m1} + C_{m2}[\left(R_{m2} - \frac{1}{g_{m3}}\right) + \frac{g_{mf}}{g_{m2} g_{m4}}] \tag{22}$$

$$N_2 = C_{m1} C_{m2}[R_{m1}\left(R_{m2} - \frac{1}{g_{m3}}\right) + \frac{g_{mf} R_{m1} - 1}{g_{m2} g_{m4}}] \tag{23}$$

$$N_3 = \frac{C_{o2} C_{m1} C_{m2}}{g_{m2} g_{m3} g_{m4}} (g_{mf} R_{m1} - 1) \tag{24}$$

$$p_0 = \frac{1}{C_{m1} g_{m2} g_{m3} g_{m4} R_{o1} R_{o2} R_{o3} R_L} \tag{25}$$

$$D_1 = C_{m2}[\left(R_{m2} - \frac{1}{g_{m3}}\right) + \frac{g_{mf}}{g_{m2} g_{m4}}] \tag{26}$$

$$D_2 = \frac{C_{m2} C_L}{g_{m2} g_{m4}} + \frac{g_{mf} C_2}{g_{m2} g_{m3} g_{m4}} (C_{m2} + C_{o3}) \tag{27}$$

$$D_3 = \frac{C_{o2}}{g_{m2}g_{m3}g_{m4}}\left[(C_{m2}+C_{o3})C_L + g_{mf}R_{m2}C_{o3}C_{m2}\right] + \frac{R_{m1}C_{o1}C_{m2}C_L}{g_{m2}g_{m4}} \quad (28)$$

To enhance push–pull behavior, the nulling resistor should be selected by the following design criteria. They are given as

$$R_{m1} = \frac{1}{g_{mf}} \quad (29)$$

$$R_{m2} \gg \frac{1}{g_{m2}}, \frac{1}{g_{m3}} \quad (30)$$

Then the *GBW* and *PM* can be obtained as follows:

$$GBW = \omega_0 = \frac{g_{m1}}{C_{m1}} \quad (31)$$

$$PM = 90 - tan^{-1}[\frac{R_{m1}C_{m1}\omega_0 + \left(D_1D_2 + R_{m1}C_{m1}\left({D_1}^2 - D_2\right)\right){\omega_0}^3}{1 + \left({D_1}^2 - D_2\right))\omega_0{}^2 - D_1D_2R_{m1}C_{m1}\omega_0{}^4}] \quad (32)$$

Separating the nested Miller compensation into two independent Miller compensation networks can improve the power efficiency of the op-amp. However, the compensation scheme may face design challenges in controlling the stability. This stems from the fact that it can only determine the position between the two poles, but not the position between the four poles. As a result, there may be overlap between multiple poles. When multiple poles coincide, there will be a stability problem and the bandwidth will be limited. In the case of ultra-low power design constraints, the extension of higher bandwidth becomes an issue.

In brief, multiple nested Miller compensation is one of the common frequency compensation methods. Because of its many nested levels and excessive capacitance, the bandwidth of the four-stage op-amp will be greatly limited and consume a larger area. According to (14), *HNMC* designed on the basis of multiple nested Miller compensation has fewer nested levels. By comparing this with *SMC*, the bandwidth attenuation that it brings is $\frac{1}{2}$ of the bandwidth attenuation by multiple nested Miller compensation. Furthermore, the realizable bandwidth of a four-stage *HNMC* amplifier can be designed the same as that of the three-stage *NMC* op-amp [15]. *NGCC* introduces a feedforward circuit and a Miller capacitor to work together for frequency compensation. It can be seen from (19) that *NGCC* can significantly increase the bandwidth, but this is at the expense of increased power consumption. Based on the review of these frequency compensation schemes, it is important to devise an effective frequency compensation that is suitable for an ultra-low-voltage four-stage amplifier design.

2.3. Review of Low-Voltage Rail-to-Rail Amplifier Circuits

The *bulk-driven* technique is widely used in low-voltage rail-to-rail circuit design, and the ICMR can offer 0–V_{dd} range. The two-stage *bulk-driven* rail-to-rail amplifier, which is realized in differential difference amplifier (DDA) [19] topology, is shown in Figure 8. Transistors M_{1A}-M_{1B} and M_{3A}-M_{3B} are the input differential pairs while the biasing circuit comprises the biasing transistor pairs M_{2A}-M_{2A}, M_{5A}-M_{5B}, M_{4A}-M_{4B}, and M_{6A}-M_{6B}. The cross-coupled transistors M_{7A} and M_{7B}, in association with the diode-connected transistors M_{8A} and M_{8B}, enhance the gain through partial positive feedback by introducing negative transconductance ($-g_{m7}$). Transistors M_{9A}, M_{9B}, M_{10A}, and M_{10B} form the differential to single-ended conversion for the first-stage gain. Transistors M_{11} and M_{12} form the second-stage gain with Miller capacitor C_C.

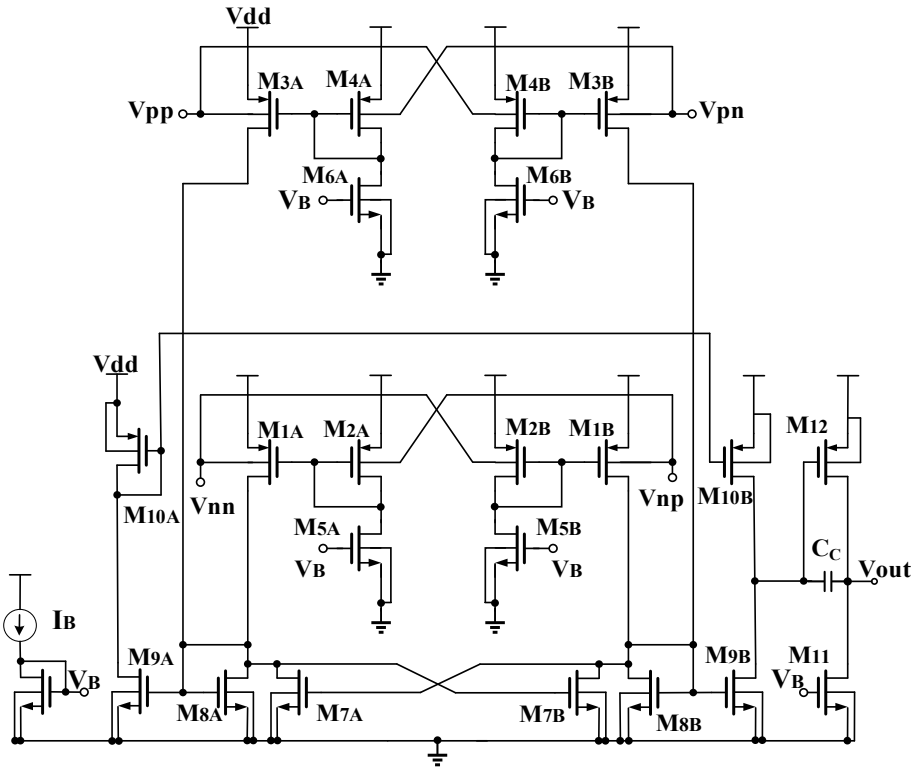

Figure 8. Bulk-driven rail-to-rail DDA circuit.

The gain of bulk-driven DDA is

$$A_{v\_bulk-driven} = \frac{g_{mi}}{g_{ds9} + g_{ds10}} \cdot \frac{g_{m12}}{g_{ds11} + g_{ds12}} \tag{33}$$

where

$$g_{mi} \cong 2g_{mb1,3} \frac{g_{m9}/g_{m8}}{\left(1 - \frac{g_{m7}}{g_{m8}}\right) + \frac{g_{ds1}+g_{ds3}+g_{ds7}+g_{ds8}}{g_{m8}}} \tag{34}$$

The *GBW* is

$$GBW_{bulk-driven} = \frac{g_{mi}}{2\pi C_C} \tag{35}$$

For bulk-driven circuits, g_{mbs} replaces g_m as the transconductance of the circuit. Since g_{mbs} is very small, the gain of the bulk-driven circuit is very small. The same goes for the gain-bandwidth product. As such, the thermal noise performance metric will be worse due to small transconductance in the front-end stage.

The traditional complementary gate-source input stage amplifier [20] is shown in Figure 9. It is regarded as one of the economical circuit techniques by utilizing a 1-to-3 current mirror. The design operates in the saturation region, with a supply voltage of 3.3V. $M_{1\text{-}4}$ are the input differential input pairs which are composed of complementary PMOS and NMOS transistors for rail-to-rail design. $M_{5\text{-}6,\,7\text{-}8}$ are the cascode transistors and $M_{15\text{-}16}$ are the current source transistors. $M_{10\text{-}11,\,13\text{-}14}$ are used to implement current mirrors with a 1-to-3 ratio for approximated constant g_m design.

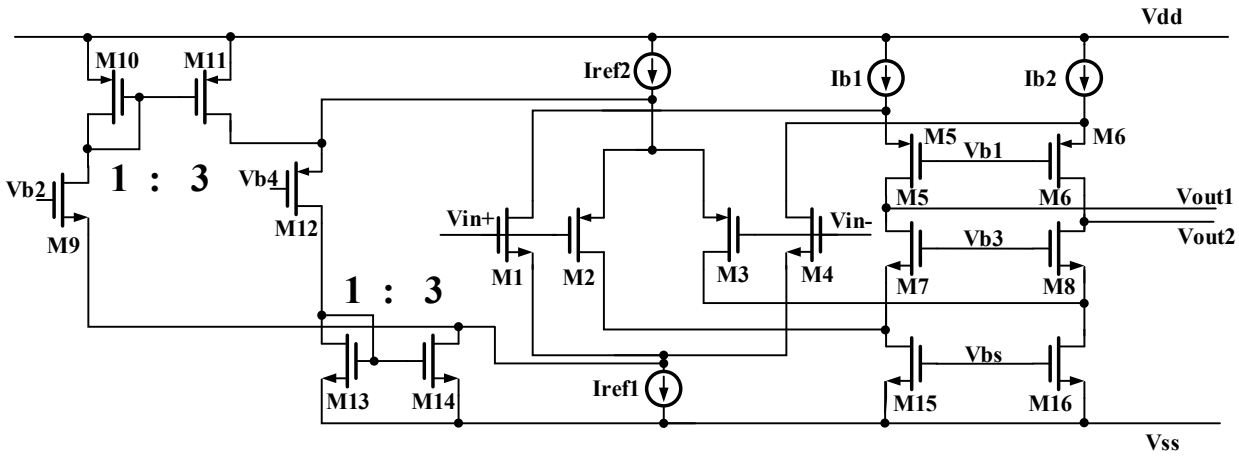

Figure 9. Gate-source driven rail-to-rail amplifier circuit with 3-to-1 ratio current mirror.

The overall transconductance of input stage is defined as

$$g_{mi} = \sqrt{\left(\frac{W}{L}\right)_n \mu_n C_{OX} I_{ref1}} + \sqrt{\left(\frac{W}{L}\right)_p \mu_p C_{OX} I_{ref2}} \tag{36}$$

where $I_{ref1,2}$ are the bias currents of the NMOS pair and PMOS pair, respectively. For complementary circuits without g_{mi} smoothing, the combined g_{mi} of the input stage under either the lower or upper part of common-mode range is half of the overall value. This will be double in value in the middle range. The same goes for unity-gain bandwidth. There are many ways to make the approximated constant g_{mi}. Alternatively, it can be achieved through the level shift approach [21], which relies on the input transistor pairs to operate in the saturation region. Similarly, it also offers less sensitivity on g_{mi} variation against the change of input signal. Unfortunately, when pushing for lower supply, the available signal headroom in conjunction with unavoidable output spikes through the variation of g_{mi} will be reduced. In poor conditions, the rail-to-rail circuit will be jeopardized in operation, and this will be particularly pronounced when the rail-to-rail complementary input pairs are biased in the sub-threshold region for obtaining low power purpose.

3. Proposed Four-Stage Amplifier with Cross-Feedforward Positive Frequency Compensation (CFPFC)

Figure 10 shows the circuit of the proposed four-stage amplifier in TSMC 40 nm process technology. The amplifier consists of a bias circuit, a bulk-drain transistor input stage, an attenuation stage, and a high-gain stage. The bias circuit consists of a supply-independent topology and a start-up network ($M_{B1\text{-}6}$, $C_{B1\text{-}2}$). For the input stage, it consists of the complementary topology which is embedded with the bulk-drain differential pairs ($M_{p1\text{-}2}$, $M_{n1\text{-}2}$) and the respective load transistors ($M_{3\text{-}6}$). This is then followed by the attenuation stage (M_{na1}-M_{na4}, $M_{7,\,8}$) in a source–follower-like topology, comprising two native transistors and one low-threshold transistor in each output of the first stage.

As mentioned before, the rail-to-rail input circuits, under a low supply voltage and a subthreshold operation region, can influence subsequent amplification stages through large variations in the first stage's output spike under high fluctuations of g_{mi}. Moreover, under limited supply, the IMCR becomes ineffective in the gate-source biased differential pairs despite the g_{mi} obtained from a gate-source biased transistor being relatively higher than that of a bulk-driven transistor.

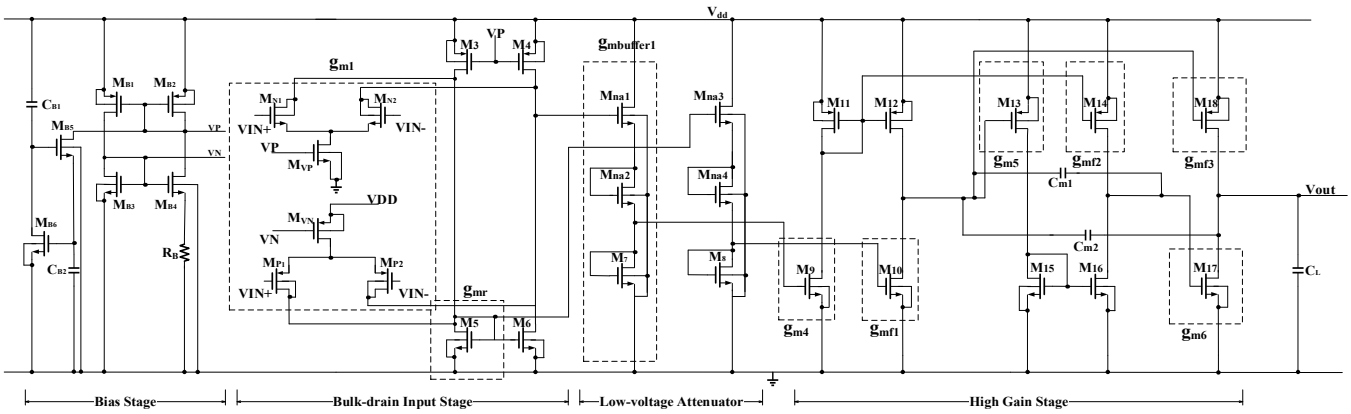

Figure 10. Circuit of the proposed amplifier.

Regarding the bulk-driven input stage, this has high ICMR capability through the use of g_{mb} as the main transconductance. However, its gain and driving capabilities are low. For this reason, the bulk-drain-driven [22] differential pairs are introduced to obtain the design tradeoff between the gate-source or bulk-driven techniques. This can offer an improved IMCR with respect to that of the gate-source driven technique, whilst the transconductance is not reduced significantly due to weak degeneration arising from bulk-drain transistor topology. As a result of this weak degeneration, the amplifier's parameters such as noise, gain, and bandwidth are still higher than that of bulk-driven circuits. Furthermore, in comparison with bulk-drain-driven circuits, the temperature effect of bulk-driven is less obvious [22]. As a result, the bulk-drain-driven circuit can provide a compromising design solution among the transconductance and signal swing in low-voltage design.

The use of native transistors (with negative threshold voltage) ensures low-voltage operation. As such, the use of diode-based transistors permits attenuation of any spike [22] that appears through the transition change of transconductance from the complementary differential pairs. This reduced spike will not overdrive the subsequent stage, thus does not jeopardize the amplification in the next circuit stage. In this way, it is economical to remove the conventional transconductance smoothing circuits [23–25]. This is particularly useful because it offers simplicity whilst reducing the power consumption and complexity as well as avoiding a higher supply in conventional methods.

After the low-voltage attenuator, it is the high-gain stage that drives the 50 pF capacitive load. This gain stage ($M_{9\text{-}20}$) contains two non-inverting amplifiers, one push–pull stage, three feed-forward paths, and the capacitors ($C_{m1\text{-}2}$) dedicated to the positive frequency compensation.

The cross-feedforward paths, with which to bypass the respective stage, enhance the bandwidth as well as the stability of the *PFC* amplifier. Furthermore, introducing a positive feedback loop effectively governs the damping ratio of the complex poles. This can be achieved by fulfilling the design equations for the compensation capacitors in subsequent transfer function analysis. By properly sizing the compensation capacitors, the usual RHP poles can be moved to LHP for stability. Furthermore, both *FF* and *PFC* yield LHP zeros to ensure stability in multi-stage amplifier design.

Figure 11 depicts the block diagram of the proposed four-stage amplifier. Assuming that the parasitic capacitances in each stage are neglectable, the open-loop transfer function of the amplifier is obtained as follows:

$$A_{CFPFC}(s) = \frac{A\left(1 + Bs + Cs^2 + Ds^3\right)}{(1 + Es + Fs^2 + Gs^3)(1 + Hs)(1 + Is)} \tag{37}$$

where

$$A = -R_1R_2R_4R_5R_6g_{m1}g_{m4}g_{m5}g_{m6}g_{mbuffer1}$$
$$B = \frac{C_{m2}g_{mf2}}{g_{m4}g_{m5}}$$
$$C = \frac{C_{m2}\left(C_5g_{m4}+C_{m1}g_{m4}+C_{m1}g_{mf2}\right)}{g_{m4}g_{m5}g_{m6}}$$
$$D = C_1C_{m1}C_{m2}R_1R_4R_5g_{mf1}$$
$$E = C_LR_6 - C_{m1}R_4R_5g_{m5} + C_{m2}R_4R_5R_6g_{m5}g_{m6}$$
$$F = R_4R_6\Big(C_LC_{m2} - C_LC_{m1}R_5g_{m5} + C_{m1}C_{m2}R_5g_{m5} + C_{m1}C_{m2}R_5g_{m6} + C_{m1}C_{m2}R_5g_{mf3}\Big)$$
$$G = C_LR_4R_5R_6(C_5C_{m2} + C_{m1}C_{m2})$$
$$H = C_1C_1$$
$$I = C_2R_2$$

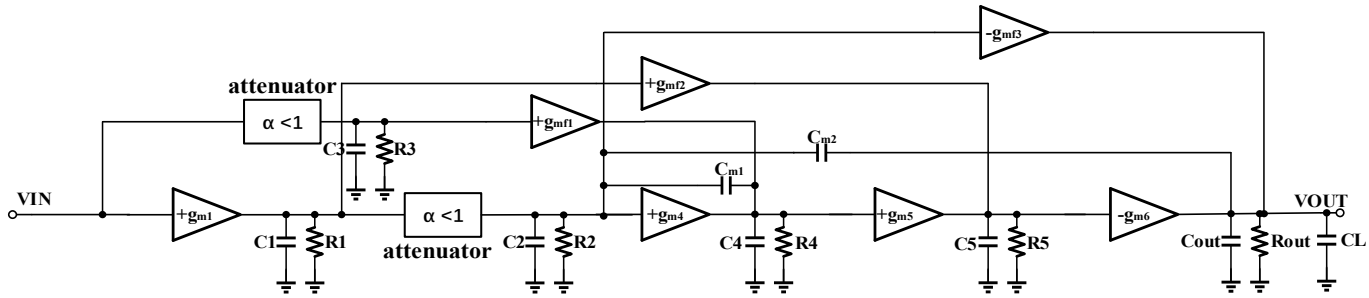

Figure 11. Block diagram of proposed amplifier.

For positive feedback compensation, the most important thing is to consider the instability which comes from two aspects:

1. There may be a RHP pole that causes oscillation;
2. The peak introduced by the existence of high-order complex polynomial.

In order to tackle the first issue, all the poles must be located in LHP. This requires each coefficient of the denominator to be greater than 0. Thus, we have

$$E > 0 \Rightarrow C_{m1} < \frac{C_LR_6 + C_{m2}R_4R_5R_6g_{m5}g_{m6}}{R_4R_5g_{m5}} \approx C_{m2}R_6g_{m6} \tag{38}$$

$$F > 0 \Rightarrow C_{m2} > \frac{C_LC_{m1}R_5g_{m5}}{C_L + C_{m1}R_5\Big(g_{m5} + g_{m6} + g_{mf3}\Big)} \approx C_{m1}R_5g_{m5} \tag{39}$$

This yields the need for a larger C_{m2} and a smaller C_{m1}. At this juncture, due to the introduction of the feedforward path, the compensation capacitor C_{m2} in the CFPFC amplifier can be made smaller than that in the PFC amplifier without a feedforward design. As a result, this achieves increased bandwidth while keeping a small area arising from the capacitors. Regarding the peak effect caused by the high-order complex pole equation, it is necessary to choose the damping ratio by controlling the ratio between C_{m1} and C_{m2} so as to permit the loop gain curve to be as smooth as possible. According to Butterworth Equations (2) and (3), it is necessary to arrange the higher-order complex pole equation into a similar form. Assuming $C_L \gg C_{m2} \gg C_{m1}$, the transfer function becomes

$$A_{CFPFC}(s) = \frac{A}{(1+Es)\Big(1+\frac{F}{E}s+\frac{G}{E}s^2\Big)(1+Hs)(1+Is)} \tag{40}$$

By replacing E, F, G with ω_0 and ω_n, we get

$$A_{CFPFC}(s) = \frac{A}{\frac{2}{\omega_0}s\left[1+\left(\frac{1}{\omega_0}\right)s+\left(\frac{1}{2\omega_0^2}\right)s^2\right](1+Hs)(1+Is)} \tag{41}$$

$$A_{CFPFC}(s) = \frac{A}{\frac{2\sqrt{2}}{\omega_n}s\left[1+(2\zeta)\left(\frac{1}{\omega_n}\right)s+\left(\frac{1}{\omega_n^2}\right)s^2\right](1+Hs)(1+Is)} \tag{42}$$

where ω_0 is the dominant pole, ω_n is the non-damped frequency. Therefore, the secondary poles are

$$|p_{2,3}| = \omega_n = \sqrt{2}\omega_0 \tag{43}$$

Then, with $\zeta = \frac{\sqrt{2}}{2}$, we can obtain the following relationship.

$$\frac{2}{\omega_0} = E \tag{44}$$

$$\frac{1}{\omega_0} = \frac{F}{E} \tag{45}$$

$$\frac{1}{2\omega_0^2} = \frac{G}{E} \tag{46}$$

By solving the above equations, we have obtained the design equations for the compensation capacitors and the dominant pole. They are given as follows:

$$C_{m1} = \frac{2}{R_5^2 g_{m5} g_{m6}} C_L \tag{47}$$

$$C_{m2} = \frac{2}{R_4 R_5^2 R_6 g_{m5}^2 g_{m6}^2} C_L \tag{48}$$

$$\omega_0 = \frac{R_5 g_{m5} g_{m6}}{C_L} \tag{49}$$

As a result, within the bandwidth, there is no peak effect caused by high-order complex poles. Since g_{m2} is derived from the attenuation buffer output (source output), its resistance R_2 is very small and so is the time constant R_2C_2. From (41), p_4 is $(1/I)$ and p_5 is $(1/H)$. These are high-frequency poles when compared with other poles. At this juncture, considering the main pole ω_0 and the secondary poles $\omega_{2,3}$, the expression can be obtained as follows:

$$GBW_{CFPFC} = \frac{\omega_0}{2} \tag{50}$$

$$PM_{CFPFC} = 180^\circ - tan^{-1}\left[\frac{GBW}{p_{-3dB}}\right] - tan^{-1}\left[\frac{2\zeta\left(\frac{GBW}{|p2.3|}\right)}{1-\left(\frac{GBW}{|p2.3|}\right)^2}\right] \approx 60^\circ \tag{51}$$

Incorporating the effect of higher frequency zero, z_1, the PM becomes

$$PM_{CFPFC} = 60^\circ + tan^{-1}\left(\frac{GBW}{|z_1|}\right) > 60^\circ \tag{52}$$

Figure 12 shows the pole-zero location of *CFPFC* op-amp. p_0 is the dominant pol, $p_{2,}$ p_3 are complex poles, and p_4, p_5 are the high-frequency poles produced by H and I in Equation (41). Of particular note, z_1, z_2, z_3 are the high-frequency LHP zeros caused by the feedforward paths and PFC. Through the stated design criteria for the compensation capacitors, the complex poles $p_{2,}$ p_3 are now moved to the LHP. The dimensions of each device are listed in Table 1.

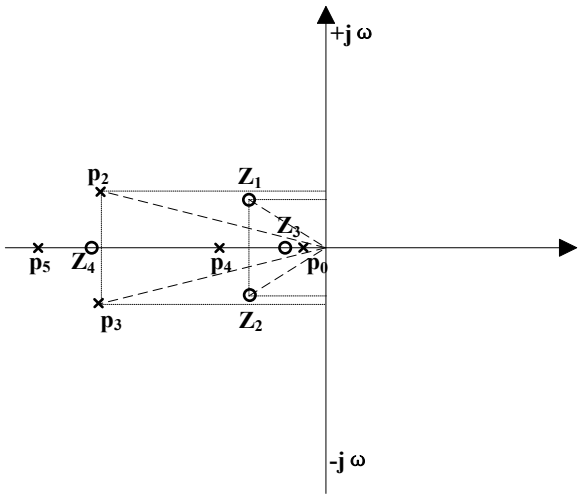

Figure 12. Pole-zero location in CFPFC op-amp.

Table 1. Device size of proposed amplifier.

Transistor	Size (Type)	Transistor	Size (Type)
M_{B1}	20/1 (1.1 V low V_{TH})	M_{B2}	20/1 (1.1 V low V_{TH})
M_{B3}	1.5/1 (1.1 V low V_{TH})	M_{B4}	12/1 (1.1 V low V_{TH})
M_{B5}	50/1 (1.1 V standard)	M_{B6}	1/1 (1.1 V standard)
C_{B1}	10 pF	C_{B2}	10 pF
R_B	4.2 MΩ		
M_{P1}	200/1 (1.1 V low V_{TH})	M_{P2}	200/1 (1.1 V low V_{TH})
M_{N1}	40/1 (1.1 V low V_{TH})	M_{N2}	40/1 (1.1 V low V_{TH})
M_3	16/1 (1.1 V low V_{TH})	M_4	16/1 (1.1 V low V_{TH})
M_5	1/7 (1.1 V low V_{TH})	M_6	1/7 (1.1 V low V_{TH})
M_{na1}	0.5/22 (2.5 V native)	M_{na2}	1/10 (1.1 V native)
M_{na3}	0.5/22 (2.5 V native)	M_{na4}	1/10 (1.1 V native)
M_7	50/1 (1.1 V low V_{TH})	M_8	50/1 (1.1 V low V_{TH})
M_9	70/1 (1.1 V low V_{TH})	M_{10}	72/1 (1.1 V low V_{TH})
M_{11}	4/1 (1.1 V low V_{TH})	M_{12}	4/1 (1.1 V low V_{TH})
M_{13}	13/1 (1.1 V low V_{TH})	M_{14}	16/1 (1.1 V low V_{TH})
M_{15}	3.57/1 (1.1 V low V_{TH})	M_{16}	3.57/1 (1.1 V low V_{TH})
M_{17}	1/1 (1.1 V low V_{TH})	M_{18}	16/1 (1.1 V low V_{TH})
C_{m1}	100 fF	C_{m2}	7 pF

4. Results and Discussion

The four-stage op-amp is designed and implemented using TSMC 40 nm CMOS process technology. The circuit operates at 0.5 V supply and drives the capacitive load of 50 pF.

Figure 13 shows the simulated DC gain, gain bandwidth (*GBW*), phase margin (*PM*), and gain margin (*GM*) of the proposed amplifier at different corners. At the tt corner, the corresponding values are 84.588 dB, 161 kHz, 96 degrees, and 5.7 dB. At the ss corner, the respective values are 88.2 dB, 65.9 kHz, 76.11 degrees, and 8.23 dB. At the ff corner, the respective values are 75.37 dB, 247.9 kHz, 101.66 degrees, and 11.94 dB. It can be observed that the amplifier is stable at all corners and maintains high gain despite some deviations in gain-bandwidth across the corners.

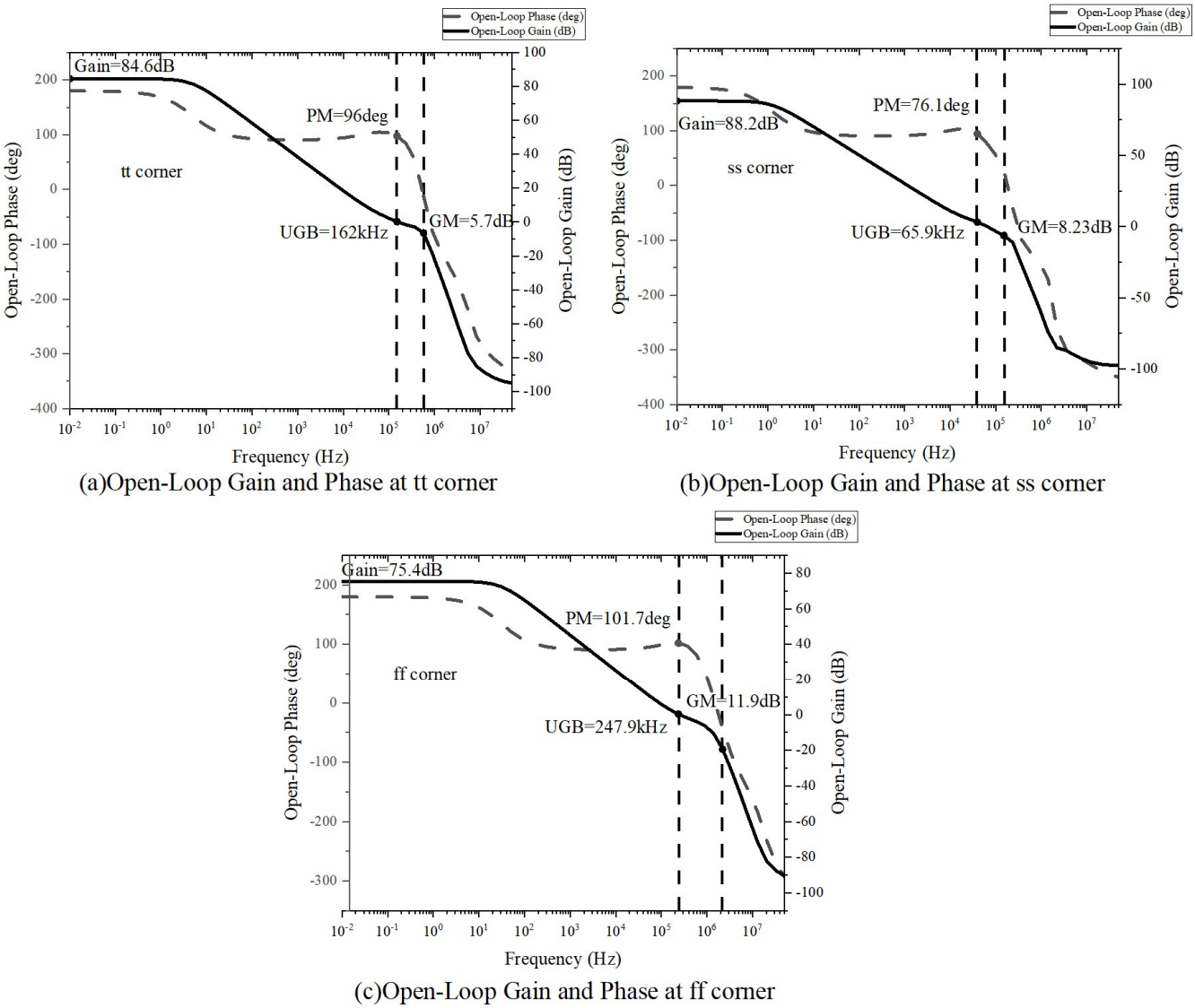

Figure 13. Open-loop gain under 50 pF load. (**a**) Open-loop gain and phase at tt corner. (**b**) Open-loop gain and phase at ss corner. (**c**) Open-loop gain and phase at ff corner.

Figure 14 depicts the power-supply gain of the proposed amplifier. These are obtained as −56.02 dB at tt, −61.35 dB at ss, and −43.37 dB at ff, respectively. Regarding the power supply rejection ratio (PSRR), the obtained values are 56.02 dB at tt, 61.35 dB at ss, and 43.37 dB at ff, respectively. Figure 15 depicts the common-mode gain of the proposed amplifier. These are −57.11 dB at tt, −66.76 dB at ss, and −42.61 dB at ff, respectively. These yield the common-mode rejection ratio (CMRR) of 57.11 dB at tt, 66.76 dB at ss, and 42.61 dB at ff, respectively. Due to the high differential-mode gain at low frequency, the obtained PSRR and CMRR values are high.

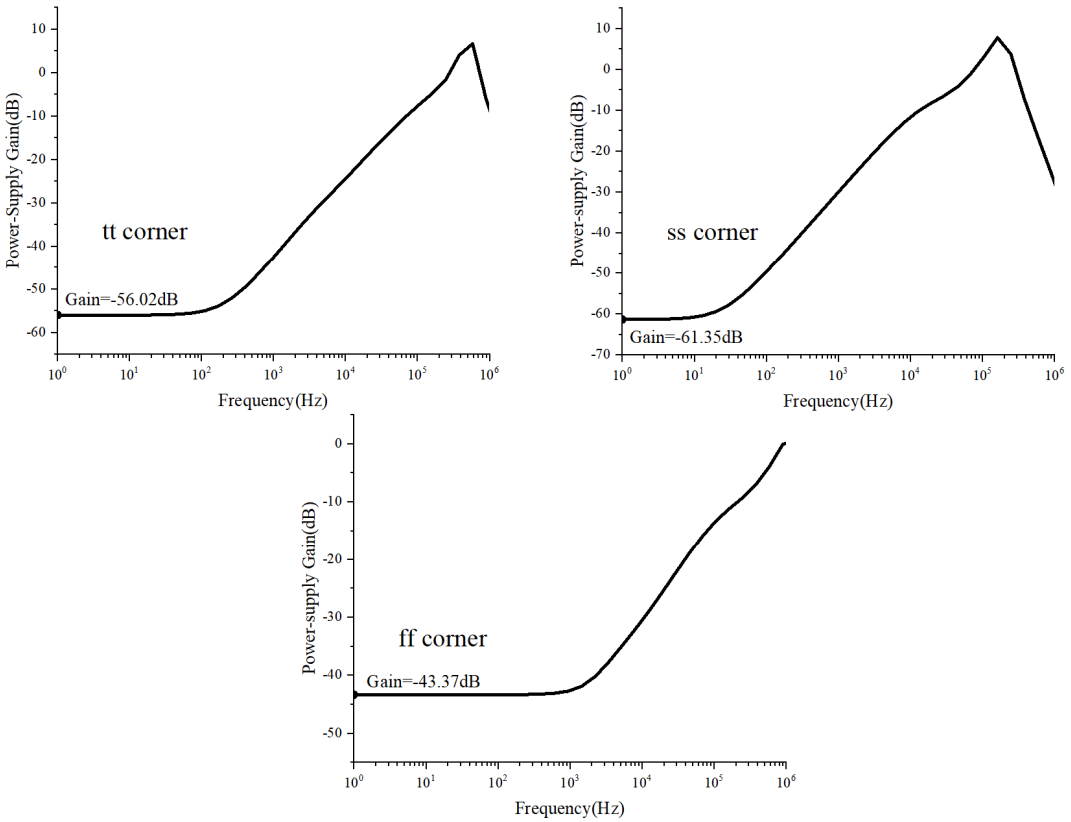

Figure 14. Power-supply gain under 50 pF load.

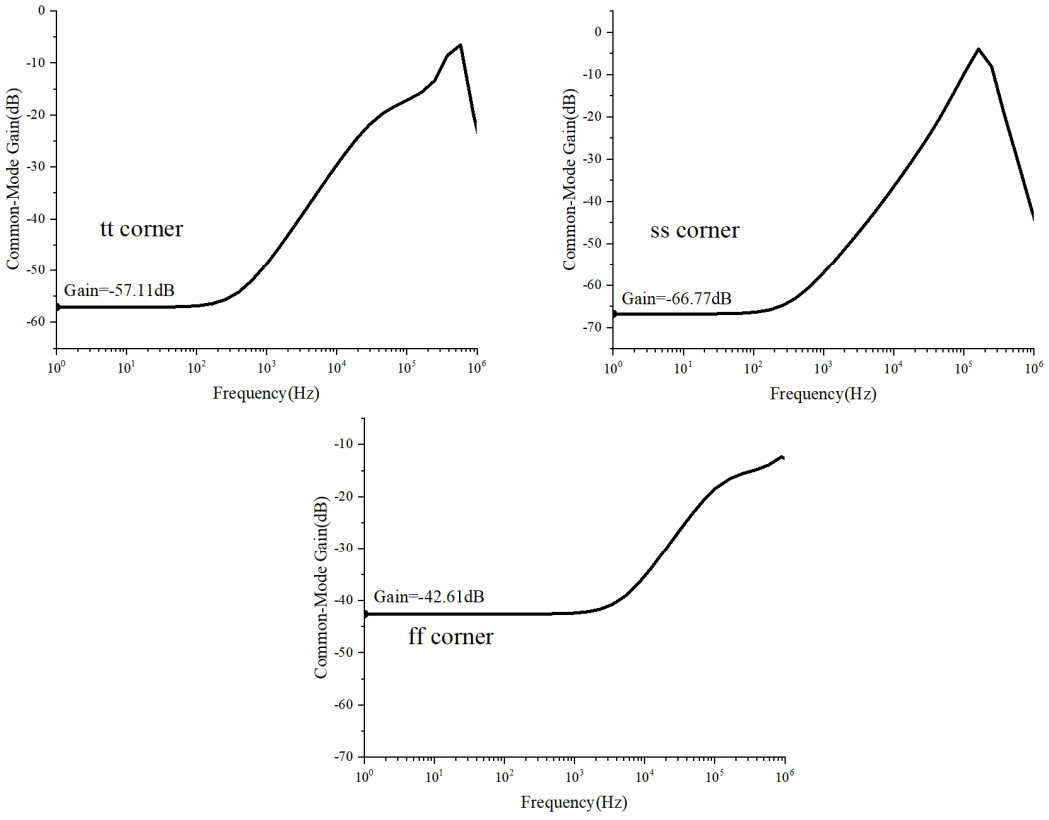

Figure 15. Common-mode gain under 50 pF load.

Figure 16 illustrates 200 runs of Monte Carlo simulations pertaining to offset voltage. The mean offset voltage is 0.391 mV, which is less than 1 mV. This suggests that the op-amp exhibits low offset in the context of process variation.

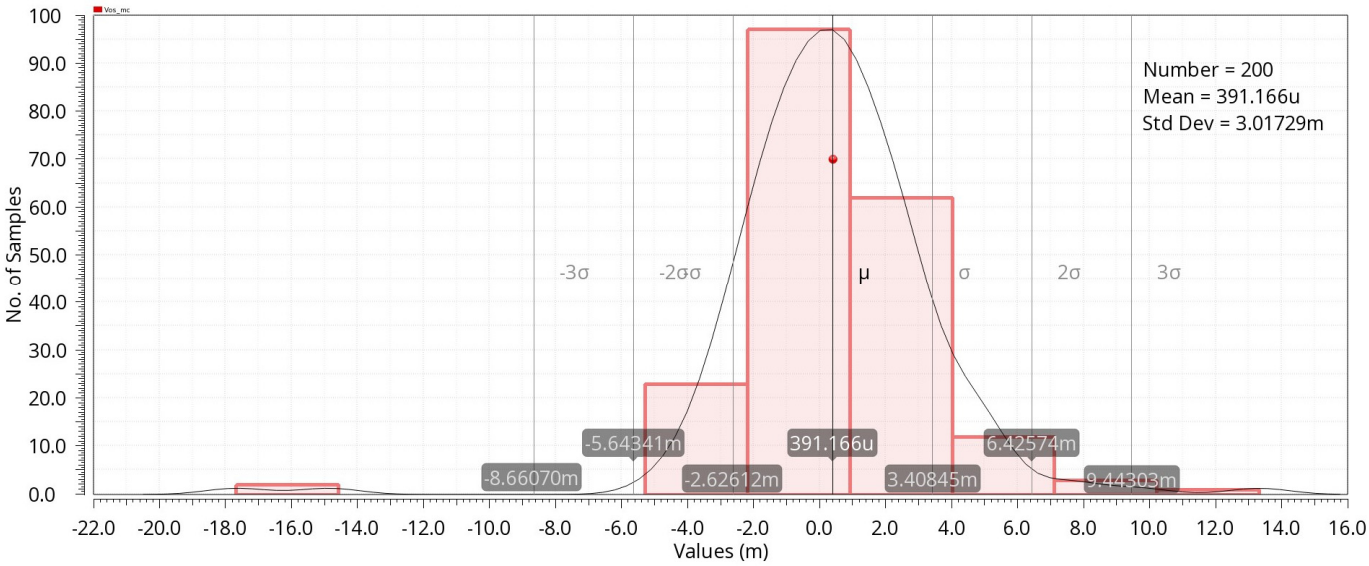

Figure 16. Histogram of offset voltage under 200 runs of Monte Carlo simulations at 50 pF load.

Figure 17 shows the plot of output swing (*y*-axis) against the input range (*x*-axis). This is based on the unity-gain configuration with different input stage designs with/without a low-voltage attenuator in the amplifier at tt condition. The input voltage V_g of all input transistors is kept at 250 mV while the supply voltage V_{dd} is kept at 500 mV and the drain current I_D is kept at 150 nA. The simulation results are shown in Figure 17. The first curve refers to the proposed bulk-drain-driven input topology with the embedded attenuator, and the obtained ICMR is 194 mV (116 mV to 310 mV). The second curve refers to the bulk-drain-driven input topology but without an attenuator, and the obtained ICMR is 105 mV (227 mV to 332 mV). The third curve denotes the gate-source driven input topology together with an attenuator, and the obtained ICMR is 147 mV (126 mV to 273 mV). The fourth curve denotes the gate-source driven input topology without an attenuator, and the obtained ICMR is 70 mV (224 mV to 294 mV). It can be confirmed that the proposed bulk-drain-driven input topology with an attenuator can effectively improve ICMR with respect to that gate-source driven topology with and without an attenuator.

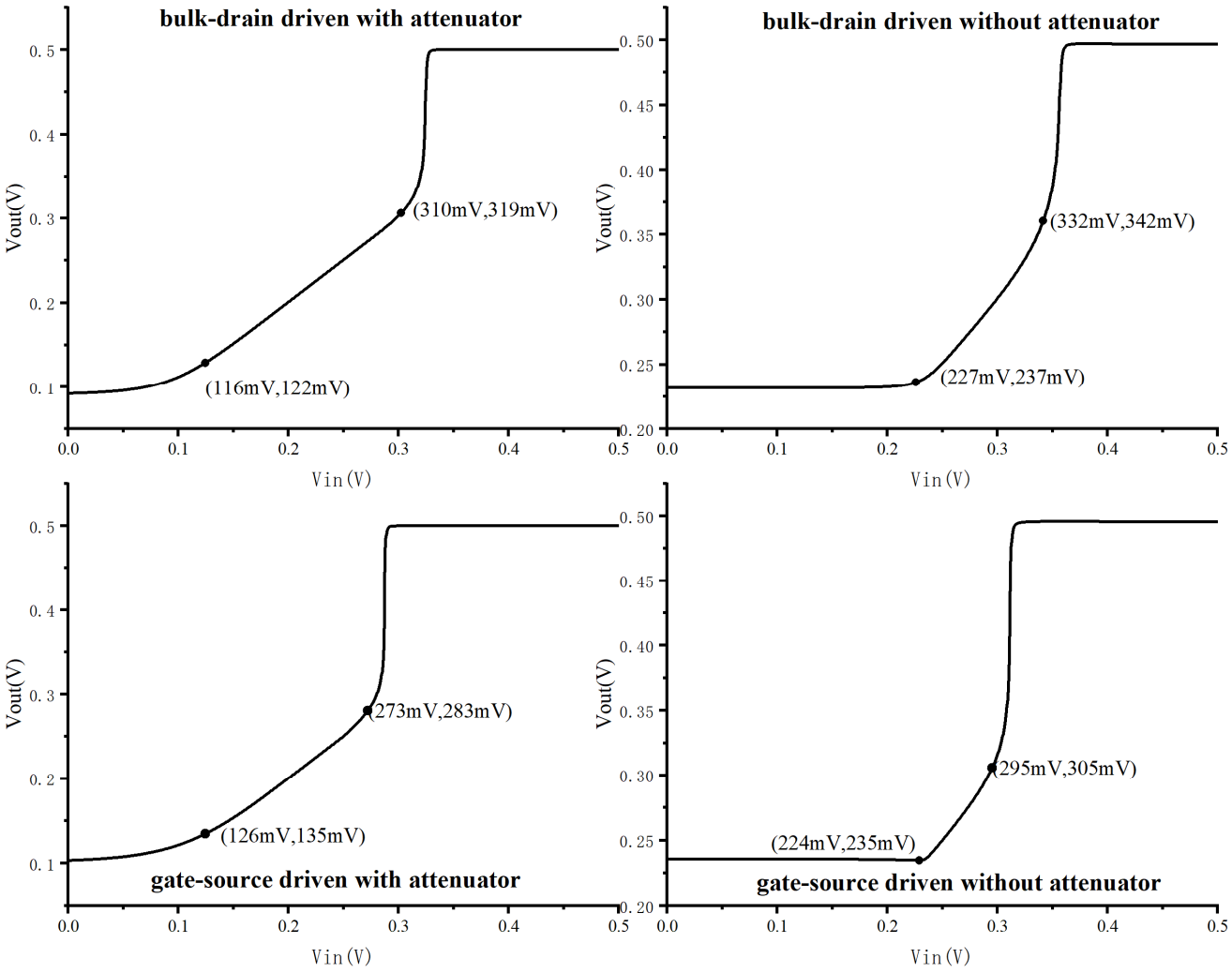

Figure 17. Common mode range of input and output with different input topology designs with/without low-voltage attenuator.

Figure 18 shows the plot of output swing (*y*-axis) of a proposed amplifier against the input range (*x*-axis). This is based on the unity-gain configuration driving a 50 pF load at different corners. As observed, the input range is from 116.3 mV to 310 mV at the tt condition, 90.0 mV to 370 mV at the ss condition, and from 160 mV to 310 mV at the ff condition. From the results, at supply of 0.5 V, the bulk-drain-driven input topology in conjunction with the low-voltage attenuator in amplifier's architectural design permits a swing of up to 40% of V_{dd}.

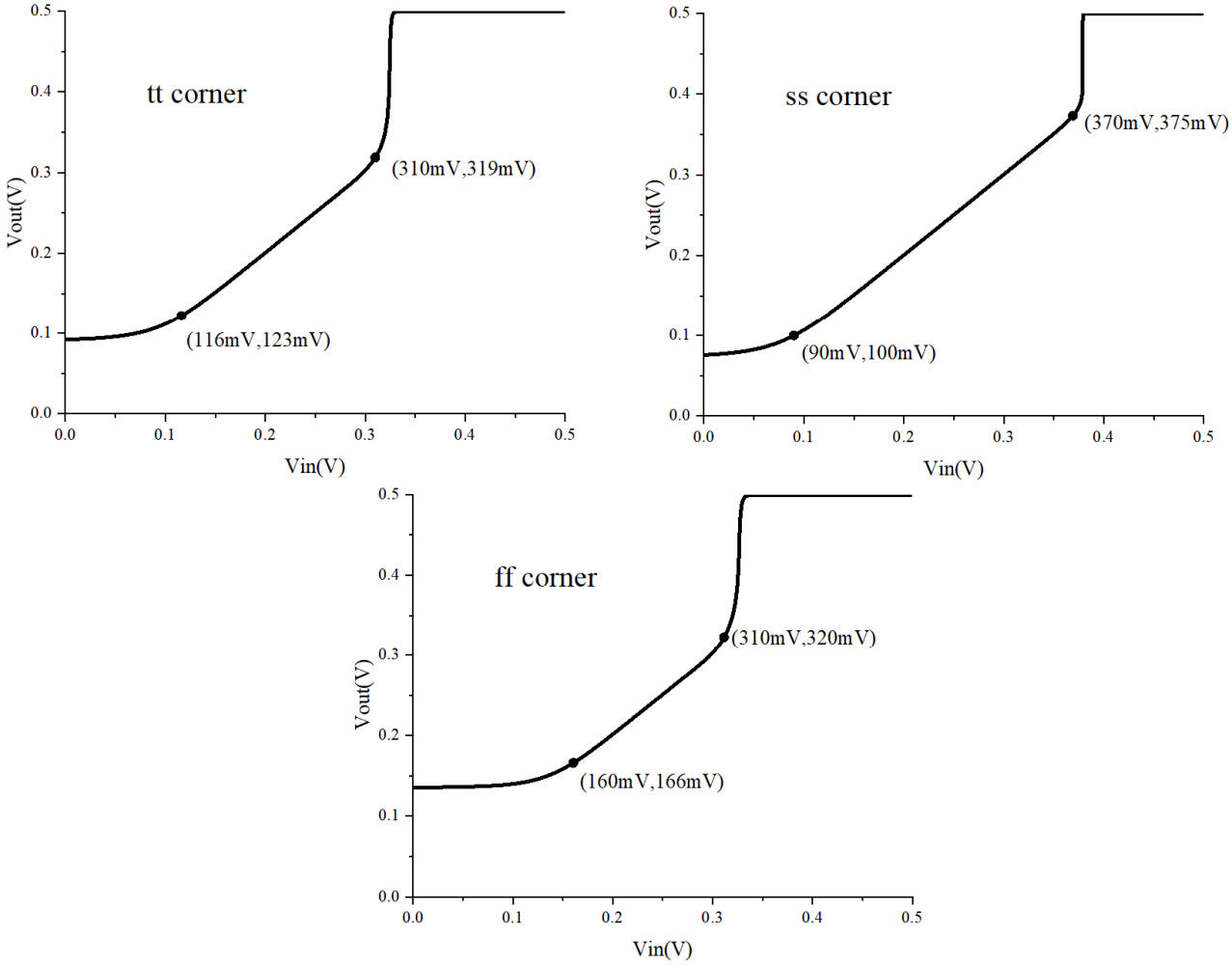

Figure 18. Common mode range of input and output under 50 pF load.

The transient responses of the proposed amplifier are shown in Figure 19. The period of the input square wave is 5 ms, and the rise time and fall time are 1 µs, respectively. It can be seen that the obtained slew rates are 0.064 V/µs and 0.017 V/µs at tt, 0.005 V/µs and 0.0025 V/µs at ss, and 0.005 V/µs and 0.006 V/µs at ff, respectively. In addition, the settling time is 72.49 µs at tt, 116.58 µs at ss, and 58.35 µs at ff, respectively. Due to the low-power design, the SR is limited but it can be improved through the use of a SR enhancement circuit or an increase in power consumption.

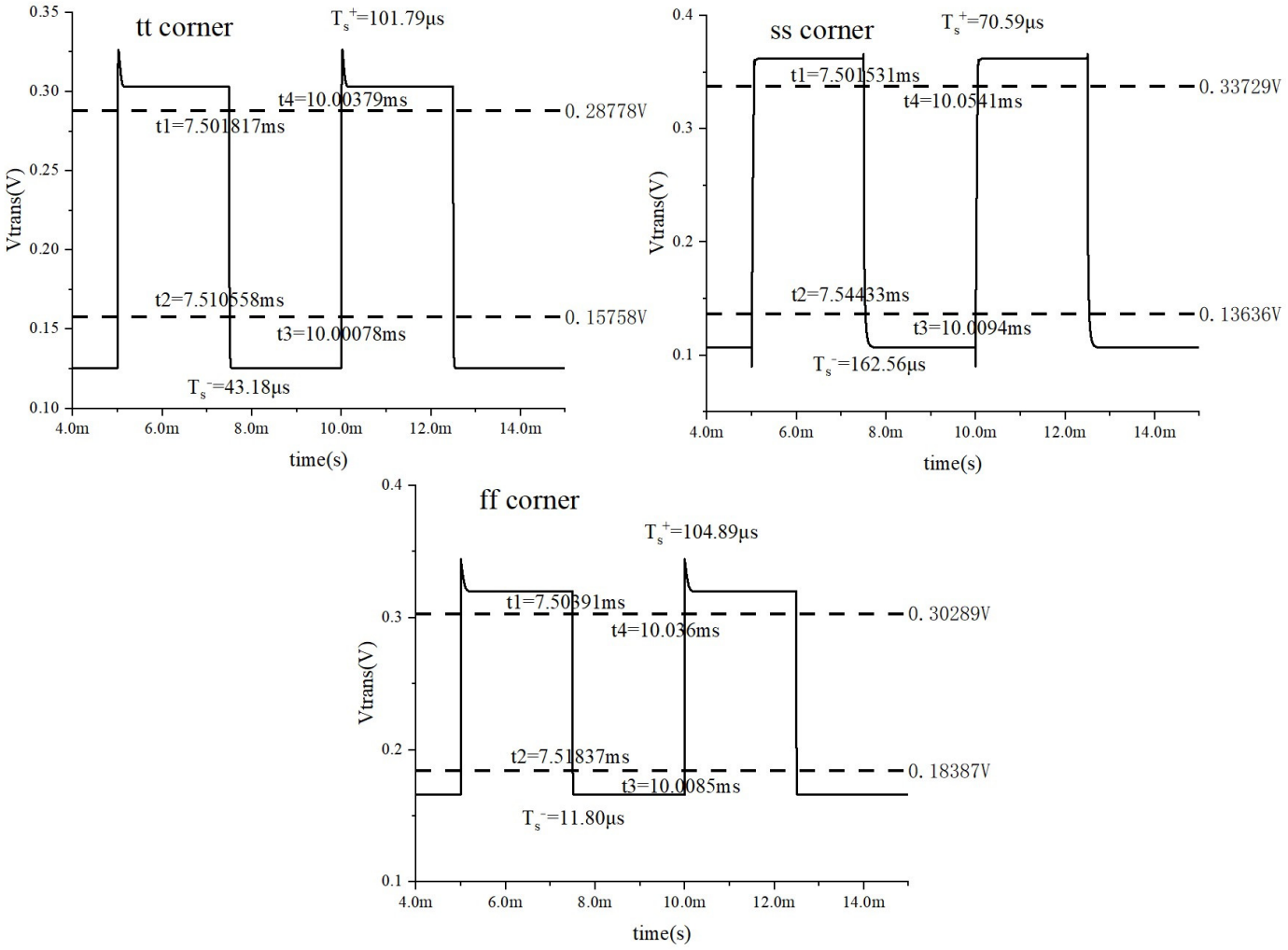

Figure 19. Transient response and slew rate of proposed amplifier.

The input-referred noise simulation results are shown in Figure 20. At 1 kHz, the input-referred noise can be obtained as 213.63 nV/$\sqrt{\text{Hz}}$ at tt, 343.96 nV/$\sqrt{\text{Hz}}$ at ss, and 214.91 nV/$\sqrt{\text{Hz}}$ at ff, respectively. Due to relatively higher g_{mi} being obtained from the rail-to-rail bulk-drain-driven topology, the noise performance metrics are better when compared to the bulk-driven input stage design. This also proves that the degeneration effect from the bulk-drain transistor is not significant. Therefore, it is not of concern.

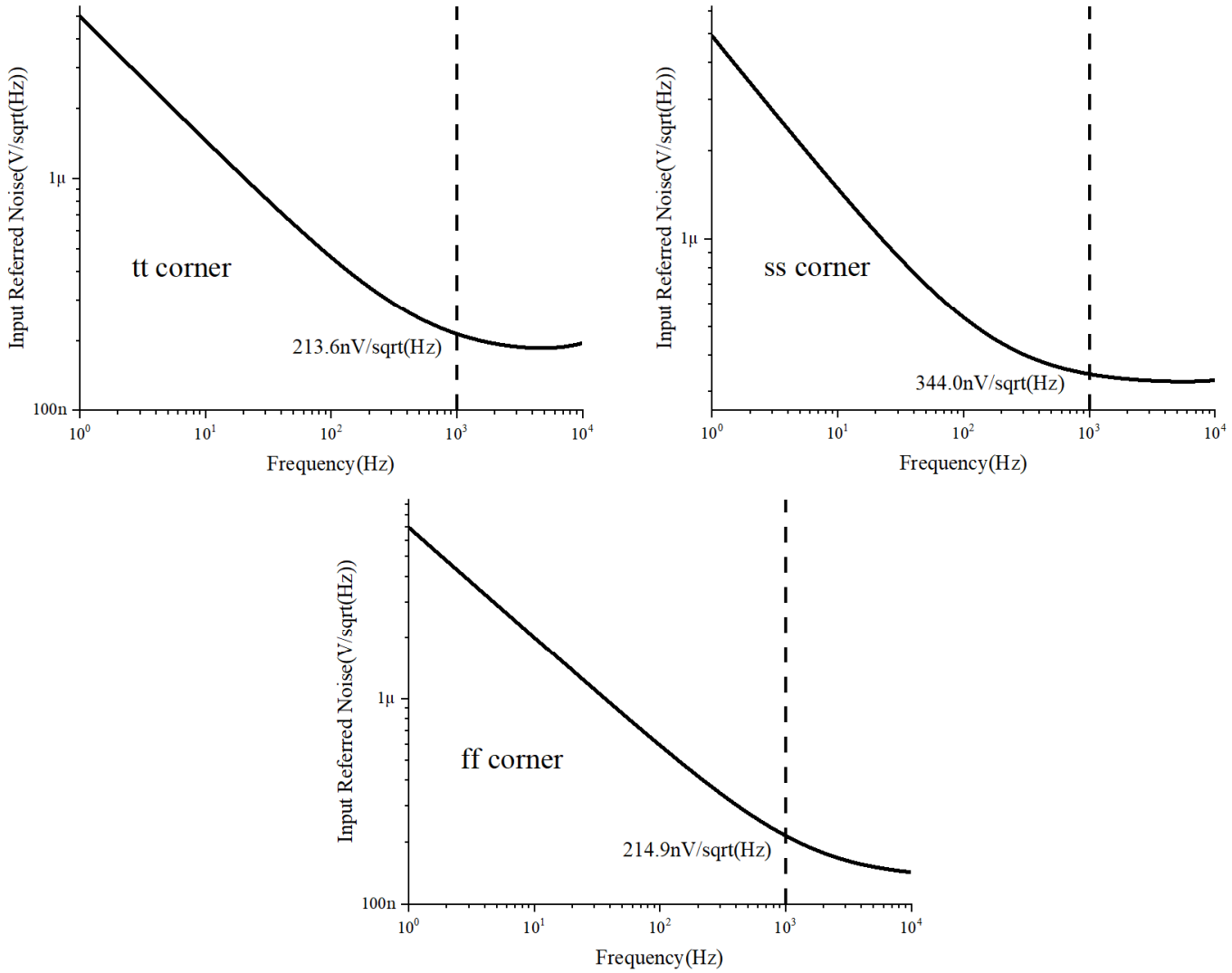

Figure 20. Input noise under 50 pF load.

The simulation results pertaining to the variation of input stage transconductance, g_{mi}, against the input voltage with and without a low-voltage attenuator are shown in Figure 21. It can be observed that due to the complementary circuit, g_{mi} will exhibit an obvious spike at the first output stage. Nevertheless, this spike is significantly suppressed after passing through the attenuator. This has demonstrated the effectiveness of using an attenuator to tackle the g_{mi} variation. Although the attenuator will attenuate the signal gain, the overall gain will be compensated by the subsequent high-gain stage.

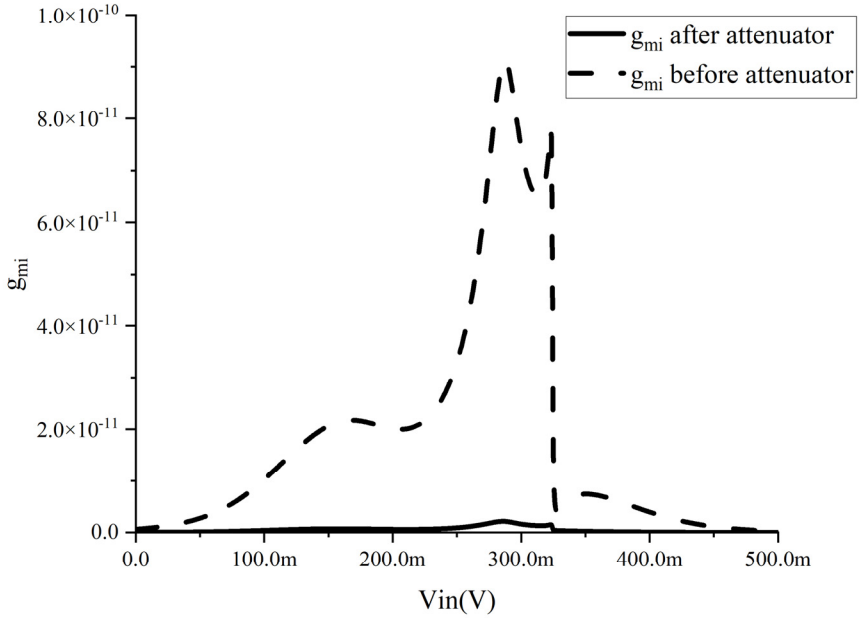

Figure 21. Simulation of g_{mi} against different input common-mode voltages.

Figures 22–28 illustrate 200 runs of Monte Carlo simulations pertaining to DC gain, GBW, PM, GM, CMRR, PSRR, and noise with estimated layout parasitics, respectively. According to Figures 22 and 23, the mean DC gain and GBW are 84.01 dB and 153.8 kHz, respectively, which are close to the simulation results without considering the parasitic capacitances. Regarding Figures 24 and 25, the mean PM and GM are 79.39 deg and 4.7 dB, respectively. Despite some reduction in PM and GM, these are still acceptable after taking into account parasitic effects, as PM is still maintained at a high rate. As seen in Figures 26 and 27, the mean CMRR and PSRR are 49.3 dB and 49.1 dB, respectively. There is no significant difference when taking the parasitic effect into account. The mean noise is obtained as 205.47 nV/$\sqrt{\text{Hz}}$, which shows that the op-amp's noise is still low when including the parasitic effect according to Figure 28. Figure 29 shows that the mean power consumption is 0.95 µW. These suggest that the op-amp exhibits good performance in the context of process variation and parasitic effects.

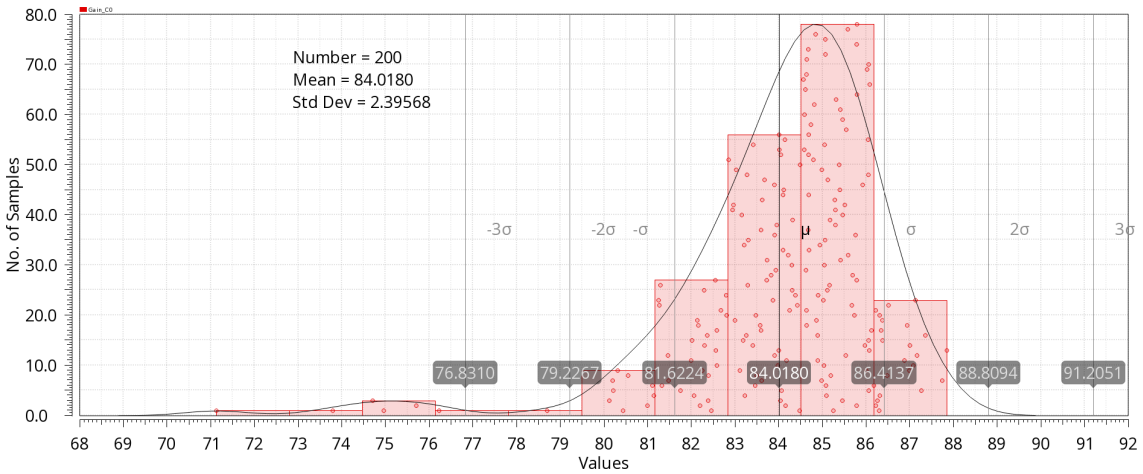

Figure 22. Histogram of DC gain under 200 runs of Monte Carlo simulations with estimated parasitics.

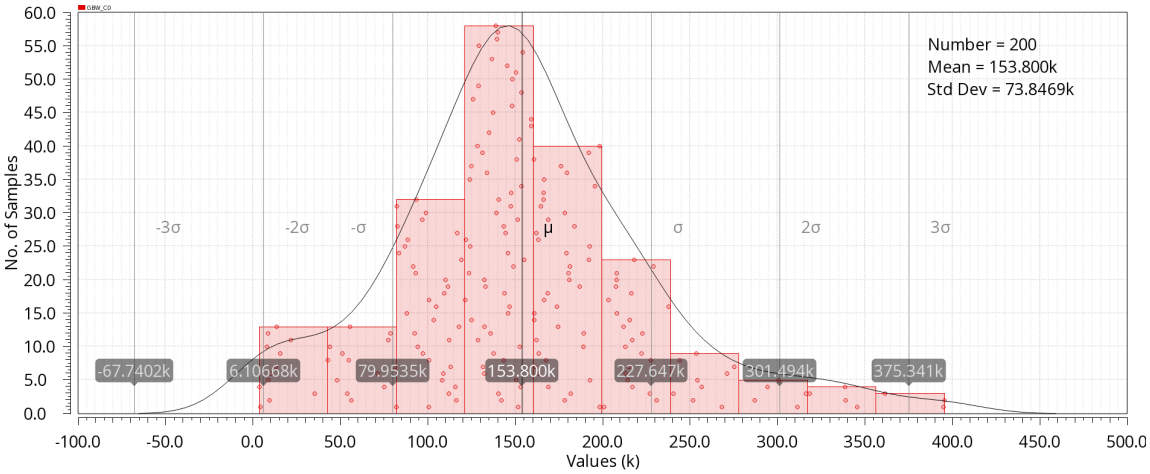

Figure 23. Histogram of GBW under 200 runs of Monte Carlo simulations with estimated parasitics.

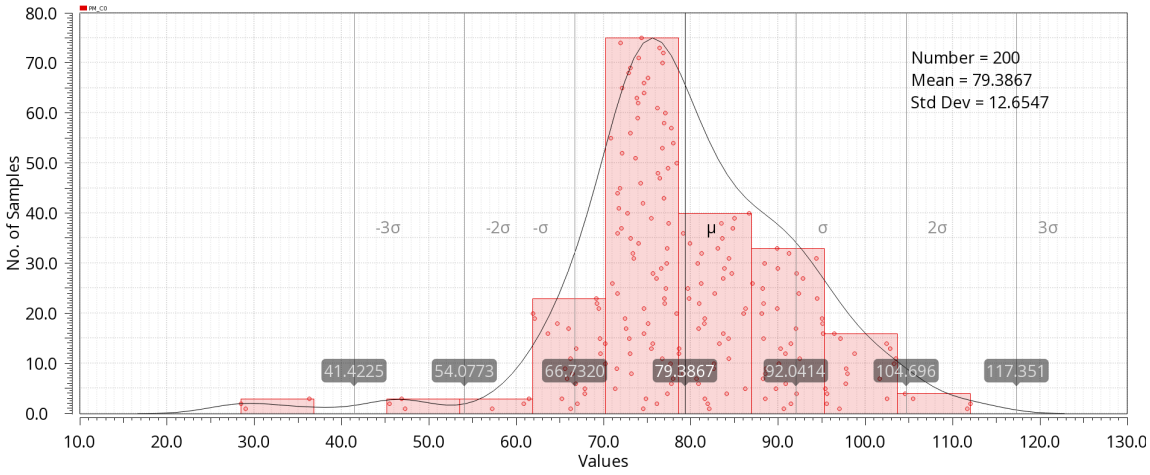

Figure 24. Histogram of PM under 200 runs of Monte Carlo simulations with estimated parasitics.

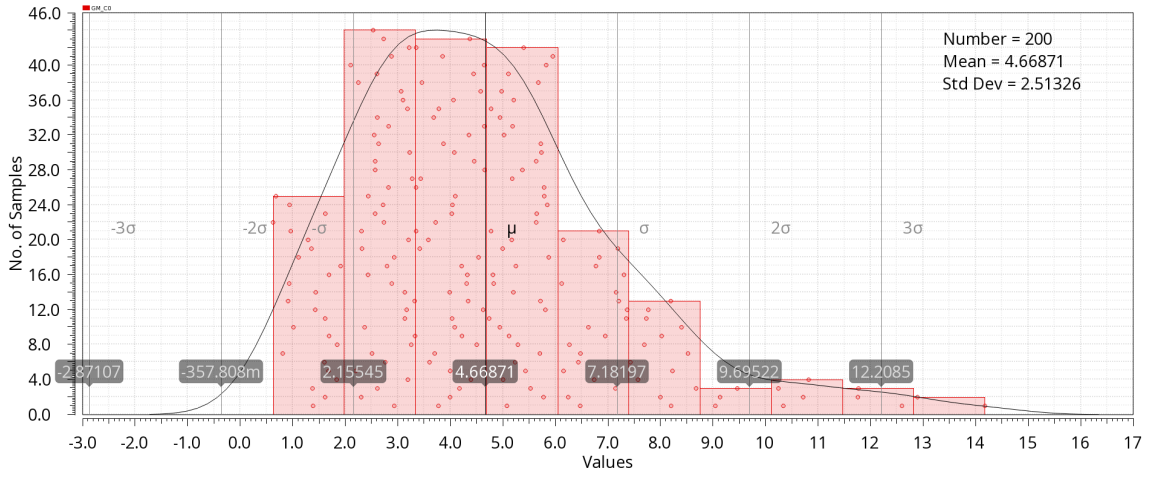

Figure 25. Histogram of GM under 200 runs of Monte Carlo simulations with estimated parasitics.

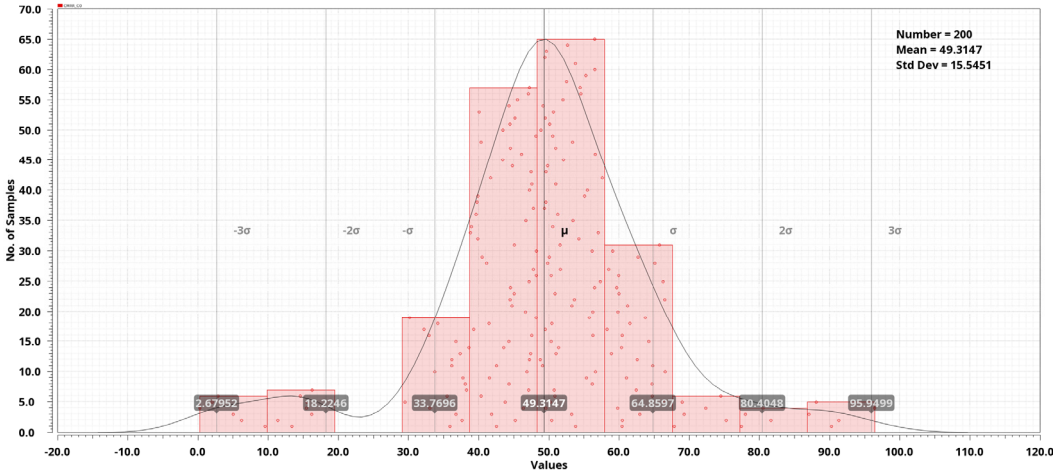

Figure 26. Histogram of CMRR under 200 runs of Monte Carlo simulations with estimated parasitics.

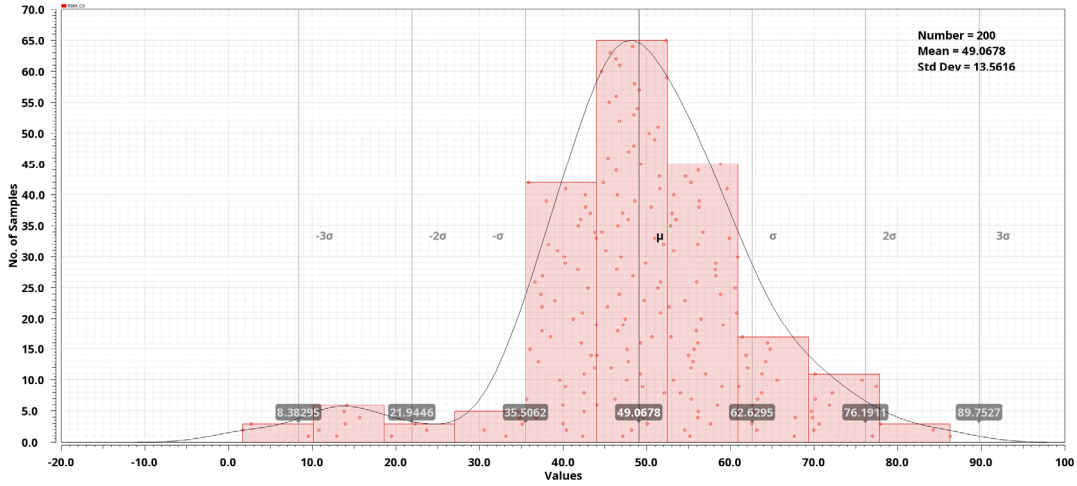

Figure 27. Histogram of PSRR under 200 runs of Monte Carlo simulations with estimated parasitics.

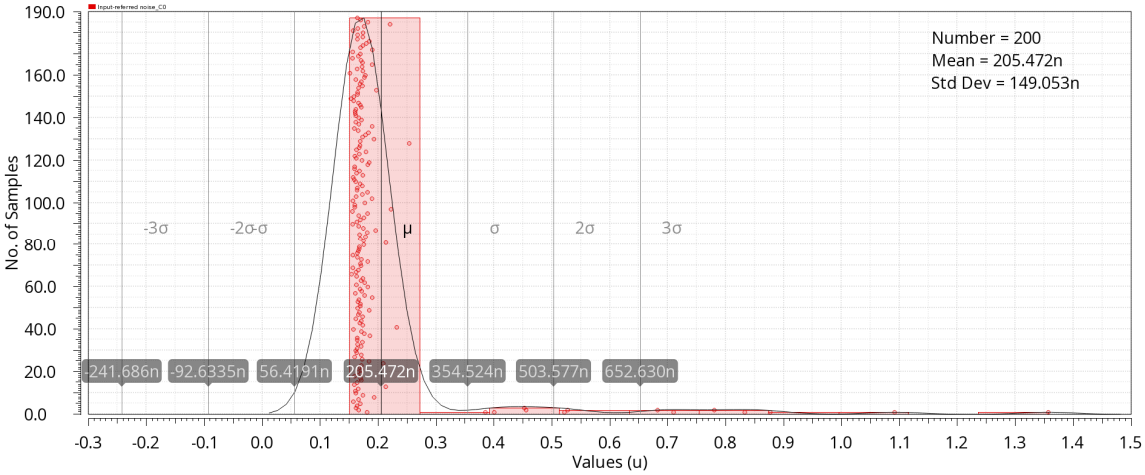

Figure 28. Histogram of noise under 200 runs of Monte Carlo simulations with estimated parasitics.

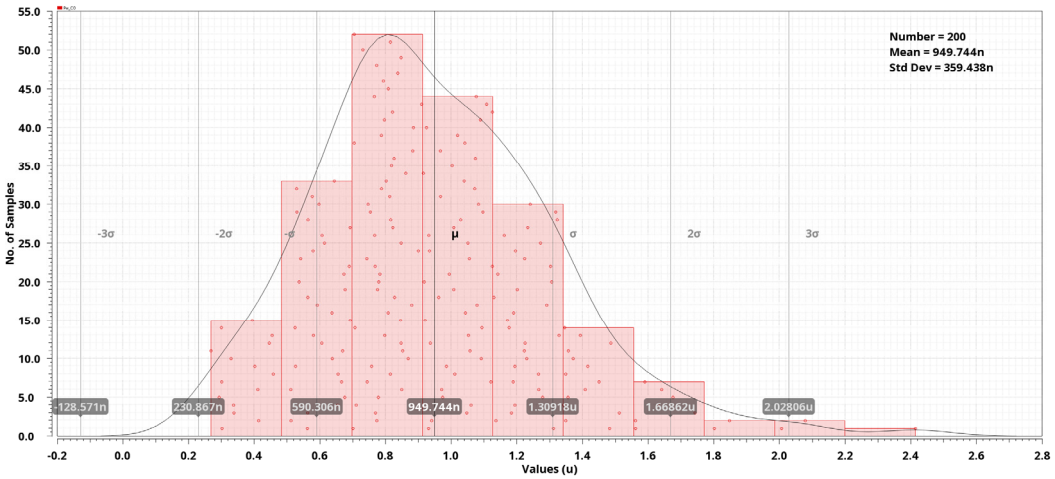

Figure 29. Histogram of P_w under 200 runs of Monte Carlo simulations with estimated parasitics.

The total current of the entire circuit is 1.73 µA, and the power consumption of the amplifier is only 0.865 µW at 0.5 V. In order compare the performance of amplifiers, different Figure-of-Merits are introduced. FoM_{ss} [23] and $IFoM_{ss}$ [16] are used to quantify the performance of amplifiers under small-signal conditions. They are defined as follows:

$$FoM_{ss} = UGB \times \frac{C_L}{P_w} \tag{53}$$

$$IFoM_{ss} = UGB \times \frac{C_L}{I_d} \tag{54}$$

where UGB is the unity-gain bandwidth, C_L is the load capacitor, P_w is the power consumption, I_d is the total current consumption, PM is the phase margin, and T_s is the settling time. Higher values of FoM_{ss} and $IFoM_{ss}$ indicate better performance metrics. Furthermore, FoM_{ls} [23] and $IFoM_{ls}$ [16] are used to quantify the large-signal performance of amplifier. They are defined as follows:

$$FoM_{ls} = SR \times \frac{C_L}{P_w} \tag{55}$$

$$IFoM_{ls} = SR \times \frac{C_L}{I_d} \tag{56}$$

where SR is slew rate. Similarly, higher values of FoM_{ls}, and $IFoM_{ls}$ indicate better performance metrics. Finally, in order to compare the effectiveness of amplifiers among the tradeoff performance metrics which involve multiple parameters such as noise, power consumption, and unity-gain bandwidth, a FoM_{npb} ($FoM_{noise\text{-}power\ per\ bandwidth}$) is used for the evaluation. It is given as follows:

$$FoM_{npb} = P_w \times \text{Input-referred Noise@1 kHz}/UGB \tag{57}$$

The lower the value of FoM_{npb}, the better the tradeoff performance.

The simulation results of the proposed amplifier show that FoM_{ss} and FoM_{ls} are 9.31 MHz·pF/µW and 2.34 (V·pF)/(µs·µW), respectively, while FoM_{npb} is 1.15×10^{-6} ((µV/$\sqrt{\text{Hz}}$)·µW/Hz). $IFoM_{ss}$ and $IFoM_{ls}$ are 4.65 (MHz·pF/µA) and 1.17 ((V·pF)/(µs·uA)), respectively. The simulation parameters of each process corner at 27 °C are shown in Table 2.

Table 2. Performance results of proposed amplifier under different process corners at 27 °C and 0.5V V_{DD}.

Parameter	tt	ss	ff
Gain (dB)	84.588	88.207	75.376
UGB (kHz)	161	66	248
PM (deg)	96	76	102
GM (deg)	5.7	8.23	11.94
Power-Supply Gain (dB)	−56	−61	−43
PSRR (dB)	56	61	43
Common-Mode Gain (dB)	−57	−67	−43
CMRR (dB)	57	67	43
Input CMR (mV)	194	280	150
Output CMR (mV)	196	275	154
SR+ (V/µs)	0.064	0.005	0.005
SR− (V/µs)	0.017	0.003	0.006
Settling Time (to 1%) (µs)	72.49	116.58	58.35
Input Noise@1 kHz (nV/$\sqrt{\text{Hz}}$)	213.63	343.96	214.91
Power (µW)	0.866	0.30	3.05
FoM_{ss} (MHz·pF/µW)	9.31	11	4.07
IfoMss (MHz·pF/µA)	4.65	5.50	2.03
FoM_{ls} ((V·pF)/(µs·µW))	2.34	0.67	0.09
IfoMls ((V·pF)/(µs·uA))	1.17	0.33	0.05
FoM_{npb} (($\mu V/\sqrt{\text{Hz}}$)·µW/Hz)	1.15×10^{-6}	1.56×10^{-6}	2.64×10^{-6}

In order to evaluate the PVT variation as well as the impact of layout parasitics on the circuit performance, Table 3 shows the comparative simulation results taking into account the process corners, supply voltage, and temperature together with the simulation results which are based on the estimated layout parasitics under a typical case. Table 4 shows the comparison between the performance results of a typical case and the mean values of the performance metrics obtained from 200 runs of Monte Carlo simulations with estimated layout parasitics. It can be seen that the proposed amplifier can work under the two worst PVT conditions. On top of that, the estimated layout parasitics which are added in the circuit had no significant impact on circuit performance. This is mainly because the circuit is designed at a low-frequency operation.

Compared with other capacitive load-driven designs which have power supply voltages of 0.5 V or below in Tables 5 and 6, FoM_{ss} and $IFoM_{ss}$ have comparable improvement. However, due to power limitations, FoM_{ls} and $IFoM_{ls}$ become smaller, but they can be improved through adding an SR boosting circuit or the increase of power consumption if the design is permitted. Finally, this also reveals that the FoM_{npb} of the proposed work is obviously better than other reported designs. This has validated that the proposed work has good tradeoff efficiency.

We compared the four-stage amplifier designs with different types of load in Table 7. Despite CFPFC having a relatively lower value of FoM_{ss} and FoM_{ls} with respect to that of [16,18], it is regarded as an acceptable value because its power consumption is merely 1/1617 in [16] and 1/180 in [18]. Furthermore, the existence of low-frequency parasitic poles under extreme low-power specifications will lead to design challenges in the frequency compensation.

Table 3. Simulation results of proposed amplifier at different operation conditions. (a) Performances under ss, 80 °C, V_{DD} = 0.475V. (b) Performances under tt, 27 °C, V_{DD} = 0.5V. (c) Performances under ff, −20 °C, V_{DD} = 0.525V. (d) Performance of typical case with estimated layout parasitics.

Parameter	(a) ss, 80 °C, V_{DD} = 0.475 V	(b) tt, 27 °C, V_{DD} = 0.5 V	(c) ff, −20 °C, V_{DD} = 0.525 V	(d) tt, 27 °C, V_{DD} = 0.5 V plus Estimated Layout Parasitics
Gain (dB)	82.4	84.6	83.5	84.6
UGB (kHz)	87	161	328	137
PM (deg)	106	96	84	78
GM (deg)	7.0	5.7	7.6	5.27
Power-Supply Gain (dB)	−69	−56	−57	−56
PSRR (dB)	69	56	57	56
Common-Mode Gain (dB)	−59	−57	−51	−57
CMRR (dB)	59	57	51	57
Input CMR (mV)	193	194	200	194
Output CMR (mV)	193	196	200	196
SR+ (V/µs)	0.01	0.064	0.03	0.05
SR− (V/µs)	0.007	0.017	0.014	0.018
Settling Time (to 1%) (µs)	74.71	72.49	50.05	74.23
Input Noise@1 kHz ($nV/\sqrt{Hz}$)	219.45	213.63	166	213.8
Power (µW)	0.66	0.866	1.62	0.866
FoM_{ss} (MHz·pF/µW)	6.59	9.31	10.12	7.91
$IFoM_{ss}$ (MHz·pF/µA)	3.13	4.65	5.31	3.95
FoM_{ls} ((V·pF)/(µs·µW))	0.64	2.34	0.68	1.96
$IFoM_{ls}$ ((V·pF)/(µs·uA))	0.31	1.17	0.36	0.98
FoM_{npb} (($\mu V/\sqrt{Hz}$)·µW/Hz)	1.66×10^{-6}	1.15×10^{-6}	0.82×10^{-6}	1.35×10^{-6}

Table 4. Simulation results of proposed amplifier under 200 runs of Monte Carlo simulations with estimated parasitics.

Parameter	Typical Spec	Mean 200 Runs of Monte Carlo Simulations with Estimated Layout Parasitics
Gain (dB)	84.6	84.02
UGB (kHz)	161	153.8
PM (deg)	96	79.39
GM (deg)	5.7	4.7
PSRR (dB)	56	49.3
CMRR (dB)	57	49.1
Input Noise@1 kHz ($nV/\sqrt{Hz}$)	213.63	205.47
Power (µW)	0.866	0.95
FoM_{ss} (MHz·pF/µW)	9.31	8.1
$IFoM_{ss}$ (MHz·pF/µA)	4.65	3.24
FoM_{npb} (($\mu V/\sqrt{Hz}$)·µW/Hz)	1.15×10^{-6}	1.26×10^{-6}

In order to compare the Cadence Spectre simulation results, an analytical MATLAB model on the basis of Equation (41) is developed. This aims at achieving an in-depth understanding of parameters that influence the transfer function. In Figure 30, the blue dotted line is the tt corner simulation data derived from Cadence Spectre, whereas the red solid line is the transmission function illustrated by MATLAB. The left side is the gain and the right side is the phase. It can be seen that the errors among the curves are small (less than 10%). Compared with the results of Spectre, the error is 0.1% (84.05 dB/84.588 dB) in DC gain, 1.9% (5.185 Hz/5.284 Hz) in dominant pole and 8.70% (175 kHz/161 kHz) in UGB. This validates the analytical Equation (41) from theory.

Table 5. Performance comparison of proposed amplifier with previously-reported low-voltage amplifiers.

Parameter Year sim/exp	**[26] 2022 (sim)**	**[27] 2022 (sim)**	**[28] 2021 (sim)**	**[29] 2020 (exp)**	**[30] 2020 (exp)**	**[31] 2020 (exp)**	**[5] 2020 (exp)**	**This Work (sim)**
V_{dd} (V)	0.6	0.5	0.5	0.4	0.3	0.3	0.25	0.5
Technology (µm)	0.18	0.18	0.18	0.18	0.18	0.18	0.065	0.04
Power (µW)	0.684	0.312	0.124	0.024	0.0126	0.013	0.026	0.866
Open Loop Gain (dB)	71.3	95	29.2	60	64.7	98.1	70	84.588
UGB (MHz)	0.0868	0.0128	2.93×10^{-4}	0.007	0.00296	0.003	0.0095	0.161
C_L (pF)	50×2	15	20pF	15×2	30	30	15	50
SR (V/us)	0.238	0.014	NA	0.079	0.0042	0.0091	0.002	0.0405
Settling Time (to 1%) (µs)	NA	NA	NA	NA	446	252	NA	72.49
CMRR@DC (dB)	102	60	84.88	85.4	110	60	62.5	57
PSRR@DC (dB)	104.5	66	58.53	76.3	56	61	38	56
Input-referred Noise ($(\mu V/\sqrt{Hz})$)	1.1@ 1 kHz	0.88	5.32	NA	1.6	1.8	NA	0.214@ 1 kHz
Input Stage Typology	bulk-driven	bulk-driven	bulk-driven	bulk-driven	bulk-driven	bulk-driven	bulk-driven	bulk-drain-driven
Input CMR /V_{dd} (mV)	NA	500/500	500/500	400/400	300/300	300/300	250/250	194/500
Output CMR /V_{dd} (mV)	NA	500/500	500/500	400/400	240/300	300/300	250/250	196/500
Output Stage Type	differential	single-ended	single-ended	differential	single-ended	single-ended	single-ended	single-ended

Table 6. FoM comparison of proposed amplifier with previously-reported low-voltage amplifiers.

Parameter Year sim/exp	[26] **2022 (sim)**	[27] **2022 (sim)**	[28] **2021 (sim)**	[29] **2020 (exp)**	[30] **2020 (exp)**	[31] **2020 (exp)**	[5] **2020 (exp)**	**This Work (sim)**
FoM_{ss} (MHz·pF/µW)	6.34	0.614	0.04	4.38	7.047	6.92	5.48	9.31
$IFoM_{ss}$ (MHz·pF/µA)	7.61	0.31	0.02	1.75	2.11	2.08	1.37	4.65
FoM_{ls} ((V/µs)·pF/µW)	17.4	0.647	NA	49.38	4.52	21	1.15	2.34
$IFoM_{ls}$ ((V·pF)/(µs·uA))	10.43	0.34	NA	19.75	3.00	6.3	0.29	1.17
FoM_{npb} $((\mu V/\sqrt{Hz})\cdot\mu W/Hz)$	8.67×10^{-6}	21.45×10^{-6}	2.93×10^{-3}	NA	6.81×10^{-6}	7.55×10^{-6}	NA	1.15×10^{-6}

Compared with other designs with supply voltage $\leq$ 0.5 V, the proposed design can achieve higher gain and higher bandwidth. Both PSRR and CMRR can also reach a moderate level with respect to that of other designs. Even with mismatches under Monte-Carlo simulation runs, the offset voltages are reasonable. In addition, through the use of bulk-drain-driven input topology in association with the embedded low-voltage attenuator in the amplifier's architectural design, the ICMR of the proposed amplifier is larger than the gate-source driven topology. In addition, the multi-parameter *FoM* performance metrics pertaining to noise, power, and bandwidth are introduced. Compared with other four-stage amplifier designs of different compensation typologies, the reduction of FoM_{ss} and FoM_{ls} is the inevitable tradeoff due to the ultra-low and constrained power design. Finally, the proposed circuit operates stably under PVT variations and is insensitive to parasitics due to the low operating frequencies.

Table 7. FoM comparison of proposed amplifier with previously-reported four-stage amplifiers.

Parameter **Year** **sim/exp**	**[12]** **1993** **(exp)**	**[13]** **1994** **(exp)**	**[14]** **2023** **(exp)**	**[15]** **1997** **(exp)**	**[16]** **2008** **(sim)**	**[17]** **2015** **(exp)**	**[18]** **2020** **(exp)**	**This Work** **(sim)**
V_{dd} (V)	5	1.5	1.2	2	1	3	1.2	0.5
Compensation Typology	Multiple Nested Miller Compensation	HNMC	Hybrid Cascode Frequency Compensation	NGCC	SMF	Passive Resistance-capacitor-Series Branch	APC	CFPFC
Technology (µm)	1.5	0.8	0.065	2	0.12	0.35	0.13	0.04
Load	50 Ω	10 kΩ//10 pF	5 nF	10 kΩ//20 pF	500 pF	1 nF	12 nF	50 pF
Power (µW)	10000	450	168	680	1400	156	175.2	0.866
UGB (MHz)	2	2	5.15	0.61	40.2	3	1.18	0.161
FoM_{ss} (MHz·pF/µW)	NA	NA	153.3	NA	14.36	19.2	80.8	9.31
FoM_{ls} ((V/µs)·pF/µW)	NA	NA	12.78	NA	6.26	7.56	9.59	2.34

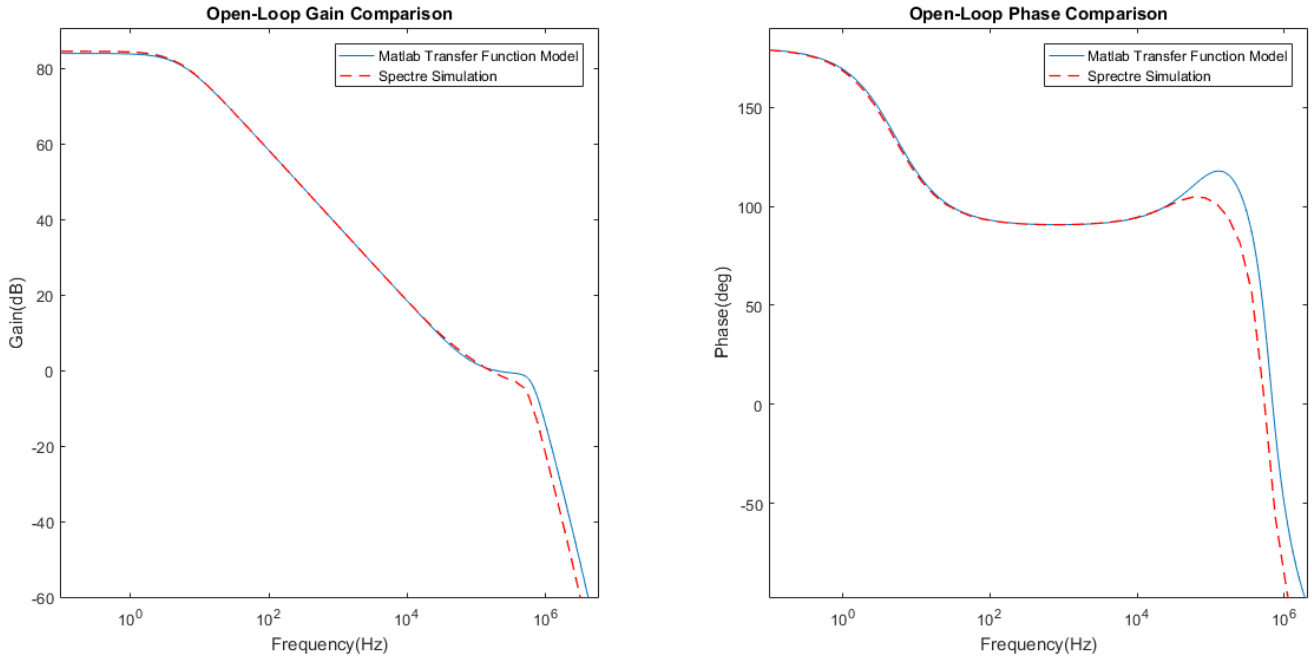

Figure 30. Comparison of open-loop results between spectra simulation and MATLAB models at 50pF capacitive load.

5. Conclusions

This paper presents a new 0.5 V four-stage amplifier design that operates at low voltage and low power consumption. Using the bulk-drain-driven input stage allows the op-amp to obtain moderately good g_{mi} while achieving an improved input common-mode range with respect to the complementary rail-to-rail input circuit. This maintains the benefits of low noise and good bandwidth even under low bias current when compared with that of a bulk-driven input stage design. More importantly, the use of a low-voltage attenuator in its architectural design reduces the impact of the output spikes caused by fluctuation of g_{mi} against input signal, thus sustaining the operation of the circuit at very low supply voltages. Furthermore, through the use of cross-feedforward positive feedback compensation, the circuit is verified to have good stability even when the amplifier is realized in a four-stage design. As a result, when the amplifier is compared with prior works, it exhibits good small-signal power-bandwidth FoM_{ss} and good multi-parameter FoM_{npb} with reference to those of bulk-driven designs. This has demonstrated the usefulness of amplifier architecture

and the frequency compensation technique. The amplifier is useful for low-voltage analog signal processing applications.

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