



Review

# CMOS Scaling for the 5 nm Node and Beyond: Device, Process and Technology

Henry H. Radamson <sup>1,\*</sup>, Yuanhao Miao <sup>1,\*</sup>, Ziwei Zhou <sup>1,†</sup>, Zhenhua Wu <sup>2,†</sup>, Zhenzhen Kong <sup>2,†</sup>, Jianfeng Gao <sup>2,†</sup>, Hong Yang <sup>2,†</sup>, Yuhui Ren <sup>1,†</sup>, Yongkui Zhang <sup>2,†</sup>, Jiangliu Shi <sup>3,†</sup>, Jinjuan Xiang <sup>3,†</sup>, Hushan Cui <sup>4,†</sup>, Bin Lu <sup>5,†</sup>, Junjie Li <sup>2,†</sup>, Jinbiao Liu <sup>2,†</sup>, Hongxiao Lin <sup>1,†</sup>, Haoqing Xu <sup>6,†</sup>, Mengfan Li <sup>2,6,†</sup>, Jiaji Cao <sup>1,†</sup>, Chuangqi He <sup>1,†</sup>, Xiangyan Duan <sup>1,†</sup>, Xuwei Zhao <sup>2,6,†</sup>, Jiale Su <sup>2,†</sup>, Yong Du <sup>2,†</sup>, Jiahao Yu <sup>2,†</sup>, Yuanyuan Wu <sup>1,†</sup>, Miao Jiang <sup>3,†</sup>, Di Liang <sup>3,†</sup>, Ben Li <sup>1,†</sup>, Yan Dong <sup>2,†</sup> and Guilei Wang <sup>3,7,\*</sup>

- <sup>1</sup> Research and Development Center of Optoelectronic Hybrid IC, Guangdong Greater Bay Area Institute of Integrated Circuit and System, Guangzhou 510535, China; zhouziwei@giics.com.cn (Z.Z.); renyuhui@giics.com.cn (Y.R.); linhongxiao@giics.com.cn (H.L.); caojiaji@giics.com.cn (J.C.); hechuangqi211@126.com (C.H.); xyduan93@163.com (X.D.); wuyuanyuan@giics.com.cn (Y.W.); liben@giics.com.cn (B.L.)
- <sup>2</sup> Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China; wuzhenhua@ime.ac.cn (Z.W.); kongzhenzhen@ime.ac.cn (Z.K.); gaojianfeng@ime.ac.cn (J.G.); yanghong@ime.ac.cn (H.Y.); zhangyongkui@ime.ac.cn (Y.Z.); lijunjie@ime.ac.cn (J.L.); liujinbiao@ime.ac.cn (J.L.); limengfan69@163.com (M.L.); zhaoxuwei@ime.ac.cn (X.Z.); sujiale@ime.ac.cn (J.S.); duyong@ime.ac.cn (Y.D.); yujiahao@ime.ac.cn (J.Y.); dongyan2019@ime.ac.cn (Y.D.)
- <sup>3</sup> Beijing Superstring Academy of Memory Technology, Beijing 100176, China; jiangliu.shi@bjsamt.org.cn (J.S.); jinjuan.xiang@bjsamt.org.cn (J.X.); miao.jiang@bjsamt.org.cn (M.J.); di.liang@bjsamt.org.cn (D.L.)
- <sup>4</sup> Jiangsu Leuven Instruments Co., Ltd., Xuzhou 221300, China; hushan.cui@gmail.com
- <sup>5</sup> School of Physics and Information Engineering, Shanxi Normal University, Linfen 041004, China; lubinsxnu@sina.cn
- <sup>6</sup> Institute of Microelectronics, University of Chinese Academy of Sciences, Beijing 100049, China; xuhaoqing@ime.ac.cn
- <sup>7</sup> Hefei National Laboratory, University of Science and Technology of China, Hefei 230088, China
- \* Correspondence: rad@giics.com.cn (H.H.R.); miaoyuanhao@giics.com.cn (Y.M.); guilei.wang@bjsamt.org.cn (G.W.)
- † These authors contributed equally to this work.



**Citation:** Radamson, H.H.; Miao, Y.; Zhou, Z.; Wu, Z.; Kong, Z.; Gao, J.; Yang, H.; Ren, Y.; Zhang, Y.; Shi, J.; et al. CMOS Scaling for the 5 nm Node and Beyond: Device, Process and Technology. *Nanomaterials* **2024**, *14*, 837. <https://doi.org/10.3390/nano14100837>

Academic Editor: Marco Lanuzza

Received: 19 March 2024

Revised: 24 April 2024

Accepted: 29 April 2024

Published: 9 May 2024



**Copyright:** © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

**Abstract:** After more than five decades, Moore’s Law for transistors is approaching the end of the international technology roadmap of semiconductors (ITRS). The fate of complementary metal oxide semiconductor (CMOS) architecture has become increasingly unknown. In this era, 3D transistors in the form of gate-all-around (GAA) transistors are being considered as an excellent solution to scaling down beyond the 5 nm technology node, which solves the difficulties of carrier transport in the channel region which are mainly rooted in short channel effects (SCEs). In parallel to Moore, during the last two decades, transistors with a fully depleted SOI (FDSOI) design have also been processed for low-power electronics. Among all the possible designs, there are also tunneling field-effect transistors (TFETs), which offer very low power consumption and decent electrical characteristics. This review article presents new transistor designs, along with the integration of electronics and photonics, simulation methods, and continuation of CMOS process technology to the 5 nm technology node and beyond. The content highlights the innovative methods, challenges, and difficulties in device processing and design, as well as how to apply suitable metrology techniques as a tool to find out the imperfections and lattice distortions, strain status, and composition in the device structures.

**Keywords:** CMOS; process integration; nanoscale transistors; FDSOI; GAA; TFET

## 1. Introduction

The development of CMOS technology is reaching its final stage where the transistor structure appears to be the most complicated. After more than fifty years following Moore's Law, the technology roadmap will finally be finishing in a few years. Simply, downscaling is approaching a brick wall where our technology is unable to continue developing beyond the 3 nm node anymore. The main issues are the uniformity, reproducibility, and quality of nanomaterials in mass production when the threshold has been reached. At that stage, where we are not able to pack more transistors in a lateral direction on the chip, we try to pack them in a vertical direction [1–3]. Then, the vertical transistors are designed with GAA in mind to create an innovative idea for tackling the SCEs. However, this design is very appealing, but creates a lot of difficulties such as creating contacts between metal and individual or stacks of transistors [4,5]. Therefore, other approaches, e.g., nanosheet (NS) transistors and fin field-effect transistors (FinFETs) which are fully depleted on SOI (FDSOI) wafers, have recently been proposed. In this way, the issue of SCEs is diminished; furthermore, we will still be able to scale down the transistors for some years to come. In the FDSOI technology, the issue of transistor SCEs is solved, but manufacturing the required SOI wafers appears to be a new challenge. The vertical scaling of SOI wafers will suffer from the non-uniformity of the Si cap and oxide box thickness. This means that it is not easy to manufacture SOI wafers to follow scaling-down procedures to reach a few nanometers (nm). A brilliant solution is to turn over the CMOS technology to TFETs where band-to-band tunneling (BTBT) requires significantly lower power consumption. Such types of chips will fulfil all the demands for low power consumption, which has been the in Moore's technology roadmap for years. Although TFETs offer an excellent platform for the industry, the problem of the stability of tunneling effect is still unsolved [1,3].

This review article presents the process integrity of CMOS to 5 nm and beyond. The content includes a survey of articles with a focus on the path to the end of the technology roadmap. Many issues around device design (e.g., GAA and tunneling FET), process difficulties and challenges, testing and characterizations, and introducing new materials are presented. The novelty of this review article lies in presenting the critical analysis and insights of the CMOS technology in the past, present, and future. For better navigation, we also provide the following short table.

Part I: Nanoscale transistor designs	The designs of Nanoscale Transistors in Approach to the End of Technology Roadmap and Beyond Moore
	Advanced TCAD with AI for the 5 nm node and beyond
Part II: Process of Nanoscale FETs	Advanced Lithography Technique
	Epitaxy in Transistor Structures
	Implantation and Advanced Doping Methods
	HKMG, ALD Technique and Negative Capacitance Materials
	Advanced Etching for Nano-Transistor Structures
	Wet Etch and Cleaning
	Metal Materials Interconnect
Part III: Materials in Beyond Moore Era	Advanced Devices Reliability
	III–V Materials
	Substrate Engineering (GOI and GeSnOI)
Part IV: Metrology technology	Beyond Moore Era-Si Optoelectronics
	Advanced Material and Structural Analysis of Miniaturized CMOS

### Part One: Nanoscale transistor designs

## 2. The Designs of Nanoscale Transistors in Approach to the End of Technology Roadmap and beyond Moore

### 2.1. Novel Structure, Gate-All-Around FETs

Compared with the Lateral GAA devices, Vertical GAA devices have more integration freedom in the vertical direction, which can increase the design space of gates, sources, and drains, reduce the area occupied by devices, and make it easier to realize vertical stacking of multi-layer devices. The wiring method further increases the integration density; therefore, it has become a basic device with great potential in logic and memory chip manufacturing technologies such as CMOS and high-density DRAM at 2 nanometers and below. Due to the space limitation and abovementioned advantages of Vertical GAA devices, we only focus on the Vertical GAA devices here. In our previous review article [1], we have talked about vertical GAA FET (VGAAFET), which is selected as one of the candidate transistors for new CMOS technology in the future [2,3]. As the channel is orthogonal to the wafer plane, VGAAFETs have the advantages of relieving Contacted Gate Pitch (CGP) constraints against further scaling [4], reducing the area of standard cells [5], and increasing integration density [6].

As the variation in gate length is a key processing issue for VGAAFET [7], a new p-type vertical sandwich, GAAFET (pVSAFET), has been processed, where high-k metal gates (HKMGs) are self-aligned with little effective gate length variation [8,9]. Such VSAFETs were manufactured through Si/SiGe/Si stacked structure epitaxy, an isotropic quasi atomic layer etching (qALE) process, and gate replacement process, as shown in Figure 1a–c. The main advantages of VSAFETs are that the gate length of the devices is mainly determined by the SiGe thickness, with little deviation in the process, and the diameter of NW and thickness of NS are precisely controlled by the Si-selective isotropic qALE of SiGe. Following the process shown in Figure 1b, Ni (Pt) silicide was formed on the surface of the source and drain region of the device (Figure 2e), and the channel of the device was protected by the inner spacer shown in Figure 2d. The external resistance of devices with silicide is about four times slower than that without silicide, and  $I_{\text{dsat}}$  of with silicide is approximately seven times higher than that without silicide when  $I_{\text{OFF}} = 10^{-9} \text{ A}/\mu\text{m}$ , as Figure 3 shows. The performance of VSAFET is sensitive to the thermal budget process, as a high thermal budget will cause doped boron to diffuse from the source and drain to the channel, resulting in poor electrical behavior. In addition, the threshold voltage can be tuned by adjusting the Ge component in the channel, Si cap film, and different work function layers.

Since the transistors structures are complicated, the integrity of the process flow has proved to be stepwise. The best choice of method is cross-section scanning electron microscopy (SEM) or transmission electron microscopy (TEM). Since many labs take a test sample along the process line, high-resolution scanning electron microscopy (HRSEM) is frequently used in line. Figure 2 demonstrates the most critical steps in VGAA transistors. The following points are the focus: (a,b) the quality of SiGe/Si in terms of defect density and interfacial roughness; (c) the shape and dimensions of the formed channel after etching; (d) spacer thickness; (e) lack of void creation after silicide formation; (f) the uniformity of high k deposition.

Because of the risk from n-type dopant segregation [10], n-type doping in the S/D of VSAFETs is preferably performed via the implantation process [11,12], which is different from the S/D in situ epitaxial doping process of pVSAFET. To protect the vertical channel during the S/D implantation, a dummy nitride is introduced in the gate (Fig.4). The n-type VSAFET is manufactured with CMOS-compatible technology and exhibits excellent output characteristics, including an excellent short-channel control capability (DIBL = 14 mV), extremely low leakage current, a small sub threshold swing of 67 mV/dec, and a high switching ratio ( $I_{\text{ON}}/I_{\text{OFF}} = 3.5 \times 10^6$ ). Thus, it could be an important candidate device for high-density and high-performance 3D-integrated circuits in the future (Figure 4).

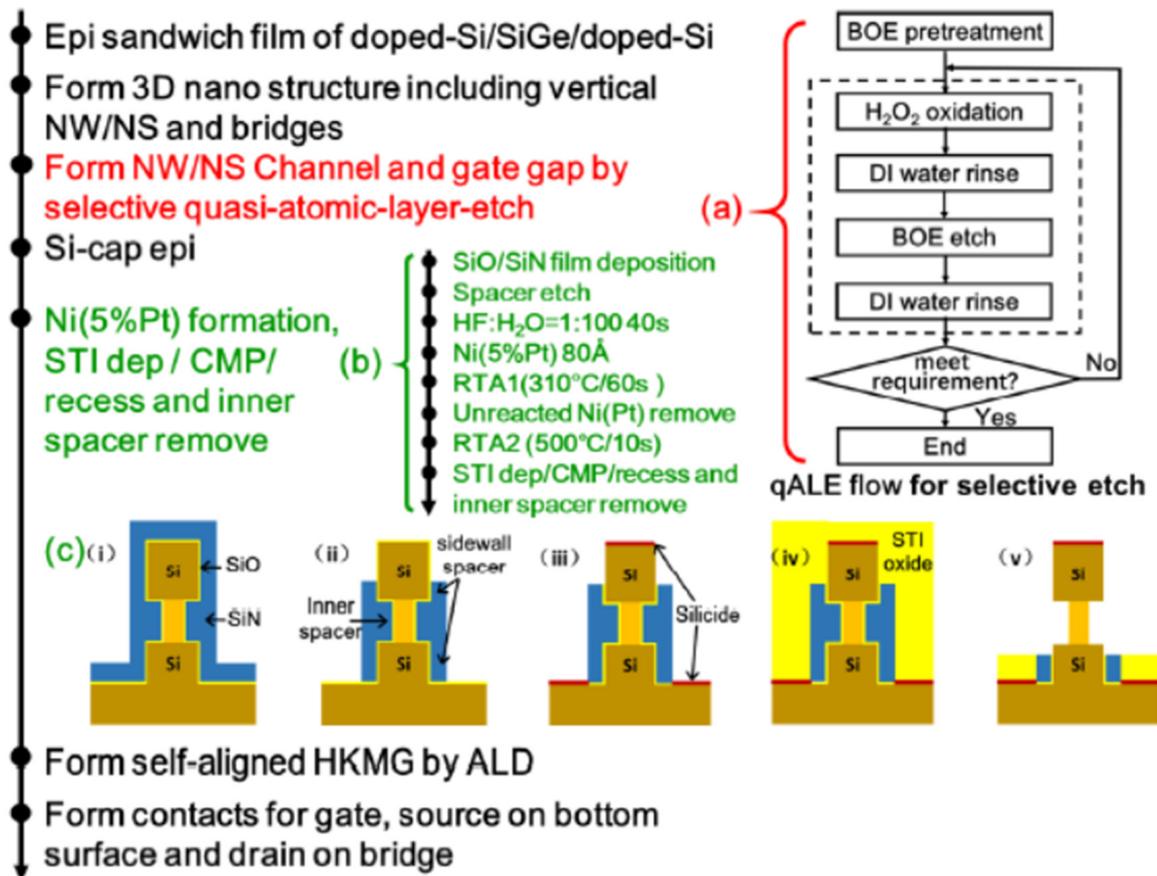


Figure 1. The process of VSAFETs, including the flow of selective qALE, and the flow and diagram of the Ni (Pt) silicide process. Reprinted with permission from ref. [9]. Copyright 2021 IEEE Publisher.

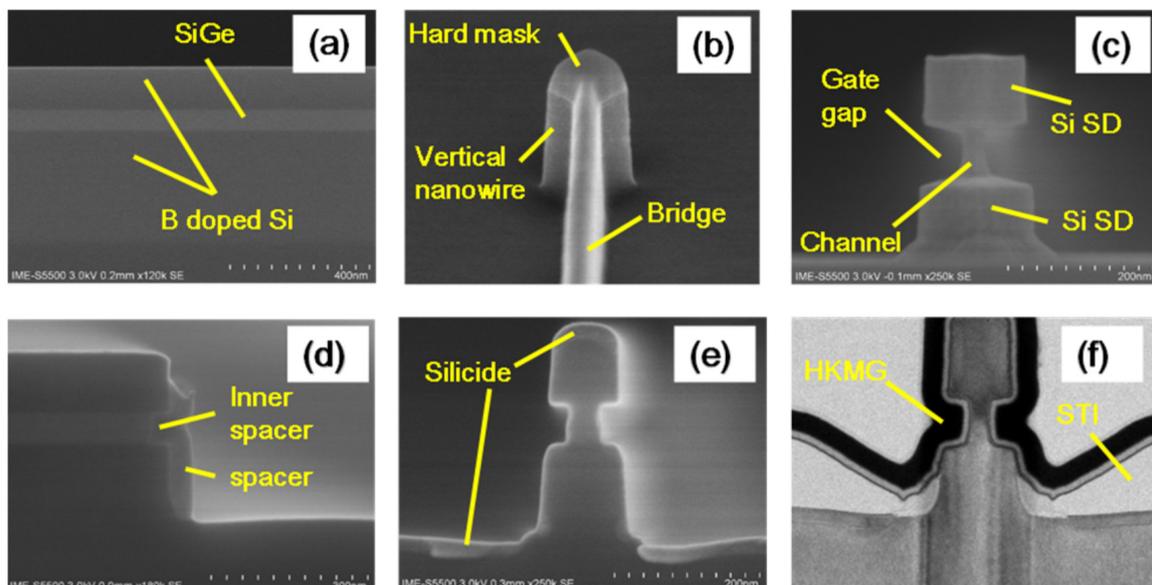
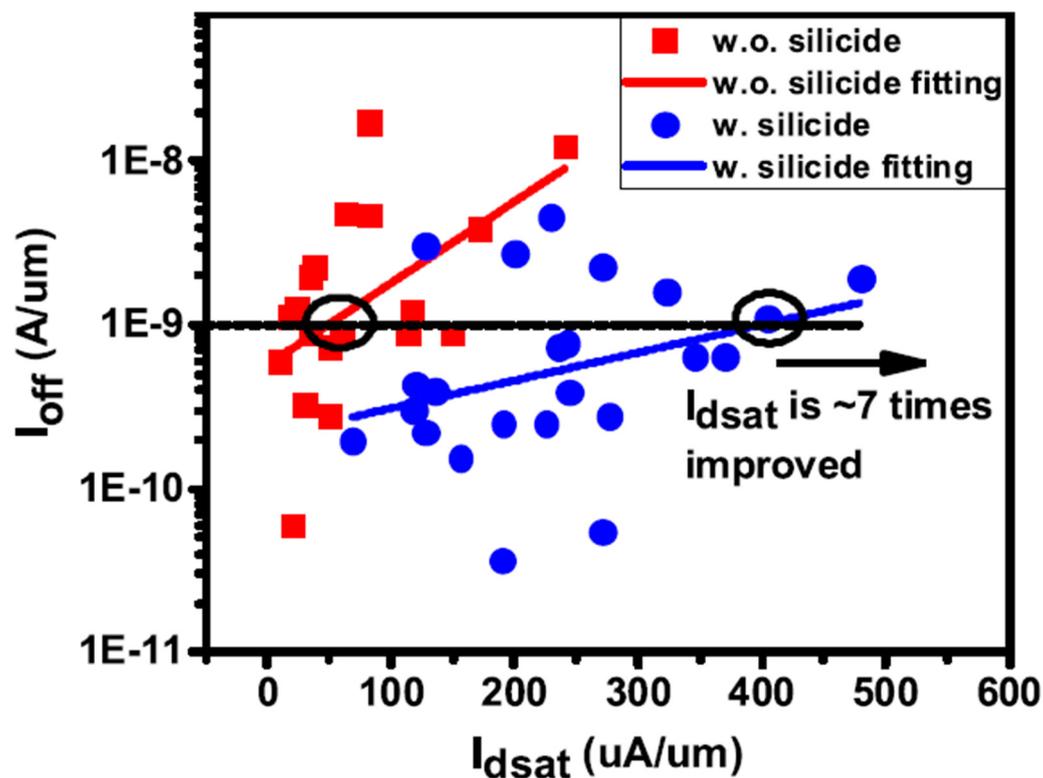
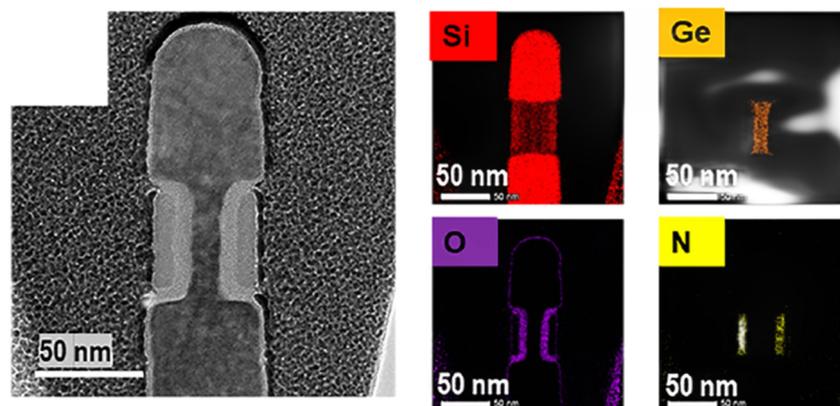


Figure 2. SEM micrographs: (a) epitaxially grown Si/SiGe/Si multilayers, (b) the tilted image of 3D nanostructure, (c) after qALE, (d) after inner spacer and sidewall spacer formation, (e) after silicide formation in structure wafer, and (f) TEM image after HKMG process. Reprinted with permission from ref. [9]. Copyright 2021 IEEE Publisher.

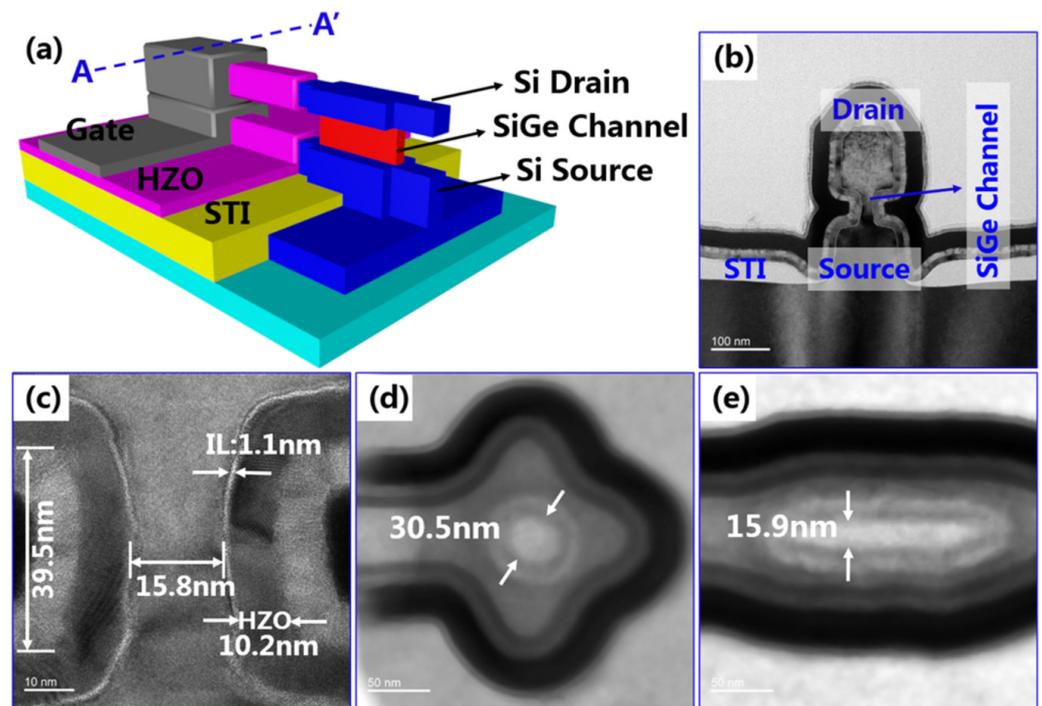


**Figure 3.**  $I_{\text{off}}-I_{\text{dsat}}$  data from transistors for with and without silicided pVSAFETs. Reprinted with permission from ref. [9]. Copyright 2021 IEEE Publisher.



**Figure 4.** High-resolution TEM micrograph with detailed information about energy-dispersive X-ray spectroscopy (EDX) analysis. The SiN dummy gate has been dry-etched followed by dHF for 60 s to stripe the oxide layer on the sidewall. Reprinted from ref. [11]. Copyright 2021 ACS Publisher.

The vertical transistors have the advantages of nonvolatile data storage, nanosecond programming/erasing speed, low-power operation, ultra-long data storage time, and compatibility with the CMOS process. The ferroelectric field-effect transistor (FeFET) is considered as a candidate device for nonvolatile memory applications in the future. Due to the constraints of thick ferroelectric film (for example,  $\sim 10$  nm  $\text{Hf}_x\text{Zr}_{1-x}\text{O}_2$ ), VGAAFET is more suitable for FeFET than FinFET and LGAAFET at the technology node of 5 nm and beyond. Figure 5 shows the ferroelectric VSAFETs (Fe-VSAFETs) with a self-aligned metal gate [13]. Fe-VSAFETs have excellent electrical characteristics such as  $I_{\text{ON}}/I_{\text{OFF}}$  ratios of more than  $10^7$ , leakage currents of less than 1 pA, long retention times, program/erase times of around 100 ns, and the largest memory window (MW) at about 2.3 V.



**Figure 5.** (a) A schematic of an Fe-VSAFET, (b) STEM cross-section for Fe-VSAFET across AA' direction, (c) STEM cross-section of channel region, (d) top view of STEM of a nanowire device, and (e) top view of a nanosheet device. Reprinted with permission from ref. [13]. Copyright 2021 IEEE Publisher.

Further studies on GAAFET have been reported, including high-mobility channel materials, e.g., Ge/GeSn [14–17] and III–V [18], and wide bandgap materials, e.g., GaN [19,20].

## 2.2. Tunneling Field-Effect Transistor (TFET) Approach

As the size of MOSFET is scaled down to nanometers, the SCEs and power consumption become increasingly important issues for chips. In order to reduce the power consumption, the  $V_T$  and operation voltage ( $V_{DD}$ ) have to be reduced. However, for transistors with a constant sub-threshold swing (SS), reducing  $V_T$  and  $V_{DD}$  would lead to exponentially increased leakage current and static power consumption. Therefore, a smaller SS, namely extremely steep switch characteristic, is required. Unfortunately, due to the tail of the Boltzmann distribution, the SS of MOSFETs has a limitation of 60 mV/dec at room temperature.

TFET operation is based on the BTBT mechanism. This can break the 60 mV/dec limitation of SS and allow further scaling of  $V_T$  and  $V_{DD}$  even with a reduced leakage current; therefore, this can be widely considered as the most promising candidate for future low-power applications.

In 2004, a carbon nanotube TFET with sub-60 mV/dec SS was reported [21]; afterwards, plenty of experimental studies were carried out for both nTFETs and pTFETs [22]. Some experimental reports based on Si and Ge materials are summarized in Table 1 [23]. It is clearly observed that most devices can exhibit a minimum SS smaller than 60 mV/dec, owing to the mature fabrication technology and nearly perfect semiconductor/oxide interface. However, an SS smaller than 60 mV/dec can only appear across a very small current range and at a very small drain current. Furthermore, the on-state current ( $I_{ON}$ ) is only around a few  $\mu\text{A}/\mu\text{m}$ , which results from the low BTBT probability owing to the large and indirect bandgap of Si and Ge. To boost the  $I_{ON}$ , more attention is focused on the III–V material with a small bandgap and tunneling mass, and the hetero tunneling junction with a small tunneling barrier. Table 2 summarizes some works based on III–V materials [22,24–37]. It is clearly observed that  $I_{ON}$  levels are greatly improved due to the

reduced tunneling barrier compared with those of conventional Si and Ge TFETs. However, it seems that it is harder for III–V TFETs to obtain an SS smaller than 60 mV/dec and some of them even show a minimum SS larger than 100 mV/dec, which is obviously not what we are expecting. Two factors may contribute to this deviation. One factor is the complex and poor stability of the interface between III–V and gate oxide inducing a high density of states, which causes Fermi pinning and degrades the gate control efficiency. The other factor is the lattice mismatch at the hetero tunneling junction inducing a large density of traps. This further leads to the trap-assisted-tunneling (TAT) process at the tunneling junction, which is nearly not under the control of gate bias. Therefore, the III–V TFETs usually exhibit a large leakage current and degraded SS.

**Table 1.** Some experimental works on TFETs based on Si and Ge materials.

Year	Ref.	Material System	$I_{ON}$ [ $\mu A/\mu m$ ]	$I_{ON}/I_{OFF}$ Ratio	$SS_{min}$ [mV/dec]	<60?
2007	[38]	Si	12.1	$10^4$	~52.8	✓
2008	[39]	Si	<0.1	$<10^7$	42	✓
2009	[40]	Ge/Si	0.4	$>10^6$	35	✓
2010	[41]	Si	~2	$10^8$	46	✓
2011	[42]	Si	$<10^{-4}$	$10^4$	30	✓
2012	[43]	Strain-Si	0.1	$10^7$	76	×
2012	[44]	Si	~0.1	$10^6$	52	✓
2012	[45]	Si	0.15	$\sim 10^5$	36	✓
2013	[46]	Ge/Si		$10^7$	49	✓
2014	[47]	Si	39	$>10^5$	69	
2014	[48]	Si	20	$10^8$	29	✓
2015	[49]	Ge/strain-SOI	<1	$10^7$	29	✓
2016	[50]	Si	<0.01	$10^5$	34	✓
2017	[51]	Si	2.0	$10^8$	75	×
2017	[52]	Ge/Si	14	$10^7$	>200	×
2019	[53]	Si	<0.01	$10^4$	17	✓
2020	[54]	Si	40	$\sim 10^8$	69	×
2020	[23]	SiGe	<0.01	$\sim 10^6$	65.4	×

“✓” or “×” stands for the SS is smaller or higher than 60 mV/dec.

**Table 2.** Some experimental works on TFETs based on III–V materials.

Year	Ref.	Material System	$I_{ON}$ [ $\mu A/\mu m$ ]	$I_{ON}/I_{OFF}$ Ratio	$SS_{min}$ [mV/dec]	<60?
2011	[24]	Hetero-InGaAs	10	$10^5$	55~60	✓
2012	[25]	GaAsSb/InGaAs	135	$10^4$	100	×
2012	[26]	InAs/Si	2.4	$10^6$	150	×
2012	[27]	InAs/GaSb	180	$10^4$	200	×
2012	[28]	InAs/Si	<1	$\sim 10^6$	21	✓
2013	[29]	InGaAs/GaAsSb	740	$10^2$	NA	×
2015	[30]	InGaAs	1	$10^6$	64	×
2015	[31]	InGaAs/GaAsSb	84	$<10^5$	64	×
2015	[32]	GaAsSb/InGaAs	275	$10^5$	55	✓
2016	[33]	InAs/Si	4		70	×
2017	[34]	Ge/GeSn	2.4	$10^4$	215	×
2018	[35]	InGaAsSb/InAs	<10	$<10^5$	75	×
2018	[36]	InGaAsSb/InAs	<0.1	$<10^4$	35	✓
2019	[37]	GaSb/InAs		$<10^4$	40	✓
2021	[22]	InGaAs/GaAsSb	<0.1	$\sim 10^3$	42	✓

“✓” or “×” stands for the SS is smaller or higher than 60 mV/dec.

In addition to the Si, Ge, and III–V materials, in recent years, some other new materials are also applied to improve TFET performance, such as a ferroelectric layer [55],

WSe<sub>2</sub>/SnSe<sub>2</sub> [56,57], graphene [58,59], MoS<sub>2</sub>/HfS<sub>2</sub> [60], and WTe<sub>2</sub>/WS<sub>2</sub> [61]. These are all excellent examples; however, the above problems are not totally addressed. Both high  $I_{ON}$  and low SS levels are required for the practical applications of TFETs; thus, further investigations are still needed to improve the device performance.

### 2.3. FDSOI Technology

The miniaturization of transistor dimensions has created faster chips with less power consumption [1,3]. However, as the chip size approaching its physical limit in recent years, SCEs has dominantly degraded the performance. Therefore, new structures are developed to overcome the physical limitations and further develop chip integration. At nodes below 28 nm, the traditional planar MOSFET structure has been basically abandoned, and multi-gate device structures with stronger gate controllability, e.g., FinFET, FDSOI, and GAA, have been proposed [2,3]. Due to their superior electrostatic control performance, FinFET and FDSOI technologies have overthrown the traditional planar body transistors. Although the cost of the FDSOI wafer is higher, it requires only small changes in production compared with the traditional bulk, allowing more of the existing technologies to be used. GAA is further improved based on FinFET, and the process cost will be higher. Based on the advantages of the merger of SOI and FinFET, as well as strain engineering, a better platform can be obtained in the technology roadmap, e.g., SOI- or strained SOI-FinFETs. It should be noted that FinFET used on bulk Si actually had many problems after reaching 5 nm. For example, its ever-increasing ratio of depth to width will make it difficult for the fins to maintain an upright shape under the internal stress of the material itself; as the gate width further increases with miniaturization, it will be difficult to fill multiple fin lines in one unit as in the past. Moreover, the static electricity problem of fin field-effect transistors will also seriously restrict the further improvement of transistor performance. Tinkering with FinFETs will eventually be insufficient, and new architectures are ready to emerge. Therefore, the use of FinFET architecture on FDSOI wafers is enough for the 5 nm node.

#### 2.3.1. What Is FDSOI (Architectures and Characteristics)

The key difference between SOI MOS and a conventional MOS structure is the buried oxide layer (BOX) of SOI, which separates the transistor from the substrate. As shown in Figure 6, the thin transistor channel is fully depleted during operation and sandwiched between two insulating layers. Usually, the channel thickness is around 1/4–1/3 of the gate length. To avoid the large access series resistance caused by the direct growth of metal silicide, the structure of the raised source/drain (RSD) is generally adopted [62–65], as is shown in Figure 7.

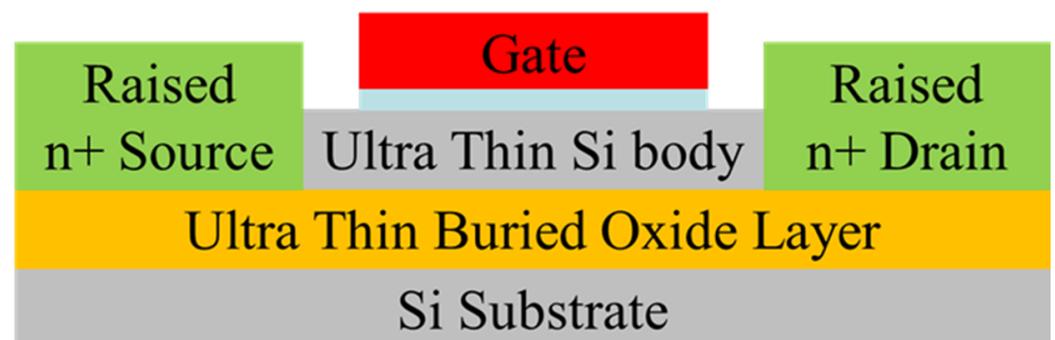
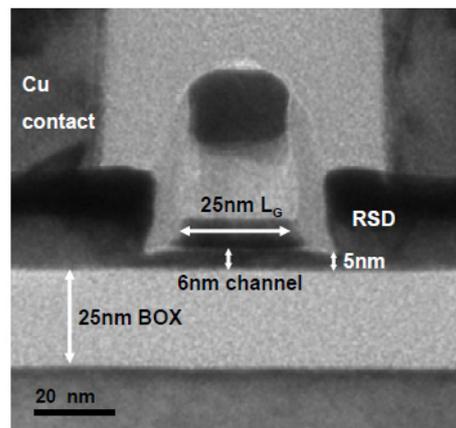


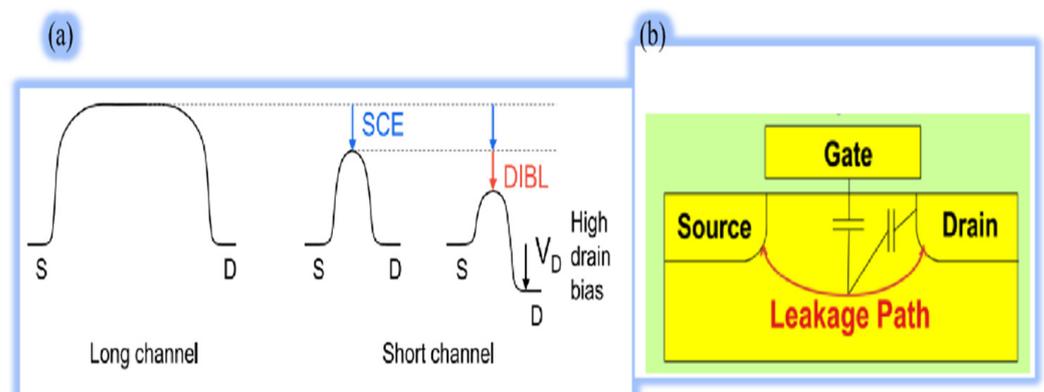
Figure 6. Schematic of planar FDSOI transistor.



**Figure 7.** The typical cross-section TEM of an ultra-thin FDSOI device [66]. Reprinted with permission from ref. [66]. Copyright 2011 IOP Publishing.

### 2.3.2. FDSOI Salient Characteristics

When scaling down further, the SCEs and drain-induced barrier lowering (DIBL) induce the channel current uncontrolled by the gate as the shorter the gate length, the lower the barrier, as shown in Figure 8 [67,68]. DIBL is another SCE, which results from decreasing the channel barrier at higher drain voltage and lowers the  $V_T$ . Thus, SCEs are intolerable while the channel length is less than the depletion width. In addition, other issues confining device performance also arise when scaling down, including a higher leakage current, higher SS [69], lower on-to-off current ratio, and random dopant fluctuation (RDF) [70,71].



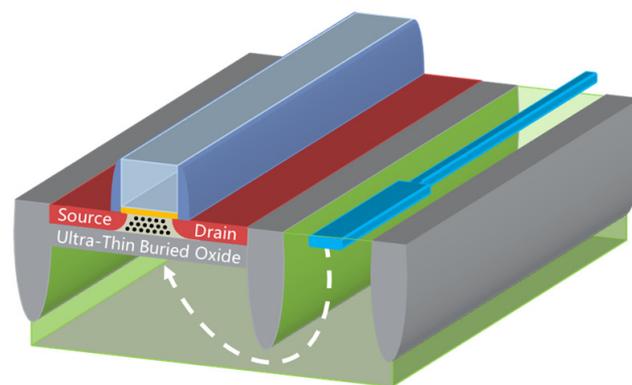
**Figure 8.** (a) Top of the band schematic, (b) bulk CMOS currents leakage path. Reprinted with permission from ref. [68]. Copyright 2012 IEEE Publisher.

FDSOI technology features improved the electrostatic controllability and channel carrier mobility of the gate, along with a decreased RDF. This technology possesses salient characteristics, such as a lower RDF with an undoped channel, eminent control of SCEs, higher carrier mobility, compatibility with planar processing library [72], lower mismatch variation, ultra-low-power applications [73–75], multi- $V_T$  option [76], and a good back gate biasing option, among others. All these features make FDSOI technology the best power/performance/cost tradeoff choice. Near-zero  $V_T$  can be readily achieved in FDSOI without degrading other characteristics of the device [77], providing a great opportunity for ultra-low operating voltage ( $V_{DD}$ ) application, especially for primary RF and high-precision analog.

It is demonstrated that ample control of SCEs achieved in FDSOI scaling down to 10 nm without performance degradation [78,79], benefiting from the inherent thin SOI architecture [80] and based on the investigation on SCEs [81], indicated that devices are still

indomitable against SCEs even with a fairly thin SOI film [82]. Naturally, the leakage current into the substrate and gate-induced drain leakage (GIDL) current are largely lessened [83,84] thanks to the carriers being strictly confined within the thin channel.

Furthermore, with the implementation of back gate biasing, excellent SCE management was obtained [85,86], and electrostatic control represented a faster transition between off-state and on-state with decreased DIBL, SS, and variability. Utilizing various polarities [87–89] in conjunction with applying a bias to the well (Figure 9) [90–92], FD-SOI  $V_T$  can be configured in different ways, enabling us to dynamically modulate the transistor speed [76,93], which is incomparably intrinsic to bulk CMOS or FinFET. Unlike the well in bulk CMOS PFET and NFET only corresponding with an n-type and p-type implant, respectively [94], the well in FDSOI features selectivity decided by the  $V_T$  required, meaning that the good polarity of the dopant is the same in the case of S/D [95]. Body bias is the most critical characteristic of FDSOI, consisting of forward body biasing (FBB) and reverse body biasing (RBB) [96]. By that, FDSOI possesses lower  $V_{DD}$  to achieve an identical drive current which leads to a decrease in both off- and on-state power, which profits the application of ultra-low power [97,98].



**Figure 9.** Schematic of body biasing in FDSOI.

### 2.3.3. FDSOI Roadmap and Future Perspectives

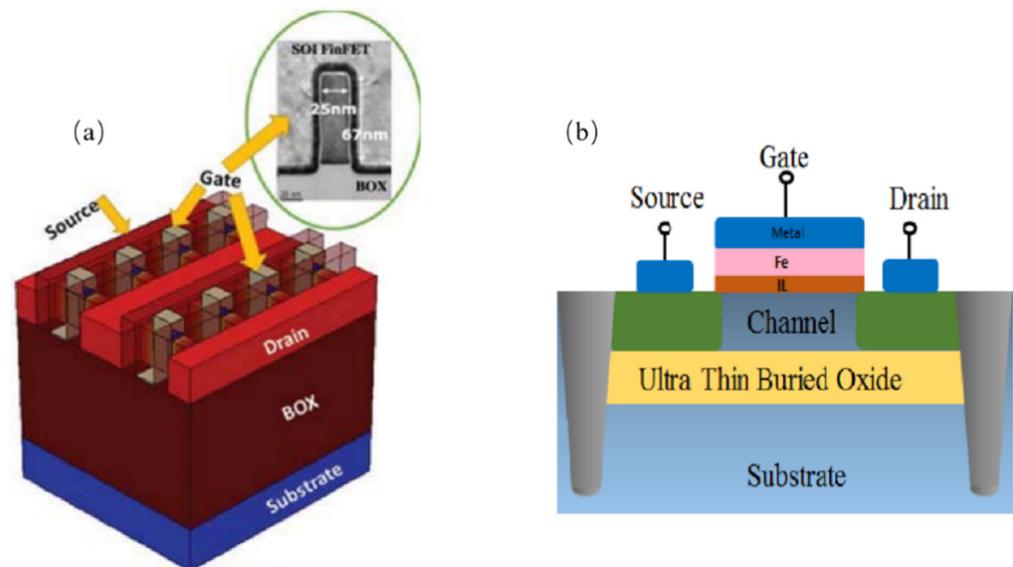
Recently, 28 nm and 22 nm node FDSOI technologies have been placed into a wide range of consumer products, especially low-power consumption and the high energy-efficiency market, thanks to the implementation of the ultra-thin BOX and SOI thickness techniques, which also enable nodes below 14, 10, and even sub-10 nm [80,99–102]. For the 7 nm node examined in the research, the SOI thickness could be thinned down to 4.5 nm [103].

Additionally, some enhancement methods to booster device performance, such as strain, new materials for the channel, access to contact, and spacers, have been recommended. With applications ranging from induced strain engineering [104] to the finite thin SOI layer of FDSOI [105], the general use of channel strain materials (intrinsically strained) is a very effective method [106,107]. Typical strained channel materials are biaxial tensile strain Si or biaxial compressive strain Ge on the SiGe layers, or uniaxial stress induced by the SiGe source/drains layer. Nitride liners are also commonly used to add stress to FETs [108,109]. However, strain integration in these low-dimensional channels is very challenging. An appealing approach to enhance the performance of such low-dimensional devices by boosting the carrier mobility is to replace the Si channel with a high-mobility material, such as Ge, SiGe, and III–V [110,111].

New MOS structures such as SOI/sSOI FinFET and negative capacitance FDSOI (NC-FDSOI) are introduced as follows (Figure 10). The more the gate numbers over the channel region are increased, the better their carrier transport control capability [112,113]. SOI/sSOI FinFET have an advantage over conventional single-gate devices concerning their performance in dealing with device leakage and current. Moreover, they have much

lower process-induced variability due to SOI technology with BOX isolation instead of junction isolation [114].

In addition, negative capacitance field-effect transistor (NCFET) incorporating a ferroelectric layer is a promising solution to device scaling down by reducing effective oxide thickness [115,116]. Since there is no reduction in the thickness of the physical gate oxide layer or the interface silicon dioxide layer, it enhances gate control without sacrificing gate leakage current or mobility. NC-FDSOI is reported to scale to a 2 nm node with high-performance applications, and meets the 100 nA/ $\mu\text{m}$  leakage requirement in the simulation level [117]. The technology also the advantage in that both the  $I_{\text{OFF}}$  and  $I_{\text{ON}}$  of NC-FDSOI can be effectively adjusted by the back-gate bias.



**Figure 10.** (a) New device structure for SOI FinFET [118] and (b) NC-FDSOI [119]. Reprinted with permission from ref. [118,119]. Copyright 2018 IEEE Publisher.

### 3. Advanced TCAD with AI for the 5 nm Node and beyond

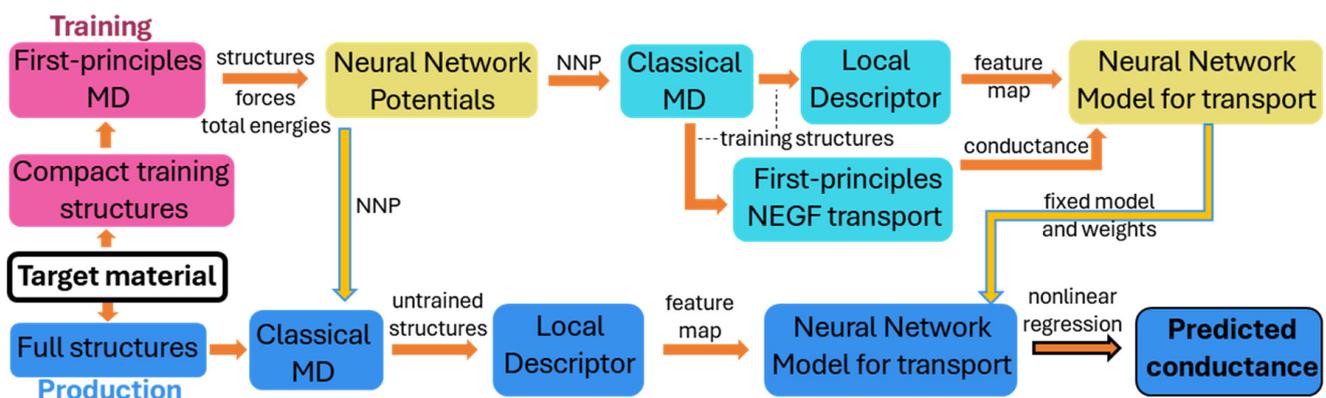
One of the major influences of AI on semiconductor applications is the use of AI-enabled technology computer-aided design (TCAD) tools and methods to optimize chip performance, power consumption, and reliability. AI can help engineers finish the layout design, verification, synthesis, and simulation, as well as to explore novel architectures and semiconductor materials. AI can also provide more efficient and scalable designs of complex systems-on-chip (SoCs) that integrate multiple functions and domains. TCAD plays a critical role in the design and pathfinding of state-of-the-art semiconductor devices. However, as semiconductor devices scale down to the 5 nm technology node and beyond, quantum-physics-induced effects are inevitable, leading to a huge rise not only in TCAD theory and methodology complexity, but also in computational cost. To improve the predictability and the computational efficiency of TCAD simulations, there have been many studies on developing advanced physical models beyond drift-diffusion DD frameworks [120], as well as incorporating high-performance computing [121]. Alternatively, artificial intelligence (AI) technology, including machine learning (ML) and deep learning (DL) approaches, is introduced into TCAD and implemented into not only atomistic calculation but also device- and circuit-level simulation.

#### 3.1. Atomistic Calculation with AI

Density functional theory (DFT) and DFT-based ab initio TCAD are powerful tools for calculating and analyzing the properties of the material in nanoscale semiconductor devices, especially when the critical dimension of devices reaches atomistic scale, and the quantum

effect is not negligible. However, DFT theory is quite computationally expensive, and a trade-off between accuracy and efficiency is required. Therefore, novel machine learning approaches are introduced when considering that the neural network (NN) shows good capability in capturing nonlinearity and predicting targets according to given samples. One example is to solve the Schrodinger equation and achieve almost exact solutions for molecules with up to 30 electrons, whose efficiency outperforms the state-of-the-art variational ansatzes with high accuracy [122]. Another is that the NN performs as a wave-function Ansatz for the many-electron system in ab initio calculation and predicts the dissociation process of the nitrogen molecule and hydrogen chain [123]. The neural network architecture could also be part of the calculation. This has been demonstrated in a recent study, in which the neurons act as the tight-binding (TB) matrix elements in the Hamiltonian parameterization of the TB model for energy band calculation [124]. From calculation methodology to case studies, several studies have been reported in which machine-learning-augmented DFT works efficiently with high accuracy in atomistic modeling for devices, including the prediction of atomic force in phase change memory [125], the calculation of potential energy surface in SiGe alloys [126], and the simulation of surface reconstruction of the Si (111)-(7 × 7) surface [127].

In practical TCAD applications in the development of the 5 nm node and beyond, quantum transport features and device merits are essential in simulations. Apart from the calculation of electrostatic properties, the quantum transport simulation using the Non-Equilibrium Green Function (NEGF) method is performed along with the machine learning method as reported in recent studies. M. Burkle et al. have proposed an NN-NEGF simulation framework that could predict the conductance of a large system whose prediction accuracy agrees with the experiment quality and the calculation cost is only a fraction of the conventional first-principle methods, as shown in Figure 11 [128]. Additionally, recently Y. Zhou et al. presented AD-NEGF, the first end-to-end differentiable NEGF model for quantum transport simulation, where the numerical calculation is carried out in the deep learning framework Pytorch v2.2.2, and the backward gradient is calculated efficiently using the proposed implicit layer technique [129]. As we could see above, the machine learning method has been a strong candidate to overcome the bottleneck of computation efficiency in the first-principle method for device analysis and optimization.

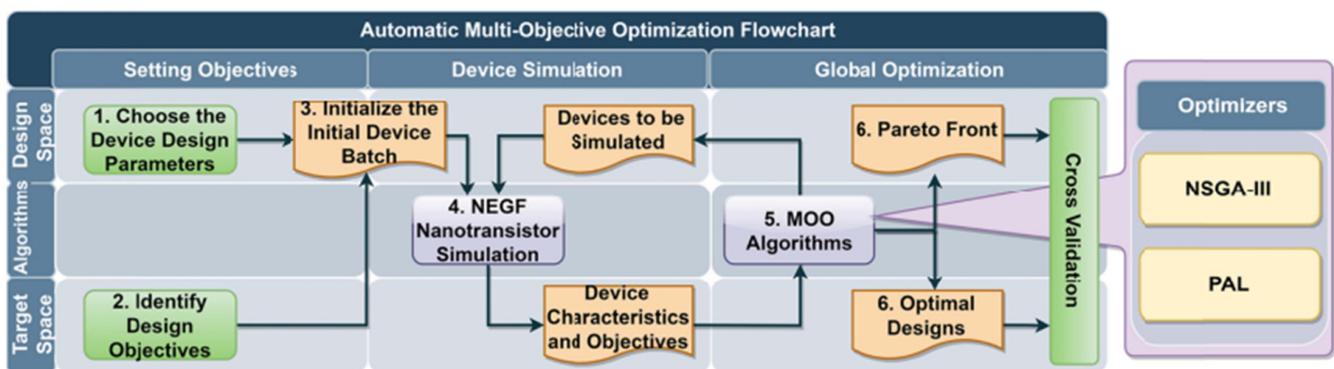


**Figure 11.** The proposed NN-NEGF computation framework.

### 3.2. Semiclassical Device Simulation with AI

Although a lot of progress in atomistic simulation with AI has been made in recent years, the computational cost is still too expensive to satisfy the massive simulations demanded by the industry. Bridging TCAD and AI in the Drift-Diffusion framework, i.e., the semiclassical level, is more compatible to current sub-5 nm node development. To this end, the following updates have been proposed and addressed by several academic and industrial research groups. In general, traditional Design of Experiment (DOE) using TCAD is time-consuming due to a huge number of calculations. A possible remedy for

this problem is machine learning-based modeling. It is commonly shown in recent studies that artificial neural networks (ANNs) have a remarkable ability in capturing nonlinear relationships with high accuracy between electrical characteristics and device parameters. This indicates a substantial decrease in computation cost in estimating electrostatic potential [130,131], capacitance–voltage (CV) relationship, current voltage (IV) [132–134],  $V_T$  [135], metal work function [136], as well as other figures of merit [137,138]. Furthermore, machine learning works well not only in the prediction of device characteristics but also in device optimization, where machine learning is coupled with a multi-objective optimization algorithm where the trade-off between electrical characteristics is carefully considered. For instance, a multi-objective optimization (MOO) framework is proposed with Pareto active learning to optimize 2D transition metal dichalcogenide (TMDC) and black phosphorene FETs as shown in Figure 12 [139]. Additionally, the 2D FET optimized by the proposed framework meets the International Roadmap of Devices and System target of 2025 and 2028 technology nodes.



**Figure 12.** The proposed MOO framework couple with machine learning for 2D TMDC and black phosphorene FETs [139]. Reprinted with permission from ref. [139]. Copyright 2021 IEEE Publisher.

### 3.3. Compact Modeling with AI

In addition to numerical simulations, analytical compact models for SPICE simulations are also very important. Compact modeling of emerging devices is essential for design-technology co-optimization (DTCO) and path-finding activities. However, quantum-physics-based standard models for FETs at the scaling limit which capture the non-linearity between electrical characteristics of transistors and design parameters demand a lot of time and domain expertise to be built [140,141]. In 2017, L. Zhang et al. proposed a new method that employs ANN design for the compact modeling of generic transistors [142], which is a novel option for the compact modeling of emerging devices. Detailed ANN design rules of compact modeling are discussed in ref. [143], where ANN model accuracy is optimized, and SPICE simulation turn-around time is reduced. Several models of novel devices, including ferroelectric FETs [144] and Si cold source GAA FETs [145], are reported to be built by ANN-based compact modeling, which indicates that ANN-based compact modeling is a promising candidate for DTCO and pathfinding.

### Part Two: Process of Nanoscale FETs

#### 4. Advanced Lithography Technique

Rayleigh formula describes the resolution limit for optical lithography, shown as:

$$R = k1 \frac{\lambda}{NA}$$

where  $R$  is the resolution term,  $NA$  stands for the numerical aperture of the project lens of the lithographic tool,  $\lambda$  denotes the wavelength of the applied light source, and the  $k1$  factor is related to the challenges of the lithography.

The formula has clearly indicated the methods whereby the resolution can be improved.

- (1) Wavelength reduction: i-line (365 nm), DUV KrF (248 nm), DUV ArF (193 nm), and EUV (13.5 nm).
- (2) DUV NA increase: from 0.93 of ArF dry tool to 1.35 of ArF immersion at 193 nm lithographic tools.
- (3) EUV NA increase: from 0.33 to 0.5 at current EUV tool and future high-NA EUV tools.
- (4) K1 reduction through various patterning enhancement techniques (PETs).

Lithographic tool providers such as ASML (Veldhoven, The Netherlands) have developed their tools to enable Moore's Law to continue.

The theoretical limit of the  $k_1$  is about 0.25. When  $k_1$  is smaller than 0.25, the image contrast is very low so that there is no image that can be printed. As Figure 13 shows, in earlier years, the  $k_1$  factor is above 0.5 when the imaging has high contrast, and there is no need to implement various PETs. When the  $k_1$  factor is below 0.5, it moves to the low-contrast era, where various PETs are required, such as optical proximity correction (OPC), and source mask optimization (SMO) [146–148]. In both high-contrast and low-contrast eras, the patterning has been achieved through single exposure and single etch approach. The wavelength has been reduced from i-line to KrF to ArF, and the NA has been enlarged to achieve the required resolution following Moore's Law.

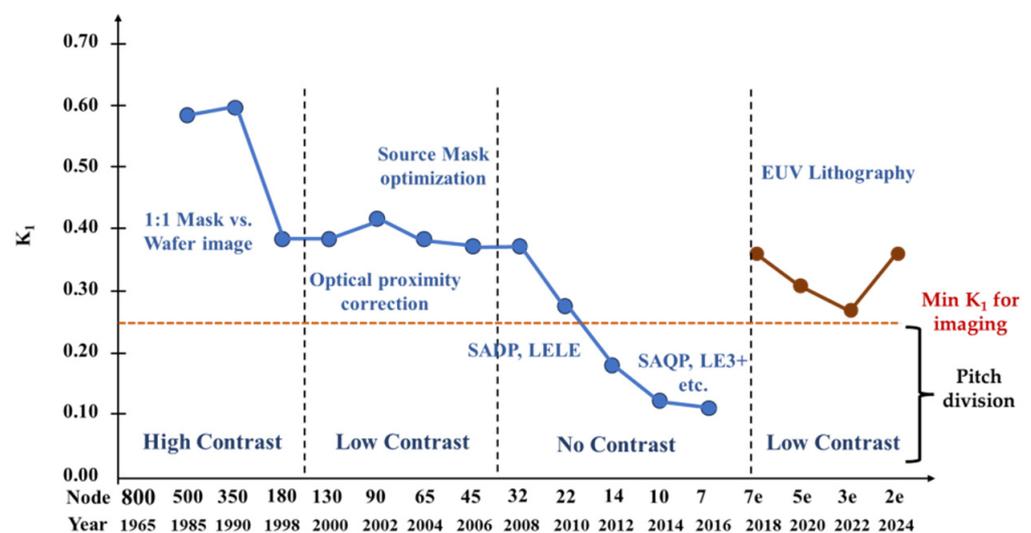


Figure 13.  $K_1$  factor evolution through the years of technological advancement.

Until sub-20 nm nodes are reached, the FinFET structure in the Logic/MPU process has been introduced [149]. At this technology node, the  $k_1$  factor is close to its theoretical limit of 0.25, using DUV ArFi lithographic tools. This is called the 'No Contrast' region, as Figure 13 shows. This means the traditional single litho-etch approach can no longer be used to shrink patterns [146,150]. EUV was not mature enough either by that time to continue the traditional approach. Double patterning and quadruple patterning thus have been developed as practical solutions to continue the node shrinkage. There are two major types of these multiple patterning techniques, litho-etch-litho-etch (LELE) and self-aligned double patterning (SADP) or self-aligned quadruple patterning (SAQP) [151]. In SADP or SAQP (SAmP), there are several steps of thin-film depositions and etchings to reduce the pitch. LELE is implemented for 2D structures such as contact holes via logic metal layers. SAmP is implemented for line and space patterns, such as Fin gate layers. After the SAmP processing steps, the lines are cut, or spaces are blocked, to form device patterns.

#### 4.1. EUV in Mass Production

EUV lithography has been used in chip mass production since 2019, when TSMC announced at the IEDM that EUV technology satisfied high volume production requirements; thus, they started the volume ramp of the enhanced 7 nm technology with EUV insertion [152]. In the same year, the first few consumer chips at 7 nm nodes with reference to EUV processing lithography, HUAWEI Kirin 990 Series 5G SoC (Shenzhen, China) [8,153], and Samsung Exynos 9825 (Suwon, Republic of Korea) [152], were also announced. EUV has been used in mass production at DRAM since Samsung's announcement of the 1z process node [154]. Since the introduction of EUV, many major technical challenges have been overcome, i.e., source power, pellicle, tool availability, resist resolution, and mask manufacturing [155]. The EUV light source, EUV photoresistance, line width roughness (LWR), etc., have been introduced as nanomaterials references therein [155]. EUV is now part of the baseline manufacturing processes, as Wallace reported at 2020 SPIE [150]. To a large part, this is thanks to the excellent progress made for all areas of EUV lithography over the past several years.

Since the successful EUV adoption in mass production [152,153,156], this has brought the  $k_1$  factor back to the low-contrast ( $k_1 > 0.25$ ) region from the no-contrast ( $k_1 < 0.25$ ) region, as shown in Figure 13. From 22 nm to 7 nm, there is no contrast and no imaging using single lithographic exposure, thus LELE and SAmP are used for pitch division. At the 7e (nm) node, the EUV is implemented, which brings the  $k_1$  factor back to the lower  $k_1 > 0.25$  region, as shown in Figure 13. In this lower  $k_1$  region, single EUV exposure (NA 0.33) is possible using various patterning enhancement techniques. At the 3e (nm) node, the EUV single exposure (NA 0.33) reaches a  $k_1$  factor of 0.25; thus, a high NA EUV (0.55) is needed to maintain a lower  $k_1$  single-exposure approach to form images.

EUV lithography can reduce the manufacturing complexity since it enables the single-exposure single-etch approach to pattern-critical layers. For the less critical layers, DUV has still been used to achieve overall cost effectiveness. Consequently, the lithography solutions need to support the mix and match use of EUV and DUV.

#### 4.2. Overlay and Edge Placement Error (EPE) Challenges

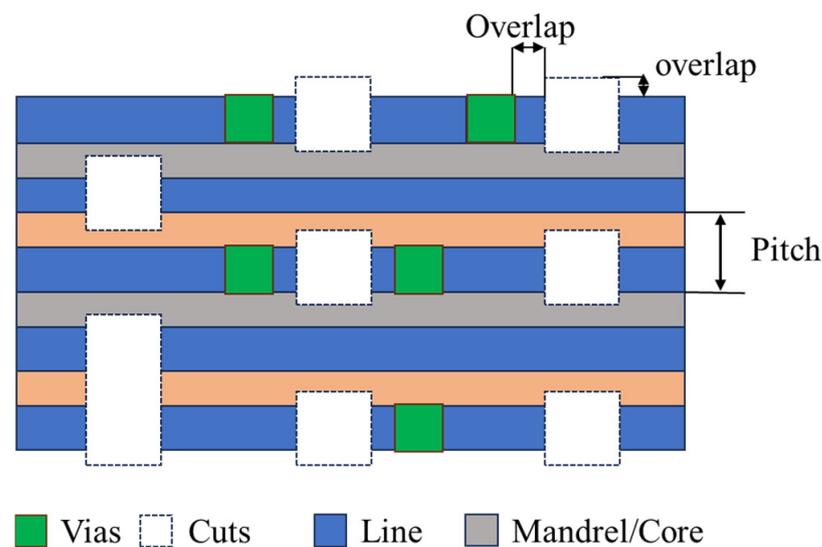
With the continuous shrinkage of the design rules, the overlay requirement is becoming more and more tight. The mass production for advanced nodes requires overlay performance to be 2 nm and below in EUV platforms [157]. This is challenging for both overlay correction by scanner as well as overlay measurements.

For the global overlay measurement, the IBO (image-based overlay) strategy has been widely used in mature products. As the technology node continues to shrink, the DBO (diffraction-based overlay) strategy has showed impressive performance. Studies suggest that IBO is better for non-tool-induced shift, while DBO is better for tool-induced shift [158,159]. However, IBO has faced more contrasting challenges when SADP and SAQP patterning film stacks have been introduced, while DBO has shown less film stack dependence with good overlay precision [160].

To support smaller technology nodes, DBO metrology marks have been reduced in size, called uDBOs. Thus, uDBOs have more flexibility to be placed not only in scribe lines, but also in primary higher-order intrafield corrections [158]. The uDBO metrology has also implemented multi-wavelength measurements. Compared with prior generations of dual-wavelength methodology, its accuracy and robustness to process variation have both been improved [159].

The second challenge in overlay is the cross-scanner platform matching between DUV and EUV. This is because the intrinsic design is different for sub-systems such as projection optics, reticle clamping, and wafer clamping for DUV and EUV systems. The current practice of EUV vs. DUV matching includes two steps with reasonable performance: I. Both EUV and DUV scanner grids need to be calibrated to a reference wafer grid which contains a dense intrafield layout. II. Fine-tuning is carried out for matching by using higher-order corrections per field on the EUV scanner [160].

In the traditional single lithography and the single-etch approach, the critical parameters to control in the lithographic process are CD (critical dimension) and overlay variations. In a multi-patterning scheme, such as SAmP and LELE, a new parameter, EPE (edge placement error) is introduced. It combines CD, overlay errors, and includes local variations of CD and LWR (line width roughness) [160]. EPE is defined as the displacement of edges of two features from their target locations, as shown in Figure 14. In this example, the line/space grating (green color) is patterned using ArFi and a subsequent SAmP. The 2D geometry is created by cutting this grating pattern. The via layer is placed on top of line and next to the cut pattern. In lithography and SAmP, because of the processing variation, the displacement of the edges of the 2D cut/via can differ from the intended locations. This results in the overlap distance in both x and y direction are out of design distance, as shown in Figure 14.



**Figure 14.** A schematic picture of an EPE as tolerance for the relative placement of two edges (litho cut, via, and spacer feature).

EPE can be calculated by an analytical method, as follows [160]:

$$3\sigma_{\text{EPE}} = \sqrt{3\sigma_{\text{overlay}}^2 + \left(\frac{3\sigma_{\text{CDU}_{\text{lines}}}}{2}\right)^2 + \left(\frac{3\sigma_{\text{CDU}_{\text{cuts}}}}{2}\right)^2 + \frac{3\sigma_{\text{LWR}_{\text{lines}}}^2 + 3\sigma_{\text{LWR}_{\text{cuts}}}^2}{2}}$$

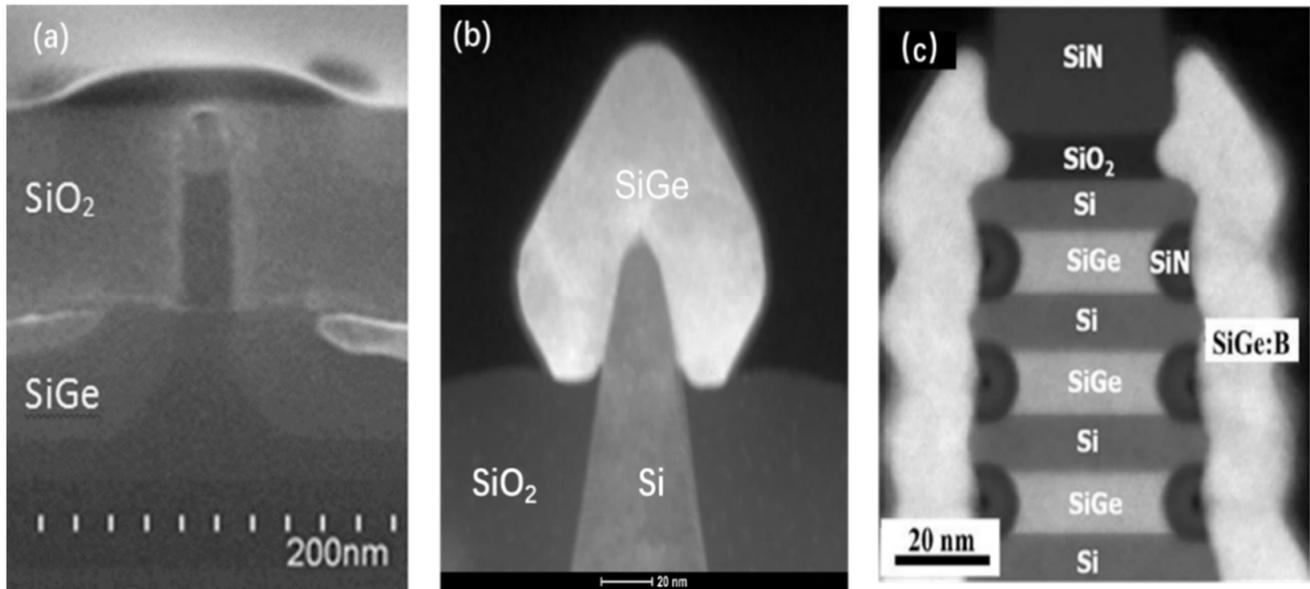
This equation consists of overlay errors and global CD errors from the lines and the cuts. It also includes local CD errors such as LWR of lines and cuts. Apparently, in order to minimize error, EPE requires optimization across the scanner platform of the lithography processing steps.

## 5. Epitaxy in Transistor Structures

### 5.1. Selective Epitaxy Growth (SEG) of SiGe in S/D Regions

As the technology node shrinks, strain engineering in the channel region is an effective technology to improve transistor performance. By depositing stressor material in S/D regions, strain is induced in the channel region which is one of the key factors in the development of aggressively scaled nano transistors. SiGe(B) and Si(P) materials are formed by SEG in the recessed S/D areas as the stressor materials in pMOS and nMOS, respectively. SEG of Si<sub>0.83</sub>Ge<sub>0.17</sub> was initially integrated to enhance the carrier mobility in the 90 nm technology node [161]. To obtain more strain inside the channel, the Ge content of SiGe in S/D areas has been increased node by node to more than 50% [162,163]. This is a huge challenge, as the increase in Ge content is accompanied by an increase in epitaxial mismatch defects. At the same time, the S/D morphology was constantly adjusted as the

device structure changes. The sigma ( $\Sigma$ ) shape of S/D was used to generate more strain in the channel area. This is because the SiGe films grew closer to the channel area [164–166]. Then, the morphology was changed from 2D planar to 3D FinFETs [167,168] and GAA Nanosheet FETs [169], as shown in Figure 15.

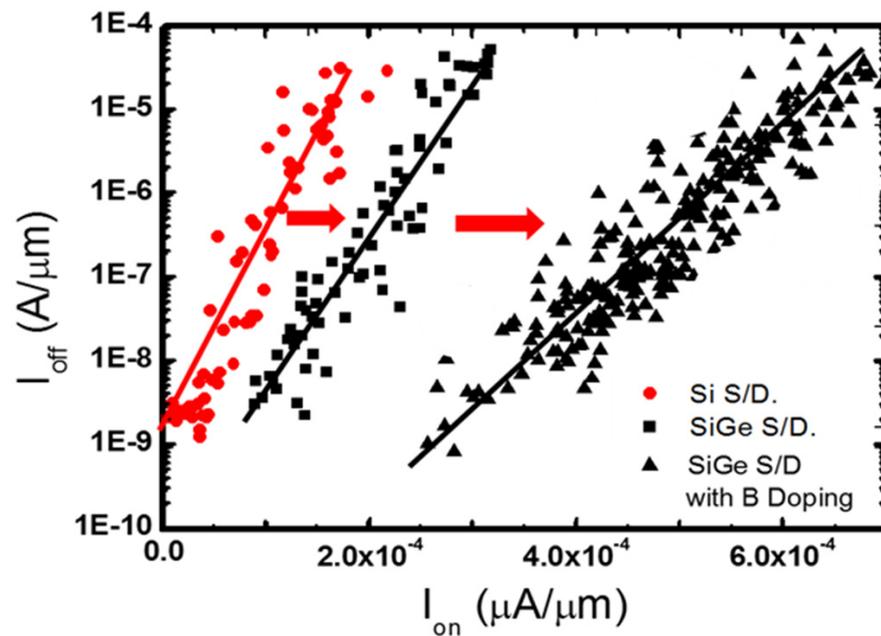


**Figure 15.** SEG SiGe in source and drain (S/D) regions in different structures: (a) 2D planar [170], (b) 3D FinFETs [7] and (c) GAAFETs [169]. Reprinted from ref. [7,169,170]. Copyright Elsevier 2016, AIP 2013, and IEEE 2022 Publisher.

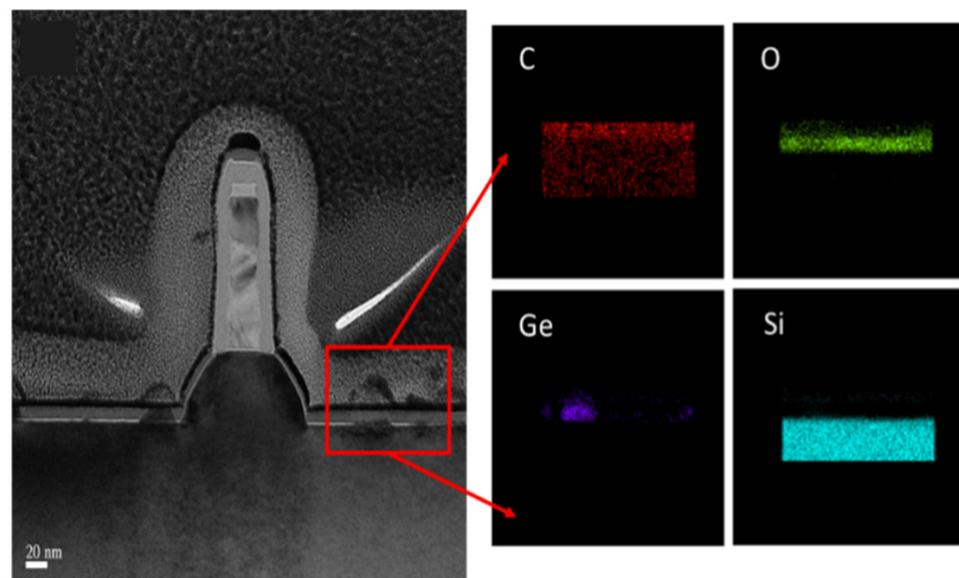
The SEG of SiGe on Si Fins requires some issues to be paid attention to, namely, defect-induced strain relaxation [171], facet formation [172,173], and Si Fins damage. However, it is extremely difficult to obtain selectivity and induce the strain in the structure of GAA Nanosheet FETs, with the inner spacer SiN, HM (hard mask) SiO<sub>2</sub> and SiN, and multi-Si nano sheets exposed. In the SEG process, the deposition of SiGe loses its selectivity on the SiN surface. Finally, the growth of SiGe film will cover the SiN inner spacer, and the topography will be discontinuous and unsmooth, which will affect the amount of strain generation [174].

During the S/D SEG process, the B in situ doping was also applied in the S/D to reduce sheet resistance in the FinFET PMOS structure [175,176]. Figure 16 shows the  $I_{ON}/I_{OFF}$  ratio comparison image of the FinFET PMOS devices. SiGe:B S/D devices show improved performance ( $I_{ON}/I_{OFF}$  ratio, drive current), which is standard for the FinFET device. Although some strain in the SiGe film is compensated after B doping, Ion levels were increased when contact resistance declined in S/D. It also can be predicted that the decrease in SiGe:B contact resistance of S/D is the most key factor for the performance enhancement of the GAA NS transistors beyond the 5 nm node. One of the critical points for losing the strain is the formation of silicides. Ni is still the most suitable metal compared to other contact metals for the 5 nm technology node due to low Si consumption [177–179].

The quality of the initial Si surface has an important role in the quality of the SEG. This relates to the cleaning and thermal treatment of the exposed Si surface prior to the epitaxy. For the 2D planar and FinFETs structure, standard cleaning methods (SPM, APM, and DHF-last) are widely used to avoid any impurities or residues on the Si surface [171]. As shown in Figure 17, the C content of the Si surface is found between SiGe and Si, and SiGe film was grown independently [171,175]. These organic contaminations and polymers are not completely removed by standard cleaning, which leads to the poor growth of SiGe.



**Figure 16.** The  $I_{ON}/I_{OFF}$  ratio of FinFET PMOS fabricated with different S/D devices [175]. Reprinted with permission from ref. [175]. Copyright Springer 2019 Publisher.



**Figure 17.** TEM cross-section image and EDS element mapping of relatively defected SiGe growth layer [171]. Reproduced from ref. [171], open access by Springer, 2017.

One of the important issues faced is contact resistance in S/D windows. This issue can be solved by forming silicides, but both the thermal budget and Si consumption are key roles in the transistor performance. Ni silicides have been widely used; moreover, the relaxation of the SiGe layer could be diminished by introducing carbon in the SiGe layers [176–179]. The SEG process of SiGe suffers from a pattern-dependency problem when, in the profile of the epi-layer, the exposed Si areas in openings (for example, in the S/D regions) in a chip differ for different layouts [19–21,38,180–183]. The main reason behind this problem is the non-uniform consumption of reactant gases ( $\text{GeH}_4$ ,  $\text{SiH}_4$ , DCS, HCl) over a patterned wafer (global effect) or an array of openings inside a chip (local effect), when the layout of chip is changed. Until now, the pattern dependency of SEG in planar devices and FinFET devices has been systematically studied [180–183], but for

GAA Nanosheet, devices have not been carried out due to the complexity of work. It is challenging to calculate and forecast the consumption of reactive gas in the 3D multiple stacks, not only because of size shrink and the density increase of the planar in the layout, but also because of the GAA device structure. A remedy to this problem is to introduce growth modeling which takes into account the chip layout and transistor's structures in advance to predict the chip layout and growth parameters in a way that results in the uniform consumption of reactant gases during the growth period [184–188].

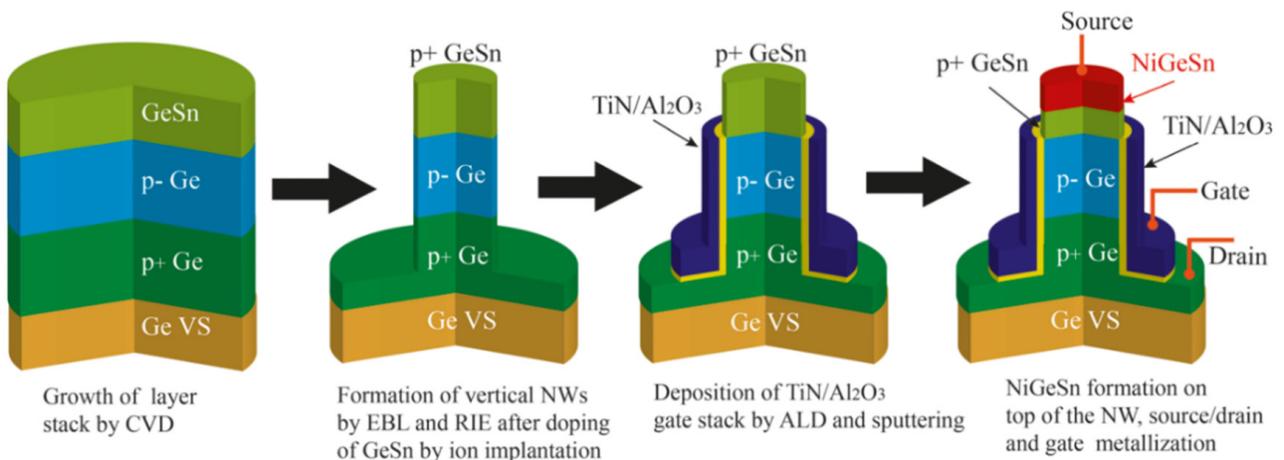
### 5.2. Epitaxy of GeSi and Ge for Channel Region

To improve the performance of MOSFETs, novel materials, new concepts, and new device architectures are under continuous research and development. Despite the rapid development of Si CMOS technology, there are several technical challenges currently faced, mainly including the gate controllability of electrical charges. To improve the gate control ability, FinFETs have been developed for the technology nodes beyond 22 nm. For the ultra-scaled sub-5 nm technology nodes, GAA nanowire (NW) transistors provide excellent gate control and immunity against the SCEs. After reviewing the evolution of Si transistors, ranging from planar MOSFETs to FinFETs and GAA NW FETs, device performance had been greatly improved via introducing group IV semiconductor materials, including SiGe, Ge, GeSn, etc. Other strategies include band engineering, heterostructure, and strain engineering, which are helpful for enhancing the carrier mobility via changing the carrier effective mass. Compared with traditional Si material, Ge (Sn) features better hole mobility due to the reduced effective mass. Thus, tremendous effort has been made to explore Ge (Sn)-related GAA NW FETs towards the sub-5 nm technology node. Up to now, there are only three groups that have demonstrated the presence of vertically stacked Ge (Sn) GAA NW FETs owing to the cutting-edge Ge (Sn) CVD growth technology (Table 3).

**Table 3.** Summary of Ge (Sn) GAA NW FETs in terms of year, institution, Sn composition, channel length,  $I_{ON}$ ,  $I_{ON}/I_{OFF}$ , SS, and stack number.

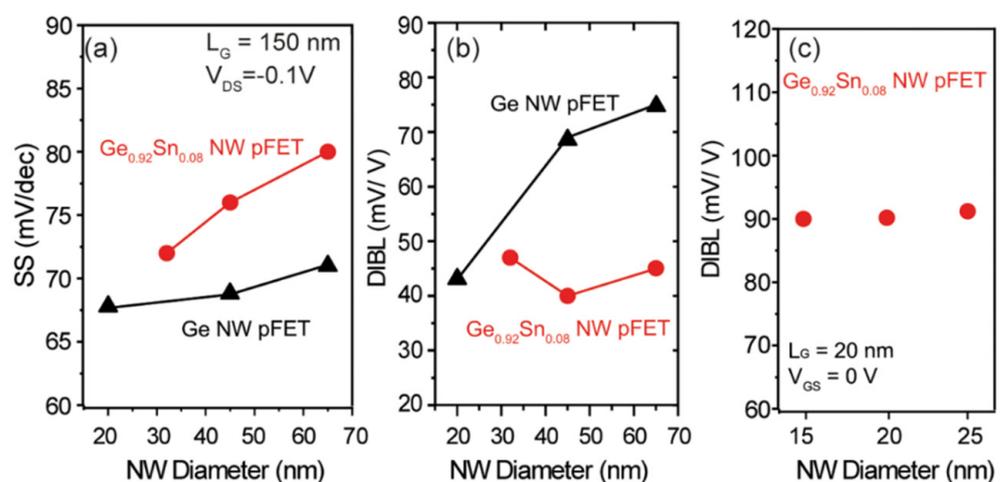
Year	Institution	Sn	Channel Length	$I_{OFF}$ ( $\mu A/\mu m$ )	$I_{ON}/I_{OFF}$ Ratio	SS (mV/dec)	Stacks	Ref.
2017	National Taiwan University	6%	150 nm	1400	— —	84	1–2	[189]
		10%	60 nm	1850	— —			
2019	National Taiwan University	9%	— —	120	— —	84	3	[190]
2020	PGI 9	8%	150 nm	— —	$3 \times 10^6$	72	1	[191]
2020	PGI 9	8%	— —	— —	$3 \times 10^6$	67	1	[192]
2021	National Taiwan University	10%	80 nm	86	— —	— —	4	[193]

After carefully considering the band alignment and strain engineering, M. Liu et al. [192] designed the GeSn/Ge heterostructure-based high-performance vertically stacked GAA NW FETs with traditional Si CMOS processing technology. The main growth processes are as follows: (I) growth of the intrinsic Ge layer on Si (100) substrate in an RPCVD reactor; (II) 200 nm thick p-type doped Ge layer growth (boron doping concentration:  $2.5 \times 10^{19} \text{ cm}^{-3}$ ); (III) 150 nm thick slightly p-type doped Ge layer growth, which is used for channel length definition; (IV) 60 nm thick GeSn layer with 8% Sn incorporation. To realize the vertically stacked  $\text{Ge}_{0.92}\text{Sn}_{0.08}/\text{Ge}$  GAA NW FETs, the processes are schematically outlined in Figure 18. It should be noted that fabrication processes should be implemented at the low thermal budget, thus maintaining the structural stability for GeSn.



**Figure 18.** Schematic diagram of the GeSn/Ge heterostructure growth and vertically stacked GAA NW FETs process [192]. Reprinted with permission from ref. [192]. Copyright 2021 ACS Publisher.

To study the diameter effect on the performance of  $\text{Ge}_{0.92}\text{Sn}_{0.08}/\text{Ge}$  GAA NW FETs, NWs with three diameters were fabricated. Electrical characteristics, such as SS and DIBL on the NWs, were extensively characterized. Compared with the Ge NW devices, GeSn/Ge NW devices with a gate length of 150 nm exhibit higher SS due to the lower thermal budget limitation of the GeSn/Ge heterostructure and higher density of interface traps ( $D_{it}$ ) (Figure 19a). With the reduced NW diameter, GeSn/Ge NW devices feature steeper SS than that of their Ge counterpart, which can be traced back to the improved gate control ability. Moreover, the DIBL behavior of GeSn/Ge NW devices was further compared to the Ge NW pFETs. It is highly expected that  $C_{it}$  should be higher than Ge NW pFETs, owing to the lower thermal budget, which, therefore, displays a lower DIBL (Figure 19b). Therefore, the GeSn/Ge heterostructure yields a better performance compared to the Ge homojunction. To verify the experimental DIBL results, DIBL values were also extracted from the simulation (Figure 19c). As a result, the simulated DIBL values are 40–50 mV/V, which is larger than the experimental data. Nevertheless, the qualitative performance is well reproducible [194].



**Figure 19.** (a) Measured SS, (b) measured DIBL, and (c) simulated DIBL as a function of NW diameters [192]. Reprinted with permission from ref. [192]. Copyright 2021 ACS Publisher.

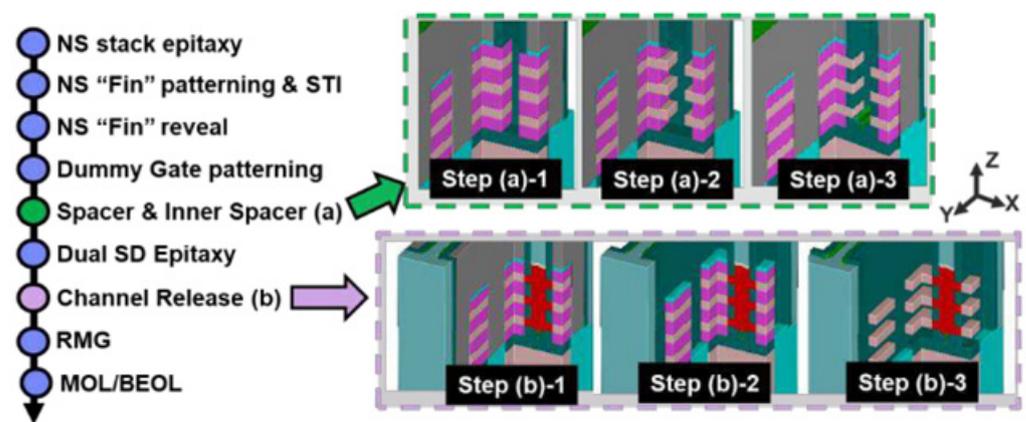
### 5.3. Growth of SiGe/Si for Gate-All-Around (GAA) Structures

In both vertical and horizontal GAA structures, fabricating nanowire or nanosheet channels from Si/SiGe multilayers is widely used because of advantages in the process

and material properties. Si and SiGe are compatible with traditional Si-based processes. High-quality Si/SiGe stacks can be epitaxially grown on Si substrates. The Si/SiGe stack has high flexibility in its process. By adjusting the growth sequence and Ge content of the Si/SiGe stack, different channel materials can be obtained, such as Si,  $\text{Si}_{0.7}\text{Ge}_{0.3}$ , and  $\text{Si}_{0.2}\text{Ge}_{0.8}$  [195,196]. Apart from that, the high mobility of Ge can boost the electrical performance of the device.

In terms of process, both Si and SiGe can be used as the channel, which depends on the structure of the Si/Ge thin film material and the etching process [197–199]. It is worth mentioning that if you want to use SiGe as the sacrificial layer and Si as the channel, then epitaxial growth of low Ge components is recommended, as this avoids creating defects during the growth process. Another advantage is the flexibility of the nanosheet width.

The deposition of Si/SiGe MLs and the subsequent etching process are the main differences between conventional FinFET and GAAFET fabrication, as shown in Figure 20 [200]. The process of Si/SiGe epitaxial growth is an important part in advanced CMOS fabrication.



**Figure 20.** A schematic of a multilayer nanosheet GAA process sequence. (a) IS formation, and (b) CR process steps illustrated along dummy gate in x-direction, and along  $W_{\text{NS}}$ /"Fin" in y-direction [200]. Reprinted with permission from ref. [200]. Copyright 2021 IOP Publisher.

The commonly used growth methods of the Si/SiGe stack are reduced pressure chemical vapor deposition (RPCVD) [2] and molecular beam epitaxy (MBE) [201]. Considering the subsequent process, what is required is Si/SiGe stacks with sharp interfaces and high quality. The thermal budget also should be considered [202,203].

#### Different Novel Epitaxial Si/SiGe Is Used as Channel to Boost the Device Performance

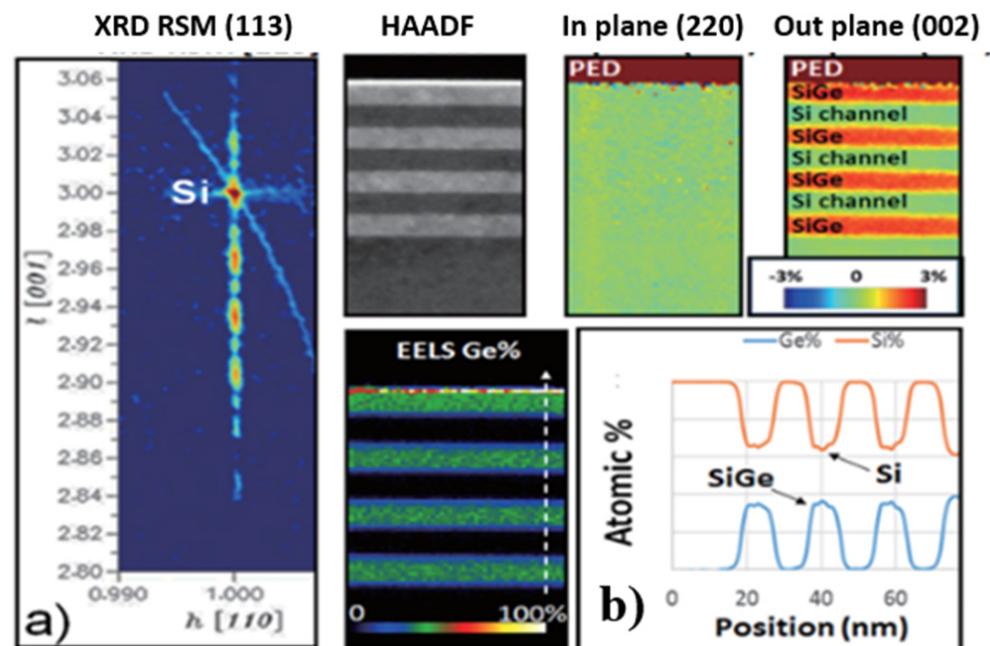
Starting from the epitaxy of  $\text{Si}_{0.7}\text{Ge}_{0.3}$ /Si multilayers, S. Barraud et al. reported a two-stacked Si nanosheet [204]. The thickness of the Si and SiGe layer was chosen at 9 nm to ensure the good crystallinity of epi-layers. SiGe was used as the sacrificed layer to form the Si channel. Similarly, a seven-level-stacked Si nanosheet GAA transistor was fabricated. Extremely high current drivability ( $I_{\text{sat}} = 3 \text{ mA}/\mu\text{m}$  at  $V_{\text{DD}} = 1 \text{ V}$ ), and electrostatic control ( $\text{SS}_{\text{sat}} = 64 \text{ mV}/\text{dec}$ ) have been shown in such devices [205].

A pTFET with a  $\text{Si}_{0.2}\text{Ge}_{0.8}$  nanosheet of 120 nm in width containing SiGe/Si multilayers as active regions (SiGe is the channel material) have been manufactured [206]. Si sacrificial layers are removed using wet etching, and a Ge condensation process was conducted to obtain  $\text{Si}_{0.2}\text{Ge}_{0.8}$  NS. The device shows 50 mV/dec minimum SS and 70 mV/dec average SS. The  $I_{\text{ON}}$  is 69.2 nA/ $\mu\text{m}$  ( $@V_{\text{DS}} = 0.7 \text{ V}$ ), and  $I_{\text{OFF}}$  is 800 fA/ $\mu\text{m}$  ( $@V_{\text{DS}} = -0.7 \text{ V}$ ).

To decrease the sub-channel leakage and to obtain an improvement for power performance as well as minor process variation in GAA structure, J. Zhang et al. used a strategy called full-bottom dielectric isolation (BDI) [207]. This is achieved through a novel Si/SiGe stack structure. They grew an SiGe layer with high Ge% content as the initial layer on the

substrate, and then SiGe/Si stacked layers with low Ge% content were grown. The SiGe layer with Ge content was used as a sacrificial layer.

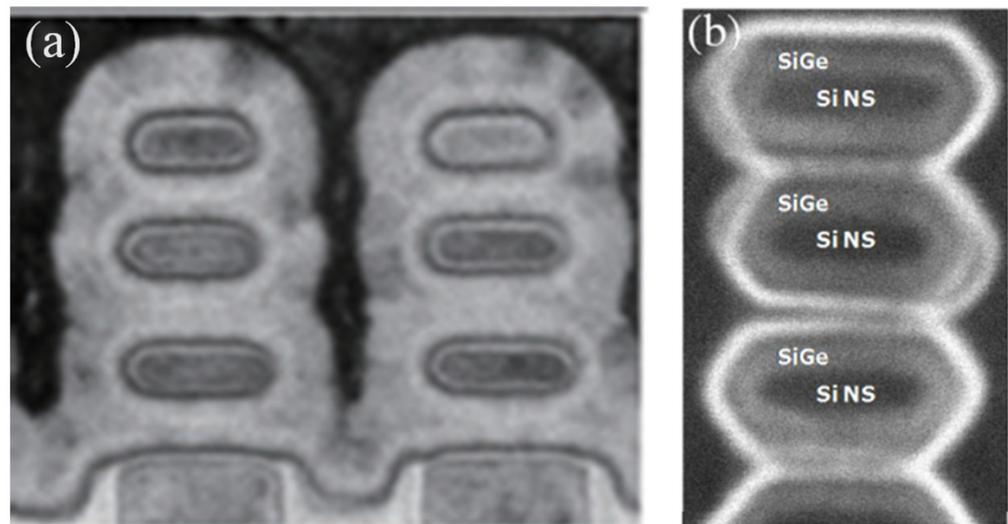
Loubet et al. investigated SiGe/Si superlattice stacks to process Si channels. Superlattice SiGe/Si multilayers were epitaxially grown to form a nanosheet [174]. As shown in Figure 21a,b, the multilayers are pseudomorphic, with compressively strained SiGe layers and unstrained Si layers. The NS structure is shown in Figure 22a.



**Figure 21.** (a) X-ray diffraction reciprocal space mapping (XRD-RSM), (b) precession electron diffraction, and electron energy loss spectroscopy (EELS) of the SiGe/Si stack [174]. Reprinted with permission from ref. [174]. Copyright 2017 IEEE Publisher.

On the basis of this research, later, J. Zhang et al. also investigated mechanical behavior in fin-patterned SiGe/Si multilayer structures [207]. Strain maps obtained by GPA show that the strain in the SiGe layer is released after fin-patterning, causing compressive strain in Si. S. Rabah et al. further studied the evolution of strains over the integration of Si-NS GAA [208]. It is shown that Si goes from unstrained to slightly tensile after fin-patterning, which is also consistent with ref. [209]. Furthermore, the recess of S/D results in the strain in Si and, later, the tensile stress is released after releasing the channels. A transition from compressive to tensile strain in SiGe/Si NS is demonstrated. SiGe/Si multilayers with Ge contents of 60% and 35% were studied. The results showed that the final stress amount is related to the Ge content of SiGe/Si multilayers.

S. Mochizuki et al. made some changes after releasing the channel and using a compressive SiGe channel for pFET [210]. Two major steps are different, with normal Si NS flow after epitaxial of SiGe/Si: Si NS trimming and SiGe selective epitaxial growth. As a result of Si nanosheet trimming and SiGe epitaxial growth on the trimmed Si nanosheet, an SiGe cladded Si nanosheet was fabricated. The structure is shown in Figure 22b. The SiGe cladded nanosheet increased hole mobility and reduced  $V_T$ . Additionally, this group later achieved a highly compressive strain in the SiGe cladded nanosheet channel by adjusting the thickness of the cladded SiGe layer and the Ge content [211]. A further improvement in hole mobility and channel resistance reduction were observed.



**Figure 22.** (a) TEM images of Si NS after replacement metal gate (RMG) [174], and (b) TEM images along the gate of the SiGe cladding layer [210]. Reprinted with permission from ref. [174,210]. Copyright 2017, 2020 IEEE Publisher.

## 6. Implantation and Advanced Doping Methods

Ever since the structure of CMOS transistors evolved from planar to 3D, e.g., inFinFETs, and even to GAA devices, homogenic doping on each side of the structure has become a challenge for the doping process [212]. Large-angle tilt implantation had been employed to realize a relatively uniform dopant distribution on both sides of the wall and the top area of a fin structure. However, for the 5 nm node and beyond, to ensure better gate control, gate all around devices like nano-sheet will take the place of FinFET gradually. Thus, the doping on the bottom area must be considered as well. Additionally, for that reason, some novel doping methods such as plasma doping and solid-state diffusion were developed. Moreover, the application of implantation was also extended by co-implantation such as in the case of Gallium to improve the contact resistance of the device.

### 6.1. Plasma Doping

Plasma doping is designed for high-dose ultra-low energy or high-aspect-ratio structure doping. It has been proven to be effective in forming ultra-shallow junctions; the whole wafer was immersed in dopant-contained plasma to obtain a conformal doping profile [212–215]. However, as there was a bias in the PLAD system to accelerate the ions, the maximum doping concentration still appears on the top area of the device and leads to nonuniform distribution. In addition, the collision between the accelerated ions and the substrate might cause lattice damage to some extent.

Recently, another plasma-related doping process named plasma-assisted doping (PaD) has been conducted to overcome the limitation of conventional implantation processes [216]. In order to reduce the surface damage created by the accelerated ion, the bias voltage in standard PLAD systems was removed. In this condition, both the damage to the substrate and doping uniformity could be improved. In the PaD process, the dopants transmit into the substrate lattice via the vacancies during doping process. There are about three steps in a PaD process. At the beginning, H plasma is generated by a low power to treat the surface of sample to obtain a high vacancy concentration near the surface area; in the following process, dopant precursor gas is ionized where the vacancies are diffused into the substrate. In the end, in situ capping layer (SiN) deposition is necessary to prevent dopant diffusion and contamination in the annealing procedure.

## 6.2. Solid-State Diffusion

Another potential solution for conformal doping is by introducing the impurities into the substrates from solid sources such as PSG or BSG films. In this method, an ultra-thin dopant-incorporated film could be deposited by ALD or CVD, etc. [217,218]. It is well known that the incident angle of implantation is restricted by the shadowing effect due to the increase in packing density. Therefore, thin film deposition has better step coverage on the whole surface of the 3D structure. Dopant-contained glasses could be a solution for conformal doping; when the deposition was completed, the dopant was then pushed into the substrate and activated under a drive-in annealing. To prevent the dopant from out diffusion, a capping layer is necessary to be deposited before the annealing. The experimental results show that the thickness of both the capping layer and the doping layer has a great impact on the final doping level of substrate [217]. For example, the concentration of Phosphorus could be improved by increasing the thickness of the PSG film, and thicker the capping layer, less dopant diffused out. As a result, the surface dopant concentration is close to  $10^{20}/\text{cm}^{-3}$ , which just satisfies the doping requirement for ultra-shallow junctions. Moreover, there is no ion bombardment in the procedure, then there is nearly no damage in the doped area.

Another doping method is called mono-layer doping (MLD). In this method, the dopant molecules are attached uniformly on the surface through a series of chemical treatment steps, and the doping level could be well-controlled by tuning the dopant composition of the molecules.

Except for the requirement of conformality, parasitic resistance is another challenge that needs to be addressed. As the critical dimension of devices decreases, the contact area decreases accordingly, and it is necessary to achieve a higher dopant activation level in S/D to lower the contact resistivity [214,219–223]. At present, the S/D of PMOS are p-type doped SiGe epitaxial films where the doping procedure is accomplished by boron in situ doping or implantation. However, p-type doping in SiGe has been a challenge for its application beyond 5 nm. An alternative solution for this is the incorporation of Gallium together with Boron, which are then activated by nanosecond laser annealing, which is believed to be one of the most promising annealing methods. As an element of ground III, both B and Ga were p-type dopant species for Ge. B shows higher active doping concentrations than Ga when they are activated by a traditional rapid thermal treatment such as RTP. However, a combination of Ga and B implantation with nanosecond laser annealing shows a lower contact resistivity. Under a determined annealing condition, the surface of the SiGe could be transmitted to melted status by nanosecond irradiation of the UV laser, and the Si concentration of this area will be increased and lead to segregation of Ga and Ge towards the melted region.

In conclusion, the doping process is still a challenge for the development of CMOS devices at 5 nm and beyond. Therefore, more conformity, less damage, and a high activation level will be the key points to be investigated in the future.

## 7. HKMG, ALD Technique and Negative Capacitance Materials

High-k dielectric and metal gate material are introduced into CMOS device by intel at the 45 nm technology node in order to improve the device performance. A series of characteristics are required for the successful implementation of high-k dielectrics, such as a high  $\epsilon$ -value, a large band gap and band offsets with Si, low interfacial trap density, thermodynamic stability with Si, etc., [224]. Metal gates should have suitable work function in order to realize the required VT. W. Xiong et al. reported the work function targets for different devices [225]. The work function for planar bulk high-performance NMOS and PMOS should be 4.2 eV and 5.0 eV, respectively. For multi-gate devices, due to the better gate control ability, the work function is about 4.4 eV and 4.85 eV for high-performance NMOS and PMOS, respectively.

Thin SiO<sub>2</sub> is used as interfacial layer and HfO<sub>2</sub> is chosen as a dielectric for industrial production. TiN is used as a PMOS work function metal, and TiAl-based alloys are used

as NMOS work function metals.  $\text{HfO}_2$  is grown by ALD (atomic layer deposition). The interfacial layer is usually a chemical oxide grown by wet cleaning, which can provide a  $-\text{OH}$ -terminated surface. The  $-\text{OH}$  provides an active chemical group for the adsorption of the ALD precursor. This can lead to good linear growth of  $\text{HfO}_2$  without incubation. The traditional growth method for the metal gate is CVD or PVD. However, when the device structure evolves from planar structure to 3D FinFET and GAA architecture, CVD or PVD can no longer realize conformal step coverage. Therefore, ALD gives the best solution due to its excellent filling capability at even nanometer-range thickness. TiN, TiAlC, and TiAl have been successfully grown by ALD, which can meet the  $V_T$  requirement [226–231]. Along with the shrinking of the feature size, the material system of high-k dielectrics and metal gates is nearly unchanged. The relative thickness tends to be decreased [170,232].

The device dimension continues to scale down, but the high-k and the metal gate layers cannot always follow this rule. Thus, the volume-free approach for multi- $V_T$  is necessary. It is known that the effective work function of the metal has dependence on its thickness. It is reported that a range of 150 to 200 mV  $V_T$  adjustment is achievable through thickness modulation in high-k and metal gate stacks [233]. Conformality and thickness control are very critical. Another  $V_T$  tuning method is by electrostatic dipole, which needs relatively less volume and can give more flexibility to the integration. The interaction of the oxide dipole layer with its interfacial layer creates a  $V_T$  shift, resulting in their group electronegativity difference [233,234]. The dipole multi- $V_T$  modulation was conducted by R. Bao et al. with ALD  $\text{La}_2\text{O}_3$ , followed by drive-in annealing before metal gate deposition in the FinFET device [235]. There is a shift of more than 200 mV  $V_{TS}$  from the reference  $V_{TS}$  device by using different  $\text{La}_2\text{O}_3$  thicknesses. This dipole multi- $V_T$  can also be combined with metal multi- $V_T$  to have more flexibility to offer more VTs. S. Hung et al. placed a thin  $\text{LaO}_x$  layer between the high-k dielectric and TiN, and then carried out a thermal drive-in process to form dipole at the interface of high k and the interfacial layer. About 0.8 nm  $\text{LaO}_x$  can provide  $\sim 300$  mV of  $V_T$  adjustment [228]. K.L. Lee et al. noted  $210 \pm 25$  mV as a  $V_{fb}$  improvement at only 0.4–0.5 nm physical and 0.1 nm electrical thickness, employing a new AlN cap on  $\text{HfSiO}$  [236]. This makes the integration more scalable. The AlN cap characteristics are nearly independent of growth method (ALD or plasma-enhanced ALD) if good nucleation of the initial layer is ensured. The technology of the interfacial  $\text{Al}_2\text{O}_3$  doping  $\text{HfO}_2$  laminated stacked layer via controlled ALD cycles was systematically investigated by R. Xu et al. [237]. As the amount of interfacial  $\text{Al}_2\text{O}_3$  doping increases,  $V_{fb}$  gradually increases to saturation. A shift of 270 mV  $V_{fb}$  was realized at 0.525 nm  $\text{Al}_2\text{O}_3$  thickness.

## 8. Advanced Etching for Nano-Transistor Structures

### 8.1. Dry Etching for 3D Transistor

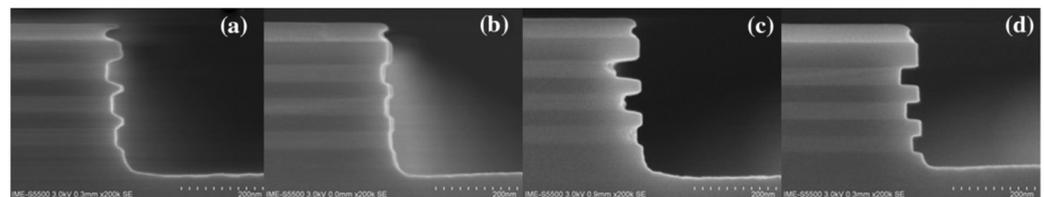
To suppress the SCEs caused by device miniaturization, from the 14 nm technology node to sub-5 nm, the transistor architecture has been experienced from FinFET to form GAA nanowires and nanosheets [238].

FinFET will always be the main structural form of the core device in many nodes below 14 nm. Recently, many special etching technologies have emerged to continue the vitality of FinFET technology [239,240]. For example, a special dry etching scheme is used to obtain ultra-high and steep fin in order to improve the performance of the device [241]. There are also methods used to trim fin by isotropic selective etching [242]. There is also special-shaped fin etching, which uses oxidation to obtain isolation from the substrate to achieve the effect of SOI [243], and scallop to obtain better gate control [244,245]. In addition, facing the etching countermeasures of new channel materials, such as Ge and SiGe and SiGe/Ge FinFET [246,247], hydrogen plasma is introduced as a new way to control morphology and CD (critical dimension) [248].

For core devices below 3 nm, nanowires or nanosheets in the form of GAA (the Si/SiGe superlattice structure) are considered to be the best device form to replace FinFET. GAA preparation technology based on FinFET architecture is considered as the most promising

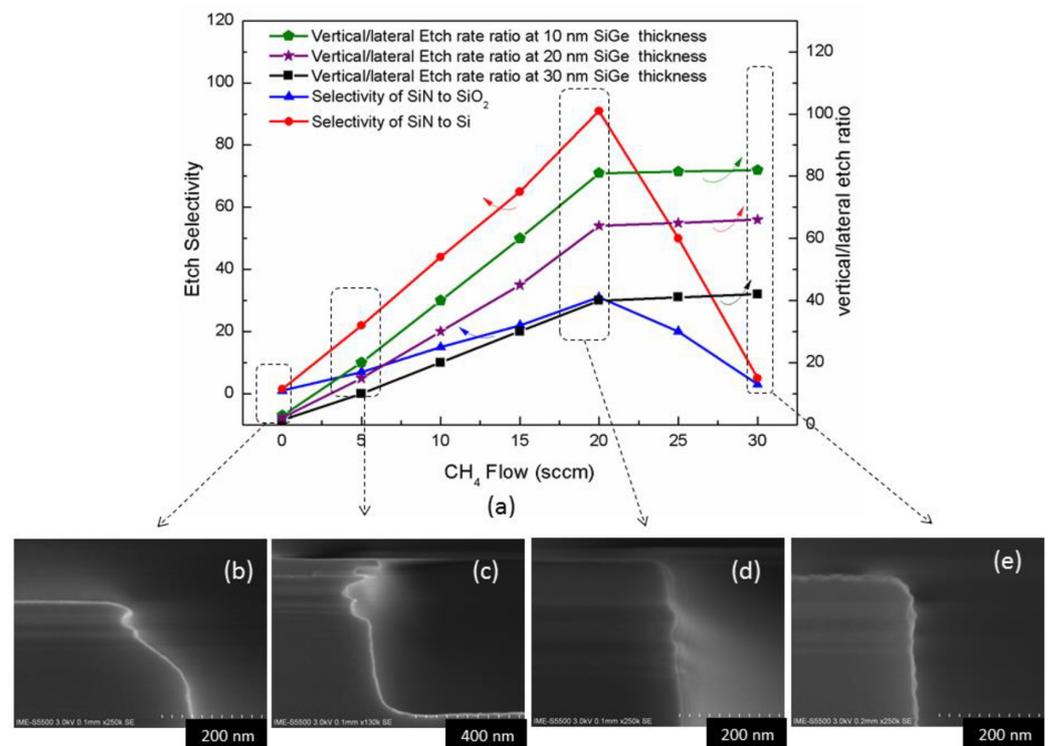
solution [249]. However, channel release and inner spacers are challenging processes not found in conventional FinFET [239].

For channel release, high selectivity and isotropy are the process requirements. Wet etching is not suitable mainly due to the capillary effect, which easily leads to structural collapse [250]. Vapor etching using HCl has also the limitation of crystal orientation selectivity [251]. Therefore, dry etching is a suitable technology for overcoming the above-mentioned limitations. Most of the research reports propose remote plasma etching as a promising etching method [252]. Based on the traditional inductively coupled plasma etching machine, better etching results can also be obtained by using the optimized process as shown in Figure 23a–d [253].



**Figure 23.** SEM cross-section micrographs of SiGe/Si multilayers after isotropic etching with reactant gas  $\text{CF}_4/\text{O}_2/\text{He}$  flow ratios of: (a) 1:0:0, (b) 1:1:0, (c) 4:1:0, and (d) 4:1:5 [253]. Reprinted with permission from ref. [253]. Copyright 2020 Springer Publisher.

The inner spacer is a process module used to balance parasitic capacitance and parasitic resistance in GAA process [254]. Challenges related to its etching include accurate control of cavity etching and anisotropic dielectric materials with high selectivity. A good etching effect can be obtained by selecting the optimized  $\text{CH}_2\text{F}_2/\text{CH}_4/\text{O}_2/\text{Ar}$  system as shown in Figure 24a–d [255].

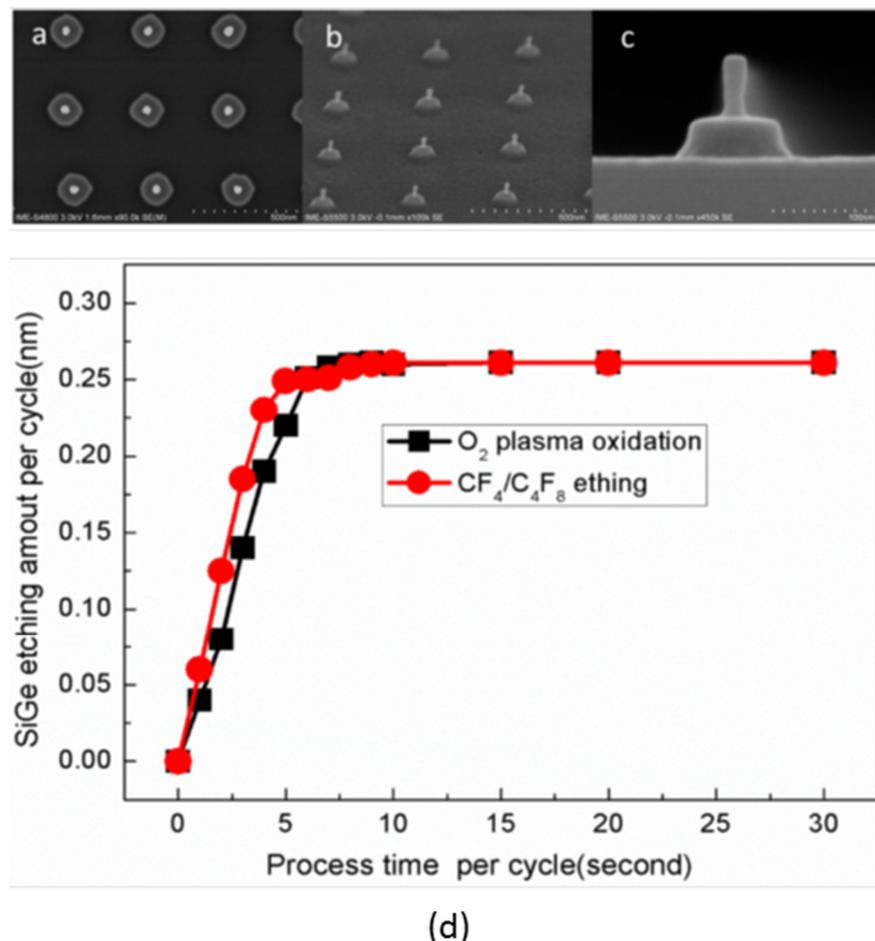


**Figure 24.** Influence on etching profile due to  $\text{CH}_4$  flow: (a) the dependence of vertical/lateral etch ratio and etch selectivity on  $\text{CH}_4$  flow; (b) etching profile with no  $\text{CH}_4$  flow; and with  $\text{CH}_4$  flow of (c) 5 sccm; (d) 20 sccm; (e) and 30 sccm [255]. Reproduced from [255], open access by MDPI, 2020.

### 8.2. Precise Etching: Atomic Layer Etching (ALE)

For horizontally stacked GAA nanowires or nanosheets, the inner spacer needs to accurately control the thickness to control the effective gate length; thus, it is necessary to accurately etch isotropic SiGe and anisotropic dielectric materials [255]. For vertical channel GAA (V-GAA), isotropic etching SiGe, controlling the channel diameter, and anisotropic accurate etching of the metal gate and high-k material are very important. Similar to the atomic layer deposition technology, atomic layer etching technology is a processing technology of great significance to advanced processes [256].

The ALE wet etching of SiGe mainly includes a combination of self-limiting oxidation and oxide layer removal, mainly using a combination of  $\text{H}_2\text{O}_2$  or  $\text{HNO}_3$  oxidation and HF/buffered oxide etching (BOE) [257,258]. Because wet etching has the limitations described in the previous section, the focus is on dry etching. The solution of  $\text{O}_2$  plasma oxidation and  $\text{NF}_3/\text{NH}_3/\text{O}_2$  oxide layer removal achieves the effect of digital high selectivity etching, but because there is no self-limiting feature, the etching accuracy of each cycle is not high [259]. Because the scheme using  $\text{O}_2$  plasma oxidation and  $\text{CF}_4/\text{C}_4\text{F}_8$  oxide layer removal is self-limiting, the etching accuracy reaches about 0.3 nm/cycle, as shown in Figure 25 [260]. Furthermore, the thermal ALE of SiGe has been shown to be dependent on the sequential exposure of oxygen ( $\text{O}_2$ ) or ozone ( $\text{O}_3$ ), hydrogen fluoride (HF), and trimethyl aluminum [ $\text{Al}(\text{CH}_3)_3$ ], with an accuracy of 0.057 nm per cycle [261].



**Figure 25.** SEM micrographs of nanowires with diameter smaller than 20 nm after 100 cycles ALE using  $\text{SiO}_2$  hard mask: (a) bird's-eye top view; (b) 45° tilt top view; (c) cross-section image; (d)  $\text{Si}_{0.72}\text{Ge}_{0.28}$  etching for different process time per cycle [260]. Reproduced from [260], open access by MDPI, 2020.

For ALE etching of SiN-based dielectric materials, the combination of downstream  $\text{CHF}_3/\text{O}_2$  plasma modification and  $>100^\circ\text{C}$  heat treatment can achieve an etching accuracy of 2.8 nm/cycle [262]. For ALE using thermal reactions, the accuracy can reach 0.02 nm/cycle [263]. In addition, atomic layer etching of 0.9 nm/cycle can be achieved by the combination of  $\text{CH}_2\text{F}_2/\text{O}_2/\text{Ar}$  modification and infrared heat treatment [264]. There are many reports about how to obtain selectivity between ALE SiN and silicon oxide [265]. ALE etching of high-K [266] and metal materials [267,268] has gradually become a research hotspot to better support advanced processes such as V-GAA [269–271].

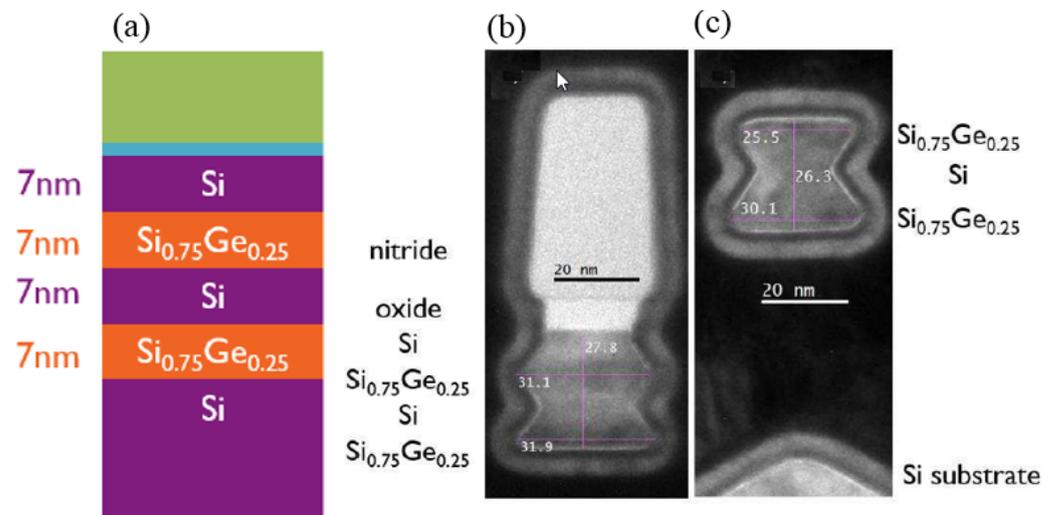
## 9. Wet Etch and Cleaning

Due to their improved mobilities, SiGe, Ge, and III–V materials have mobilities of  $\sim 40,000\text{ cm}^2\cdot\text{V}^{-1}\text{s}^{-1}$  for InGaAs (electron) and  $1900\text{ cm}^2\cdot\text{V}^{-1}\text{s}^{-1}$  for Ge [1] (hole) compared to  $1400\text{ cm}^2\cdot\text{V}^{-1}\text{s}^{-1}$  for electrons and  $450\text{ cm}^2\cdot\text{V}^{-1}\text{s}^{-1}$  for hole of Si [272]. By entering the 10 nm technology node, the pure Si channel has been replaced with the abovementioned materials as listed. The device shape changes from fin-like to lateral GAA (LGAA) and vertical GAA (VGAA) for better channel control for the 5 nm node and beyond. It has been also reported that the nanosheet devices have better power performance than finfet [273]. Meanwhile, the device fabrication of the 5 nm node and beyond considers not only the selective etching of sacrificial materials to the channel ones, but also prevents the collapse of the closely stacked channel material's pattern during the nanowire/nanosheet release processes [273].

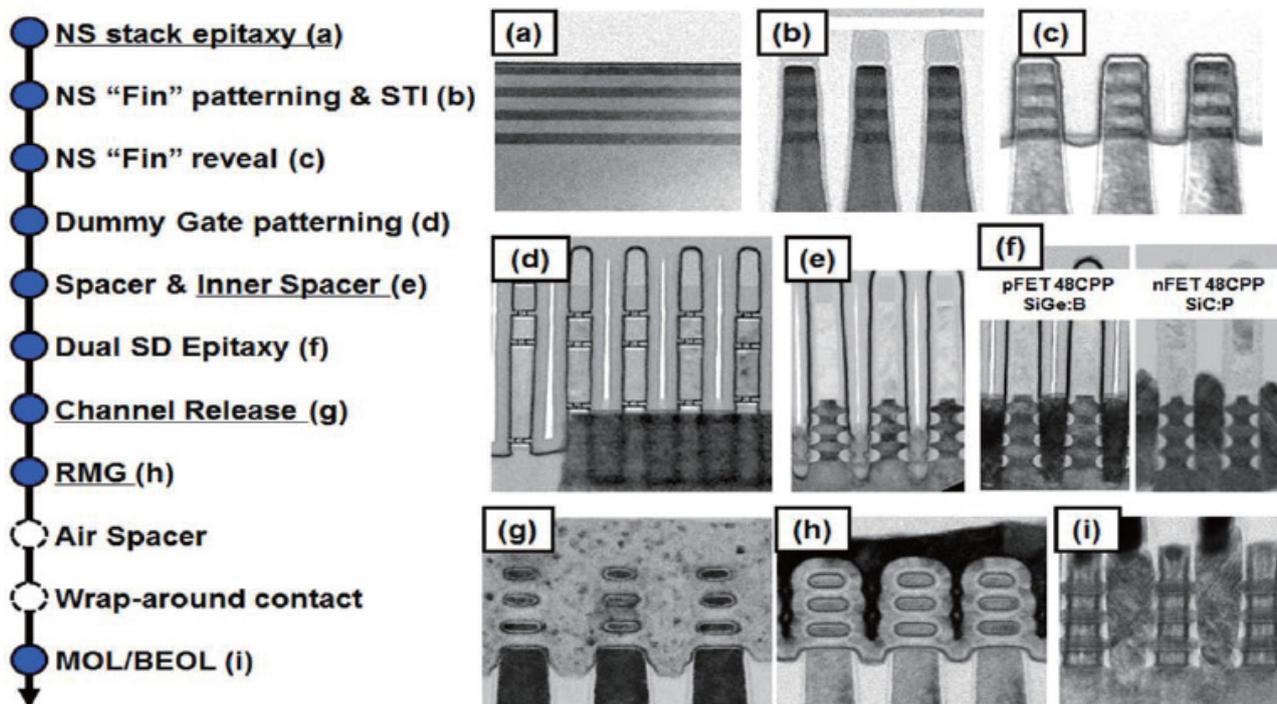
To overcome the high-temperature annealing processes [274], poly crystalline Si is used as the dummy gate and silicon dioxide as the dummy gate oxide material to occupy the space of the real gate and gate oxide. After the high-temperature annealing processes, the dummy gate of poly crystalline Si was etched away by metal alkaline solutions. Since the RMG is used to avoid crystallizations of the high-k dielectric during the rapid thermal annealing (RTA) process for dopant activation, this is successfully prevented in order to increase the leakage current of the gates [274]. On the other hand, RMG prevents the chemical reactions between the metal gate and the high-k in RTA processes [275]; furthermore, it avoids the boron diffusion into high-k [276].

In the 7 nm and 5 nm technology node, the RMG process is still applied to selectively remove the sacrificial Si material from the SiGe channel [277]. Increasing Ge content in SiGe could greatly decrease the alkaline etch rate of SiGe, which enables the selective removal of Si to  $\text{Si}_{0.75}\text{Ge}_{0.25}$  [273–276]. Si etching behavior in the alkaline solution is also well understood [277,278]. It is well known that the etch rate of the Si (111) direction is much slower than Si (001) and (110) crystallographic planes [284]. With a TMAH 5% solution at  $60^\circ\text{C}$ , the material underneath Si of the NW stack can be selectively etched away without losing SiGe, as shown in Figure 26. The 7 nm thick Si layers, which are sandwiched in between the  $\text{Si}_{0.75}\text{Ge}_{0.25}$  NWs, are removed until the (111) limiting planes are formed.

By using a conventional alkaline Si etchant such as TMAH (aq), it becomes difficult to remove the Si sacrificial layer from the SiGe stack during SiGe NW processing. The selectivity of Si and SiGe etching is not high enough [280,281]. ACT<sup>®</sup> SG-201, containing a surface modifier, could improve the relative etch rates of Si (110) and Si (111) orientations, and result in etching selectivity of Si (110)/Si (100) in the range of 1 to 2.5 and Si (111)/Si (100) of about 0.5 or above. The selectivity of Si (111)/SiGe 25% is significantly improved compared to the conventional Si etchants with the help of the Si surface modifier and an effective SiGe corrosion inhibitor in ACT<sup>®</sup> SG-201. Consequently, ACT<sup>®</sup> SG-201 is able to more efficiently to etch the sacrificial Si layer in the SiGe/Si multilayers [287]. The reduced Si etch rate anisotropy in combination with an effective SiGe corrosion inhibitor avoids the loss of the SiGe layer during the nanowire release [287] (Figure 27).



**Figure 26.** (a) Schematic illustration of a multilayer of Si<sub>0.75</sub>Ge<sub>0.25</sub>/Si nanowires applied for selective etching and TEM across image of 30 nm wide Si-Si<sub>0.75</sub>Ge<sub>0.25</sub> nanowires after selective etching of Si (b) in TMAH 5% and (c) without the oxide–nitride hard mask 284. Reprinted with permission from ref. [279]. Copyright 2015, IOP Publisher.

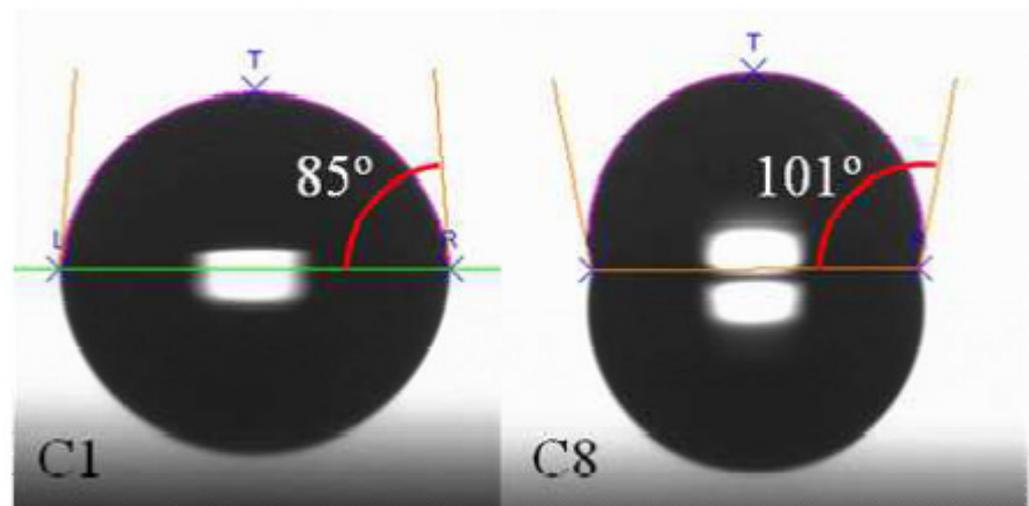


**Figure 27.** Multilayer of nanosheet channel is released by applying HCl vapor [282]. Reprinted with permission from ref. [282]. Copyright 2017, IEEE Publisher.

For devices with the 5 nm technology node and beyond, both dry etching [282] and wet etching [174,283] have been investigated. Using the dry-etching method, the stacked nanosheet channel release was well released using vapor-phase HCl [282]. In the case of wet etching, we use aqueous solutions which have water as the solvent, and, finally, the wafers are rinsed with deionized water (DIW) or ultrapure water (UPW) to remove the residual chemicals from the substrate surface [283–286]. Due to the surface tension of water, different defects may appear. For instance, the high capillary force of water could pull nearby structures to form permanent imperfections during the drying process, which are

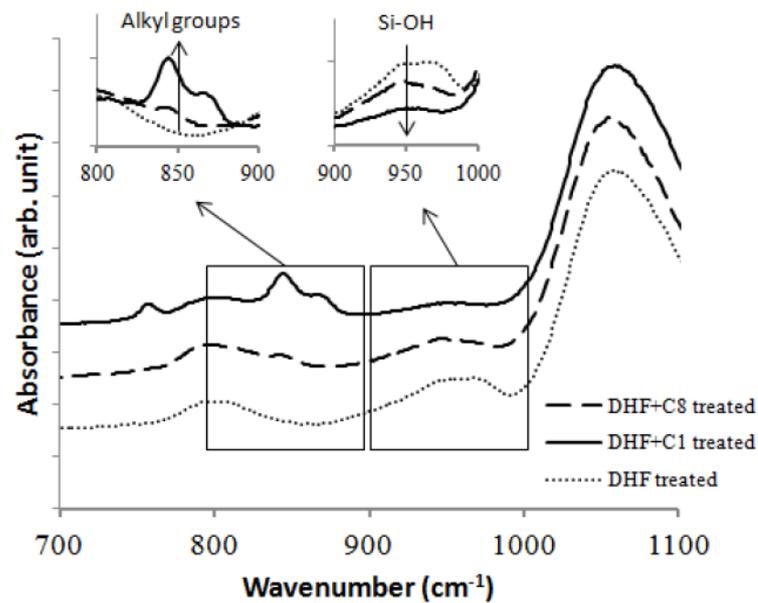
known as pattern collapse 292, or stiction 293 in micro electro-mechanical systems (MEMS). To minimize the surface tension, liquid isopropanol (IPA) was used 295, but this turned out to be ineffective as the pattern spacing decreased and the aspect ratio increased.

The adhesive force (due to the capillary force) which pulls the neighboring high-aspect-ratio (HAR) structures overcomes the elastic force to generate stiction. By introducing lower-surface-tension liquids like isopropyl alcohol (IPA) to replace the water, the capillary forces can be effectively minimized during the drying process. The hydroxyl groups are considered as highly reactive, and are often seen from the silicon oxide surfaces after SC1 or ozonated water treatment in the field of microfabrication. Replacing the hydroxyl groups with inactive molecules like silylation agents, therefore, is a good solution to minimize the stiction 297. For drying HAR structure evaluation, two kinds of straight-chain alkyl group were compared. The straight-chain alkyl group in the agents possesses a carbon number of 1 and 8; therefore, they are noted as C1 and C8, respectively 297. The contact angle of C1 ( $85^\circ$ ) is measured as lower than that of C8 ( $101^\circ$ ), as illustrated in Figure 28. This is important to mention here as it is known that longer straight-chain alkyl groups result in the sample surface showing more hydrophobic behavior 297.

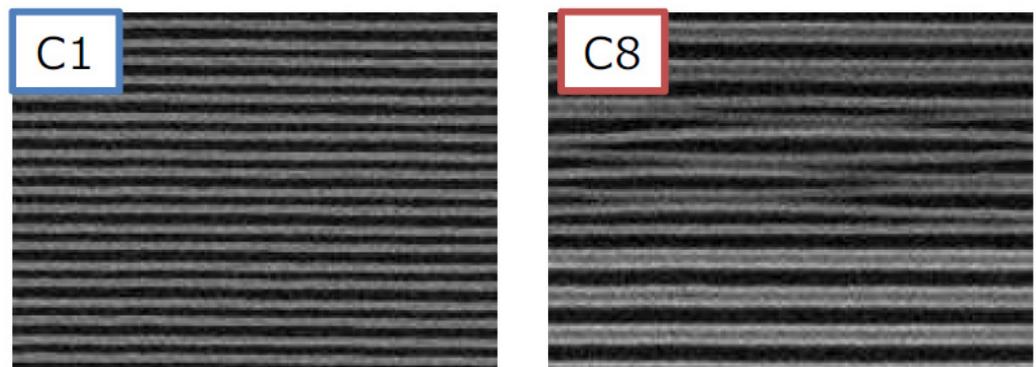


**Figure 28.** Illustration of contact angle test of C1 and C8 (the straight-chain alkyl group in the agents has carbon numbers of 1 and 8, respectively) 297. Reprinted with permission from ref. [287]. Copyright 2017, IOP Publisher.

However, the samples of silicon oxide powder treated with C1 and C8 showed different results. As shown in Figure 29, that C1 treatment sufficiently eliminates the hydroxyl groups by measuring with attenuated total reflection–infrared spectroscopy (ATR-FTIR). In these experiments, the C8 reaction was suppressed by its steric hindrance; as a result, the existing hydroxyl groups could not be efficiently replaced with alkyl groups [287]. The drying process of the HAR structures with an aspect ratio of 13.3 applying C1 and C8 showed that it is not crucial to obtain high water repellency; however, it is significant to obtain lower surface free energy, as illustrated in Figure 30 [42]. The alkyl group surface can be simply removed by oxidative or reductive plasma strip by using N<sub>2</sub>O or N<sub>2</sub>/H<sub>2</sub> reactant gases [288]. Farid et al. reported the formation of STI patterns with 9 nm CD, 25 nm pitch, and 160 nm fin height [288]. Therefore, it is expected that wet etching can be applied for the 5 nm node and beyond, as well as dry etching, to avoid any stiction of the nanostructures.



**Figure 29.** ATR-IR spectrum obtained from  $\text{SiO}_2$  powder after C1 or C8 treatment demonstrates that C1 is better due to higher hydrocarbon groups around  $750$  to  $900\text{ cm}^{-1}$ , whereas lower hydroxyl group is at  $960\text{ cm}^{-1}$  [297]. Reprinted with permission from ref. [287]. Copyright 2017, IOP Publisher.



**Figure 30.** Top view micrographs of wafers after C1 and C8 treatment and drying [297]. Reprinted with permission from ref. [287]. Copyright 2017, IOP Publisher.

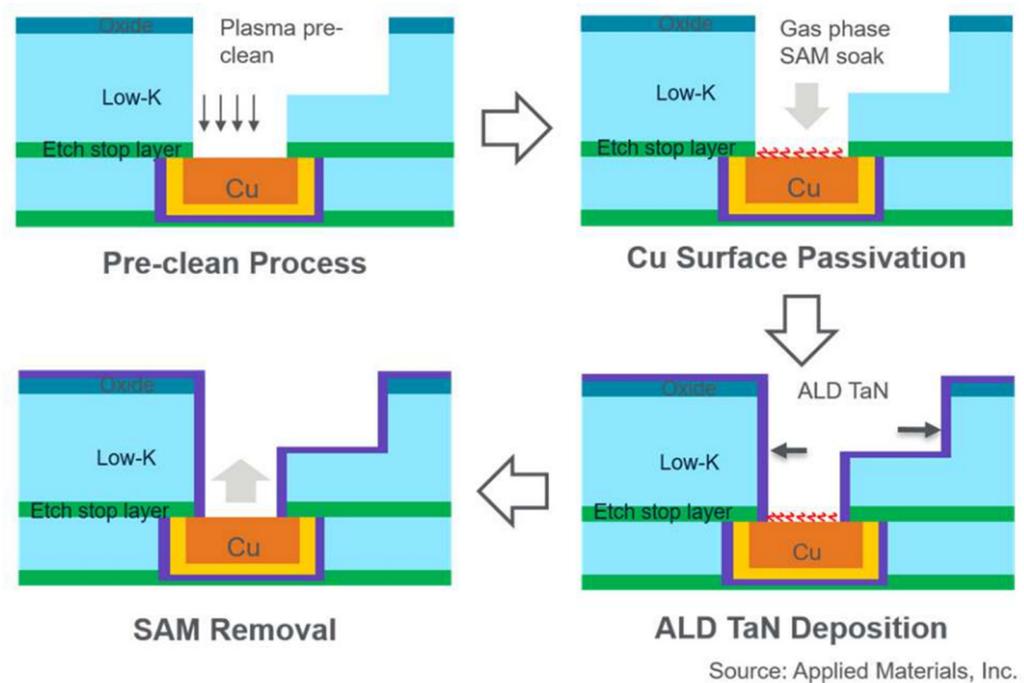
## 10. Metal Materials Interconnect

Copper has been replacing aluminum as a BEOL interconnecting metal material for over 20 years. However, copper interconnection faces many difficulties in balancing line resistance (line R) and reliability for advanced technology nodes [289]. Some strategies have been investigated to improve via and line resistance as well as reliability at small dimensions [290].

The self-forming barrier layer uses the seed layer of copper-based alloy to form a barrier layer through post-metalization annealing. The alloy elements in the experiment include V, Al, and Mn [291–295]. A widely considered promising copper interconnection method is based on the concept of a through-cobalt self-forming barrier (tCoSFB), in which Mn atoms in the doped copper seed layer diffuse through a thin cobalt liner and react with Si, O, and Ta to form a strong diffusion barrier layer at the interface between the liner and the dielectric. The concentration of Mn in the CuMn target material can vary between 0.5% and 10%; the final concentration value depends on a comprehensive evaluation of the line resistance and reliability [296]. Nogami et al. believed PVD/ALD TaN and/or tCoSFB as a viable solution to continue scaling barrier/wetting layers, and the interconnection resistance of metals such as cobalt and ruthenium will be better than that of copper due

to the limitation of the reduced thickness of the barrier layer in the 5 nm technology node [289].

Gas-phase self-assembled monolayers (SAM) only provide highly selective adsorption on metal. Based on the reasons given above, a new integration method using a selective barrier is invented by passivating the metal surface to achieve a reverse selective barrier of ALD TaN, with a reduced barrier at the bottom [297]. Figure 31 demonstrates the selective barrier integration flow in Cu interconnection; the via resistance could be reduced by 50% by using this new ALD TaN process, and the performance reliability (e.g., TDDB and EM) shows that no major difference was observed in the selective barrier scheme [297].

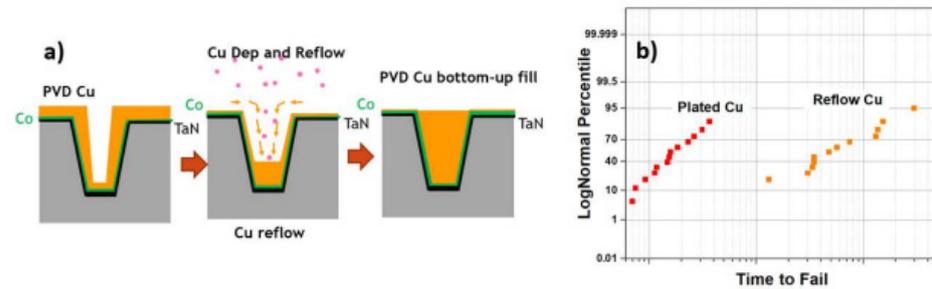


**Figure 31.** Schematic pictures showing the integration flow of selective barrier in Cu interconnection [297]. Reprinted with permission from ref. [297]. Copyright 2021, IEEE Publisher.

Copper-reflow is a potential gap-fill solution as it eliminates the copper seed overhang formation and creates the perfect bottom-up fill to replace electrochemical plating (ECP). Beyond advanced 7 nm technology, Samsung adopted a “Cu reflow” process improving copper fill ability in smallest design features as part of Back End of Line (BEOL) contacts and metal islands, ensuring manufacturability by aggressive chip scaling [298]. Figure 32 shows the flow diagram for the Cu reflow process on Co liner and the corresponding improvement in electromigration (EM). The reflow process has better gap-fill (lower defectivity); therefore, it improves EM lifetime values [299]. Grain boundary diffusion is the main failure mechanism of EM and SM when a good copper line capping layer is used. Due to the use of higher process temperatures, the copper reflow process results in larger grain sizes of the deposited copper film compared to the copper electroplating process, thus exhibiting better SM and EM performance [298].

Another potential solution is to use other metals with good conductivity instead of copper conductors [300]. Daniel Gall evaluated five elemental metals (Co, Cu, Rh, Ru, Ir) with first-principle simulations and transport measurements on epitaxial layers. Rh and Ir are promising because their  $\rho_0 \times \lambda$  is the smallest ( $\rho_0$ : the bulk resistivity,  $\lambda$ : the bulk electron mean free path). However, the probability of grain boundary reflection for Rh and Ir is approximately twice that of copper. Ru is considered a candidate for interconnection metal because of its  $\rho_0 \times \lambda$  value is 24% lower than copper. But more importantly, narrow Ru interconnected lines require a thinner barrier layer compared to copper interconnected lines. [301] Seong Jun Yoon et al. demonstrated that maximizing the

grain sizes in Ru interconnected lines can effectively lower the total line resistivity [302]. The total line resistivity has been successfully reduced by more than 30% by suppressing the grain boundary scattering effect.



**Figure 32.** (a) Schematics showing Cu reflow process. (b) Electromigration lifetime values for plated Cu vs. reflow Cu with Co liner at 32 nm pitch [299]. Reprinted with permission from ref. [299]. Copyright 2021, IEEE Publisher.

Some studies have proposed new integration schemes such as subtractive patterning flows as an alternative to dual damascene (DD) interconnection [299,303]. The subtractive patterning flow uses non-Cu conductors (Ru) that can enable lower R, better reliability, and potentially even provide 1x line R reduction (for line width < 12 nm) [303]. This method firstly forms the via layer in low k, and then fills the via and trench layers with metal deposition. The advantage of this process method is that it does not require metal–chemical mechanical polishing (CMP) and barrier layers. Then, the metal Ru is patterned using EUV single-exposure and subtractive etch to generate lines with CD down to 10.5 nm, which eliminates plasma damage to low-k trenches [304]. This method has good process control, stability, and a very high production line yield. These indicate that the subtractive etch of Ru is a feasible solution for advanced interconnected technology nodes.

An electroplating void-free cobalt interconnection was developed by Lam Research Tighe A. Spurlin [305]. Superconformal bottom-up Co deposition with a high aspect ratio was formed using a  $H^+$  and single suppressor at low current and long plating time. Compared with the copper/porous low-k SiOCH film integration process, the cobalt/porous low-k SiOCH film integration process exhibits less degradation in its electrical characteristics and reliability under thermal and electrical stress. The results indicate that the barrier free process can meet the requirements of Co interconnection, which is a promising solution for advanced interconnected technology nodes [306].

By introducing a via pre-filling process, a more significant change has been made to the conventional gap-filling process flow. This metalization process in the dual damascene structure is called a hybrid metalization. The hybrid metalization scheme of replacing metal pre-filled vias can reduce the aspect ratio of trench/via. This alleviates the poor Cu gap filling related to the scaling of the barrier/wetting layer, thereby increasing the Cu volume fraction in the trenches. A selective deposition process is applied in this scheme. By introducing the pre-filled Co process, seamless and bottom-up filling of metals was achieved in advanced interconnections [307,308]. The report demonstrated [308] a high selectivity CVD Co deposition has been achieved on copper, which can fill vias with a diameter of 45 nm and an aspect ratio of 3:1 in a copper dual damascene structure. IMEC and Lam have also demonstrated the feasibility of using the electroless deposition (ELD) technology to deposit Co as a pre-filled via material [307,309,310]. The main advantage of Co via the pre-filling process is that it can reduce via-layer resistance. As the via CD shrinks, compared to the conventional PVD-ECP via process, the chemical Co via process has a greater relative resistance reduction. For example, the via resistance of CD at about 40 nm is reduced by about 30% [309]. By using a hybrid Cu metalization with Co pre-filled via, the resistance in the 87° tapered vias can be reduced by 42% in the via of a 12 nm half pitch, and the resistance in the chamfered vias can be reduced by up to 52% [311]. The selective CVD

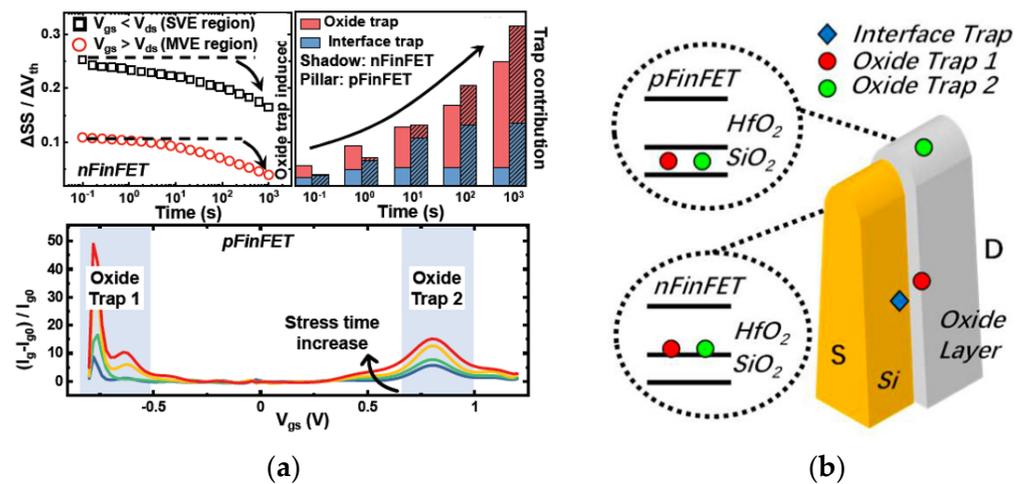
Ru process is also used in the hybrid metalization scheme of Ru, which involves pre-filling Ru and then metalizing copper trenches [312]. The Ru prefill clearly decreased the via resistance for the Cu metalization in the 21 nm metal pitch. When using 1 nm TiN as the barrier layer with Co and Ru fully filled as the reference at this dimension, the resistance of the Ru–Cu hybrid metalization was reduced by 35%. The EM performance of Ru–Cu hybrid metalization is similar to the full copper metalization. A selective tungsten (W) deposition has also been used for via pre-filling [313]. Compared with the Cu dual damascene-filled via layer, the via resistance of W–Cu hybrid metalization is reduced by 40%. Therefore, the selective deposition hybrid metalization of contact and via pre-fill may be applied in the miniaturization process of future advanced interconnected technology nodes.

Intermetallic compounds (such as,  $\text{Cu}_2\text{Mg}$ ,  $\text{AlNi}$ ,  $\text{Al}_3\text{Sc}$ ,  $\text{AlCu}$ , and  $\text{Al}_2\text{Cu}$ ) are proposed as candidate interconnected materials for advanced semiconductor devices [314–317]. The stoichiometric NiAl film with a thickness of 56 nm exhibits a resistivity of  $13.9 \mu\Omega \text{ cm}$  after annealing at  $600^\circ\text{C}$ . Additionally, different capping layers were tested to overcome the formation of metal surface oxides to achieve low resistivity [316]. The resistivity of 24 nm  $\text{Al}_3\text{Sc}$  thin film can reach  $12.5 \mu\Omega \text{ cm}$  after post-deposition annealing at  $500^\circ\text{C}$ . At a thickness of 20 nm and above, the conductivity of  $\text{AlCu}$  and  $\text{Al}_2\text{Cu}$  films is better than that of Ru films, and the resistance of  $\text{AlCu}$  and  $\text{Al}_2\text{Cu}$  films with a thickness of 28 nm is only  $9.5 \mu\Omega \text{ cm}$  [314]. Meanwhile,  $\text{Al}_2\text{Cu}$  exhibits low resistivity, excellent gap-filling performance, and good reliability in TDDB, EM and BTS [315]. Based on the above series of good properties,  $\text{Al}_2\text{Cu}$  may become an alternative to Cu [314].  $\text{Cu}_2\text{Mg}$  intermetallic compound shows a low resistivity of  $25.5 \mu\Omega \text{ cm}$  and good gap filling performance by sputtering reflow. The thickness dependence of the resistivity of  $\text{Cu}_2\text{Mg}$  thin films is better than that of Cu and Co, which is comparable to that of Ru.  $\text{Cu}_2\text{Mg}$  is also considered an excellent interconnection material due to its excellent properties [317].

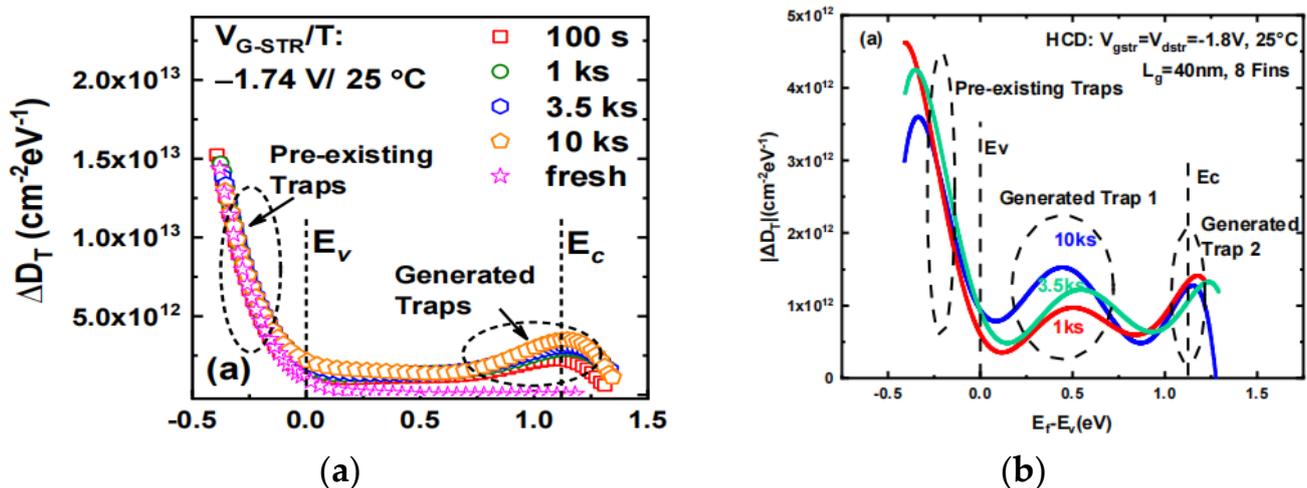
## 11. Advanced Devices Reliability

The reliability issues of advanced CMOS device beyond the 7 nm node are becoming more serious and complicated due to the 3D novel structure and nano-scaling [318–321], such as bias temperature instability (BTI), hot carrier degradation (HCD) and self-heating effect (SHE). Generally, trap-based approaches play very important roles in understanding the physical mechanisms in the study of reliability for advanced CMOS devices [321–323]. As we already know, there are interface traps in substrate/dielectrics and oxide trap in the dielectrics. Taking the 3D FinFET as an example, there are interface traps and two oxide traps (named trap 1 and trap 2) shown in Figure 33a [321]. Moreover, the locations of the interface trap and oxide trap 1 are crowded in the middle of the Fin side, while oxide trap 2 are in the Fin top in Figure 33b [321].

Moreover, to deeply understand oxide traps in terms of the reliability of the advanced CMOS device, the energy distribution of the oxide trap is also widely studied using the discharging-based multi-pulse (DMP) technique [322]. According to the origin of oxide traps, oxide traps can be classified as pre-existing oxide traps and generated traps, which are related to the process and stress, respectively. As shown in Figure 34, pre-existing oxide traps are above the valance band of Si in both (a) negative-bias-temperature instability (NBTI) stress and (b) HCD stress [323,324]. However, two generated traps are located at 0.4 eV above  $E_v$  and near the conduction band ( $E_c$ ) of Si, respectively (Figure 34). Therefore, in HCD degradation of FinFET, both locations and energy distributions of oxide traps show the two kinds of generated oxide traps.

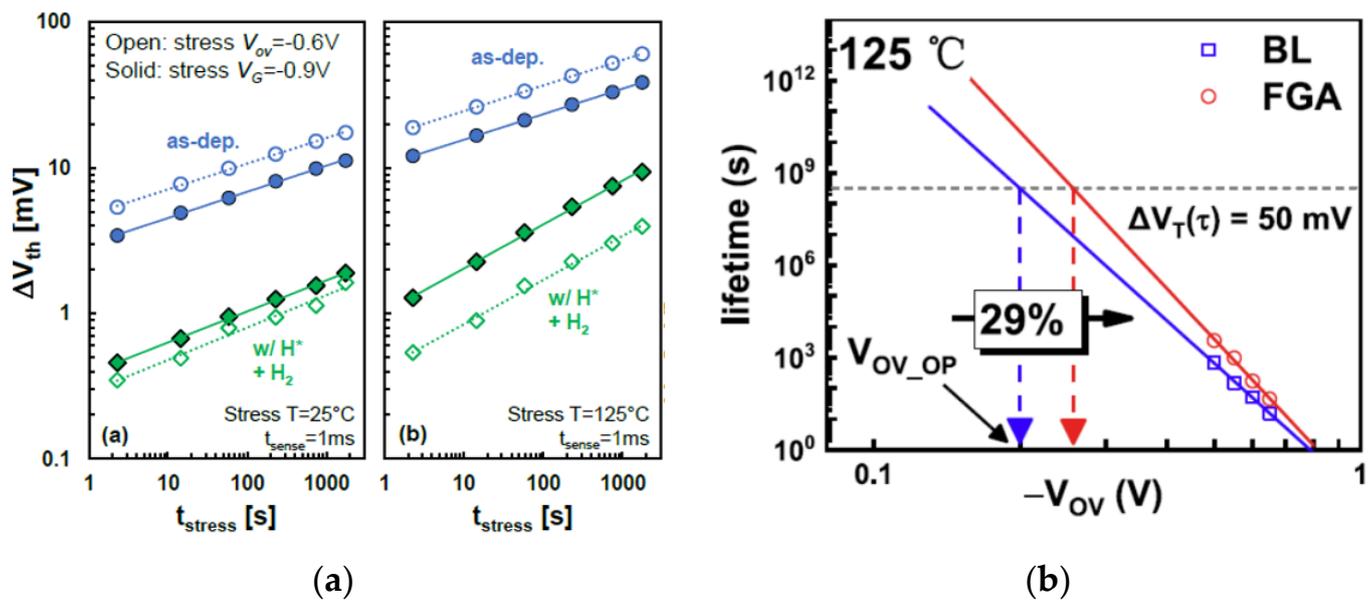


**Figure 33.** (a) Different oxide traps in FinFET illustrated in SILC spectrums, notated as oxide trap1 and oxide trap 2. (b) Typical positions of the interface traps as well as oxide traps created by HCD in a p- and n-type FinFET [321]. Reprinted with permission from ref. [321]. Copyright 2021, IEEE Publisher.



**Figure 34.** (a) Energy distribution of oxide traps in Si FinFETs for different NBTI stress time [323], reprinted with permission from ref. [323]. Copyright 2020, IEEE Publisher. (b) Energy distribution of oxide traps in Si FinFETs for different HCD stress time, and there are two generated oxide traps [324], reprinted with permission from ref. [324]. Copyright 2021, IEEE Publisher.

From the physical understanding of trap locations and trap energy distribution in the advanced CMOS device, the reliability of the HKMG stack process is optimized, especially for the annealing process. As shown in Figure 35a, a low-temperature atomic and molecular hydrogen annealing method is proposed to enhance chemical interfacial layer quality. Furthermore, the NBTI degradation is also clearly decreased by almost one order due to the passivation of the hydroxyl-E' defects [325]. Figure 35b shows that optimized formation gas annealing (FGA) is an effective route to improve the 29% NBTI lifetime by reducing the generated oxide trap [326]. Therefore, in the study of the reliability of the advanced CMOS device, a trap-based approach is proven to be a useful and effective technique to improve reliability by process optimization. At the same time, metal thickness variation in the stacked nanosheet transistor will also affect the threshold voltage ( $V_{th}$ ) due to the changed wave function of metal gate, thus contributing to the significant  $V_{th}$  variability.



**Figure 35.** (a) NBTI-induced  $\Delta V_{th}$  for different stress time measured at the low-T RMG pMOS processed w/o and w/H\* – H<sub>2</sub> IL treatment at 25 °C and 125 °C [325], reprinted with permission from ref. [325]. Copyright 2021, IEEE Publisher. (b) Comparison of extrapolated lifetimes between baseline transistors and FGA-optimized ones [326], reprinted from ref. [326]. Open Access, 2021, IEEE Publisher.

### Part Three: Materials in Beyond Moore Era

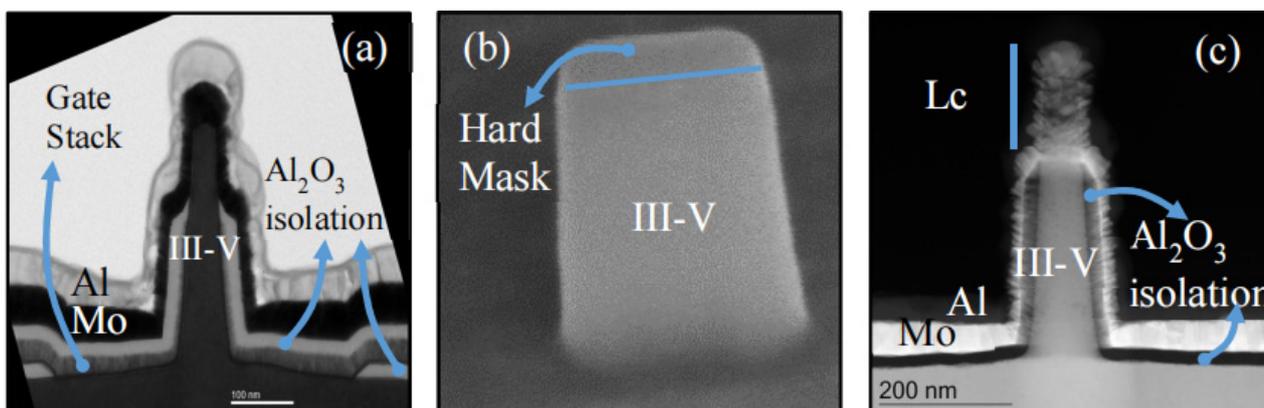
#### 12. III–V Materials

High-mobility III–V materials used as channels for GAAFET have been demonstrated as excellent candidates for high-speed and low-power circuits; these have been proposed for use in sub-10 nm CMOS technology [327,328]. Meanwhile, there is a large challenge to grow high-quality III–V layers on Si substrate for III–V GAAFETs, which stems from the incompatibility of III–V with the Si-based process [329,330]. Early studies on III–V GAAFET were focused only on simulation [331,332]. S. Ramesh et al. [333] presented high-performance devices of In<sub>0.53</sub>Ga<sub>0.47</sub>As vertical nanowire (VNW) and vertical nanosheet (VNS) by using dry etching. Figure 36 illustrates the TEM and SEM micrographs of In<sub>0.53</sub>Ga<sub>0.47</sub>As NS transistors and fabrication. The outcomes showed that scaling the effective oxide thickness together with (NH<sub>4</sub>)<sub>2</sub>S channel treatment and forming gas annealing improved the transistor characteristics, for example, Q (Gm/SS) by over 55%. In these transistors, a minimum SS = 63 mV/dec was obtained at V<sub>DS</sub> = 0.5 V, and I<sub>ON</sub> = 397  $\mu\text{A}/\mu\text{m}$  at I<sub>OFF</sub> = 100 nA/ $\mu\text{m}$ , while the G<sub>m</sub> peak was at 1.6 mS/ $\mu\text{m}$  and maximum Q = 21. These results were the best values obtained so far for vertical III–V transistors.

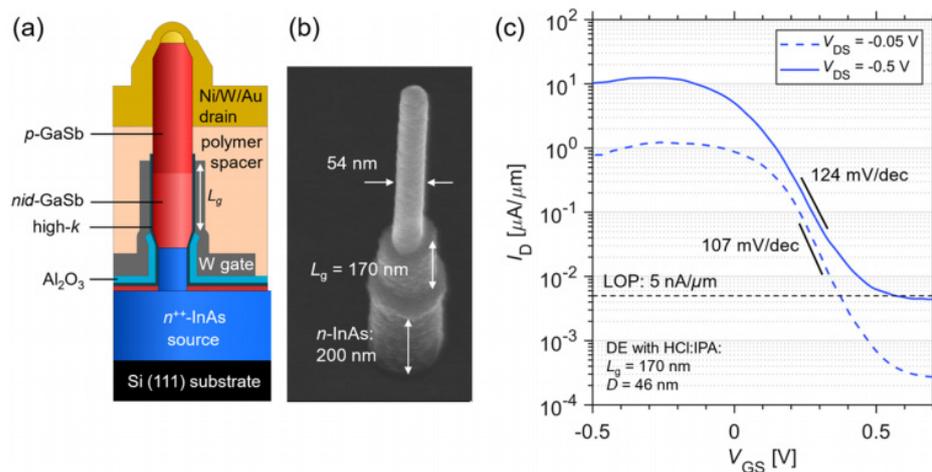
However, a 1D nanowire can exhibit additional advantages for many purposes, e.g., higher stress relaxation, possibility of complicated gate stacking integration, more effective adsorption, and trapping of light [334]. X. Zhao et al. [335] reported In<sub>0.53</sub>Ga<sub>0.47</sub>As VNW MOSFETs of 7 nm in diameter. The transistors were processed by a top-down approach by applying RIE (reactive ion etching), alcohol-based digital etching, and Ni alloyed metal contacts. The research showed a record I<sub>ON</sub> of 350  $\mu\text{A}/\mu\text{m}$  at I<sub>OFF</sub> = 100  $\mu\text{A}/\mu\text{m}$  and V<sub>DD</sub> = 0.5 V. The transistors showed a peak transconductance (g<sub>m, pk</sub>) of 1.7 mS/ $\mu\text{m}$  and minimal SS of 90 mV/dec at V<sub>ds</sub> = 0.5 V, reaching the highest quality factor 19.

Other types of III–V nanowires, e.g., InAs and GaSb, were also reported to be integrated for Si-GAAFETs. Among these studies, for example, Z. Zhu et al. [336] reported a vertical NW p-MOSFET with the GaSb channel by applying digital etch (DE) schemes. Figure 37a shows the schematic of a single NW-GAA MOSFET. In this study, two types of processes which are based on buffer-oxide etcher (BOE), 30:1 and HCl:IPA 1:10, are

demonstrated and compared. Figure 37b shows the SEM image of a single NW transistor after gate length definition. By optimizing the DE conditions for GaSb NW MOSFETs, transistors with DE-HCl:IPA showed a minimum SS of around 107 mV/dec, while the  $I_{ON}/I_{OFF}$  ratio could be increased by over three orders of magnitude (see Figure 36c). At present, high-mobility III-V channel materials instead of conventional Si is an important direction of advanced CMOS technology, and some research progress has been obtained. However, crystal quality optimization for Si-based III-V materials is still very challenging to achieve good device performance.



**Figure 36.** (a) TEM image showing across the width of single nanosheet FET; (b) SEM image of a single vertical nanosheet after dry etch; (c) TEM image of a vertical nanowire resistor after TLM process step [333]. Reprinted with permission from ref. [333]. Copyright 2017, IEEE Publisher.

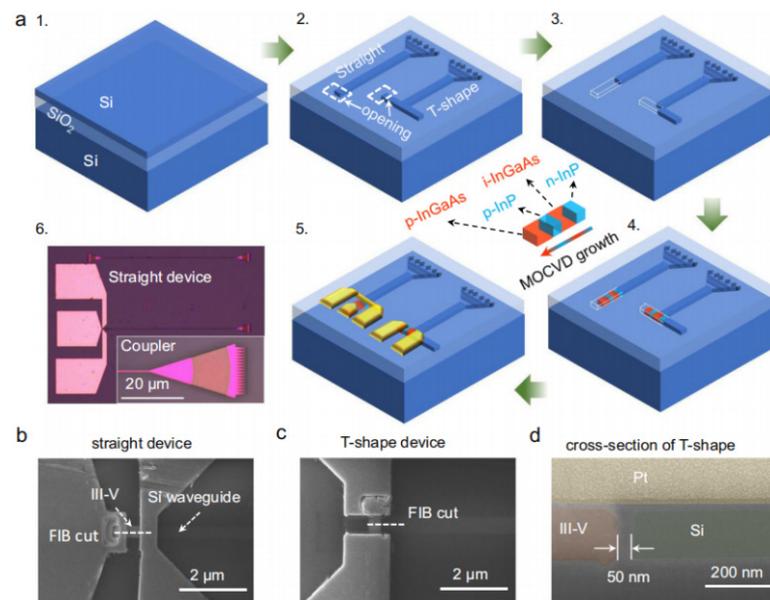


**Figure 37.** (a) Schematic image of a single NW MOSFET with GaSb channel where digital etching was used as the first step of the process; (b) SEM micrograph of a single NW transistor after defining the gate length; (c) transfer characteristics of the NW transistor with two-cycle DE- HCl:IPA 1:10 prior to high- $\kappa$  deposition [336]. Reproduced from [336], open access by ACS, 2022.

Si-based optoelectronic integration chips (OEICs) are a promising development in advanced CMOS technology. However, conventional IV-group materials of Si or Ge are indirect band structure, which result in low emission efficiency. In contrast, most group III-V materials have a direct bandgap, illustrating stronger efficiency of photon absorption and emission, nailing themselves for the optoelectronic devices in OEICs. To achieve a monolithic integration of III-V devices on the Si platform, it is important to develop a heteroepitaxy approach. There are some challenges for high-quality III-V heteroepitaxy on Si such as antiphase boundary (APB) and threading dislocation density (TDD) [329–338].

Y. Du et al. reported comprehensive research about the defect engineering methods for the growth of III–V materials on Si, which provided guidance for the optimization of high-quality III–V heteroepitaxy [329].

Even though high-epitaxy-quality III–V materials can be utilized for GAAFET or optoelectronic applications, the vertical geometry can be complicated in terms of device processing, and further engineering is necessary for on-chip integration as well as for waveguide-coupled solutions [339]. Template-assisted selective epitaxy (TASE) was considered as an effective method to overcome these limitations [340,341]. P. Wen et al. [342] demonstrated scaled and waveguide-coupled III–V photodiodes monolithically integrated on Si by TASE, implemented as InP/In<sub>0.5</sub>Ga<sub>0.5</sub>As/InP p-i-n heterostructures. Figure 38 illustrates the process of device fabrication on a conventional silicon-on-insulator (SOI) substrate using TASE. In Figure 38a, the dielectric layer used as a template is patterned and drilled to expose the Si seed below. TMAH would then be used to etch the exposed Si and form the (111) face, following the epitaxy of III–V materials to fill the cavity. Since the facet is small and along the (111) direction, APBs and TDs generated at the (111) facet would be blocked by dielectric template. As for device fabrication, an n-InP/i-InGaAs/p-InP/p-InGaAs multilayer structure was deposited within the template for metal–organic chemical vapor deposition (MOCVD). Two types of transistor architectures, namely “straight-shape” in Figure 38b and “T-shape” in Figure 38c, were compared. Figure 38d demonstrates the SEM cross-section image of a T-shape transistor which was cut by the focused ion beam (FIB): a small oxide-filled gap separated the Si waveguide from the vertically deposited III–V structure. This study showed a responsivity of 0.2 A/W at –2 V and a dark current of 0.048 A/cm<sup>2</sup> at –1 V.



**Figure 38.** Illustration of process fabrication using template-assisted selective deposition. (a) Schematic of the process flow: 1. Preparation of SOI wafer. 2. Patterning of the Si layer and openings. 3. Etch-back of Si to create hollow SiO<sub>2</sub> template with a Si seed. 4. MOCVD of a p-i-n structure, the small arrow in the picture displays the growth direction. 5. Formed Ni/Au contacts. 6. Optical microscopy micrograph of a straight device and the coupler in the inset. (b) Top-view SEM micrograph of a straight device. (c) Top-view SEM image of a T-shape device displaying the FIB cut line. (d) Cross-section SEM micrograph of a T-shape device displaying an oxide-filled gap (with 50 nm width) separating the III–V-based active material and Si waveguide [342]. Reproduced from [342], open access by Springer Nature, 2022.

### 13. Substrate Engineering (GOI and GeSnOI)

GeSn has attracted attention due to its bandgap tunable and high-mobility properties [343–345]. Compared with Si and Ge, GeSn has a wide window of absorption coefficient in the short-wave infrared, and high carrier mobility. Compared with bulk GeSn/Ge materials, the GeSnOI substrate has higher mobility due to the removal of its high defect density Ge layer, as well as the following properties: higher operating temperature, greater optical confinement, higher light emission efficiency, higher net gain, resonator effect, low leakage current, lower coupling loss with waveguide, and greater suitability for integration of photonic devices with CMOS devices. It is a promising Si-based optoelectronic platform for optoelectronic devices and high-speed electronic devices materials. Therefore, we conclude this section by summarizing the growth of GeSnOI substrates, GeSnOI transistors, optoelectronic devices, and device simulation.

#### 13.1. Growth of GeSnOI Substrates

Using patterned substrate and epitaxial overgrowth, Masashi Kurosawa et al. fabricated a GeSnOI substrate with 2% Sn. Square grooves of  $10 \times 10 \mu\text{m}^2$  were formed by wet etching of  $\text{SiO}_2$  to make a seed layer window, and then Ge (50 nm), Sn (10 nm) and Ge (50 nm) thin films were sequentially deposited by vacuum evaporation system, followed by 800 nm  $\text{SiO}_2$ . After rapid thermal annealing at 1000 °C for 1 s, Ge/Sn diffused and mixed to form GeSn material [346]. In 2019, Youki Wada et al. used a rapid fusion growth method, called “nucleation-controlled liquid phase crystallization” (NCLPC), to grow a GeSn layer on a quartz substrate by MBE, etch out GeSn lines by photolithography, and then cover with  $\text{SiO}_2$ . Finally, slow cooling annealing is performed at a temperature higher than the melting temperature of GeSn. The resulting NCLPC-GeSn lines are almost intrinsic, and the charge carriers not only depend on the Sn concentration but also increase with the cooling rate in NCLPC [347].

In 2016, Dian Lei et al. reported that using MBE to fabricate GeSnOI substrates with Sn concentration of 4.0% and GeSn layer has  $-0.1\%$  compressive strain. A 100 nm thick  $\text{Ge}_{1-x}\text{Sn}_x$  layer was deposited on a Si at 180 °C. Later, a 500 nm-thick silicon dioxide layer was deposited on the  $\text{Ge}_{1-x}\text{Sn}_x$  layer by using PECVD. The wafers were bonded by applying the direct wafer bonding (DWB) technique. The bonded wafers are then post-bond annealed in the  $\text{N}_2$  environment. Si epitaxial wafers are etched in TMAH solution [348].

In 2017, the fabrication method was improved. GeSnOI substrates were fabricated by epitaxial Ge on Si wafers, followed by CVD growth of  $\text{Ge}_{0.92}\text{Sn}_{0.08}$  direct bonding and layer transfer methods. Among them, the Sn concentration measured by XRD (004) is 8.0%, and the  $\text{Ge}_{0.92}\text{Sn}_{0.08}$  has  $-0.9\%$  compressive strain [349–352].

In 2018, Krista R Khiangteet et al. used MBE to grow  $\text{Gd}_2\text{O}_3$  as an insulating layer on a 12-inch Si<111> substrate, increasing to 8% GeSn on  $\text{Gd}_2\text{O}_3$  at 180 °C, and the compressive strain was  $-0.9\%$  GeSnOI. The surface RMS roughness of Si<111> was 3.5 nm, almost twice that of the GeSnOI<001> substrate ( $\sim 1.9$  nm) fabricated by DWB [353].

In 2018, Tatsuro Maeda et al. fabricated GeSnOI substrates on the Ge<001> surface by direct bonding with a concentration of 6.95% and  $-1.0\%$  compressive strain, respectively, with a thickness as low as 10 nm.

X. Wang et al. demonstrated how to form  $\alpha$ -GeSn layer and finally formed a GeSnOI substrate by using PVD evaporation to deposit Ge and Sn on a Si wafer with 5 nm natural oxide through rapid thermal annealing [354].

In 2020, A. Elbaz et al. fabricated a microdisk cavity made of  $\text{Ge}_{0.946}\text{Sn}_{0.054}$  alloy. The epitaxial GeSn layer of the Ge substrate is bonded on the Al substrate with a layer of  $\text{SiN}_x$  with compressive stress. A tensile strain of 1.4% was introduced in GeSn using all round  $\text{SiN}_x$  [355]. In 2021, D. Burt fabricated a GeSnOI substrate with 6% Sn content by using LPCVD epitaxy and direct bonding. The  $\text{Al}_2\text{O}_3/\text{GeSn}/\text{Ge}/\text{Si}$  epitaxial wafer is bonded to the  $\text{Al}_2\text{O}_3/\text{SiO}_2/\text{Si}$  oxide wafer by direct bonding. The Si layer and the CMP Ge layer are etched with a KOH solution with a concentration of 30% and a temperature of 80 °C, and the GeSn disc is formed by etching to expose the  $\text{Al}_2\text{O}_3$  layer. The above KOH solution

is used to etch the Al<sub>2</sub>O<sub>3</sub> layer again to obtain suspended structures and strain-relaxed GeSnOI substrate [356].

In 2022, Z. Kong et al. used an RPCVD epitaxial-grown Ge buffer layer and GeSn layer on the Si<100> substrate, and ALD Al<sub>2</sub>O<sub>3</sub> for fusion bonding with the oxidized Si substrate. Finally, the GeSnOI substrate with relatively less defect density was obtained by wet etching [357]. Table 4 summarizes some parameters of published GeSnOI substrates, Sn concentration, growth method of GeSn layer, bonding type, stress generated, and the crystal orientation of the wafer.

**Table 4.** Summary of parameters of GeSnOI substrate, Sn concentration, growth method of GeSn layer, bonding type, stress generated, and crystal orientation of wafer.

Year	Sn Composition	GeSn Growth	Bonding Type	Strain	Direction of Wafer	Ref.
2012	0–3%	vacuum evaporation system	Seed epitaxy	3%	<100>	[346]
2017	8%	CVD	DWB	−0.9%		[349]
2018	8%	MBE	Epitaxy	−0.9%	<111>	[353]
2020	5.4%			1.4%		[355]
2022	7%	RP-CVD	fusion bonding	−0.32–0.47%	<100>	[357]

### 13.2. GeSnOI Transistor

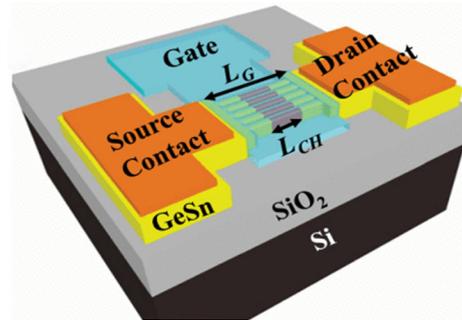
In 2017, D. Lei et al. processed FinFETs on Ge<sub>0.96</sub>Sn<sub>0.04</sub> with channel length and fin width of 50 nm and 20 nm, respectively. The measured SS values were smaller than 90 mV/decade. Meanwhile, the long channel transistors demonstrated a lowest SS of 79 mV/decade with a  $G_{m,int}/S_{sat}$  of ~8.6. The results showed the morphology and thermal stability of the Ge<sub>0.96</sub>Sn<sub>0.04</sub> fins on the GeSnOI substrate are remarkably different than blanket GeSn layers, while these Ge<sub>0.96</sub>Sn<sub>0.04</sub> layers had better thermal stability [260–349,358–367].

In 2018, the National University of Singapore’s team studied the strain relaxation when a biaxially strained Ge<sub>1-x</sub>Sn<sub>x</sub> layer processed to a Ge<sub>1-x</sub>Sn<sub>x</sub> fins. In the beginning, the strain in the biaxially strain of compressively Ge<sub>0.92</sub>Sn<sub>0.08</sub> layer is measured to be ~1%, and Raman spectroscopy measurements showed that strain relaxation is being increased with decreasing  $W_{Fin}$ . The strain relaxation occurs only in the lateral direction, and a full relaxation can be obtained when the fin width is smaller than 30 nm [352].

In 2018, D. Lei et al. reported a study about the effect of post-metal annealing (PMA) on the electrical performance of p-channel GeSn FinFETs (Figure 39). The transistors showed a high mobility of 295 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> at a reverse carrier density  $N_{inv}$  of  $8 \times 10^{12}$  cm<sup>-2</sup> V<sup>-1</sup>s<sup>-1</sup> after 400 °C PMA. Further investigations showed the SS improved from 153 mV/decade to 139 mV/decade for transistors with gate length of 4 μm and gate width of 40 nm after PMA treatment. The  $D_{it}$  value decreased from  $1.19 \times 10^{13}$  cm<sup>-2</sup>eV<sup>-1</sup> to  $5.8 \times 10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup> after 400 °C PMA [368].

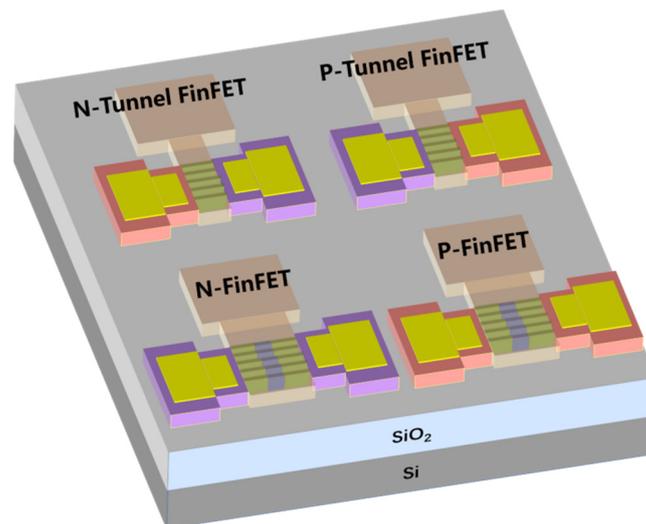
D. Lei et al. p-FinFETs fabricated by optimized etching. When  $V_{DS}$  of −0.05 V, SS is 83 mV/decade, and the  $I_{ON}/I_{OFF}$  ratio exceeds four orders of magnitude. At a gate bias (VG) of −1 V, the gate leakage current ( $I_C$ ) is maintained at  $\sim 2 \times 10^{-4}$  μA/μm. When  $V_{DS}$  is −0.05 V, the GeSn p-FinFET device has a minimum S value of 79 mV/decade when  $W_{Fin}$  is 30 nm and  $L_{CH}$  is 200 nm [354].

Later, D. Lei et al. reported p-FinFET on Ge<sub>0.95</sub>Sn<sub>0.05</sub>OI with a fin width of sub-10 nm, while the top widths were as small as 5 nm. The transistors with a channel length of 50 nm showed a minimum SS value of 63 mV/decade and a maximum  $G_{m,int}$  900 μS/μm ( $V_{DS}$  of −0.5 V) [369].



**Figure 39.** Three-dimensional schematic picture of a FinFET designed on GeSnOI wafer with multiple parallel fins [354]. Reproduced from [354], open access by OSA, 2018.

K. Han et al. demonstrated both GeSn n- and p-channel FinFETs and TFFETs on the same substrate for the first-time integration (Figure 40). GeSn p- and n-FinFETs with fin width of 20 nm showed SS values of 110 and 120 mV/decade, respectively. Meanwhile, by applying a bias voltage of 1.5 V, SS was as low as 20 mV/decade for both n- and p-TFETs [370].



**Figure 40.** Three-dimensional schematic design of the integrated FETs on GeSnOI substrate [370].

Yuye Kang et al. reported a GeSn GAA p-FET formed on GeSnOI substrate. The transistors in this study had a channel length of 60 nm and a gate width of 15 nm where a good SS value of 74 mV/decade was obtained [371]. Later, Shengqiang Xu et al. reported the fabrication of a GeSn p-FinFET with a channel length and fin width of 80 nm and 40 nm, respectively. This study demonstrated a SS value of 114 mV/decade while  $I_{ON}/I_{OFF}$  ratio was increased about 4 orders of magnitude in the linear region [372].

In 2021, Yuye Kang et al. showed  $Ge_{0.95}Sn_{0.05}$  p-GAAFET with an NW width of sub-3 nm and  $L_{CH}$  of 60 nm on  $Ge_{0.95}Sn_{0.05}$ OI substrate. The transistors demonstrated a SS value of 66 mV/decade, an  $I_{ON}/I_{OFF}$  ratio of  $\sim 1.2 \times 10^6$ , while the effective hole mobility ( $\mu_{eff}$ ) was  $\sim 115 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  [373].

In 2021, Guangyang Lin et al. optimized the anisotropic etching of  $Ge_{0.875}Sn_{0.125}$  by inductively coupled plasma (ICP), and obtained a sidewall angle of  $89^\circ$  using  $Cl_2$  100sccm,  $Ar_2$  5sccm,  $O_2$  10sccm, and P10mTorr. An SS value of 240 mV/dec for a fabricated 45 nm thickness  $Ge_{0.875}Sn_{0.125}$ OI back-gate transistor [374]. Table 5 summarizes the transistors fabricated with GeSnOI, such as substrate, transistor type, gate length, gate width, sub-threshold slope, and  $I_{ON}/I_{OFF}$  ratio.

**Table 5.** The transistors fabricated with GeSnOI such as substrate, transistor type, gate length, gate width, subthreshold slope, and switching ratio.

Year	Transistor Type	Gate Length/nm	Fin Width/nm	Subthreshold Slope/mV/Decade	$I_{ON}/I_{OFF}$ Ratio	Ref.
2017	p-FinFET	50	20	<90	$>10^4$	[350]
2018	p-FinFET	4 $\mu\text{m}$	40	139	$>10^4$	[368]
2018	p-FinFET	200	30	79		[354]
2018	p-FinFET	50	5	63	$10^4$	[369]
2018	p-FinFET	100	15	93	$>10^4$	[354]
2019	p-GAAFET	60	15	74	$10^4$	[371]
2019	p-FinFET	80	40	114		[372]
2021	p-GAAFET	60	3	66	$1.2 \times 10^6$	[373]

Two references for GeSn lasers [375,376]: In 2021, Hyo-Jun Joo et al. fabricated a 1D photonic crystal (PC) nanobeam laser. The strain-free nanobeam laser demonstrated threshold density at  $18.2 \text{ kW cm}^{-2}$  for 4 K, which is remarkably lower compared to unreleased nanobeam one showing  $38.4 \text{ kW cm}^{-2}$  at 4 K [375].

A. Bjelajac et al. developed a  $\text{Ge}_{0.831}\text{Sn}_{0.169}\text{OI}$  at a compressive strain of  $-0.5\%$  by bonding a thick layer of GeSn with partial strain relaxation. A room-temperature optically pumped operation GeSn laser was created in a microdisk resonator fabricated on the platform [376].

In 2017, Jadavpur University team used SILVACOATLAS to conduct a detailed study of numerous transistor parameters for simulation and logic circuit applications of strained GeSnOI MOSFETs with different Sn contents. Compared with the equivalent Ge transistors formed on GeOI (10 nm thick channel and 20 nm long), the  $\text{Ge}_{0.94}\text{Sn}_{0.06}$  MOSFET showed an improvement of the peak transconductance  $g_m$ , and peak gain  $A_v$  of 80.5%, and 18.8%, respectively, as well as an improvement of peak cut-off frequency ( $f_T$ ) and maximum frequency of oscillations ( $f_{max}$ ) 83.5% and 81.7%, respectively. In addition, such transistors showed 78.8% improvement in  $I_{ON}$  and a 44.5% decrease in delay in comparison with Ge transistors [351].

In 2019, Jayanti Paul et al. of the University of Calcutta used TCAD to simulate a subthreshold model of a GeSn-on-insulator (GeSnOI) MOSFET based on a two-dimensional surface potential, which takes interfacial trapping and fixed oxide charge density as well as quantum effects into account. A 2D analytical model based on quantum effects was introduced to calculate different transistor parameters of GeSnOI pMOSFETs which relates to SCEs with channel lengths of 14 nm, channel thicknesses in range of 5–10 nm, while interface trapped charge densities within  $10^{12}$  to  $10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$  and Sn composition in the interval of 0–6%. The GeSnOI MOSFET with 5 nm channel thickness demonstrated the lowest  $V_{th}$ , DIBL, SS and  $V_{th}$  offset values. Furthermore, DIBL and SS increased slightly with Sn concentrations in the range of 0–6% [377].

#### 14. Beyond Moore Era-Si Optoelectronics

With the rapid technological development in the information age, more and more demands for information transmission capability, computing capacity, and processing speed in the integrated circuit industry are required. However, there are various signs that “Moore’s Law” once followed by Si-based chips is declining. The development of Si-based integrated circuits has encountered many bottlenecks.

The field of optoelectronics has developed rapidly in recent years and has become one of the key technologies in next-generation data interconnection and communication systems [378]. People have been expecting to combine photonics and electronics processing to realize the Optoelectronic Integrated Circuit (OEIC). The OEIC can provide monolithic solutions with lower cost, higher performance, and higher integration density [379]. The widespread application of Si-based OEIC lies in the need to use CMOS-compatible fabri-

cation processes to enable low-cost mass production, which is a key factor in introducing optoelectronics into a range of technical fields [380].

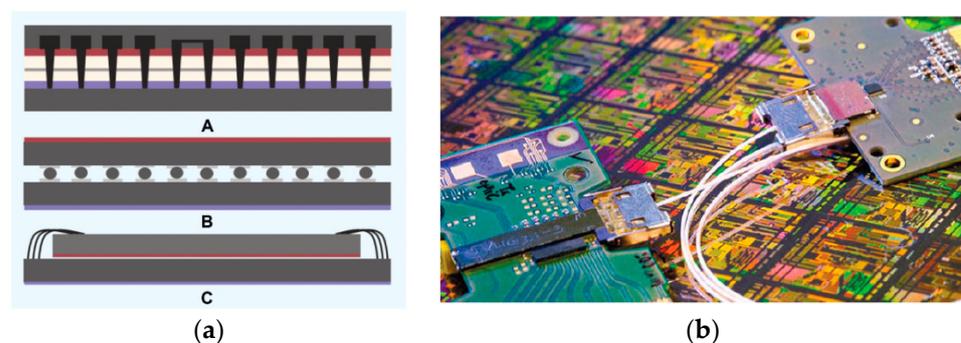
The minimum optical loss window of silica fiber is in the wavelength range of 1300–1550 nm, and most long-distance data transmission also works in this window. Therefore, many photonic devices, e.g., lasers, detectors, and modulators, operating within this wavelength range can be directly integrated to external servers without wavelength conversion [381–383].

#### *Optoelectronic Integration*

The integration of electronics with photonics provides more complicated optical systems and improves the performance of photonic ICs. There are two main types of integration: monolithic and multi-chip.

Monolithic integration can be realized by adjusting the CMOS processes to high-speed optics, or by placing the building optical circuits (for example by wafer bonding) within the steps of today's CMOS flow. The latter method is more conducive to reducing costs, but it still faces some limitations for the development of high-speed devices.

Multi-chip integration is based on two chips to be separately fabricated and later bonded together. Compared to the high cost of developing a monolithic integration process, this approach also has significant advantages to some extent. Compared to expensive electronic processes that require smaller critical dimensions, cheaper processes can be used to fabricate photonic devices, which significantly reduces manufacturing costs in total. A major challenge with the multi-chip integration method is necessary to obtain the high-speed connections between the processed chips. The electrical contact is carried out by bonding techniques for multi-chip integration, e.g., wire bonding, and flip-chip bump bonding, which decreases parasitic capacitance and higher density, can be obtained compared to wire bonding, using Si vias (provides even higher density and lower parasitics) (see Figure 41) [384–386].



**Figure 41.** (a) A scheme for electronic and photonic integration: (A) through Si vias, (B) bump bonding, (C) wire bonding [385]. Reproduced from [385], open access by Walter de Gruyter, 2014. (b) Intel's integrated link contains fully integrated Si photonic transmitter chip with hybrid Si lasers (left side) and a fully integrated receiver chip based on Ge photodetectors (right side) [386]. Reprinted with permission from ref. [386]. Copyright 2010, Springer Nature Publisher.

### **Part Four: Metrology technologies**

#### **15. Advanced Material and Structural Analysis of Miniaturized CMOS**

The scaling technology is approaching its physical limits where cost and reliability issues far outweigh the benefits. The requirements for the development of metrology are increasingly crucial in the semiconductor industry. Metrology enables control of the manufacturing process, helps production, reduce costs, and regulates the time-to-market for new products.

Over the past several years, complex 3D device structures, like FinFET and GAAFET, have been developed in CMOS technologies and beyond. New materials, patterning tech-

niques and processes are also introduced to the fabrication of new generation devices. These all have been raising considerable challenges for all areas of metrology. For example, the challenges in measurement of the FinFET structure are amplified by shrinking dimensions [1,3]. There are difficulties in the analysis of Van der Waal bonded 2D materials such as graphene and other graphene-like materials [2,3]. The patterning techniques contain nanoimprint, extreme ultra-violet (EUV) lithography, and multi-patterning. These techniques will bring new challenges or difficulties for measuring critical dimensions (CD), defectivity and overlay [387–389].

In this section, we will discuss the recent progresses in metrology techniques.

#### 15.1. Scanning Electron Microscopy (SEM)

SEM has been providing at-line or in-line imaging for analysis of in top or cross-sectional view of samples, particles, detecting defects and CD measurements. At this stage, more improvements are now demanded for effectively estimate CD and defect review at and beyond 10 nm node technology [390]. Ultra-low/high energy electron beams have been applied in SEM technique to overcome image degradation. By reducing the spherical aberration, the resolution of SEM can be improved. However, a few focus steps might be needed because the reduction in spherical aberration results in a small depth of field. SEM has also been used to construct the 3D structure features by using the multiple SEM beams [391,392] and detecting the backscattered electrons from multiple primary beam energies. This method is much faster than that of TEM techniques.

#### 15.2. Transmission/Scanning Transmission Electron Microscopy (TEM/STEM) Technology

The aberration corrected lens technology is now commercially available, which can significantly improve the TEM/STEM technique's resolution. Aberration-corrected STEM systems have been reported to image single layer graphene with defects in the stacking configuration of multilayer graphene [393,394].

#### 15.3. X-ray Metrology

Mainstream X-ray metrology, such as HR-XRD [395–398], X-ray fluorescence (XRF), total reflection X-ray fluorescence (TXRF), XRR, X-ray photoelectron spectroscopy (XPS), and small-angle X-ray scattering (SAXS), has been used to determine thin film's parameters, like thickness, composition, strain/relaxation state, tilt, and lattice constant.

It should be noted that SAXS is a technique routinely applied to study structural features with sizes of 1–100 nm. The technique can be used to measure any complex periodic nanostructures such as FinFETs in any dimension. Two types of SAXS techniques have been developed: transmission-based SAXS (or CD-SAXS) and grazing incidence SAXS (GISAXS).

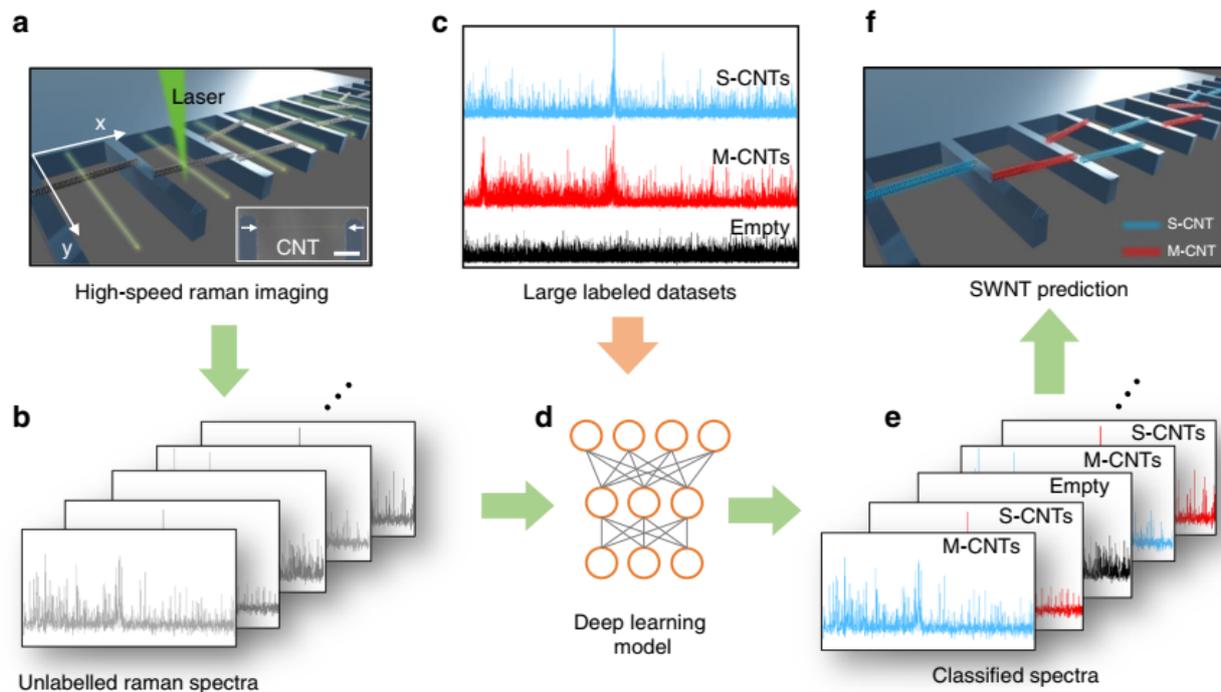
CD-SAXS can analyze the features of sub-5 nm devices, e.g., 3D FinFETs. Since CD-SAXS is a transmission measurement through the substrate, then a high brightness light source is needed to obtain a decent throughput with a small spot size. Meanwhile, to use such strong light sources make this technique impractical in both laboratory and factory environments. Therefore, the improvement of sources in SAXS is of great challenge to realize the measurements of sub-5 nm devices.

While GISAXS has a larger spot size in comparison with CD-SAXS. The measurement time is remarkably shorter than CD-SAXS. This technique is generally applied to estimate the average size of nanoparticles or diameter of nanowires, pitch, height of Si gratings, and sidewall angle [395].

#### 15.4. Raman Spectroscopy

Raman spectroscopy can measure stress. Recent research on SiGe devices demonstrated that in-line Raman spectroscopy is a fast and accurate measurement of composition and strain state [12].

Moreover, by combining with the machine learning technique, the scanning rates were significantly increased. This in turn reduces the laser exposure time, which helps minimizing the laser-induced sample damage. This metrology has been demonstrated by measuring the features of suspended CNTs [399], as shown in Figure 42.



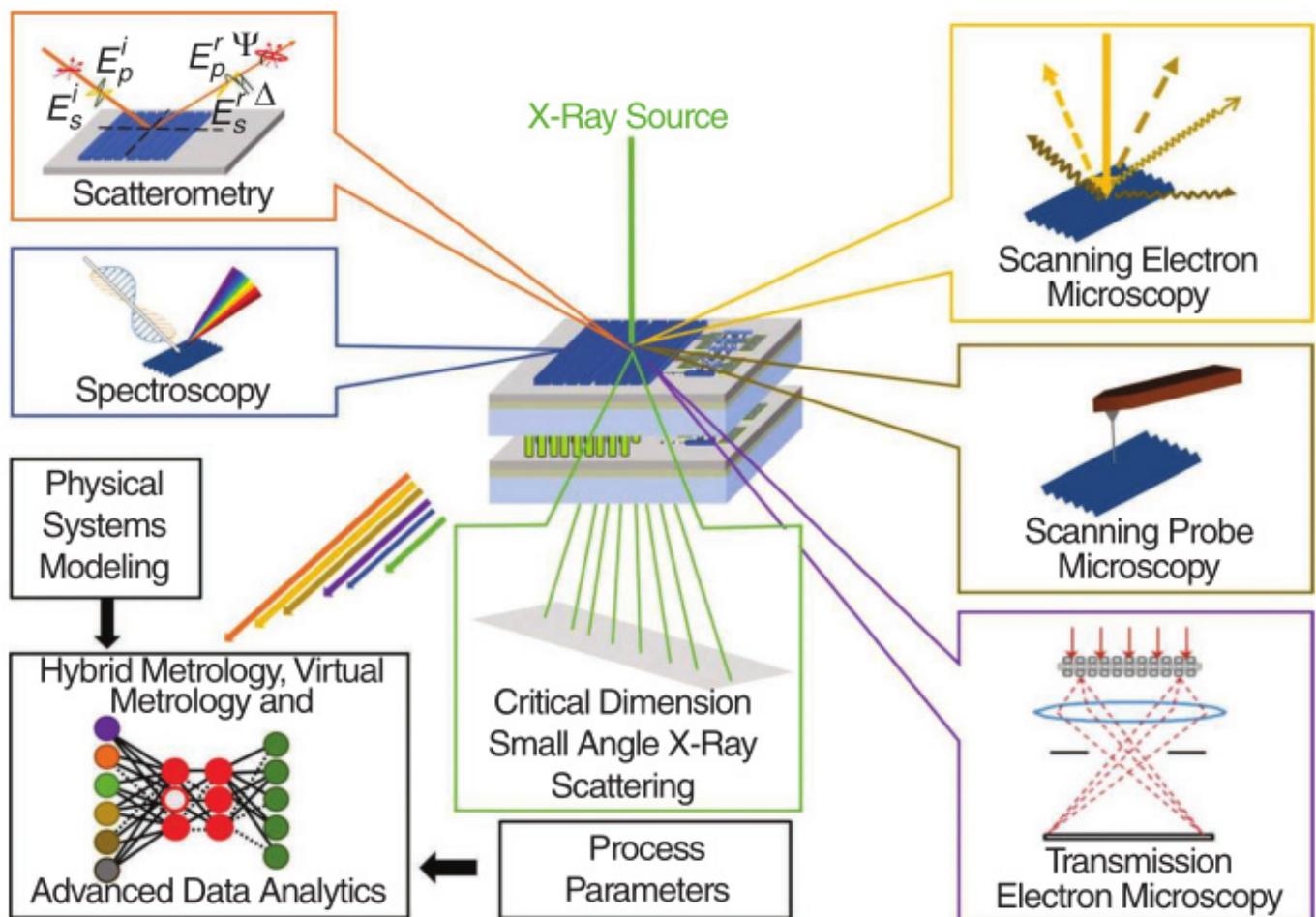
**Figure 42.** Schematic drawing of carbon nano tube (CNT) analysis using deep learning-based Raman spectra measurement. (a) Employment of high-speed Raman to image a fork-like sample. (b) Piling up and finally generating an unlabeled Raman spectrum. (c) To classify the large, labeled datasets into the following categories: S-CNTs, MCNTs, and empty. (d) Using the deep learning model. (e) Organizing of individual spectra applying the model. (f) Identifying the CNTs [399]. Reproduced from [399], open access by Springer Nature, 2022.

### 15.5. Hybrid Metrology

Figure 43 shows a series of characterization methods for nanometer scale material. In general, Hybrid metrology has shown promising advantages in reducing the uncertainties in the characterization of sub-10 nm dimensions [400]. With the assistance of modelling data analysis and treatment algorithms, a set of parameters can be obtained from correlative tools by comparison and merge.

It has been reported that multiple patterning errors can be easily obtained by combining CD-SAXS with optical metrology [401]. The idea behind this is that the buried layers are usually opaque to optical metrology techniques which can simply be analyzed by CD-SAXS. By incorporating SAXS data into the optical models, an enormous improvement in the optical measurements can be obtained. Hybrid STEM systems equipped with EELS and X-ray detection are applied to obtain valuable analysis into interface chemical bonding.

As another example, AFM and TEM imaging tools have recently been combined for advanced 3D imaging. This combined metrology provides nm-resolved 3D electrical and chemical analysis of Si- and Ge-based structures for sub-20 nm technology nodes [402]. It is extremely effective when performing failure analysis, because multiple material properties can be acquired by using the entire spectrum of different AFM modes [403–405].



**Figure 43.** Multiple-techniques approach to device metrology [405]. Reprinted with permission from ref. [405]. Copyright 2024, IEEE Publisher.

## 16. Conclusions

This review article is presented in four parts with the following outcomes:

In part one, GAAFET was presented as an excellent candidate for the 5 nm node technology and beyond due to its high control of SCEs. The design of GAAFET in vertical (vGAAFET) and horizontal (hGAAFET) was defined. One of the main advantages of vGAAFETs over hGAAFETs is the high integration density since the architecture limitations for gate length, spacer width, and S/D contact region for hGAAFET. For vGAAFET design a multilayer of SiGe/Si can firstly be grown and later, this original structure is patterned and vertically etched to form mesa structure. In vGAAFET design, SiGe channel is formed by selective etch in lateral direction.

One of the purposes of MOSFET size shrinking is also for the power consumption reduction. In general, reduced  $V_T$  and  $V_{DD}$  are eligible for lower power consumption. Other transistors issue refers to smaller SS requirement, where extremely steep switch characteristic is sought. As transistors have constant SS, reducing  $V_T$  and  $V_{DD}$  results in an exponential increase in leakage current and static power consumption. In the nano transistors, the SS of transistors has a limitation of  $\sim 60$  mV/dec due to the tail of Boltzmann distribution. Therefore, a new design as such as TFET design which is based on the BTBT mechanism is presented to overcome the 60 mV/dec limitation of SS and scale further  $V_T$  and  $V_{DD}$  with low leakage current. In this way, TFET is considered as excellent candidate for low power applications.

FDSOI technology was also presented as another approach to control SCEs during scaling down the transistor dimensions. The cost of the FDSOI wafer is higher, but it

demands minor changes in production compared with normal bulk processing, giving more possibility to employ new technologies. If we compare the total cost for FDSOI transistors to GAA transistors, it is almost compatible. Therefore, due to the advantages of FDSOI and FinFET, as well as strain engineering, a new platform is being offered in the technology roadmap such as FDSOI- (or strained) FDsOI-FinFETs. The effect of SiGe channel and doubly delta-doped layers on high frequency performance still need further study [406,407].

Transistor simulation using TCAD device models has also been discussed. As transistor devices scale down to the 5 nm technology node and beyond, a quantum-physics-induced effect is highly expected. This results in a huge rise not only in TCAD theory and methodology complexity but also in computational cost. To improve the predictability and computational efficiency of TCAD simulations, advanced physical models beyond drift-diffusion frameworks, as well as incorporating high-performance computing, have been presented. Further improvement can be achieved by introducing AI technology, including machine learning and deep learning approaches into TCAD and implemented not only atomistic calculation but also device- and circuit-level simulation.

In part two, advanced lithography techniques using self-aligned double pattern (SADP) and self-aligned quadruple pattern (SAQP) technology for 5 nm technology node and beyond were presented.

As the continuous shrinkage of transistor design rules, overlay requirement becomes more demanding. The mass production for advanced node requires overlay performance to be 2 nm and below in EUV platform. This is a real challenge for both overlay correction by scanner as well as overlay measurement. For the global overlay measurement, image-based overlay strategy has been mostly applied in mature products. As the technology node continues to shrink, diffraction-based overlay strategy has showed impressive performance. In this field, image-based overlay is better for non-tool-induced shift, whereas diffraction-based overlay is better for tool-induced shift.

Epitaxy growth of GeSi/Ge or SiGe/Si stacks where Si, Ge, or SiGe can be used as channel material of the GAAFETs have also been presented. Later, the Si or SiGe channel is formed by partial removal using wet etching.

For doping of GAAFET structures, the plasma doping method has been applied instead of traditional ion implantation.

For 3D CMOS, Ti silicide contact has been demonstrated as a suitable metal contact due to its low contact resistivity and high thermal stability. For such integration, pre-amorphous Ge implantation is performed to improve the property of Ti silicide.

HfO<sub>2</sub> as high-k material has thermal instability at HfO<sub>2</sub>/Si interface in nanoscale transistors. A solution for this problem is introducing a SiO<sub>x</sub> interlayer between HfO<sub>2</sub> and Si substrate. Meanwhile in each technology node, the thicknesses of SiO<sub>x</sub> and HfO<sub>2</sub> have constantly decreased.

TiN is used as PMOS work function metal and a TiAl-based alloy is used as the NMOS work function metal.

For the latest scaling down in technology nodes, copper interconnection shows difficulty in maintaining the trade-off between line resistance and reliability.

One solution is forming a barrier which is an alloy of Cu with V, Al, or -Mn seed layer by post-metalization annealing.

The reliability issues of an advanced CMOS device beyond the 5 nm node remains a complicated issue due to bias temperature instability, hot carrier degradation, and the self-heating effect. Usually, the traps are involved in physical mechanisms in reliability studies for advanced CMOS devices. Based on the physical understanding of location and energy distribution of traps in CMOS devices, the reliability of the process of HKMG stack in CMOS devices is optimized, especially the annealing process.

In part three, the material technology for sub-10 nm GAAFET and beyond the Moore era has been discussed. Later, the content covers the integration of III-V materials as high-

mobility channel application. The challenges of the high-quality growth of the III–V layer on the Si substrate and the difficulties in manufacturing III–V GAAFET were highlighted.

The application of 1D nanowire of III–V for transistor application was highlighted. The benefits of nanowire integration are due to the capability of advanced gate stacking, better stress relaxation, and more effective light trapping and adsorption. InAs, GaSb nanowires were presented for use in manufacturing Si-GAAFET devices.

Then, Si-based OEICs were proffered as a promising development in advanced CMOS technology. Most group III–V materials have direct bandgap, illustrating stronger efficiency of photon absorption and emission, nailing themselves for the optoelectronic devices in OEICs. To achieve a monolithic integration of III–V devices on the Si platform, it is important to develop a heteroepitaxy approach. There are some challenges for high-quality III–V heteroepitaxy on Si such as antiphase boundary and threading dislocation density.

Later, GeSn material was introduced due to its tunable bandgap and high-mobility properties. Compared with Si and Ge, GeSn has a wide window of absorption coefficient in the short-wave infrared, and higher carrier mobility. Compared with bulk GeSn/Ge materials, GeSnOI substrate has higher mobility due to its' high defect density Ge layer been removed. More discussions about the manufacturing and using of GeSnOI substrates for optoelectronics application was presented.

In part four, metrology technologies were discussed. As the scaling technology is approaching its physical limits, the requirements for the metrology development becomes increasingly crucial in the semiconductor industry. Metrology enables manufacturing process control, helps production, and reduces costs and the time-to-market for new products.

The aberration-corrected lens technology is adopted to improve the TEM/STEM technique's resolution. Mainstream X-ray metrology, such as HR-XRD, XRF, TXRF, XRR, XPS, and SAXS, has been used to determine thin film's parameters, like thickness, composition, strain/relaxation state, tilt, lattice constant.

It should be noted that SAXS is a technique routinely employed to study the structural features with the sizes ranging from 1 to 100 nm. The technique can be used to analyze any complex periodic nanostructures such as FinFETs in any dimension. The CD-SAXS technique can provide analysis of features and devices down to sub-5 nm, e.g., 3D FinFETs. CD-SAXS can perform a transmission through wafer measurement.

Hybrid metrology has demonstrated many advantages in the reduction in uncertainties for characterizing sub-10 nm dimensions. As an example, hybrid STEM systems equipped with EELS and X-ray detection are applied to provide valuable analysis into interface chemical bonding.

**Author Contributions:** H.H.R. and G.W. conceived and designed the manuscript; furthermore, H.H.R. has worked on the writing and quality control of all parts of this article, including the Introduction, Abstract, and Conclusion, as well as the References. Y.Z. was responsible for the "Vertical GAAFETs"; B.L. (Bin Lu) was responsible for the "TFETs"; J.S. (Jiangliu Shi), M.J. and D.L. were responsible for the "advanced Litho technology"; G.W. was responsible for the "S/D engineering"; Y.M. was responsible for the "new Ge and GeSn channel materials"; Y.D. (Yong Du) and B.L. (Ben Li) were responsible for the "III–V materials"; J.L. (Junjie Li) was responsible for the "dry etch, ALE"; J.G. was responsible for the "PVD and metal"; J.X. was responsible for the "High-K&Metal Gate, ALD"; H.L. and M.L. were responsible for the "Si/SiGe for Nanowires and Nanosheets"; X.D., C.H. and J.C. were responsible for the "FDSOI"; Y.W. and J.Y. were responsible for the "material characterization"; J.L. (Jinbiao Liu) was responsible for the "doping and implantation"; Z.W. was responsible for the "Simulation"; X.Z., J.S. (Jiale Su) and Z.Z. were responsible for the "photonic integration"; Z.K., Y.R., H.X., J.C., X.D. and H.Y. were responsible for the "GOI and GeSnOI substrate engineering"; H.C. was responsible for the "wet cleaning and etch"; H.Y. was responsible for the "reliability"; and Y.D. (Yan Dong) was responsible for the "language polish and editing". All the authors contributed equally to this article. All authors have read and agreed to the published version of the manuscript.

**Funding:** This work was supported in part by the "Pearl River Talent Plan" Innovation and Entrepreneurship Team Project of Guangdong Province (Grant No. 2021ZT09X479), in part funded by the Key Area R & D Program of Guangdong Province (Grant 2022B0701180001), in part by the

Innovation Program for Quantum Science and Technology (Grant No. 2021ZD0302301), the National Key Project of Science and Technology of China (Grant No. 2017ZX02315001-002), the Academy of Integrated Circuit Innovation (Grant No. Y7YC01X001) the Youth Innovation Promotion Association of CAS (Grant No. 2020037), and National Natural Science Foundation of China (Grant No. 92064002).

**Data Availability Statement:** Data are contained within the article.

**Conflicts of Interest:** Hushan Cui is employed in Jiangsu Leuven Instruments Co., Ltd. The authors declare no conflicts of interest.

## References

- Radamson, H.H.; Zhu, H.; Wu, Z.; He, X.; Lin, H.; Liu, J.; Xiang, J.; Kong, Z.; Xiong, W.; Li, J.; et al. State of the art and future perspectives in advanced CMOS technology. *Nanomaterials* **2020**, *10*, 1555. [\[CrossRef\]](#)
- Radamson, H.H.; He, X.; Zhang, Q.; Liu, J.; Cui, H.; Xiang, J.; Kong, Z.; Xiong, W.; Li, J.; Gao, J.; et al. Miniaturization of CMOS. *Micromachines* **2021**, *10*, 293. [\[CrossRef\]](#)
- Radamson, H.; Simoen, E.; Luo, J.; Zhao, C. *CMOS Past, Present and Future*; Woodhead Publishing: Cambridge, UK, 2018; ISBN 9780081021392.
- Jebalin, B.K.; Ajayan, J.; Franklin, S.A.; Nirmal, D. A new Vertical C-shaped Silicon Channel Nanosheet FET with Stacked High-K Dielectrics for Low Power Applications. *Silicon* **2024**, *16*, 2659–2670.
- Rezgui, H.; Wang, Y.; Mukherjee, C.; Deng, M.; Maneux, C. Signature of electrothermal transport in 18nm vertical junctionless gate-all-around nanowire field effect transistors. *J. Phys. D Appl. Phys.* **2024**. [\[CrossRef\]](#)
- Maheshwaram, S.; Manhas, S.K.; Kaushal, G.; Anand, B.; Singh, N. Vertical silicon nanowire gate-all-around field effect transistor-based nanoscale CMOS. *IEEE Electron Device Lett.* **2011**, *32*, 1011–1013. [\[CrossRef\]](#)
- Wang, G.; Qin, C.; Yin, H.; Luo, J.; Duan, N.; Yang, P.; Gao, X.; Yang, T.; Li, J.; Yan, J.; et al. Study of SiGe selective epitaxial process integration with high-k and metal gate for 16/14 nm nodes FinFET technology. *Microelectron. Eng.* **2016**, *163*, 49–54. [\[CrossRef\]](#)
- Yin, X.; Zhang, Y.; Zhu, H.; Wang, G.L.; Li, J.J.; Du, A.Y.; Li, C.; Zhao, L.H.; Huang, W.X.; Yang, H.; et al. Vertical Sandwich Gate-All-Around Field-Effect Transistors with Self-Aligned High-k Metal Gates and Small Effective Gate-Length Variation. *IEEE Electron Device Lett.* **2019**, *41*, 8–11. [\[CrossRef\]](#)
- Zhang, Y.; Ai, X.; Yin, X.; Zhu, H.; Yang, H.; Wang, G.L.; Li, J.J.; Du, A.Y.; Li, C.; Huang, W.X.; et al. Vertical Sandwich GAA FETs with Self-Aligned High-k Metal Gate Made by Quasi Atomic Layer Etching Process. *IEEE Trans. Electron Devices* **2021**, *68*, 2604–2610. [\[CrossRef\]](#)
- Kim, S.; Lee, K.; Lee, J.H.; Park, B.G.; Kwon, D. Gate-first negative capacitance field-effect transistor with self-aligned nickel-silicide source and drain. *IEEE Trans. Electron Devices* **2021**, *68*, 4754–4757. [\[CrossRef\]](#)
- Li, C.; Zhu, H.; Zhang, Y.; Wang, Q.; Yin, X.; Li, J.; Wang, G.; Kong, Z.; Ai, X.; Xie, L.; et al. First Demonstration of Novel Vertical Gate-All-Around Field-Effect-Transistors Featured by Self-Aligned and Replaced High- $\kappa$  Metal Gates. *Nano Lett.* **2021**, *21*, 4730–4737. [\[CrossRef\]](#)
- Zhang, Q.; Zhang, Y.; Luo, Y.; Yin, H. New structure transistors for advanced technology node CMOS ICs. *Natl. Sci. Rev.* **2024**, *11*, nwae008. [\[CrossRef\]](#)
- Huang, W.; Zhu, H.; Zhang, Y.; Yin, X.; Ai, X.; Li, J.; Li, C.; Li, Y.; Xie, L.; Liu, Y.; et al. Ferroelectric Vertical Gate-All-Around Field-Effect-Transistors with High Speed, High Density, and Large Memory Window. *IEEE Electron Device Lett.* **2022**, *43*, 25–28. [\[CrossRef\]](#)
- Liu, M.; Schlykow, V.; Hartmann, J.M.; Knoch, J.; Grützmacher, D.; Buca, D.; Zhao, Q.T. Vertical Heterojunction Ge<sub>0.92</sub>Sn<sub>0.08</sub>/Ge GAA Nanowire pMOSFETs: Low SS of 67 mV/dec, Small DIBL of 24 mV/V and Highest G<sub>m,ext</sub> of 870  $\mu$ S/ $\mu$ m. In Proceedings of the 2020 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 16–19 June 2020; pp. 1–2.
- Liu, M.; Scholz, S.; Mertens, K.; Bae, J.H.; Hartmann, J.M.; Knoch, J.; Buca, D.; Zhao, Q.T. First Demonstration of Vertical Ge<sub>0.92</sub>Sn<sub>0.08</sub>/Ge and Ge GAA Nanowire pMOSFETs with Low SS of 66 mV/dec and Small DIBL of 35 mV/V. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019.
- Liu, M.; Scholz, S.; Hardtdegen, A.; Bae, J.H.; Hartmann, J.M.; Knoch, J.; Grützmacher, D.; Buca, D.; Zhao, Q.T. Vertical Ge Gate-All-Around Nanowire pMOSFETs With a Diameter Down to 20 nm. *IEEE Electron Device Lett.* **2020**, *41*, 533–536. [\[CrossRef\]](#)
- Liu, M.; Lentz, F.; Trellenkamp, S.; Hartmann, J.M.; Knoch, J.; Grützmacher, D.; Buca, D.; Zhao, Q.T. Diameter Scaling of Vertical Ge Gate All-Around Nanowire pMOSFETs. *IEEE Trans. Electron Devices* **2020**, *67*, 2988–2994. [\[CrossRef\]](#)
- Tomiok, K.; Motohisa, J. Scaling effect on vertical gate-all-around FETs using III–V NW-channels on Si. In Proceedings of the Silicon Nanoelectronics Workshop (SNW), Virtual, 13 June 2021; pp. 1–2.
- Thingujam, T.; Dai, Q.; Kim, E.; Lee, J.H. A Simulation Study on the Effects of Interface Charges and Geometry on Vertical GAA GaN Nanowire MOSFET for Low-Power Application. *IEEE Access* **2021**, *9*, 101447–101453. [\[CrossRef\]](#)
- Thingujam, T.; Son, D.H.; Kim, J.G.; Cristoloveanu, S.; Lee, J.H. Effects of Interface Traps and Self-Heating on the Performance of GAA GaN Vertical Nanowire MOSFET. *IEEE Trans. Electron Devices* **2020**, *67*, 816–821. [\[CrossRef\]](#)
- Appenzeller, J.; Lin, Y.M.; Knoch, J.; Avouris, P. Band-to-band tunneling in carbon nanotube field-effect transistors. *Phys. Rev. Lett.* **2004**, *93*, 196805. [\[CrossRef\]](#)

22. Choi, W.Y.; Park, B.G.; Lee, J.D.; Liu, T.J.K. Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. *IEEE Electron Device Lett.* **2007**, *28*, 743–745. [[CrossRef](#)]
23. Mayer, F.; Le Royer, C.; Damlencourt, J.F.; Romanjek, K.; Andrieu, F.; Tabone, C.; Previtali, B.; Deleonibus, S. Impact of SOI, Si<sub>1-x</sub>Ge<sub>x</sub>OI and GeOI substrates on CMOS compatible tunnel FET performance. In Proceedings of the 2008 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2008; pp. 1–5. [[CrossRef](#)]
24. Kim, S.H.; Kam, H.; Hu, C.; Liu, T.J.K. Germanium-source tunnel field effect transistors with record high I<sub>ON</sub>/I<sub>OFF</sub>. In Proceedings of the 2009 Symposium on VLSI Technology, Kyoto, Japan, 16–18 June 2009; pp. 178–179, ISBN 978-1-4244-3308-7.
25. Jeon, K.; Loh, W.Y.; Patel, P.; Kang, C.Y.; Oh, J.; Bowonder, A.; Park, C.; Park, C.S.; Smith, C.; Majhi, P.; et al. Si tunnel transistors with a novel silicided source and 46 mV/dec swing. In Proceedings of the 2010 Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2010; pp. 121–122. [[CrossRef](#)]
26. Gandhi, R.; Chen, Z.; Singh, N.; Banerjee, K.; Lee, S. Vertical Si-nanowire n-type tunneling FETs with low subthreshold swing ( $\leq 50$  mV/decade) at room temperature. *IEEE Electron Device Lett.* **2011**, *32*, 437. [[CrossRef](#)]
27. Richter, S.; Sandow, C.; Nichau, A.; Trellenkamp, S.; Schmidt, M.; Luptak, R.; Bourdelle, K.K.; Zhao, Q.T.; Mantl, S. Omega-Gated Silicon and Strained Silicon Nanowire Array Tunneling FETs. *IEEE Electron Device Lett.* **2012**, *33*, 1535–1537. [[CrossRef](#)]
28. Huang, Q.; Huang, R.; Zhan, Z.; Wu, C.; Qiu, Y.; Wang, Y. Performance improvement of Si Pocket-Tunnel FET with steep subthreshold slope and high I<sub>ON</sub>/I<sub>OFF</sub> ratio. In Proceedings of the 2012 IEEE 11th International Conference on Solid-State and Integrated Circuit Technology, Xi'an, China, 29 October–1 November 2012; pp. 1–3. [[CrossRef](#)]
29. Huang, Q.; Huang, R.; Zhan, Z.; Qiu, Y.; Jiang, W.; Wu, C.; Wang, Y. A novel Si tunnel FET with 36 mV/dec subthreshold slope based on junction depleted-modulation through striped gate configuration. In Proceedings of the 2012 International Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012. [[CrossRef](#)]
30. Liu, Y.; Wang, H.J.; Yan, J.; Han, G.Q. A Silicon Tunnel Field-Effect Transistor with an In Situ Doped Single Crystalline Ge Source for Achieving Sub-60 mV/decade Subthreshold Swing. *Chin. Phys. Lett.* **2013**, *30*, 088502. [[CrossRef](#)]
31. Richter, S.; Schulte-Braucks, C.; Knoll, L.; Luong, G.V.; Schäfer, A.; Trellenkamp, S.; Zhao, Q.T.; Mantl, S. Experimental Demonstration of Inverter and NAND operation in p-TFET logic at Ultra-low Supply Voltages down to VDD = 0.15 V. In Proceedings of the 72nd Device Research Conference, Santa Barbara, CA, USA, 22–25 June 2014; Volume 1911, pp. 22–27. [[CrossRef](#)]
32. Huang, Q.; Huang, R.; Wu, C.; Zhu, H.; Chen, C.; Wang, J.; Guo, L.; Wang, R.; Ye, L.; Wang, Y. Comprehensive performance re-assessment of TFETs with a novel design by gate and source engineering from device/circuit perspective. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014. [[CrossRef](#)]
33. Takagi, S.; Kim, M.S.; Noguchi, M.; Nishi, K.; Takenaka, M. Tunneling FET device technologies using III–V and Ge materials. In Proceedings of the 2015 Fourth Berkeley Symposium on Energy Efficient Electronic Systems (E3S), Berkeley, CA, USA, 1–2 October 2015; pp. 1–2. [[CrossRef](#)]
34. Kim, S.W.; Kim, J.H.; Liu, T.J.K.; Choi, W.Y.; Park, B.G. Demonstration of L-Shaped Tunnel Field-Effect Transistors. *IEEE Trans. Electron Devices* **2016**, *63*, 1774–1778. [[CrossRef](#)]
35. Liu, C.; Glass, S.; Luong, G.V.; Narimani, K.; Han, Q.; Tiedemann, A.T.; Fox, A.; Yu, W.; Wang, X.; Mantl, S.; et al. Experimental Investigation of C-V Characteristics of Si Tunnel FETs. *IEEE Electron Device Lett.* **2017**, *38*, 818–821. [[CrossRef](#)]
36. Zhao, Y.; Wu, C.; Huang, Q.; Chen, C.; Zhu, J.; Guo, L.; Jia, R.; Lv, Z.; Yang, Y.; Li, M.; et al. A Novel Tunnel FET Design Through Adaptive Bandgap Engineering with Constant Sub-Threshold Slope Over 5 Decades of Current and High I<sub>ON</sub>/I<sub>OFF</sub> Ratio. *IEEE Electron Device Lett.* **2017**, *38*, 540–543. [[CrossRef](#)]
37. Kim, J.H.; Kim, S.; Park, B.G. Double-Gate TFET With Vertical Channel Sandwiched by Lightly Doped Si. *IEEE Transactions on Electron Devices* **2019**, *66*, 1656–1661. [[CrossRef](#)]
38. Cheng, W.; Liang, R.; Xu, G.; Yu, G.; Zhang, S.; Yin, H.; Zhao, C.; Ren, T.L.; Xu, J. Fabrication and characterization of a novel Si line tunneling TFET with high drive current. *IEEE J. Electron Devices Soc.* **2020**, *8*, 336–340. [[CrossRef](#)]
39. Kato, K.; Jo, K.W.; Matsui, H.; Tabata, H.; Mori, T.; Morita, Y.; Matsukawa, T.; Takenaka, M.; Takagi, S. P-channel TFET operation of bilayer structures with type-II heterotunneling junction of oxide-and group-IV semiconductors. *IEEE Trans. Electron Devices* **2020**, *67*, 1880–1886. [[CrossRef](#)]
40. Dewey, G.; Chu-Kung, B.; Boardman, J.; Fastenau, J.M.; Kavalieros, J.; Kotlyar, R.; Liu, W.K.; Lubyshev, D.; Metz, M.; Mukherjee, N.; et al. Fabrication, characterization, and physics of III–V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing. In Proceedings of the 2011 International Electron Devices Meeting, Washington, DC, USA, 5–7 December 2011. [[CrossRef](#)]
41. Mohata, D.K.; Bijesh, R.; Zhu, Y.; Hudait, M.K.; Southwick, R.; Chbili, Z.; Gundlach, D.; Suehle, J.; Fastenau, J.M.; Loubychev, D.; et al. Demonstration of improved heteroepitaxy, scaled gate stack and reduced interface states enabling heterojunction tunnel FETs with high drive current and high on-off ratio. In Proceedings of the 2012 Symposium on VLSI Technology (VLSIT), Honolulu, HI, USA, 12–14 June 2012; pp. 53–54. [[CrossRef](#)]
42. Riel, H.; Moselund, K.E.; Bessire, C.; Björk, M.T.; Schenk, A.; Ghoneim, H.; Schmid, H. InAs-Si heterojunction nanowire tunnel diodes and tunnel FETs. In Proceedings of the 2012 International Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012. [[CrossRef](#)]

43. Zhou, G.; Li, R.; Vasen, T.; Qi, M.; Chae, S.; Lu, Y.; Zhang, Q.; Zhu, H.; Kuo, J.M.; Kosel, T.; et al. Novel gate-recessed vertical InAs/GaSb TFETs with record high  $I_{ON}$  of 180  $\mu\text{A}/\mu\text{m}$  at  $V_{DS}=0.5$  V. In Proceedings of the 2012 International Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012. [CrossRef]
44. Tomioka, K.; Yoshimura, M.; Fukui, T. Steep-slope tunnel field-effect transistors using III–V nanowire/Si heterojunction. In Proceedings of the 2012 Symposium on VLSI Technology (VLSIT), Honolulu, HI, USA, 12–14 June 2012; pp. 47–48. [CrossRef]
45. Bijesh, R.; Liu, H.; Madan, H.; Mohata, D.; Li, W.; Nguyen, N.V.; Gundlach, D.; Richter, C.A.; Maier, J.; Wang, K.; et al. Demonstration of In<sub>0.9</sub>Ga<sub>0.1</sub>As/GaAs<sub>0.18</sub>Sb<sub>0.82</sub> near broken-gap tunnel FET with  $I_{ON} = 740 \mu\text{A}/\mu\text{m}$   $G_M = 700 \mu\text{S}/\mu\text{m}$  and Gigahertz Switching Performance at  $V_{DS} = 0.5$  V. In Proceedings of the 2013 IEEE International Electron Devices Meeting, Washington, DC, USA, 9–11 December 2013. [CrossRef]
46. Noguchi, M.; Kim, S.; Yokoyama, M.; Ichikawa, O.; Osada, T.; Hata, M.; Takenaka, M.; Takagi, S. High  $I_{on}/I_{off}$  and low subthreshold slope planar-type InGaAs tunnel FETs with Zn-diffused source junctions. *J. Appl. Phys.* **2015**, *118*, 785. [CrossRef]
47. Rajamohanam, B.; Pandey, R.; Chobpattana, V.; Vaz, C.; Gundlach, D.; Cheung, K.P.; Suehle, J.; Stemmer, S.; Datta, S. 0.5 V Supply Voltage Operation of In<sub>0.65</sub>Ga<sub>0.35</sub>As/GaAs<sub>0.45</sub>Sb<sub>0.6</sub>, Tunnel FET. *IEEE Electron Device Lett.* **2015**, *36*, 20–22. [CrossRef]
48. Pandey, R.; Madan, H.; Liu, H.; Chobpattana, V.; Barth, M.; Rajamohanam, B.; Hollander, M.J.; Clark, T.; Wang, K.; Datta, S.; et al. Demonstration of p-type In<sub>0.7</sub>Ga<sub>0.3</sub>As/GaAs<sub>0.35</sub>Sb<sub>0.65</sub> and n-type GaAs<sub>0.45</sub>Sb<sub>0.6</sub>/In<sub>0.65</sub>Ga<sub>0.35</sub>As complimentary Heterojunction Vertical Tunnel FETs for ultra-low power logic. In Proceedings of the 2015 Symposium on VLSI Technology (VLSI Technology), Kyoto, Japan, 16–18 June 2015; pp. 296–313. [CrossRef]
49. Cutaia, D.; Moselund, K.E.; Schmid, H.; Borg, M.; Olziersky, A.; Riel, H. Complementary III–V heterojunction lateral NW Tunnel FET technology on Si. In Proceedings of the 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 14–16 June 2016; pp. 1–2. [CrossRef]
50. Schulte-Braucks, C.; Pandey, R.; Sajjad, R.N.; Barth, M.; Ghosh, R.K.; Grisafe, B.; Sharma, P.; von den Driesch, N.; Vohra, A.; Rayner, G.B.; et al. Fabrication, Characterization, and Analysis of Ge/GeSn Heterojunction p-Type Tunnel Transistors. *IEEE Trans. Electron Devices* **2017**, *64*, 4354–4362. [CrossRef]
51. Hellenbrand, M.; Memisevic, E.; Svensson, J.; Krishnaraja, A.; Lind, E.; Wernersson, L.E. Capacitance Measurements in Vertical III–V Nanowire TFETs. *IEEE Electron Device Lett.* **2018**, *39*, 943–946. [CrossRef]
52. Memisevic, E.; Svensson, J.; Lind, E.; Wernersson, L.E. Vertical Nanowire TFETs With Channel Diameter Down to 10 nm and Point SMIN of 35 mV/Decade. *IEEE Electron Device Lett.* **2018**, *39*, 1089–1091. [CrossRef]
53. Vasen, T.; Ramvall, P.; Afzalilian, A.; Doornbos, G.; Holland, M.; Thelander, C.; Dick, K.A.; Wernersson, L.E.; Passlack, M. Vertical gate-all-around nanowire GaSb-InAs core-shell n-type tunnel FETs. *Sci. Rep.* **2019**, *9*, 202. [CrossRef]
54. Convertino, C.; Zota, C.B.; Schmid, H.; Caimi, D.; Czornomaz, L.; Ionescu, A.M.; Moselund, K.E. A hybrid III–V tunnel FET and MOSFET technology platform integrated on silicon. *Nat. Electron.* **2021**, *4*, 162–170. [CrossRef]
55. Zhao, Y.; Liang, Z.; Huang, Q.; Chen, C.; Yang, M.; Sun, Z.; Zhu, K.; Wang, H.; Liu, S.; Liu, T.; et al. A novel negative capacitance tunnel FET with improved subthreshold swing and nearly non-hysteresis through hybrid modulation. *IEEE Electron Device Lett.* **2019**, *40*, 989–992. [CrossRef]
56. Kamaei, S.; Saeidi, A.; Gastaldi, C.; Rosca, T.; Capua, L.; Cavalieri, M.; Ionescu, A.M. Gate energy efficiency and negative capacitance in ferroelectric 2D/2D TFET from cryogenic to high temperatures. *NPJ 2d Mater. Appl.* **2021**, *5*, 76. [CrossRef]
57. Oliva, N.; Backman, J.; Capua, L.; Cavalieri, M.; Luisier, M.; Ionescu, A.M. WSe<sub>2</sub>/SnSe<sub>2</sub> vdW heterojunction Tunnel FET with subthermionic characteristic and MOSFET co-integrated on same WSe<sub>2</sub> flake. *NPJ 2d Mater. Appl.* **2020**, *4*, 5. [CrossRef]
58. Gayduchenko, I.; Xu, S.G.; Alymov, G.; Moskotin, M.; Tretyakov, I.; Taniguchi, T.; Watanabe, K.; Goltsman, G.; Geim, A.K.; Fedorov, G.; et al. Tunnel field-effect transistors for sensitive terahertz detection. *Nat. Commun.* **2021**, *12*, 543. Available online: <https://arxiv.org/abs/2010.03040> (accessed on 22 January 2021). [CrossRef]
59. Hwang, W.S.; Zhao, P.; Kim, S.G.; Yan, R.; Klimeck, G.; Seabaugh, A.; Fullerton-Shirey, S.K.; Xing, H.G.; Jena, D. Room-temperature graphene-nanoribbon tunneling field-effect transistors. *NPJ 2d Mater. Appl.* **2019**, *3*, 43. [CrossRef]
60. Zhang, W.; Kanazawa, T.; Miyamoto, Y. Performance improvement of a p-MoS<sub>2</sub>/HfS<sub>2</sub> van der Waals heterostructure tunneling FET by UV-O<sub>3</sub> treatment. *Appl. Phys. Express* **2019**, *12*, 065005. [CrossRef]
61. Afzalilian, A.; Akhouni, E.; Gaddemane, G.; Duflou, R.; Houssa, M. Advanced DFT–NEGF Transport Techniques for Novel 2-D Material and Device Exploration Including HfS<sub>2</sub>/WSe<sub>2</sub> van der Waals Heterojunction TFET and WTe<sub>2</sub>/WS<sub>2</sub> Metal/Semiconductor Contact. *IEEE Trans. Electron Devices* **2021**, *68*, 5372–5379. [CrossRef]
62. Hartmann, J.M.; Benevent, V.; André, A.; Sirisopanaporn, C.; Veillerot, M.; Samson, M.P.; Sermage, B. Very Low Temperature (Cyclic) Deposition / Etch of In Situ Boron-Doped SiGe Raised Sources and Drains. *ECS J. Solid State Sci. Technol.* **2014**, *3*, P382–P390. [CrossRef]
63. Chakraborty, W.; Aabrar, K.A.; Gomez, J.; Saligram, R.; Raychowdhury, A.; Fay, P.; Datta, S. Characterization and modeling of 22 nm FDSOI cryogenic RF CMOS. *IEEE J. Explor. Solid-State Comput. Devices Circuits* **2021**, *7*, 184–192. [CrossRef]
64. Radamson, H.H.; Kolahdouz, M. Selective epitaxy growth of Si<sub>1-x</sub>Ge<sub>x</sub> layers for MOSFETs and FinFET. *J. Mater. Sci. Mater. Electron.* **2015**, *26*, 4584–4603. [CrossRef]
65. Villalon, A.; Le Royer, C.; Cristoloveanu, S.; Cassé, M.; Cooper, D.; Mazurier, J.; Prévitali, B.; Tabone, C.; Perreau, P.; Faynot, O.; et al. High-Performance Ultrathin Body c-SiGe Channel FDSOI pMOSFETs Featuring SiGe Source and Drain: V<sub>th</sub> Tuning, Variability, Access Resistance, and Mobility Issues. *IEEE Trans. Electron Devices* **2013**, *60*, 1568–1574. [CrossRef]

66. Liu, Q.; Yagishita, A.; Kumar, A. Ultra-Thin Body and BOX (UTBB) Device for Aggressive Scaling of CMOS Technology. *ECS Trans.* **2019**, *34*, 37–42. [[CrossRef](#)]
67. Mohsen, A. *Harmonic Feedback Multi-Oscillator for 5G Application*; Université de Bordeaux: Bordeaux, France, 2018.
68. Hu, C. Thin-body FinFET as scalable low voltage transistor. In Proceedings of the Technical Program of 2012 VLSI Technology, System and Application, Hsinchu, Taiwan, 23–25 April 2012; pp. 1–4. [[CrossRef](#)]
69. Cristoloveanu, S. Trends in SOI Technology: Hot and Green. *J. Korean Phys. Soc.* **2011**, *58*, 1461–1467. [[CrossRef](#)]
70. Bhavnagarwala, A.; Kosonocky, S.; Radens, C.; Stawiasz, K.; Mann, R.; Ye, Q.; Chin, K. Fluctuation limits & scaling opportunities for CMOS SRAM cells. In Proceedings of the IEEE International Electron Devices Meeting, Washington, DC, USA, 5 December 2005. [[CrossRef](#)]
71. Skotnicki, T.; Fenouillet-Beranger, C.; Gallon, C.; Boeuf, F.; Monfray, S.; Payet, F.; Pouydebasque, A.; Szczap, M.; Farcy, A.; Arnaud, F.; et al. Innovative Materials, Devices, and CMOS Technologies for Low-Power Mobile Multimedia. *IEEE Trans. Electron Devices* **2008**, *55*, 96–130. [[CrossRef](#)]
72. Hällstedt, J.; Hellström, P.E.; Zhang, Z.; Malm, B.G.; Edholm, J.; Lu, J.; Zhang, S.L.; Radamson, H.H.; Östling, M. A robust spacer gate process for deca-nanometer high-frequency MOSFETs. *Microelectron. Eng.* **2006**, *83*, 434–439. [[CrossRef](#)]
73. Triyoso, D.; Carter, R.; Kluth, J.; Luning, S.; Child, A.; Wahl, J.; Mulfinger, B.; Punchihewa, K.; Kumar, A.; Kang, L.; et al. Factors Impacting Threshold Voltage in Advanced CMOS Integration: Gate Last (FINFET) vs. Gate First (FDSOI). *ECS Trans.* **2015**, *69*, 103–110. [[CrossRef](#)]
74. Andrieu, F.; Weber, O.; Mazurier, J.; Thomas, O.; Noel, J.-P.; Fenouillet-Beranger, C.; Mazellier, J.-P.; Perreau, P.; Poiroux, T.; Morand, Y.; et al. Low leakage and low variability Ultra-Thin Body and Buried Oxide (UT2B) SOI technology for 20nm low power CMOS and beyond. In Proceedings of the 2010 Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2010. [[CrossRef](#)]
75. Magarshack, P.; Flatresse, P.; Cesana, G. UTBB FD-SOI: A process/design symbiosis for breakthrough energy-efficiency. In Proceedings of the 2013 Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, 18–22 March 2013. [[CrossRef](#)]
76. Fenouillet-Beranger, C.; Thomas, O.; Perreau, P.; Bajolet, A.; Haendler, S.; Tosti, L.; Barnola, S.; Beneyton, R.; Perrot, C.; de Buttet, C.; et al. Efficient multi Vt FDSOI technology with UTBOX for low power circuit design. In Proceedings of the 2010 Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2010; pp. 65–66. [[CrossRef](#)]
77. Umesao, R.; Ida, J.; Kawabata, K.; Tashino, S.; Noguchi, K.; Itoh, K. High efficiency rectification by SOI based gate controlled diode for RF energy harvesting. In Proceedings of the 2013 IEEE Wireless Power Transfer (WPT), Perugia, Italy, 15–16 May 2013. [[CrossRef](#)]
78. Iwai, H. CMOS downsizing toward sub-10 nm. *Solid-State Electron.* **2004**, *48*, 497–503. [[CrossRef](#)]
79. Grenouillet, L.; Liu, Q.; Wacquez, R.; Morin, P.; Loubet, N.; Cooper, D.; Pofelski, A.; Weng, W.; Bauman, F.; Gribelyuk, M.; et al. UTBB FDSOI scaling enablers for the 10nm node. In Proceedings of the 2013 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Monterey, CA, USA, 7–10 October 2013. [[CrossRef](#)]
80. Faynot, O.; Andrieu, F.; Fenouillet-Beranger, C.; Weber, O.; Perreau, P.; Tosti, L.; Brevard, L.; Rozeau, O.; Scheiblin, P.; Thomas, O.; et al. Planar FDSOI technology for sub 22nm nodes. In Proceedings of the 2010 International Symposium on VLSI Technology, System and Application, Hsinchu, Taiwan, 26–28 April 2010. [[CrossRef](#)]
81. Su, E.M.H.; Hong, D.C.; Cristoloveanu, S.; Taur, Y. Effects of BOX thickness, silicon thickness, and backgate bias on SCE of ET-SOI MOSFETs. *Microelectron. Eng.* **2021**, *238*, 111506. [[CrossRef](#)]
82. Morin, P.; Maitrejean, S.; Allibert, F.; Augendre, E.; Liu, Q.; Loubet, N.; Grenouillet, L.; Pofelski, A.; Chen, K.; Khakifirooz, A.; et al. A review of the mechanical stressors efficiency applied to the ultra-thin body & buried oxide fully depleted silicon on insulator technology. *Solid-State Electron.* **2016**, *117*, 100–116.
83. Chan, T.Y.; Chen, J.; Ko, P.K.; Hu, C. The impact of gate-induced drain leakage current on MOSFET scaling. In Proceedings of the 1987 International Electron Devices Meeting, Washington, DC, USA, 6–9 December 1987. [[CrossRef](#)]
84. Wann, H.-J.; Hu, C. Gate-induced band-to-band tunneling leakage current in LDD MOSFETs. In Proceedings of the 1992 International Technical Digest on Electron Devices Meeting, San Francisco, CA, USA, 13–16 December 1992. [[CrossRef](#)]
85. Yan, R.; Duane, R.; Razavi, P.; Afzal, A.; Ferain, I.; Lee, C.-W.; Akhavan, N.D.; Nguyen, B.-Y.; Bourdelle, K.K.; Colinge, J.-P. Back-gate mirror doping for fully depleted planar SOI transistors with thin buried oxide. In Proceedings of the 2010 International Symposium on VLSI Technology, System and Application, Hsinchu, Taiwan, 26–28 April 2010; pp. 76–77. [[CrossRef](#)]
86. Fenouillet-Beranger, C. FDSOI devices with thin BOX and ground plane integration for 32nm node and below. *Solid-State Electron.* **2009**, *53*, 730–734. [[CrossRef](#)]
87. Monfray, S.; Skotnicki, T. UTBB FDSOI: Evolution and opportunities. *Solid-State Electron.* **2016**, *125*, 63–72. [[CrossRef](#)]
88. Liu, Q.; Yagishita, A.; Loubet, N.; Khakifirooz, A.; Kulkarni, P.; Yamamoto, T.; Cheng, K.; Fujiwara, M.; Cai, J.; Dorman, D.; et al. Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22nm node and beyond. In Proceedings of the 2010 Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2010; pp. 61–62. [[CrossRef](#)]
89. Liang, J.; Sun, C.; Xu, H.; Kong, E.Y.J.; Nguyen, B.Y.; Schwarzenbach, W.; Maleville, C.; Berthelon, R.; Weber, O.; Arnaud, F.; et al. Strained silicon-on-insulator platform for co-integration of logic and RF—Part II: Comb-like device architecture. *IEEE Trans. Electron Devices* **2022**, *69*, 1769–1775. [[CrossRef](#)]

90. Jacquet, D.; Hasbani, F.; Flatresse, P.; Wilson, R.; Arnaud, F.; Cesana, G.; Di Gilio, T.; Lecocq, C.; Roy, T.; Chhabra, A.; et al. A 3 GHz dual core processor ARM cortex TM-A9 in 28 nm UTBB FD-SOI CMOS with ultra-wide voltage range and energy efficiency optimization. *IEEE J. Solid-State Circuits* **2014**, *49*, 812–826. [[CrossRef](#)]
91. Nomura, S.; Tachibana, F.; Fujita, T.; Teh, C.K.; Usui, H.; Yamane, F.; Miyamoto, Y.; Kumtornkittikul, C.; Hara, H.; Yamashita, T.; et al. A 9.7mw aac-decoding, 620mw h. 264 720p 60fps decoding, 8-core media processor with embedded forward-body-biasing and power-gating circuit in 65nm cmos technology. In Proceedings of the 2008 IEEE International Solid-State Circuits Conference-Digest of Technical Papers, San Francisco, CA, USA, 3–7 February 2008; pp. 262–612. [[CrossRef](#)]
92. Ong, S.N.; Chan, L.H.K.; Chew, K.W.J.; Lim, C.K.; Oo, W.L.; Bellaouar, A.; Haramé, D. 22nm FD-SOI technology with back-biasing capability offers excellent performance for enabling efficient, ultra-low power analog and RF/millimeter-wave designs. In Proceedings of the 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2–4 June 2019; pp. 323–326.
93. Grenouillet, L.; Vinet, M.; Gimbert, J.; Giraud, B.; Noel, J.P.; Liu, Q.; Khare, P.; Jaud, M.A.; Le Tiec, Y.; Wacquez, R.; et al. UTBB FDSOI transistors with dual STI for a multi-Vt strategy at 20nm node and below. In Proceedings of the 2012 International Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012. [[CrossRef](#)]
94. Cai, J.; Majumdar, A.; Ning, T.H.; Ren, Z. Method for Fabricating Super-Steep Retrograde Well Mosfet on Soi or Bulk Silicon Substrate, and Device Fabricated in Accordance with the Method. U.S. Patent 8,329,564, 30 April 2009.
95. Skotnicki, T. Competitive SOC with UTBB SOI. In Proceedings of the IEEE 2011 International SOI Conference, Tempe, AZ, USA, 3–6 October 2011; pp. 1–61. [[CrossRef](#)]
96. Flatresse, P.; Giraud, B. Ultra-wide body-bias range LDPC decoder in 28nm UTBB FDSOI technology. In Proceedings of the 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, San Francisco, CA, USA, 17–21 February 2013; pp. 424–425. [[CrossRef](#)]
97. Rudenko, T.E.; Nazarov, A.N.; Lysenko, V.S. The advancement of silicon-on-insulator (SOI) devices and their basic properties. *Semicond. Phys. Quantum Electron. Optoelectron.* **2020**, *23*, 227–252. [[CrossRef](#)]
98. Hallstedt, J.; von Haartman, M.; Hellstrom, P.E.; Ostling, M.; Radamsson, H.H. Hole mobility in ultrathin body SOI pMOSFETs with SiGe or SiGeC channels. *IEEE Electron Device Lett.* **2006**, *27*, 466. [[CrossRef](#)]
99. Cheng, K.; Khakifirooz, A.; Jiang, X. FDSOI technology and its implications for analog and digital design. In *Digitally-Assisted Analog and Analog-Assisted Digital IC Design*; Cambridge University Press: Cambridge, UK, 2015; pp. 56–97. [[CrossRef](#)]
100. Planes, N.; Weber, O.; Barral, V.; Haendler, S.; Noblet, D.; Croain, D.; Bocat, M.; Sassoulas, P.-O.; Federspiel, X.; Cros, A.; et al. 28 nm FDSOI technology platform for high-speed low-voltage digital applications. In Proceedings of the 2012 Symposium on VLSI Technology (VLSIT), Honolulu, HI, USA, 12–14 June 2012; pp. 133–134. [[CrossRef](#)]
101. Litty, A.; Ortolland, S.; Golanski, D.; Cristoloveanu, S. Optimization of a high-voltage MOSFET in ultra-thin 14nm FDSOI technology. In Proceedings of the 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Hong Kong, China, 10–14 May 2015. [[CrossRef](#)]
102. Khakifirooz, A.; Cheng, K.; Reznicek, A.; Adam, T.; Loubet, N.; He, H.; Kuss, J.; Li, J.; Kulkarni, P.; Ponoth, S.; et al. Scalability of Extremely Thin SOI (ETSOI) MOSFETs to Sub-20-nm Gate Length. *IEEE Electron Device Lett.* **2012**, *33*, 149–151. [[CrossRef](#)]
103. Stanojevic, Z.; Baumgartner, O.; Schanovsky, F.; Strof, G.; Kernstock, C.; Karner, M.; Medina, J.M.G.; Ruiz, F.G.; Godoy, A.; Gamiz, F. Scaling FDSOI technology down to 7 nm—A physical modeling study based on 3D phase-space subband boltzmann transport. In Proceedings of the 2018 Joint International EUROSOCI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOCI-ULIS), Granada, Spain, 19–21 March 2018; pp. 1–4. [[CrossRef](#)]
104. Bae, D.-I.; Bae, G.; Bhuwarka, K.K.; Lee, S.-H.; Song, M.-G.; Jeon, T.-S.; Kim, C.; Kim, W.; Park, J.; Kim, S.; et al. A novel tensile Si (n) and compressive SiGe (p) dual-channel CMOS FinFET co-integration scheme for 5nm logic applications and beyond. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016. [[CrossRef](#)]
105. Ungersboeck, E.; Sverdlov, V.; Kosina, H.; Selberherr, S. Strain engineering for CMOS devices. In Proceedings of the 2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings, Shanghai, China, 23–26 October 2006; pp. 123–127. [[CrossRef](#)]
106. Le Royer, C.; Cassé, M.; Cooper, D.; Andrieu, F.; Weber, O.; Brevard, L.; Perreau, P.; Damlencourt, J.-F.; Baudot, S.; Prévitali, B.; et al. Dual strained channel CMOS in FDSOI architecture: New insights on the device performance. *Solid-State Electron.* **2011**, *65*, 9–15. [[CrossRef](#)]
107. Liu, Q.; DeSalvo, B.; Morin, P.; Loubet, N.; Pilorget, S.; Chafik, F.; Maitrejean, S.; Augendre, E.; Chanemougame, D.; Guillaumet, S.; et al. FDSOI CMOS devices featuring dual strained channel and thin BOX extendable to the 10nm node. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014. [[CrossRef](#)]
108. Chan, V.; Rim, K.; Jeong, M.; Yang, S.; Malik, R.; Teh, Y.W.; Yang, M. Strain for CMOS performance improvement. In Proceedings of the IEEE 2005 Custom Integrated Circuits Conference, San Jose, CA, USA, 18–21 September 2005; pp. 667–674. [[CrossRef](#)]
109. Raymond, G.; Morin, P.; Devos, A.; Hess, D.A.; Braccini, M.; Volpi, F. Characterisation of silicon nitride thin films used as stressor liners on CMOS FETs. In Proceedings of the 2008 9th International Conference on Ultimate Integration of Silicon, Udine, Italy, 12–14 March 2008; pp. 199–202. [[CrossRef](#)]

110. Cheng, K.; Khakifirooz, A.; Loubet, N.; Luning, S.; Nagumo, T.; Vinet, M.; Liu, Q.; Reznicek, A.; Adam, T.; Naczas, S.; et al. High performance extremely thin SOI (ETSOI) hybrid CMOS with Si channel NFET and strained SiGe channel PFET. In Proceedings of the 2012 International Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012. [\[CrossRef\]](#)
111. Le Royer, C.; Villalon, A.; Casse, M.; Cooper, D.; Mazurier, J.; Previtali, B.; Tabone, C.; Perreau, P.; Hartmann, J.-M.; Scheiblin, P.; et al. First demonstration of ultrathin body c-SiGe channel FDSOI pMOSFETs combined with SiGe(B) RSD: Drastic improvement of electrostatics ( $V_{th,p}$  tuning, DIBL) and transport ( $\mu_0$ ,  $I_{sat}$ ) properties down to 23nm gate length. In Proceedings of the 2011 International Electron Devices Meeting, Washington, DC, USA, 5–7 December 2011. [\[CrossRef\]](#)
112. Colinge, J.-P. *The SOI MOSFET: From Single Gate to Multigate, in FinFETs and Other Multi-Gate Transistors*; Colinge, J.-P., Ed.; Springer: Boston, MA, USA, 2008; pp. 1–48. [\[CrossRef\]](#)
113. Chaudhry, A.; Kumar, M.J. Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: A review. *IEEE Trans. Device Mater. Reliab.* **2004**, *4*, 99–109. [\[CrossRef\]](#)
114. Deshmukh, R.; Khanzode, A.; Kakde, S.; Shah, N. Comparing FinFETs: SOI Vs Bulk: Process variability, process cost, and device performance. In Proceedings of the 2015 International Conference on Computer, Communication and Control (IC4), Indore, India, 10–12 September 2015; pp. 1–4. [\[CrossRef\]](#)
115. Chowdhury, N.; Azad, S.M.F.; Khosru, Q.D.M. Negative Capacitance Tunnel Field Effect Transistor: A Novel Device with Low Subthreshold Swing and High on Current. *ECS Trans.* **2014**, *58*, 1–8. [\[CrossRef\]](#)
116. Dabhi, C.K.; Parihar, S.S.; Dasgupta, A.; Chauhan, Y.S. Compact Modeling of Negative-Capacitance FDSOI FETs for Circuit Simulations. *IEEE Trans. Electron Devices* **2020**, *67*, 2710–2716. [\[CrossRef\]](#)
117. Hu, V.P.H.; Chiu, P.C.; Sachid, A.B.; Hu, C. Negative capacitance enables FinFET and FDSOI scaling to 2 nm node. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017. [\[CrossRef\]](#)
118. Sharma, S.M.; Dasgupta, S.; Kartikeyan, M.V. FinFETs for RF Applications: A Literature review. In Proceedings of the 2018 Conference on Emerging Devices and Smart Systems (ICEDSS), Tiruchengode, India, 2–3 March 2018; pp. 280–287. [\[CrossRef\]](#)
119. Agarwal, H.; Kushwaha, P.; Lin, Y.-K.; Kao, M.-Y.; Liao, Y.-H.; Duarte, J.-P.; Salahuddin, S.; Hu, C. NCFET Design Considering Maximum Interface Electric Field. *IEEE Electron Device Lett.* **2018**, *39*, 1254–1257. [\[CrossRef\]](#)
120. Maassen, J.; Harb, M.; Michaud-Rioux, V.; Zhu, Y.; Guo, H. Quantum Transport Modeling from First Principles. *Proc. IEEE* **2013**, *101*, 518–530. [\[CrossRef\]](#)
121. Ziogas, A.N.; Ben-Nun, T.; Fernández, G.I.; Schneider, T.; Luisier, M.; Hoefler, T. A data-centric approach to extreme-scale ab initio dissipative quantum transport simulations. In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, Denver, CO, USA, 17–22 November 2019; pp. 1–13. [\[CrossRef\]](#)
122. Hermann, J.; Schätzle, Z.; Noé, F. Deep-neural-network solution of the electronic Schrödinger equation. *Nat. Chem.* **2020**, *12*, 891–897. [\[CrossRef\]](#)
123. Pfau, D.; Spencer, J.S.; Matthews, A.G.; Foulkes, W.M.C. Ab initio solution of the many-electron Schrödinger equation with deep neural networks. *Phys. Rev. Res.* **2020**, *2*, 033429. [\[CrossRef\]](#)
124. Wang, Z.; Ye, S.; Wang, H.; He, J.; Huang, Q.; Chang, S. Machine learning method for tight-binding Hamiltonian parameterization from ab-initio band structure. *NPJ Comput. Mater.* **2021**, *7*, 1–10. [\[CrossRef\]](#)
125. Mengchao, S.; Mo, P.; Jie Liu, J. Deep neural network for accurate and efficient atomistic modeling of phase change memory. *IEEE Electron Device Lett.* **2020**, *41*, 365–368. [\[CrossRef\]](#)
126. Mo, P.; Shi, M.; Yao, W.; Liu, J. Transfer Learning of Potential Energy Surfaces for Efficient Atomistic Modeling of Doping and Alloy. *IEEE Electron Device Lett.* **2020**, *41*, 633–636. [\[CrossRef\]](#)
127. Lin, H.; Huang, B.; Feng Liu, F. Atomistic Mechanism Underlying the Si (111)–(7 × 7) Surface Reconstruction Revealed by Artificial Neural-Network Potential. *Phys. Rev. Lett.* **2021**, *126*, 176101. [\[CrossRef\]](#)
128. Bürkle, M.; Perera, U.; Gimbert, F.; Nakamura, H.; Kawata, M.; Asai, Y. Deep-Learning Approach to First-Principles Transport Simulations. *Phys. Rev. Lett.* **2021**, *126*, 177701. [\[CrossRef\]](#)
129. Zhou, Y.; Chen, X.; Zhang, P.; Wang, J.; Wang, L.; Guo, H. AD-NEGF: An End-to-End Differentiable Quantum Transport Simulator for Sensitivity Analysis and Inverse Problems. *arXiv* **2022**, arXiv:2202.05098. [\[CrossRef\]](#)
130. Han, S.-C.; Hong, S.-M. Deep neural network for generation of the initial electrostatic potential profile. In Proceedings of the 2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Udine, Italy, 4–6 September 2019; pp. 1–4. [\[CrossRef\]](#)
131. Han, S.-C.; Choi, J.; Hong, S.-M. Acceleration of semiconductor device simulation with approximate solutions predicted by trained neural networks. *IEEE Trans. Electron Devices* **2021**, *68*, 5483–5489. [\[CrossRef\]](#)
132. Raju, S.S.; Wang, B.; Mehta, K.; Xiao, M.; Zhang, Y.; Wong, H.Y. Application of noise to avoid overfitting in TCAD augmented machine learning. In Proceedings of the 2020 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Kobe, Japan, 23 September–6 October 2020; pp. 351–354. [\[CrossRef\]](#)
133. Kashyap, M.; Wong, H.-Y. Prediction of FinFET current-voltage and capacitance-voltage curves using machine learning with autoencoder. *IEEE Electron Device Lett.* **2020**, *42*, 136–139.
134. Chandni, A.; Li, Y.; Sung, W.-L. Machine learning aided device simulation of work function fluctuation for multichannel gate-all-around silicon nanosheet MOSFETs. *IEEE Trans. Electron Devices* **2021**, *68*, 5490–5497. [\[CrossRef\]](#)
135. Carrillo-Nuñez, H.; Dimitrova, N.; Asenov, A.; Georgiev, V. Machine learning approach for predicting the effect of statistical variability in Si junctionless nanowire transistors. *IEEE Electron Device Lett.* **2019**, *40*, 1366–1369. [\[CrossRef\]](#)

136. Dhillon, H.; Mehta, K.; Xiao, M.; Wang, B.; Zhang, Y.; Wong, H.Y. TCAD-augmented machine learning with and without domain expertise. *IEEE Trans. Electron Devices* **2021**, *68*, 5498–5503. [[CrossRef](#)]
137. Ko, K.; Lee, J.K.; Kang, M.; Jeon, J.; Shin, H. Prediction of process variation effect for ultrascaled GAA vertical FET devices using a machine learning approach. *IEEE Trans. Electron Devices* **2019**, *66*, 4474–4477. [[CrossRef](#)]
138. Kyul, K.; Lee, J.K.; Shin, H. Variability-aware machine learning strategy for 3-D NAND flash memories. *IEEE Trans. Electron Devices* **2020**, *67*, 1575–1580. [[CrossRef](#)]
139. Wu, T.; Guo, J. Multiobjective Design of 2-D-Material-Based Field-Effect Transistors with Machine Learning Methods. *IEEE Trans. Electron Devices* **2021**, *68*, 5476–5482. [[CrossRef](#)]
140. Huo, Q.; Wu, Z.; Wang, X.; Huang, W.; Yao, J.; Bu, J.; Zhang, F.; Li, L.; Liu, M. Physics-based device-circuit cooptimization scheme for 7-nm technology node SRAM design and beyond. *IEEE Trans. Electron Devices* **2020**, *67*, 907–914. [[CrossRef](#)]
141. Huo, Q.; Wu, Z.; Huang, W.; Wang, X.; Tang, G.; Yao, J.; Liu, Y.; Zhao, X.; Zhang, F.; Li, L.; et al. A novel general compact model approach for 7-nm technology node circuit optimization from device perspective and beyond. *IEEE J. Electron Devices Soc.* **2020**, *8*, 295–301. [[CrossRef](#)]
142. Zhang, L.; Chan, M. Artificial neural network design for compact modeling of generic transistors. *J. Comput. Electron.* **2017**, *16*, 825–832. [[CrossRef](#)]
143. Wang, J.; Kim, Y.H.; Ryu, J.; Jeong, C.; Choi, W.; Kim, D. Artificial neural network-based compact modeling methodology for advanced transistors. *IEEE Trans. Electron Devices* **2021**, *68*, 1318–1325. [[CrossRef](#)]
144. Lu, D.D.; De, S.; Baig, M.A.; Qiu, B.-H.; Lee, Y.-J. Computationally efficient compact model for ferroelectric field-effect transistors to simulate the online training of neural networks. *Semicond. Sci. Technol.* **2020**, *35*, 095007. [[CrossRef](#)]
145. Yang, Q.; Qi, G.; Gan, W.; Wu, Z.; Yin, H.; Chen, T.; Hu, G.; Wan, J.; Yu, S.; Lu, Y. Transistor Compact Model Based on Multigradient Neural Network and Its Application in SPICE Circuit Simulations for Gate-All-Around Si Cold Source FETs. *IEEE Trans. Electron Devices* **2021**, *68*, 4181–4188. [[CrossRef](#)]
146. Levinson, H.J. *Principles of Lithography*, 4th ed.; SPIE Press: Bellingham, WA, USA, 2019.
147. Mulken, J.; Hanna, M.; Wei, H.; Vaenkatesan, V.; Megens, H.; Slotboom, D. Overlay and edge placement control strategies for the 7nm node using EUV and ArF lithography. In Proceedings of the Extreme Ultraviolet (EUV) Lithography VI, San Jose, CA, USA, 13 March 2015; SPIE: Bellingham, WA, USA, 2015; Volume 9422. [[CrossRef](#)]
148. Radamson, H.H.; Thylen, L. *Monolithic Nanoscale Photonics Electronics Integration in Silicon and other Group IV Elements*; Elsevier: Amsterdam, The Netherlands, 2014; pp. 121–150. ISBN 978-012-419-975-0.
149. Mulken, J.; Kubis, M.; Tel, W.; Maslow, M.; Ma, E.; Chou, K.; Liu, X.; Ren, W.; Hu, X.; Wang, F.; et al. Holistic approach for overlay and edge placement error to meet the 5nm technology node requirements. In *Metrology, Inspection, and Process Control for Microlithography XXXII*; SPIE: Bellingham, WA, USA, 2018; Volume 105851. [[CrossRef](#)]
150. Where Are My GAA-FETs? TSMC to Stay with FinFET for 3 nm. Available online: <https://www.anandtech.com/show/16041/where-are-my-gaafets-tsmc-to-stay-with-finfet-for-3nm> (accessed on 26 August 2020).
151. Charlie, W.; Anna, L.; Sam, S. Next generation patterning using EUV lithography. In *Extreme Ultraviolet (EUV) Lithography XI, 2020*; SPIE: San Jose, CA, USA, 2020; Volume 11323.
152. Sarohan, P.; Inwhan, L.; Sunyoung, K.; Jungnyung, L.; Chang-Moon, L. Extension of practical k1 limit in EUV lithography. In Proceedings of the Extreme Ultraviolet (EUV) Lithography VII. Extreme Ultraviolet (EUV) Lithography VII, San Jose, CA, USA, 18 March 2016; SPIE: Bellingham, WA, USA, 2016; Volume 9776.
153. Yeap, G.; Chen, X.; Yang, B.R.; Yang, F.C.; Leung, Y.K.; Lin, D.W.; Yu, K.F.; Chen, D.H.; Chang, C.Y.; Lin, S.S.; et al. 5 nm CMOS Production Technology Platform featuring full-fledged EUV, and High Mobility Channel FinFETs with densest 0.021  $\mu\text{m}^2$  SRAM cells for Mobile SoC and High Performance Computing Applications. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019. [[CrossRef](#)]
154. Lin, M.S.; Huang, T.C.; Tsai, C.C.; Tam, K.H.; Hsieh, K.C.H.; Chen, C.F.; Huang, W.H.; Hu, C.W.; Chen, Y.C.; Lee, F.; et al. A 7-nm 4-GHz Arm<sup>1</sup>-core-based CoWoS<sup>1</sup> chiplet design for high-performance computing. *IEEE J. Solid-State Circuits* **2020**, *55*, 956–966. [[CrossRef](#)]
155. Felix, N.M.; Attwood, D.T., Jr. EUV Lithography Perspective: From the beginning to HVM. In Proceedings of the Extreme Ultraviolet (EUV) Lithography XI, San Jose, CA, USA, 24–27 February 2020; SPIE: Bellingham, WA, USA, 2020.
156. Vikram, A.; Agarwal, V.; Agarwal, A. Lithography technology for advanced devices and introduction to integrated CAD analysis for hotspot detection. *IET Circuits Devices Syst.* **2017**, *11*, 1–101. [[CrossRef](#)]
157. Yaegashi, H. Pattern fidelity control in Multi-patterning towards 7 nm node. In Proceedings of the 2016 IEEE 16th International Conference on Nanotechnology (IEEE-NANO), Sendai, Japan, 22–25 August 2016; pp. 249–263.
158. Smilde, H.-J.H.; van Haren, R.J.F.; van Buël, W.; Driessen, L.H.D.; Dépré, J.; Beltman, J.; Dettoni, F.; Ducoté, J.; Dezaudier, C.; Blancquaert, Y. Target design optimization for overlay scatterometry to improve on-product overlay. In Proceedings of the Metrology, Inspection, and Process Control for Microlithography XXIX, San Jose, CA, USA, 19 March 2015; SPIE: Bellingham, WA, USA; Volume 9424, pp. 355–364. [[CrossRef](#)]
159. Calado, V.; Depre, J.; Massacrier, C.; Tarabrin, S.; van Haren, R.; Dettoni, F.; Bouyssou, R.; Dezaudier, C. Study of  $\mu\text{DBO}$  overlay target size reduction for application broadening. In Proceedings of the Metrology, Inspection, and Process Control for Microlithography XXXII, San Jose, CA, USA, 25 February–5 March 2018; SPIE: Bellingham, WA, USA, 13 March 2018; Volume 10585, p. 1058507. [[CrossRef](#)]

160. Leray, P.; Kandel, D.; Vasconi, M.; Salski, B. Overlay metrology for double patterning processes. In Proceedings of the Metrology, Inspection, and Process Control for Microlithography XXIII, San Jose, CA, USA, 22–27 February 2009; SPIE: Bellingham, WA, USA, 2009; Volume 7272. [\[CrossRef\]](#)
161. Ghani, T.; Armstrong, M.; Auth, C.; Bost, M.; Charvat, P.; Glass, G.; Hoffmann, T.; Johnson, K.; Kenyon, C.; Klaus, J.; et al. A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors. In Proceedings of the IEEE International Electron Devices Meeting, Washington, DC, USA, 8–10 December 2003; pp. 11.16.11–11.16.13. [\[CrossRef\]](#)
162. Wang, G.L.; Kolahdouz, M.; Luo, J. Growth of SiGe layers in source and drain regions for 10 nm node complementary metal-oxide semiconductor (CMOS). *J. Mater. Sci. Mater. Electron.* **2020**, *31*, 26–33. [\[CrossRef\]](#)
163. Mistry, K.; Chau, R.; Choi, C.-H.; Ding, G.; Fischer, K.; Ghani, T.; Grover, R.; Han, W.; Hanken, D.; Hattendorf, M.; et al. A 45 nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 10–12 December 2007; pp. 247–250. [\[CrossRef\]](#)
164. Packan, P.; Akbar, S.; Armstrong, M.; Bergstrom, D.; Brazier, M.; Deshpande, H.; Dev, K.; Ding, G.; Ghani, T.; Golonzka, O.; et al. High Performance 32 nm Logic Technology Featuring 2nd Generation High-k+ Metal Gate Transistors. In Proceedings of the 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009; pp. 1–4. [\[CrossRef\]](#)
165. Hartmann, J.M.; Bertin, F.; Rolland, G.; Laugier, F.; Semena, M. Selective epitaxial growth of Si and SiGe for metal oxide semiconductor transistors. *J. Cryst. Growth* **2003**, *259*, 419–427. [\[CrossRef\]](#)
166. Qin, C.L.; Yin, H.X.; Wang, G.L.; Hong, P.Z.; Ma, X.L.; Cui, H.S.; Lu, Y.H.; Meng, L.K.; Yin, H.Z.; Zhong, H.C.; et al. Study of sigma-shaped source/drain recesses for embedded-SiGe pMOSFETs. *Microelectron. Eng.* **2017**, *181*, 22–28. [\[CrossRef\]](#)
167. Kolahdouz, M.; Hällstedt, J.; Khatibi, A.; Östling, M.; Wise, R.; Riley, D.J.; Radamson, H. Comprehensive Evaluation and Study of Pattern Dependency Behavior in Selective Epitaxial Growth of B-Doped SiGe Layers. *IEEE Trans. Nanotechnol.* **2009**, *8*, 291. [\[CrossRef\]](#)
168. Hällstedt, J.; Kolahdouz, M.; Ghandi, R.; Wise, R.; Radamson, H.H. Pattern dependency in selective epitaxy of B-doped SiGe layers for advanced metal oxide semiconductor field effect transistors. *J. Appl. Phys.* **2008**, *103*, 054907. [\[CrossRef\]](#)
169. Xu, H.; Khazaka, R.; Zhang, J.; Zheng, Z.; Chen, Y.; Gong, X. 300 mm Wafer-scale In-situ CVD Growth Achieving  $5.1 \times 10^{-10} \Omega\text{-cm}^2$  P-Type Contact Resistivity: Record  $2.5 \times 10^{21} \text{ cm}^{-3}$  Active Doping and Demonstration on Highly-Scaled 3D Structures. In Proceedings of the 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 12–17 June 2022; pp. 367–368. [\[CrossRef\]](#)
170. Wang, G.; Luo, J.; Qin, C.; Liang, R.; Xu, Y.; Liu, J.; Ye, T. Integration of Highly Strained SiGe in Source and Drain with HK and MG for 22 nm Bulk PMOS Transistors. *Nanoscale Res. Lett.* **2017**, *12*, 123. [\[CrossRef\]](#)
171. Vescan, L.; Grimm, K.; Dieker, C. Facet investigation in selective epitaxial growth of Si and SiGe on (001) Si for optoelectronic devices. *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. Process. Meas. Phenom.* **1998**, *16*, 1549–1554. [\[CrossRef\]](#)
172. Dutartre, D.; Talbot, A. Facet propagation in Si and SiGe epitaxy or etching. *ECS Trans.* **2006**, *3*, 473–487. [\[CrossRef\]](#)
173. Barraud, S.; Lapras, V.; Samson, M.P.; Gaben, L.; Grenouillet, L.; Maffini-Alvaro, V.; Vinet, M. Vertically stacked-nanowires MOSFETs in a replacement metal gate process with inner spacer and SiGe source/drain. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016.
174. Wang, G.; Wang, G. SiGe S/D Integration and Device Verification. In *Investigation on SiGe Selective Epitaxy for Source and Drain Engineering in 22 nm CMOS Technology Node and beyond*; Springer Nature: Berlin/Heidelberg, Germany, 2019; pp. 49–92.
175. Nur, O.; Willander, M.; Radamson, H.H.; Sardela, M.R., Jr.; Hansson, G.V.; Petersson, C.S.; Maex, K. Strain characterization of  $\text{CoSi}_2/\text{n-Si}_{0.9}\text{Ge}_{0.1}/\text{p-Si}$  heterostructures. *Appl. Phys. Lett.* **1994**, *64*, 440. [\[CrossRef\]](#)
176. Hallstedt, J.; Blomqvist, M.; Persson, P.; Hultman, L.; Radamson, H.H. The effect of carbon and germanium on phase transformation of nickel on  $\text{Si}_{1-x}\text{Ge}_x$  epitaxial layers. *J. Appl. Phys.* **2004**, *95*, 2397. [\[CrossRef\]](#)
177. Nur, O.; Willander, M.; Hultman, L.; Radamson, H.H.; Hansson, G.V.; Sardela, M.R., Jr.; Greene, J.E.  $\text{CoSi}_2/\text{Si}_{1-x}\text{Ge}_x/\text{Si}(001)$  heterostructures formed through different reaction routes: Silicidation-induced strain relaxation, defect formation, and interlayer diffusion. *J. Appl. Phys.* **1995**, *78*, 7063. [\[CrossRef\]](#)
178. Hu, C.; Xu, P.; Fu, C.; Zhu, Z.; Gao, X.; Jamshidi, A.; Noroozi, M.; Radamson, H.; Wu, D.; Zhang, S.-L. Characterization of Ni(SiGe) films on epitaxial SiGe(100) formed by microwave annealing. *Appl. Phys. Lett.* **2021**, *101*, 092101. [\[CrossRef\]](#)
179. Kolahdouz, M.; Hällstedt, J.; Ostling, M.; Wise, R.; Radamson, H.H. Selective epitaxial growth with full control of pattern dependency behavior for pMOSFET structures. *J. Electrochem. Soc.* **2009**, *156*, 169. [\[CrossRef\]](#)
180. Mujumdar, S.; Maitra, K.; Datta, S. Layout-Dependent Strain Optimization for p-Channel Trigate Transistors. *IEEE Trans. Electron Devices* **2012**, *59*, 72–78. [\[CrossRef\]](#)
181. Menon, C.; Bentzen, C.A.; Radamson, H.H. Loading effect in SiGe layers grown by dichlorosilane- and silane-based epitaxy. *J. Appl. Phys.* **2001**, *90*, 4805. [\[CrossRef\]](#)
182. Liu, J.; Chew, H.; See, A.; Zhou, M.; Hsia, L. Loading effect of selective epitaxial growth of silicon germanium in submicrometer-scale Silicon (001) windows. *Electrochem. Solid-State Lett.* **2009**, *12*, H58–H59. [\[CrossRef\]](#)
183. Kolahdouz, M.; Salemi, A.; Moen, M.; Östling, M.; Radamson, H.H. Kinetic modeling of low temperature epitaxy growth of SiGe using disilane and digermane. *J. Electrochem. Soc.* **2012**, *159*, H478. [\[CrossRef\]](#)
184. Menon, C.; Lindgren, A.C.; Persson, P.; Hultman, L.; Radamson, H.H. Selective Epitaxy of  $\text{Si}_{1-x}\text{Ge}_x$  Layers for Complementary Metal Oxide Semiconductor Applications. *J. Electrochem. Soc.* **2003**, *150*, G253–G257. [\[CrossRef\]](#)

185. Loo, R.; Wang, G.; Souriau, L.; Lin, J.C.; Takeuchi, S.; Brammertz, G.; Caymax, M. Epitaxial Ge on standard STI patterned Si wafers: High quality virtual substrates for Ge pMOS and III/V nMOS. *ECS Trans.* **2009**, *25*, 335–350. [[CrossRef](#)]
186. Kolahdouz, M.; Maresca, L.; Ghandi, R.; Khatibi, A.; Radamson, H.H. Kinetic Model of SiGe Selective Epitaxial Growth using RPCVD Technique. *J. Electrochem. Soc.* **2011**, *158*, H457. [[CrossRef](#)]
187. De Boer, W.B.; Terpstra, D.; Dekker, R. Loading effects during low-temperature SEG of Si and SiGe. *MRS Online Proc. Libr.* **2011**, *533*, 315–320. [[CrossRef](#)]
188. Huang, Y.S.; Lu, F.L.; Tsou, Y.J.; Tsai, C.E.; Lin, C.Y.; Huang, C.H.; Liu, C.W. First vertically stacked GeSn nanowire pGAAFETs with  $I_{on} = 1850 \mu\text{A}/\mu\text{m}$  ( $V_{ov} = V_{ds} = -1\text{V}$ ) on Si by GeSn/Ge CVD epitaxial growth and optimum selective etching. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 37.5.1–37.5.4. [[CrossRef](#)]
189. Liu, C.W.; Huang, Y.S.; Lu, F.L.; Ye, H.Y. Vertically Stacked n Channel and p Channel Transistors. In *Electrochemical Society Meeting Abstracts*; The Electrochemical Society, Inc.: Pennington, NJ, USA, 2019; Volume 236, p. 1167. [[CrossRef](#)]
190. Liu, M.; Mertens, K.; Driesch, N.v.D.; Schlykow, V.; Grap, T.; Lentz, F.; Trellenkamp, S.; Hartmann, J.-M.; Knoch, J.; Buca, D.; et al. Vertical heterojunction Ge<sub>0.92</sub>Sn<sub>0.08</sub>/Ge gate-all-around nanowire pMOSFETs with NiGeSn contact. *Solid-State Electron.* **2020**, *168*, 107716. [[CrossRef](#)]
191. Liu, M.; Yang, D.; Shkurmanov, A.; Bae, J.H.; Schlykow, V.; Hartmann, J.-M.; Ikonic, Z.; Baerwolf, F.; Costina, I.; Mai, A.; et al. Epitaxial GeSn/Ge vertical nanowires for p-type field-effect transistors with enhanced performance. *ACS Appl. Nano Mater.* **2020**, *4*, 94–101. [[CrossRef](#)]
192. Tu, C.-T.; Huang, Y.-S.; Cheng, C.-Y.; Tsai, C.-E.; Chen, J.-Y.; Ye, H.-Y.; Lu, F.-L.; Liu, C.W. Uniform 4-stacked Ge<sub>0.9</sub>Sn<sub>0.1</sub> nanosheets using double Ge<sub>0.95</sub>Sn<sub>0.05</sub> caps by highly selective isotropic dry etch. *IEEE Trans. Electron Devices* **2021**, *68*, 2071–2076. [[CrossRef](#)]
193. Liu, X.; Hu, H.; Wang, M.; Miao, Y.; Han, G.; Wang, B. Design and theoretical calculation of novel GeSn fully-depleted n-tunneling FET with quantum confinement model for suppression on GIDL effect. *Superlattices Microstruct.* **2018**, *118*, 266–274. [[CrossRef](#)]
194. Liu, H.; Li, Y.; Cheng, X.; Zan, Y.; Lu, Y.; Wang, G.; Wang, W. Fabrication and selective wet etching of Si<sub>0.2</sub>Ge<sub>0.8</sub>/Ge multilayer for Si<sub>0.2</sub>Ge<sub>0.8</sub> channel gate-all-around MOSFETs. *Mater. Sci. Semicond. Process.* **2021**, *121*, 105397. [[CrossRef](#)]
195. AHikavy, A.Y.; Porret, C.; Mencarelli, M.; Loo, R.; Favia, P.; Ayyad, M.; Briggs, B.; Langer, R.; Horiguchi, N. Cutting-Edge Epitaxial Processes for Sub 3 Nm Technology Nodes: Application to Nanosheet Stacks and Epitaxial Wrap-Around Contacts. *ECS Trans.* **2021**, *104*, 139–146. [[CrossRef](#)]
196. Carter, R.J.; Sporer, R.; McArdle, T.J.; Mulfinger, G.R.; Holt, J.R.; Beasor, S.; Child, A.; Fronheiser, J.; Wahl, J.A.; Geisler, H.; et al. Extending Advanced CMOS Scaling with SiGe Channel Materials. *ECS Trans.* **2018**, *85*, 3–10. [[CrossRef](#)]
197. Li, C.; Lin, H.; Li, J.; Yin, X.; Zhang, Y.; Kong, Z.; Radamson, H.H. Growth and Selective Etch of Phosphorus-Doped Silicon/Silicon-Germanium Multilayers Structures for Vertical Transistors Application. *Nanoscale Res. Lett.* **2020**, *15*, 225. [[CrossRef](#)] [[PubMed](#)]
198. Rachidi, S.; Campo, A.; Loup, V.; Vizioz, C.; Hartmann, J.M.; Barnola, S.; Posseme, N. Isotropic dry etching of Si selectively to Si<sub>0.7</sub>Ge<sub>0.3</sub> for CMOS sub-10 nm applications. *J. Vac. Sci. Technol. A* **2020**, *38*, 033002. [[CrossRef](#)]
199. Miao, Y.H.; Hu, H.Y.; Li, X.; Song, J.J.; Xuan, R.X.; Zhang, H.M. Evaluation of threading dislocation density of strained Ge epitaxial layer by high resolution X-ray diffraction. *Chin. Phys. B* **2017**, *26*, 127309. [[CrossRef](#)]
200. Rachidi, S.; Loup, V.; Campo, A.; Hartmann, J.-M.; Posseme, N. Wet Alkaline Etching of Si Selectively to SiGe for sub 10 nm Gate All around Architectures. *ECS J. Solid State Sci. Technol.* **2021**, *10*, 014007. [[CrossRef](#)]
201. Durfee, C.; Kal, S.; Pancharatnam, S.; Bhuiyan, M.; Otto, I.V.; Flaugh, M.; Smith, J.; Chanemougame, D.; Alix, C.; Zhou, H.; et al. Highly Selective SiGe Dry Etch Process for the Enablement of Stacked Nanosheet Gate-All-Around Transistors. *ECS Trans.* **2021**, *104*, 217–227. [[CrossRef](#)]
202. Saito, S.; Sano, Y.; Yamada, T.; Hara, K.O.; Yamanaka, J.; Nakagawa, K.; Arimoto, K. Strain relaxation process and evolution of crystalline morphologies during the growths of SiGe on Si(110) by solid-source molecular beam epitaxy. *Mater. Sci. Semicond. Process.* **2020**, *113*, 105042. [[CrossRef](#)]
203. Barraud, S.; Previtali, B.; Lapras, V.; Vizioz, C.; Hartmann, J.M.; Martinie, S.; Lacord, J.; Cassé, M.; Dourthe, L.; Loup, V.; et al. Tunability of Parasitic Channel in Gate-All-Around Stacked Nanosheets. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 21.3.1–21.3.4. [[CrossRef](#)]
204. Barraud, S.; Previtali, B.; Vizioz, C.; Hartmann, J.M.; Sturm, J.; Lassarre, J.; Perrot, C.; Rodriguez, P.; Loup, V.; Magalhaes-Lucas, A.; et al. 7-Levels-Stacked Nanosheet GAA Transistors for High Performance Computing. In Proceedings of the 2020 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 16–19 June 2020. [[CrossRef](#)]
205. Lee, R.; Lee, J.; Lee, K.; Kim, S.; Ahn, H.; Kim, S.; Kim, H.M.; Kim, C.; Lee, J.H.; Kim, S.; et al. Vertically-Stacked Si<sub>0.2</sub>Ge<sub>0.8</sub> Nanosheet Tunnel FET With 70 mV/Dec Average Subthreshold Swing. *IEEE Electron Device Lett.* **2021**, *42*, 962–965. [[CrossRef](#)]
206. Zhang, J.; Frougier, J.; Greene, A.; Miao, X.; Yu, L.; Vega, R.; Montanini, P.; Durfee, C.; Gaul, A.; Pancharatnam, S.; et al. Full Bottom Dielectric Isolation to Enable Stacked Nanosheet Transistor for Low Power and High Performance Applications. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019; pp. 11.6.1–11.6.4. [[CrossRef](#)]
207. Reboh, S.; Coquand, R.; Barraud, S.; Loubet, N.; Bernier, N.; Audoit, G.; Rouviere, J.L.; Augendre, E.; Li, J.; Gaudiello, J.; et al. Strain, stress, and mechanical relaxation in fin-patterned Si/SiGe multilayers for sub-7 nm nanosheet gate-all-around device technology. *Appl. Phys. Lett.* **2018**, *112*, 051901. [[CrossRef](#)]

208. Reboh, S.; Coquand, R.; Loubet, N.; Bernier, N.; Augendre, E.; Chao, R.; Li, J.; Zhang, J.; Muthinti, R.; Boureau, V.; et al. Imaging, Modeling and Engineering of Strain in Gate-All-Around Nanosheet Transistors. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019; pp. 11.5.1–11.5.4. [[CrossRef](#)]
209. Zhou, L.; Zhang, Q.; Yang, H.; Ji, Z.; Zhang, Z.; Xu, R.; Yin, H.; Wang, W. Comparative study on the energy profile of NBTI-related defects in Si and ferroelectric p-FinFETs. In Proceedings of the 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 28 April–30 May 2020; pp. 1–6.
210. Mochizuki, S.; Bhuiyan, M.; Zhou, H.; Zhang, J.; Stuckert, E.; Li, J.; Zhao, K.; Wang, M.; Basker, V.; Loubet, N.; et al. Stacked Gate-All-Around Nanosheet pFET with Highly Compressive Strained Si<sub>1-x</sub>Ge<sub>x</sub> Channel. In Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 12–18 December 2020; pp. 2.3.1–2.3.4. [[CrossRef](#)]
211. Ray, D.; Meaney, F.; Galluccio, E. Doping considerations for finfet, gate-all-around, and nanosheet based devices. *ECS Trans.* **2020**, *97*, 63. [[CrossRef](#)]
212. Lee, K.; Ameen, M.S.; Rubin, L.M.; Roh, D.D.; Hong, R.; Reece, R.N.; Yoon, D. Damage control of ion implantation for advanced doping process by using in-situ temperature control. *Mater. Sci. Semicond. Process.* **2020**, *117*, 105164. [[CrossRef](#)]
213. Khaja, F.A. Contact Resistance Improvement for Advanced Logic by Integration of Epi, Implant and Anneal Innovations. *MRS Adv.* **2019**, *4*, 2559–2576. [[CrossRef](#)]
214. Qin, S. Ultrashallow Junction (USJ) Fabrication by Advanced Ion Implantation Processes. *IEEE Trans. Electron Devices* **2021**, *68*, 1855–1860. [[CrossRef](#)]
215. Baik, S.; Kwon, D.-J.; Kang, H.; Jang, J.E.; Jang, J.; Kim, Y.S.; Kwon, H.-J. Conformal and ultra-shallow junction formation achieved using a pulsed-laser annealing process integrated with a modified plasma assisted doping method. *IEEE Access* **2020**, *8*, 172166–172174. [[CrossRef](#)]
216. Kikuchi, Y.; Peter, A.; Pawlak, B.J.; De Keersgieter, A.; Eyben, P.; Horiguchi, N.; Mocuta, A. Solid-source doping by using phosphosilicate glass into p-type bulk Si (100) substrate: Role of the capping SiO<sub>2</sub> barrier. *J. Vac. Sci. Technol. B Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.* **2018**, *36*, 061205. [[CrossRef](#)]
217. Kikuchi, Y.; Chiarella, T.; De Roest, D.; Blanquart, T.; De Keersgieter, A.; Kenis, K.; Peter, A.; Ong, P.; Van Besien, E.; Tao, Z.; et al. Electrical characteristics of p-Type bulk Si fin field-effect transistor using solid-source doping with 1-nm phosphosilicate glass. *IEEE Electron Device Lett.* **2016**, *37*, 1084–1087. [[CrossRef](#)]
218. Margetis, J.; Kohen, D.; Porret, C.; Lima, L.; Khazaka, R.; Rengo, G.; Loo, R.; Tolle, J.; Demos, A. Epitaxial growth of Ga-doped SiGe for reduction of contact resistance in finFET source/drain materials. *ECS Trans.* **2019**, *93*, 7. [[CrossRef](#)]
219. Lee, K.; Baik, S.; Kang, J.; Shin, H.; Yoon, D.; Kim, S.; Moon, J.; Suh, D.-C.; Ko, D.-H. Quantitative analysis of effect of dopant interaction on microstructural, physical, and electrical properties in laser-annealed SiGe: B: Ga film. *Thin Solid Film.* **2022**, *748*, 139173. [[CrossRef](#)]
220. Everaert, J.-L.; Schaekers, M.; Yu, H.; Wang, L.-L.; Hikavy, A.; Date, L.; Borniquel, J.d.A.; Hollar, K.; Khaja, F.A.; Aderhold, W.; et al. Sub-10<sup>-9</sup> Ω·cm<sup>2</sup> contact resistivity on p-SiGe achieved by Ga doping and nanosecond laser. In Proceedings of the 2017 Symposium on VLSI Technology, Kyoto, Japan, 5–8 June 2017. [[CrossRef](#)]
221. Qin, C.; Yin, H.; Wang, G.; Zhang, Y.; Liu, J.; Zhang, Z.; Zhu, H.; Zhao, C.; Radamson, H. A novel method for source/drain ion implantation for 20 nm FinFETs and beyond. *J. Mater. Sci. Mater. Electron.* **2020**, *31*, 98–104. [[CrossRef](#)]
222. Liu, J.; Wang, G.; Li, J.; Kong, Z.; Radamson, H.H. Study of n-type doping in germanium by temperature based PF<sup>+</sup> implantation. *J. Mater. Sci. Mater. Electron.* **2020**, *31*, 161–166. [[CrossRef](#)]
223. Houssa, M.; Pantisano, L.; Ragnarsson, L.Å.; Degraeve, R.; Schram, T.; Pourtois, G.; De Gendt, S.; Groeseneken, G.; Heyns, M.M. Electrical properties of high-k gate dielectrics: Challenges, current issues, and possible solutions. *Mater. Sci. Eng. R* **2006**, *51*, 37–85. [[CrossRef](#)]
224. Xiong, W. Multigate MOSFET Technology. In *FinFETs and Other Multi-Gate Transistors*; Colinge, J.-P., Ed.; Springer: Berlin/Heidelberg, Germany, 2008; pp. 49–111. ISBN 978-0-387-71751-7.
225. Lujan, G.; Schram, T.; Pantisano, L.; Hooker, J.; Kubicek, S.; Rohr, E.; Schuhmacher, J.; Kilpela, O.; Sprey, H.; De Gendt, S.; et al. Impact of ALCVD and PVD Titanium Nitride Deposition on Metal Gate Capacitors. In Proceedings of the 32nd European Solid-State Device Research Conference, Firenze, Italy, 24–26 September 2002; pp. 583–586. [[CrossRef](#)]
226. Westlinder, J.; Schram, T.; Pantisano, L.; Cartier, E.; Kerber, A.; Lujan, G.S.; Olsson, J.; Groeseneken, G. On the thermal stability of atomic layer deposited TiN as gate electrode in MOS devices. *IEEE Electron Device Lett.* **2003**, *24*, P550–P552. [[CrossRef](#)]
227. Xiang, J.; Ding, Y.; Du, L.; Xu, C.; Li, T.; Wang, X.; Li, J.; Zhao, C. Investigation of N Type Metal TiAlC by Thermal Atomic Layer Deposition Using TiCl<sub>4</sub> and TEA as Precursors. *ECS J. Solid State Sci. Technol.* **2016**, *5*, P299–P303. [[CrossRef](#)]
228. Ragnarsson, L.Å.; Chew, S.A.; Dekkers, H.; Luque, M.T.; Parvais, B.; De Keersgieter, A.; Devriendt, K.; Van Ammel, A.; Schram, T.; Yoshida, N.; et al. Highly scalable bulk FinFET Devices with Multi-VT options by conductive metal gate stack tuning for the 10-nm node and beyond. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, USA, 9–12 June 2014; p. 1. [[CrossRef](#)]
229. Radamson, H.H.; Zhang, Y.; He, X.; Cui, H.; Li, J.; Xiang, J.; Liu, J.; Gu, S.; Wang, G. The challenges of advanced CMOS process from 2D to 3D. *Appl. Sci.* **2017**, *7*, 1047. [[CrossRef](#)]
230. Wang, G.; Xu, Q.; Yang, T.; Xiang, J.J.; Xu, J.; Gao, J.F.; Li, C.L.; Li, J.F.; Yan, J.; Chen, D.P.; et al. Application of atomic layer deposition tungsten (ALD W) as gate filling metal for 22 nm and beyond nodes CMOS technology. *ECS J. Solid State Sci. Technol.* **2014**, *3*, 82–85. [[CrossRef](#)]

231. Johansson, M.; Yousif, M.Y.A.; Lundgren, P.; Bengtsson, S.; Sundqvist, J.; Hårsta, A.; Radamson, H.H. HfO<sub>2</sub> gate dielectrics on strained-Si and strained-SiGe layers. *Semicond. Sci. Technol.* **2003**, *18*, 820. [[CrossRef](#)]
232. Wang, G.L.; Moeen, M.; Abedin, A.; Kolahdouz, M.; Luo, J.; Qin, C.L.; Zhu, H.L.; Yan, J.; Yin, H.Z.; Li, J.F.; et al. Optimization of SiGe selective epitaxy for source/drain engineering in 22 nm node complementary metal-oxide semiconductor (CMOS). *J. Appl. Phys.* **2013**, *114*, 123511. [[CrossRef](#)]
233. Hung, S. Multi-Vt Engineering and Gate Performance Control for Advanced FinFET Architecture. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017.
234. Yousif, M.Y.A.; Johansson, M.; Lundgren, P.; Bengtsson, S. HfO<sub>2</sub> for strained-Si and strained-SiGe MOSFETs. In Proceedings of the 33rd European Solid-State Device Research-ESSDERC'03, Estoril, Portugal, 16–18 September 2003; p. 255. [[CrossRef](#)]
235. Bao, R.; Zhou, H.; Wang, M.; Guo, D.; Haran, B.S.; Narayanan, V.; Divakaruni, R. Extendable and Manufacturable Volume-Less Multi-Vt Solution for 7nm Technology Node and beyond. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 648–651. [[CrossRef](#)]
236. Lee, K.; Frank, M.; Paruchuri, V.; Cartier, E.; Linder, B.; Bojarczuk, N.; Wang, X.; Rubino, J.; Steen, M.; Kozlowski, P.; et al. Poly-Si/AlN/HfSiO stack for ideal threshold voltage and mobility in sub-100 nm MOSFETs. In Proceedings of the 2006 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 13–15 June 2006; pp. 160–161. [[CrossRef](#)]
237. Xu, R.; Yao, J.; Xu, G.; Wei, Y.; Yin, H.; Zhang, Q.; Tian, G.; Wang, Y.; Yan, G.; Xiang, J.; et al. Experimental Investigation of Ultrathin Al<sub>2</sub>O<sub>3</sub> Ex-Situ Interfacial Doping Strategy on Laminated HKMG Stacks via ALD. *IEEE Trans. Electron Devices* **2022**, *69*, P1964–P1971. [[CrossRef](#)]
238. Zhang, Q.; Gu, J.; Xu, R.; Cao, L.; Li, J.; Wu, Z.; Wang, G.; Yao, J.; Zhang, Z.; Xiang, J.; et al. Optimization of Structure and Electrical Characteristics for Four-Layer Vertically-Stacked Horizontal Gate-All-Around Si Nanosheets Devices. *Nanomaterials* **2021**, *11*, 646. [[CrossRef](#)] [[PubMed](#)]
239. Colombeau, B. Processes and Materials Engineering Innovations for Advanced Logic Transistor Scaling. In Proceedings of the IEEE 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 13–15 December 2021.
240. Moraes, K.; Chan, P.W. New Processes and Materials for Future Logic Devices. In Proceedings of the Symposium on VLSI Technology and Circuits (VLSI), Kyoto, Japan, 13–19 June 2021; pp. 1–2.
241. Shamiryan, D.; Redolfi, A.; Boullart, W. Dry etching process for bulk finFET manufacturing. *Microelectron. Eng.* **2009**, *86*, 96–98. [[CrossRef](#)]
242. Miyashita, T.; Sun, S.; Mittal, S.; Kim, M.S.; Pal, A.; Sachid, A.; Pathak, K.; Cogorno, M.; Kim, N.S. Selective Fin Trimming after Dummy Gate Removal as the Local Fin Width Scaling Approach for N5 and Beyond. In Proceedings of the Symposium on VLSI Technology and Circuits (VLSI), San Francisco, CA, USA, 1–5 December 2018; pp. 13–19. [[CrossRef](#)]
243. Zhang, Q.; Yin, H.; Luo, J.; Yang, H.; Meng, L.; Li, Y.; Wu, Z.; Zhang, Y.; Zhang, Y.; Qin, C.; et al. FOI FinFET with Ultra-Low Parasitic Resistance Enabled by Fully Metallic Source and Drain Formation on Isolated Bulk-Fin. In Proceedings of the IEEE 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016. [[CrossRef](#)]
244. Zhang, Q.Z.; Tu, H.L.; Yin, H.X. Influence of the hard masks profiles on formation of nanometer Si scalloped fins arrays. *Microelectron. Eng.* **2018**, *198*, 48–54. [[CrossRef](#)]
245. Zhang, Z.H.; Gan, W.Z.; Li, J.J. Scallop-shaped p-type FinFETs with improved short-channel effects immunity and driving current. *Mater. Sci. Semicond. Process.* **2022**, *14*, 106337. [[CrossRef](#)]
246. Xu, B.; Wang, G.; Du, Y.; Miao, Y.; Wu, Y.; Kong, Z.; Su, J.; Li, B.; Yu, J.; Radamson, H.H. Investigation of the Integration of Strained Ge Channel with Si-Based FinFETs. *Nanomaterials* **2022**, *12*, 1403. [[CrossRef](#)]
247. Li, Y.L.; Zhao, F.; Chen, X.H. Four-Period Vertically Stacked SiGe/Si Channel FinFET Fabrication and Its Electrical Characteristics. *Nanomaterials* **2021**, *11*, 1689. [[CrossRef](#)] [[PubMed](#)]
248. Ishii, Y.; Scott-McCabe, R.; Yu, A. Anisotropic selective etching between SiGe and Si. *Jpn. J. Appl. Phys.* **2018**, *57*, 06JC04. [[CrossRef](#)]
249. Oniki, Y.; Altamirano-Sánchez, E.; Holsteyns, F. Selective Etches for Gate-All-Around (GAA) Device Integration: Opportunities and Challenges. *ECS Trans.* **2019**, *92*, 3–12. [[CrossRef](#)]
250. Holländer, B.; Buca, D.; Mantl, S. Wet chemical etching of Si, Si<sub>1-x</sub>Ge<sub>x</sub>, and Ge in HF:H<sub>2</sub>O<sub>2</sub>:CH<sub>3</sub>COOH. *J. Electrochem. Soc.* **2010**, *157*, 643–646. [[CrossRef](#)]
251. Hartmann, J.M.; Destefanis, V.; Rabill, G. HCl selective etching of SiGe versus Si in stacks grown on (1 1 0). *Semicond. Sci. Technol.* **2010**, *25*, 105009. [[CrossRef](#)]
252. Loubet, N.; Kal, S.; Alix, C. A Novel Dry Selective Etch of SiGe for the Enablement of High Performance Logic Stacked Gate-All-Around NanoSheet Devices. In Proceedings of the IEEE 2019 IEEE International Electron Devices Meeting (IEDM), Grenoble, France, 13–22 September 2019. [[CrossRef](#)]
253. Li, J.; Wang, W.; Li, Y.; Zhou, N.; Wang, G.; Kong, Z.; Fu, J.; Yin, X.; Li, C.; Wang, X.; et al. Study of selective isotropic etching Si<sub>1-x</sub>Ge<sub>x</sub> in process of nanowire transistors. *J. Mater. Sci. Mater. Electron.* **2020**, *31*, 134–143. [[CrossRef](#)]
254. Rawat, A.; Bhuwalka, K.; Matagne, P. Performance Trade-Off Scenarios for GAA Nanosheet FETs Considering Inner-spacers and Epi-induced Stress: Understanding & Mitigating Process Risks. In Proceedings of the IEEE 47th European Solid State Circuits Conference (ESSCIRC), Grenoble, France, 13–22 September 2021. [[CrossRef](#)]
255. Li, J.; Li, Y.; Zhou, N.; Xiong, W.; Wang, G.; Zhang, Q.; Du, A.; Gao, J.; Kong, Z.; Lin, H.; et al. Study of Silicon Nitride Inner Spacer Formation in Process of Gate-all-around Nano-transistors. *Nanomaterials* **2020**, *10*, 793. [[CrossRef](#)]

256. Xie, L.; Zhu, H.; Zhang, Y.; Ai, X.; Li, J.; Wang, G.; Du, A.; Kong, Z.; Wang, Q.; Lu, S.; et al. Investigation on Ge0.8Si0.2-Selective Atomic Layer Wet-Etching of Ge for Vertical Gate-All-Around Nanodevice. *Nanomaterials* **2021**, *11*, 1408. [[CrossRef](#)]
257. Le Thanh, V.; Bouchier, D.; Débarre, D. Fabrication of SiGe quantum dots on a Si (100) surface. *Phys. Rev. B* **1997**, *56*, 10505. [[CrossRef](#)]
258. Li, C.; Zhu, H.L.; Zhang, Y.K. Selective Digital Etching of Silicon–Germanium Using Nitric and Hydrofluoric Acids. *ACS Appl. Mater. Interfaces* **2020**, *42*, 48170–48178. [[CrossRef](#)]
259. Pargon, E.; Petit-Etienne, C.; Youssef, L.; Thomachot, G.; David, S. New route for selective etching in remote plasma source: Application to the fabrication of horizontal stacked Si nanowires for gate all around devices. *J. Vac. Sci. Technol. A* **2019**, *37*, 040601. [[CrossRef](#)]
260. Li, J.; Li, Y.; Zhou, N.; Wang, G.; Zhang, Q.; Du, A.; Zhang, Y.; Gao, J.; Kong, Z.; Lin, H.; et al. A Novel Dry Selective Isotropic Atomic Layer Etching of SiGe for Manufacturing Vertical Nanowire Array with Diameter Less than 20 nm. *Materials* **2020**, *13*, 771. [[CrossRef](#)] [[PubMed](#)]
261. Abdulagatov, A.; Sharma, V.; Murdzek, J. Thermal atomic layer etching of germanium-rich SiGe using an oxidation and “conversion-etch” mechanism. *J. Vac. Sci. Technol. A* **2021**, *39*, 022602. [[CrossRef](#)]
262. Shinoda, K.; Miyoshi, N.; Kobayashi, H. Self-limiting reactions of ammonium salt in CHF<sub>3</sub>/O<sub>2</sub> downstream plasma for thermal-cyclic atomic layer etching of silicon nitride. *J. Vac. Sci. Technol. A* **2019**, *37*, 051002. [[CrossRef](#)]
263. Abdulagatov, A.; George, S. Thermal atomic layer etching of silicon nitride using an oxidation and “conversion etch” mechanism. *J. Vac. Sci. Technol. A* **2020**, *38*, 022607. [[CrossRef](#)]
264. Miyoshi, N.; Shinoda, K.; Kobayashi, H. Atomic layer etching of Si<sub>3</sub>N<sub>4</sub> with high selectivity to SiO<sub>2</sub> and poly-Si. *J. Vac. Sci. Technol. A* **2021**, *39*, 052601. [[CrossRef](#)]
265. Gasvoda, R.J.; Zhang, Z.H.; Wang, S. Etch selectivity during plasma-assisted etching of SiO<sub>2</sub> and SiNx: Transitioning from reactive ion etching to atomic layer etching. *J. Vac. Sci. Technol. A* **2020**, *38*, 050803. [[CrossRef](#)]
266. Lee, Y.; George, S.M. Thermal atomic layer etching of HfO<sub>2</sub> using HF for fluorination and TiCl<sub>4</sub> for ligand-exchange. *J. Vac. Sci. Technol. A* **2018**, *36*, 061504. [[CrossRef](#)]
267. Lee, Y.; George, S.M. Thermal Atomic Layer Etching of Titanium Nitride Using Sequential, Self-Limiting Reactions: Oxidation to TiO<sub>2</sub> and Fluorination to Volatile TiF<sub>4</sub>. *Chem. Mater.* **2017**, *29*, 8202–8210. [[CrossRef](#)]
268. Johnson, N.R.; George, S.M. WO<sub>3</sub> and W Thermal Atomic Layer Etching Using “Conversion-Fluorination” and “Oxidation-Conversion-Fluorination” Mechanisms. *ACS Appl. Mater. Interfaces* **2017**, *9*, 34435–34447. [[CrossRef](#)]
269. Kim, D.S.; Kim, J.B.; Ahn, D.W.; Choe, J.H.; Kim, J.S.; Jung, E.S.; Pyo, S.G. Atomic layer etching applications in nano-semiconductor device fabrication. *Electron. Mater. Lett.* **2023**, *19*, 424–441. [[CrossRef](#)]
270. Yin, X.; Zhu, H.; Zhao, L.; Wang, G.; Li, C.; Huang, W.; Zhang, Y.; Jia, K.; Li, J.; Radamson, H.H. Study of isotropic and Si-selective quasi atomic layer etching of Si<sub>1-x</sub>Ge<sub>x</sub>. *ECS J. Solid State Sci. Technol.* **2020**, *9*, 034012. [[CrossRef](#)]
271. Xiao, Z.R.; Wang, Q.; Zhu, H.L.; Chen, Z.; Zhang, Y.K.; Li, J.J.; Zhou, N.; Gao, J.F.; Ai, X.Z.; Lu, S.S.; et al. Vertical C-shaped-channel nanosheet FETs featured with precise control of both channel-thickness and gate-length. *IEEE Electron Device Lett.* **2022**, *43*, 1183–1186. [[CrossRef](#)]
272. Lim, S.W. Toward the Surface Preparation of InGaAs for the Future CMOS Integration. *Solid State Phenom.* **2018**, *282*, 39–42. [[CrossRef](#)]
273. Ryckaert, J.; Na, M.H.; Weckx, P.; Jang, D.; Schuddinck, P.; Chehab, B.; Patli, S.; Sarkar, S.; Zografos, O.; Baert, R.; et al. Enabling Sub-5nm CMOS Technology Scaling Thinner and Taller! In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019; Volume 685. [[CrossRef](#)]
274. Kuhn, K.J. Considerations for Ultimate CMOS Scaling. *IEEE Trans. Electron Devices* **2012**, *59*, 1813–1828. [[CrossRef](#)]
275. Hussain, M.; Shamiryan, D.; Paraschiv, V.; Sano, K.; Reinhardt, K. Cleaning Challenges of High-κ/Metal Gate Structures. In *Handbook of Cleaning in Semiconductor Manufacturing*; Scrivener Publishing LLC: Salem, MA, USA, 2011; pp. 249–251. [[CrossRef](#)]
276. Huff, H.R.; Richter, C.A.; Green, M.L.; Lucovsky, G.; Hattori, T. *Ultrathin SiO<sub>2</sub> and High-K Materials for ULSI Gate Dielectrics*; Materials Research Society: Warrendale, PA, USA, 1999; Volume 567.
277. Mertens, H.; Ritzenthaler, R.; Arimura, H.; Franco, J.; Sebaai, F.; Hikavy, A.; Pawlak, B.J.; Machkaoutsan, V.; Devriendt, K.; Tsvetanova, D.; et al. Si-cap-free SiGe p-channel FinFETs and gate-all-around transistors in a replacement metal gate process: Interface trap density reduction and performance improvement by high-pressure deuterium anneal. In Proceedings of the 2015 Symposium on VLSI Technology (VLSI Technology), Kyoto, Japan, 16–18 June 2015; pp. T142–T143. [[CrossRef](#)]
278. Destefanis, V.; Hartmann, J.M.; Borel, S.; Bensahel, D. High pressure in situ HCl etching of Si<sub>1-x</sub>Ge<sub>x</sub> versus Si for advanced devices. *Semicond. Sci. Technol.* **2008**, *23*, 105019. [[CrossRef](#)]
279. Hållstedt, J.; Hellström, P.E.; Radamson, H.H. Sidewall transfer lithography for reliable fabrication of nanowires and decanometer MOSFETs. *Thin Solid Films* **2008**, *517*, 117. [[CrossRef](#)]
280. Chang, G.K.; Carns, T.K.; Rhee, S.S.; Wang, K.L. Selective etching of SiGe on SiGe/Si heterostructures. *J. Electrochem. Soc.* **1991**, *138*, 202–204. [[CrossRef](#)]
281. Carns, T.K.; Tanner, M.O.; Wang, K.L. Chemical Etching of Si<sub>1-x</sub>Ge<sub>x</sub> in Hf-H<sub>2</sub>O<sub>2</sub>-CH<sub>3</sub>COOH. *J. Electrochem. Soc.* **1995**, *142*, 1260–1266. [[CrossRef](#)]
282. Seidel, H.; Csepregi, L.; Heuberger, A.; Baumgartel, H. Anisotropic etching of crystalline silicon in alkaline solutions I. Orientation dependence and behavior of passivation layers. *J. Electrochem. Soc.* **1990**, *137*, 3612–3626. [[CrossRef](#)]

283. Wostyn, K.; Sebaai, F.; Rip, J.; Mertens, H.; Witters, L.; Loo, R.; Hikavy, A.Y.; Milenin, A.; Horiguchi, N.; Collaert, N.; et al. Selective etch of Si and SiGe for gate all-around device architecture. *ECS Trans.* **2015**, *69*, 147. [[CrossRef](#)]
284. Wang, F.; Shi, Y.; Liu, J.L.; Lu, Y.; Gu, S.L.; Zheng, Y.D. Highly selective chemical etching of Si vs.  $\text{Si}_{1-x}\text{Ge}_x$  using  $\text{NH}_4\text{OH}$  solution. *J. Electrochem. Soc.* **1997**, *144*, L37–L39. [[CrossRef](#)]
285. Fischer, A.C.; Belova, L.M.; Rikers, Y.G.; Malm, B.G.; Radamson, H.H.; Kolahdouz, M.; Gylfason, K.B.; Stemme, G.; Niklaus, F. 3D Free-Form Patterning of Silicon by Ion Implantation, Silicon Deposition, and Selective Silicon Etching. *Adv. Funct. Mater.* **2012**, *22*, 4004. [[CrossRef](#)]
286. Kil, Y.H.; Yang, J.H.; Kang, S.; Jeong, T.S.; Kim, T.S.; Shim, K.H. Selective Chemical Wet Etching of  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}$  Multilayer. *J. Semicond. Technol. Sci.* **2013**, *13*, 668–675. [[CrossRef](#)]
287. Loubet, N.; Hook, T.; Montanini, P.; Yeung, C.W.; Kanakasabapathy, S.; Guillom, M.; Yamashita, T.; Zhang, J.; Miao, X.; Wang, J.; et al. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. In Proceedings of the 2017 Symposium on VLSI technology, Kyoto, Japan, 5–8 June 2017; pp. T230–T231.
288. Xie, L.; Zhu, H.; Zhang, Y.; Ai, X.; Li, J.; Wang, G.; Liu, J.; Du, A.; Yang, H.; Yin, X.; et al. Demonstration of Germanium Vertical Gate-All-Around Field-Effect Transistors Featured by Self-Aligned High- $\kappa$  Metal Gates with Record High Performance. *ACS Nano* **2023**, *17*, 22259–22267. [[CrossRef](#)]
289. Komori, K.; Rip, J.; Yoshida, Y.; Wostyn, K.; Sebaai, F.; Liu, W.D.; Lee, Y.C.; Sekiguchi, R.; Mertens, H.; Hikavy, A.; et al. SiGe vs. Si Selective Wet Etching for Si Gate-All-Around. *Solid State Phenom.* **2018**, *282*, 107. [[CrossRef](#)]
290. Li, Y.; Zhu, H.; Kong, Z.; Zhang, Y.; Ai, X.; Wang, G.; Wang, Q.; Liu, Z.; Lu, S.; Xie, L.; et al. The Effect of Doping on the Digital Etching of Silicon-Selective Silicon–Germanium Using Nitric Acids. *Nanomaterials* **2021**, *11*, 1209. [[CrossRef](#)] [[PubMed](#)]
291. Xie, L.; Zhu, H.; Zhang, Y.; Ai, X.; Wang, G.; Li, J.; Du, A.; Kong, Z.; Yin, X.; Li, C.; et al. Strained  $\text{Si}_{0.2}\text{Ge}_{0.8}/\text{Ge}$  multilayer stacks epitaxially grown on a low-/high-temperature Ge buffer layer and selective wet-etching of germanium. *Nanomaterials* **2020**, *10*, 1715. [[CrossRef](#)] [[PubMed](#)]
292. Yoshimoto, K.; Stoykovich, M.P.; Cao, H.B.; de Pablo, J.J.; Nealey, P.F.; Drugan, W.J. A two-dimensional model of the deformation of photoresist structures using elastoplastic polymer properties. *J. Appl. Phys.* **2004**, *96*, 1857–1865. [[CrossRef](#)]
293. Tas, N.; Sonnenberg, T.; Jansen, H.; Legtenberg, R.; Elwenspoek, M. Stiction in surface micromachining. *J. Micromechanics Microengineering* **1996**, *6*, 385–397. [[CrossRef](#)]
294. Ogawa, Y. Cleaning Technology for Advanced Devices beyond 20 nm Node. *Solid State Phenom.* **2012**, *195*, 7–12. [[CrossRef](#)]
295. Koliopoulou, S.; Dimitrakis, P.; Goustouridis, D.; Normand, P.; Pearson, C.; Petty, M.C.; Radamson, H.; Tsoukalas, D. Metal nano-floating gate memory devices fabricated at low temperature. *Microelectron. Eng.* **2006**, *83*, 1563. [[CrossRef](#)]
296. Kim, G. Effect of Drying Liquid on Stiction of High Aspect Ratio Structures. *Solid State Phenom.* **2012**, *187*, 75. [[CrossRef](#)]
297. Koideetal, T. Nano-Structures Stiction Suppression by Molecular Structure Optimized Surface Energy Reduction Agent. *ECS Trans.* **2017**, *80*, 53. [[CrossRef](#)]
298. Sebaai, F.; Vereecke, G.; Xu, X.M.; Baudot, S.; Amemiya, F.; Komori, K.; Holsteys, F. Cleaning of High Aspect Ratio STI Structures for Advanced Logic Devices by Implementation of a Surface Modification Drying Technique. *Solid State Phenom.* **2018**, *282*, 190. [[CrossRef](#)]
299. Nogami, T. Overview of interconnect technology for 7 nm node and beyond—New materials and technologies to extend Cu and to enable alternative conductors (invited). In Proceedings of the 2019 Electron Devices Technology and Manufacturing Conference, Singapore, 12–15 March 2019; pp. 38–40. [[CrossRef](#)]
300. Croes, K.; Adelman, C.; Wilson, C.J.; Zahedmanesh, H.; Pedreira, O.V.; Wu, C.; Leśniewska, A.; Oprins, H.; Beyne, S.; Ciofi, I.; et al. Interconnect metals beyond copper: Reliability challenges and opportunities. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018. [[CrossRef](#)]
301. Christiansen, C.J.; Li, B.; Angyal, M.; Kane, T. Geometry, kinetics, and short length effects of electromigration in Mn doped Cu interconnects at the 32nm technology node. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, USA, 15–19 April 2012; pp. 5E.1.1–5E.1.4. [[CrossRef](#)]
302. Cao, L.; Ho, P.S.; Justison, P. Electromigration reliability of Mn-doped Cu interconnects for the 28 nm technology. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 14–18 April 2013; pp. EM.5.1–EM.5.4. [[CrossRef](#)]
303. Cao, L.; Zhang, L.; Ho, P.S.; Justison, P.; Hauschildt, M. Scaling Effects on Microstructure and Electromigration Reliability for Cu and Cu (Mn) Interconnects. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS), Waikoloa, HI, USA, 1–5 June 2014; pp. 5A.5.1–5A.5.5. [[CrossRef](#)]
304. Cao, F.; Wu, G.H.; Jiang, L.T.; Chen, G.Q. Application of Cu-C and Cu-V Alloys in Barrier-less Copper Metallization. *Vacuum* **2015**, *122*, 122–126. [[CrossRef](#)]
305. Hu, C.-K.; Ohm, J.; Gignac, L.M.; Breslin, C.M.; Mittal, S.; Bonilla, G.; Edelstein, D.; Rosenberg, R.; Choi, S.; An, J.J.; et al. Electromigration in Cu(Al) and Cu(Mn) Damascene Lines. *J. Appl. Phys.* **2012**, *111*, 093722. [[CrossRef](#)]
306. Bonilla, G.; Lanzillo, N.; Hu, C.-K.; Penny, C.-J.; Kumar, A. Interconnect scaling challenges, and opportunities to enable system-level performance beyond 30 nm pitch. In Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 12–18 December 2020; pp. 20.4.1–20.4.4. [[CrossRef](#)]

307. You, S.; Ren, H.; Naik, M.; Chen, L.; Chen, F.; Cervantes, C.L.; Xie, X.; Kashefzadeh, K. Selective Barrier for Cu Interconnect Extension in 3 nm Node and beyond. In Proceedings of the 2021 IEEE International Interconnect Technology Conference (IITC), Kyoto, Japan, 6–9 July 2021. [\[CrossRef\]](#)
308. Park, K.C.; Simka, H. Advanced interconnect challenges beyond 5nm and possible solutions. In Proceedings of the 2021 IEEE International Interconnect Technology Conference (IITC), Kyoto, Japan, 6–9 July 2021. [\[CrossRef\]](#)
309. Bhosale, P.; Lanzillo, N.; Motoyama, K.; Nogami, T.; Simon, A.; Huang, H.; Chen, K.; Mignot, Y.; Edelstein, D.; Natarajan, S.; et al. Dual Damascene BEOL Extendibility with Cu Reflow/Selective TaN and Co/Cu Composite. In Proceedings of the 2021 Symposium on VLSI Technology, Kyoto, Japan, 13–19 June 2021. ISSN 07431562; ISBN 9784863487802.
310. Gall, D. The search for the most conductive metal for narrow interconnect lines. *J. Appl. Phys.* **2020**, *127*, 050901. [\[CrossRef\]](#)
311. Gall, D.; Jog, A.; Zhou, T. Narrow interconnects: The most conductive metals. In Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 12 December 2020; pp. 32.3.1–32.3.4. [\[CrossRef\]](#)
312. Yoon, S.J.; Lee, S.; Lee, T.I.; Yoon, A.; Cho, B.J. Large grain ruthenium for alternative interconnects. *IEEE Electron Device Lett.* **2018**, *40*, 91–94. [\[CrossRef\]](#)
313. Nogami, T.; Gluschenkov, O.; Sulehria, Y.; Nguyen, S.; Huang, H.; Lanzillo, N.A.; DeSilva, A.; Mignot, Y.; Church, J.; Lee, J.; et al. Advanced BEOL Interconnects. In Proceedings of the 2020 IEEE International Interconnect Technology Conference (IITC), San Jose, CA, USA, 5–9 October 2020; pp. 1–3. [\[CrossRef\]](#)
314. Wan, D.; Paolillo, S.; Rassoul, N.; Kotowska, B.K.; Blanco, V.; Adelman, C.; Lazzarino, F.; Ercken, M.; Murdoch, G.; Bömmels, J.; et al. Subtractive Etch of Ruthenium for Sub-5nm Interconnect. In Proceedings of the IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018; pp. 10–12. [\[CrossRef\]](#)
315. Spurlin, T.A.; Rigsby, M.A.; Brogan, L.; Doubina, N.; Liu, Y.; Opocensky, E.; Zhou, J.; Reid, J. Cobalt electrofill for future generations of contacts and interconnects. In Proceedings of the China Semiconductor Technology International Conference, CSTIC 2019, Shanghai, China, 18–19 March 2019. [\[CrossRef\]](#)
316. Cheng, Y.L.; Huang, H.C.; Lee, C.Y.; Chen, G.S.; Fang, J.S. Comparison of Cu and Co Integration with Porous Low-k SiOCH Dielectrics. *Thin Solid Films* **2020**, *704*, 138010. [\[CrossRef\]](#)
317. Zheng, J.F.; Chen, P.; Baum, T.H.; Lieten, R.R.; Hunks, W.; Lippy, S.; Frye, A.; Li, W.; O'Neill, J.; Xu, J.; et al. Selective co growth on Cu for void-free via fill. In Proceedings of the IEEE International Interconnect Technology Conference and IEEE Materials for Advanced Metallization Conference (IITC/MAM), Grenoble, France, 18–21 May 2015; pp. 265–268. [\[CrossRef\]](#)
318. Van der Veen, M.H.; Vandersmissen, K.; Dictus, D.; Demuynck, S.; Liu, R.; Bin, X.; Nalla, P.; Lesniewska, A.; Hall, L.; Croes, K.; et al. Cobalt Bottom-Up Contact and Via Prefill enabling Advanced Logic and DRAM Technologies. In Proceedings of the IEEE International Interconnect Technology Conference and IEEE Materials for Advanced Metallization Conference (IITC/MAM), Grenoble, France, 18–21 May 2015; pp. 25–28. [\[CrossRef\]](#)
319. Jiang, Y.; Nalla, P.; Matsushita, Y.; Harm, G.; Wang, J.; Kolics, A.; Zhao, L.; Mountsier, T.; Besser, P.; Wu, H.J. Development of electroless Co via-prefill to enable advanced BEOL metallization and via resistance reduction. In Proceedings of the IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 23–26 May 2016; pp. 111–113. [\[CrossRef\]](#)
320. Pedreira, O.V.; Croes, K.; Zahedmanesh, H.; Vandersmissen, K.; Van Der Veen, M.H.; Gonzalez, V.V.; Dictus, D.; Zhao, L.; Kolies, A.; Tókei, Z. Electromigration and Thermal Storage Study of Barrierless Co Vias. In Proceedings of the IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018; pp. 48–50. [\[CrossRef\]](#)
321. Ciofi, I.; Roussel, P.J.; Baert, R.; Contino, A.; Gupta, A.; Croes, K.; Wilson, C.J.; Mocuta, D.; Tókei, Z. RC Benefits of Advanced Metallization Options. *IEEE Trans. Electron Devices* **2019**, *66*, 2339–2345. [\[CrossRef\]](#)
322. van der Veen, M.H.; Soethoudt, J.; Delabie, A.; Pedreira, O.V.; Gonzalez, V.V.; Lariviere, S.; Teugels, L.; Jourdan, N.; Decoster, S.; Struyf, H.; et al. Hybrid Metallization with Cu in sub 30nm Interconnects. In Proceedings of the 2020 IEEE International Interconnect Technology Conference (IITC), San Jose, CA, USA, 5–8 October 2020; pp. 16–18. [\[CrossRef\]](#)
323. van der Veen, M.H.; Pedreira, O.V.; Heylen, N.; Jourdan, N.; Lariviere, S.; Park, S.; Struyf, H.; Tókei, Z.; Lei, W.; Pethe, S.; et al. Exploring W-Cu hybrid dual damascene metallization for future nodes. In Proceedings of the IEEE International Interconnect Technology Conference (IITC), Kyoto, Japan, 6–9 July 2021. [\[CrossRef\]](#)
324. Soulié, J.P.; Tókei, Z.; Swerts, J.; Adelman, C. Aluminum intermetallics for advanced interconnect metallization: Thin film studies. In Proceedings of the 2021 IEEE International Interconnect Technology Conference (IITC), Kyoto, Japan, 6–9 July 2021. [\[CrossRef\]](#)
325. Koike, J.; Kuge, T.; Chen, L.; Yahagi, M. Intermetallic Compounds for Interconnect Metal beyond 3 nm Node. In Proceedings of the 2021 IEEE International Interconnect Technology Conference (IITC), Kyoto, Japan, 6–9 July 2021. [\[CrossRef\]](#)
326. Soulié, J.P.; Tókei, Z.; Swerts, J.; Adelman, C. Thickness scaling of NiAl thin films for alternative interconnect metallization. In Proceedings of the 2020 IEEE International Interconnect Technology Conference (IITC), San Jose, CA, USA, 5–8 October 2020; pp. 151–153. [\[CrossRef\]](#)
327. Chen, L.; Chen, Q.; Ando, D.; Sutou, Y.; Kubo, M.; Koike, J. Potential of low-resistivity Cu<sub>2</sub>Mg for highly scaled interconnects and its challenges. *Appl. Surf. Sci.* **2021**, *537*, 148035. [\[CrossRef\]](#)
328. Nigam, T.; Paliwoda, P.; Wang, X.; Kerber, A. Addressing reliability challenges in advance nodes for commercial and automotive application. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019. [\[CrossRef\]](#)

329. Ji, Z.; Chen, H.; Li, X. Design for reliability with the advanced integrated circuit (IC) technology, challenges and opportunities. *Sci. China Inf. Sci.* **2019**, *62*, 226401. [[CrossRef](#)]
330. Bury, E.; Kaczer, B.; Linten, D.; Witters, L.; Mertens, H.; Waldron, N.; Zhou, X.; Collaert, N.; Horiguchi, N.; Spessot, A.; et al. Self-heating in FinFET and GAA-NW using Si, Ge and III/V channels. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016. [[CrossRef](#)]
331. Wang, R.; Sun, Z.; Liu, Y.Y.; Yu, Z.; Wang, Z.; Jiang, X.; Huang, R. Understanding Hot Carrier Reliability in FinFET Technology from Trap-based Approach. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 11–16 December 2021. [[CrossRef](#)]
332. Ji, Z.; Zhang, X.; Franco, J.; Gao, R.; Duan, M.; Zhang, J.F.; Groeseneken, G. An investigation on border traps in III–V MOSFETs with an In<sub>0.53</sub>Ga<sub>0.47</sub>As channel. *IEEE Trans. Electron Devices* **2015**, *62*, 3633–3639. [[CrossRef](#)]
333. Gu, X.; Wan, Z.; Iyer, S.S. Charge-trap transistors for CMOS-only analog memory. *IEEE Trans. on Electron Devices* **2019**, *66*, 4183–4187. [[CrossRef](#)]
334. Chang, H.; Zhou, L.; Yang, H.; Ji, Z.; Liu, Q.; Simoen, E.; Yin, H.; Wang, W. Comparative Study on the Energy Distribution of Defects under HCD and NBTI in Short Channel p-FinFETs. In Proceedings of the 2021 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 21–25 March 2021. [[CrossRef](#)]
335. Franco, J.; Arimura, H.; de Marneffe, J.-F.; Wu, Z.; Vandooren, A.; Ragnarsson, L.-Å.; Litta, E.D.; Horiguchi, N.; Croes, K.; Linten, D.; et al. Low-temperature atomic and molecular hydrogen anneals for enhanced chemical SiO<sub>2</sub> IL quality in low thermal budget RMG stacks. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 11–16 December 2021. [[CrossRef](#)]
336. Zhou, L.; Liu, Q.; Yang, H.; Ji, Z.; Xu, H.; Wang, G.; Simoen, E.; Jiang, H.; Luo, Y.; Kong, Z.; et al. Alleviation of Negative-Bias Temperature Instability in Si p-FinFETs with ALD W Gate-Filling Metal by Annealing Process Optimization. *IEEE J. Electron Devices Soc.* **2021**, *9*, 229–235. [[CrossRef](#)]
337. Yakimets, D.; Eneman, G.; Schuddinck, P.; Bao, T.H.; Bardon, M.G.; Raghavan, P.; Veloso, A.; Collaert, N.; Mercha, A.; Verkest, D.; et al. Vertical GAAFETs for the Ultimate CMOS Scaling. *IEEE Trans. Electron Devices* **2015**, *16*, 1433–1439. [[CrossRef](#)]
338. Kilpi, O.P.; Svensson, J.; Wernersson, L.-E. Sub-100-nm gate-length scaling of vertical InAs/InGaAs nanowire MOSFETs on Si. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017. [[CrossRef](#)]
339. Du, Y.; Xu, B.; Wang, G.; Gu, S.; Li, B.; Kong, Z.; Yu, J.; Bai, G.; Li, J.; Wang, W. Growth of high-quality epitaxy of GaAs on Si with engineered Ge buffer using MOCVD. *J. Mater. Sci. Mater. Electron.* **2021**, *32*, 6425–6437. [[CrossRef](#)]
340. Aggerstam, T.; Lourduoss, S.; Radamson, H.H.; Sjodin, M.; Lorenzini, P.; Look, D.C. Investigation of the interface properties of MOVPE grown AlGaIn/GaN high electron mobility transistor (HEMT) structures on sapphire. *Thin Solid Film.* **2006**, *515*, 705. [[CrossRef](#)]
341. Waldron, N.; Merckling, C.; Teugels, L.; Ong, P.; Ibrahim, S.A.U.; Sebaai, F.; Pourghaderi, A.; Barla, K.; Collaert, N.; Thean, A.V.-Y. InGaAs Gate-All-Around Nanowire Devices on 300mm Si Substrates. *IEEE Electron Device Lett.* **2014**, *35*, 1097–1099. [[CrossRef](#)]
342. Seo, J.H.; Yoon, Y.J.; Kang, I.M. Design Optimization of Ge/GaAs-Based Heterojunction Gate-All-Around (GAA) Arch-Shaped Tunneling Field-Effect Transistor (A-TFET). *J. Nanosci. Nanotechnol.* **2018**, *18*, 6602–6605. [[CrossRef](#)] [[PubMed](#)]
343. Caimi, D.; Sousa, M.; Karg, S.; Zota, C.B. Scaled III–V-on-Si transistors for low-power logic and memory applications. *Jpn. J. Appl. Phys.* **2021**, *60*, SB0801. [[CrossRef](#)]
344. Ramesh, S.; Ivanov, T.; Putcha, V.; Alian, A.; Sibaja-Hernandez, A.; Rooyackers, R.; Camerotto, E.; Milenin, A.; Pinna, N.; El Kazzi, S.; et al. Record Performance Top-down In<sub>0.53</sub>Ga<sub>0.47</sub>As Vertical Nanowire FETs and Vertical Nanosheets. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017. [[CrossRef](#)]
345. Zhang, C.; Miao, X.; Chabak, K.D.; Li, X.L. A review of III–V planar nanowire arrays: Selective lateral VLS epitaxy and 3D transistors. *J. Phys. D Appl. Phys.* **2017**, *50*, 393001. [[CrossRef](#)]
346. Zhao, X.; Heidelberger, C.; Fitzgerald, E.A.; Lu, W.; Vardi, A.; del Alamo, J.A. Sub-10 nm Diameter InGaAs Vertical Nanowire MOSFETs. *IEEE Int. Electron Devices Meet. (IEDM)* **2017**, *65*, 3762–3768. [[CrossRef](#)]
347. Zhu, Z.Y.; Jönsson, A.; Liu, Y.-P.; Svensson, J.; Timm, R.; Wernersson, L.-E. Improved Electrostatics through Digital Etch Schemes in Vertical GaSb Nanowire p-MOSFETs on Si. *ACS Appl. Electron. Mater.* **2022**, *4*, 531–538. [[CrossRef](#)]
348. Du, Y.; Xu, B.Q.; Wang, G.L.; Miao, Y.H.; Li, B.; Kong, Z.Z.; Dong, Y.; Wang, W.W.; Radamson, H.H. Review of Highly Mismatched III–V Heteroepitaxy Growth on (001) Silicon. *Nanomaterials* **2022**, *12*, 741. [[CrossRef](#)]
349. Masato, T.; Satoshi, S.; Kouta, T.; Edward, C.; Kengo, N.; Sylvain, S.; Eiichi, K.; Akihiko, S.; Masaya, N. Hybrid nanowire photodetector integrated in a silicon photonic crystal. *ACS Photon* **2020**, *7*, 3467–3473. [[CrossRef](#)]
350. Borg, M.; Schmid, H.; Gooth, J.; Rossell, M.D.; Cutaia, D.; Knoedler, M.; Riel, H. High-Mobility GaSb Nanostructures Cointegrated with InAs on Si. *ACS Nano* **2017**, *11*, 2554–2560. [[CrossRef](#)] [[PubMed](#)]
351. Borg, M.; Gignac, L.; Bruley, J.; Malmgren, A.; Sant, S.; Convertino, C.; Schmid, H. Facet-selective group-III incorporation in InGaAs template assisted selective epitaxy. *Nanotechnology* **2019**, *30*, 084004. [[CrossRef](#)]
352. Wen, P.; Tiwari, P.; Mauthe, S.; Schmid, H.; Sousa, M.; Scherrer, M.; Moselund, K.E. Waveguide coupled III–V photodiodes monolithically integrated on Si. *Nat. Commun.* **2022**, *13*, 909. [[CrossRef](#)]
353. Miao, Y.; Wang, G.; Kong, Z.; Xu, B.; Zhao, X.; Luo, X.; Lin, H.; Dong, Y.; Lu, B.; Dong, L.; et al. Review of Si-Based GeSn CVD Growth and Optoelectronic Applications. *Nanomaterials* **2021**, *11*, 2556. [[CrossRef](#)] [[PubMed](#)]

354. Xu, S.; Han, K.; Huang, Y.C.; Lee, K.H.; Kang, Y.; Masudy-Panah, S.; Yeo, Y.C. Integrating GeSn photodiode on a 200 nm Ge-on-insulator photonics platform with Ge CMOS devices for advanced OEIC operating at 2  $\mu\text{m}$  band. *Opt. Express* **2019**, *27*, 26924–26939. [CrossRef]
355. Noroozi, M.; Hamawandi, B.; Toprak, M.S.; Radamson, H.H. Fabrication and thermoelectric characterization of GeSn nanowires. In Proceedings of the 2014 15th International Conference on Ultimate Integration on Silicon (ULIS), Stockholm, Sweden, 7–9 April 2014; pp. 125–128. [CrossRef]
356. Kurosawa, M.; Tojo, Y.; Matsumura, R.; Sadoh, T.; Miyao, M. Single-crystalline laterally graded GeSn on insulator structures by segregation controlled rapid-melting growth. *Appl. Phys. Lett.* **2012**, *101*, 091905. [CrossRef]
357. Wada, Y.; Inoue, K.; Hosoi, T.; Shimura, T.; Watanabe, H. Demonstration of mm long nearly intrinsic GeSn single-crystalline wires on quartz substrate fabricated by nucleation-controlled liquid-phase crystallization. *Jpn. J. Appl. Phys.* **2019**, *58*, SBBK01. [CrossRef]
358. Lei, D. Advanced Germanium-tin p-Channel Metal-Oxide-Semiconductor Field-Effect Transistors. 2017. Available online: <http://scholarbank.nus.edu.sg/handle/10635/138652> (accessed on 2017).
359. Lei, D.; Lee, K.H.; Bao, S.; Wang, W.; Masudy-Panah, S.; Tan, C.S.; Tok, E.S.; Gong, X.; Yeo, Y.-C. Thermal stability of germanium-tin (GeSn) fins. *Appl. Phys. Lett.* **2017**, *111*, 252103. [CrossRef]
360. Lei, D.; Lee, K.H.; Bao, S.; Wang, W.; Masudy-Panah, S.; Yadav, S.; Kumar, A.; Dong, Y.; Kang, Y.; Xu, S.; et al. The first GeSn FinFET on a novel GeSnOI substrate achieving lowest S of 79 mV/decade and record high  $G_{m, \text{int}}$  of 807  $\mu\text{S}/\mu\text{m}$  for GeSn P-FETs. In Proceedings of the 2017 Symposium on VLSI Technology, Kyoto, Japan, 5–8 June 2017; pp. T198–T199. [CrossRef]
361. Mondal, C.; Biswas, A. Performance analysis of nanoscale GeSn MOSFETs for mixed-mode circuit applications. *Mater. Sci. Semicond. Process.* **2017**, *66*, 109–116. [CrossRef]
362. Kang, Y.; Huang, Y.-C.; Lee, K.H.; Bao, S.; Wang, W.; Lei, D.; Masudy-Panah, S.; Dong, Y.; Wu, Y.; Xu, S.; et al. Strain relaxation of germanium-tin (GeSn) fins. *AIP Adv.* **2018**, *8*, 025111. [CrossRef]
363. Khiangte, K.R.; Rathore, J.S.; Schmidt, J.; Osten, H.J.; Laha, A.; Mahapatra, S. Wafer-scale all-epitaxial GeSn-on-insulator on Si (1 1 1) by molecular beam epitaxy. *J. Phys. D Appl. Phys.* **2018**, *51*, 32LT01. [CrossRef]
364. Wang, W.; Lei, D.; Huang, Y.-C.; Lee, K.H.; Loke, W.-K.; Dong, Y.; Xu, S.; Tan, C.S.; Wang, H.; Yoon, S.-F.; et al. High-performance GeSn photodetector and fin field-effect transistor (FinFET) on an advanced GeSn-on-insulator platform. *Opt. Express* **2018**, *26*, 10305–10314. [CrossRef]
365. Radamson, H.H.; Noroozi, M.; Jamshidi, A.; Thompson, P.E.; Östling, M. Strain engineering in GeSnSi materials. *ECS Trans.* **2013**, *50*, 527. [CrossRef]
366. Burt, D.; Joo, H.J.; Jung, Y.; Kim, Y.; Chen, M.; Huang, Y.C.; Nam, D. Strain-relaxed GeSn-on-insulator (GeSnOI) microdisks. *Opt. Express* **2021**, *29*, 28959–28967. [CrossRef] [PubMed]
367. Kong, Z.; Wang, G.; Liang, R.; Su, J.; Xun, M.; Miao, Y.; Gu, S.; Li, J.; Cao, K.; Lin, H.; et al. Growth and Strain Modulation of GeSn Alloys for Photonic and Electronic Applications. *Nanomaterials* **2022**, *12*, 981. [CrossRef]
368. Lei, D.; Han, K.; Lee, K.H.; Huang, Y.-C.; Wang, W.; Yadav, S.; Kumar, A.; Wu, Y.; Helio, H.; Xu, S.; et al. GeSn p-FinFETs with Sub-10 nm Fin Width Realized on a 200 nm GeSnOI Substrate: Lowest SS of 63 mV/decade, Highest  $G_{m, \text{int}}$  of 900  $\mu\text{S}/\mu\text{m}$ , and High-Field  $\mu_{\text{eff}}$  of 275  $\text{cm}^2/\text{V}\cdot\text{s}$ . In Proceedings of the 2018 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 18–22 June 2018; pp. 197–198. [CrossRef]
369. Lei, D.; Lee, K.H.; Huang, Y.-C.; Wang, W.; Masudy-Panah, S.; Yadav, S.; Kumar, A.; Dong, Y.; Kang, Y.; Xu, S.; et al. Germanium-Tin (GeSn) P-Channel Fin Field-Effect Transistor Fabricated on a Novel GeSn-on-Insulator Substrate. *IEEE Trans. Electron Devices* **2018**, *65*, 3754–3761. [CrossRef]
370. Han, K.; Wu, Y.; Huang, Y.C.; Xu, S.; Kumar, A.; Kong, E.; Kang, Y.; Zhang, J.; Wang, C.; Xu, H.; et al. First Demonstration of Complementary FinFETs and Tunneling FinFETs Co-Integrated on a 200 nm GeSnOI Substrate: A Pathway towards Future Hybrid Nano-electronics Systems. In Proceedings of the 2019 Symposium on VLSI Technology, Kyoto, Japan, 9–14 June 2019; pp. T182–T183. [CrossRef]
371. Kang, Y.; Han, K.; Kong, E.Y.-J.; Lei, D.; Xu, S.; Wu, Y.; Huang, Y.-C.; Gong, X. The First GeSn Gate-All-Around Nanowire P-FET on the GeSnOI Substrate with Channel Length of 20 nm and Subthreshold Swing of 74 mV/decade. In Proceedings of the 2019 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, Taiwan, 22–25 April 2019; pp. 1–2. [CrossRef]
372. Xu, S.; Huang, Y.C.; Lei, D.; Masudy-Panah, S.; Gong, X.; Yeo, Y.C. Toward Monolithic Optoelectronic Integration of GeSn Photodiode and FinFET on GeSnOI Platform. In Proceedings of the 2019 IEEE 16th International Conference on Group IV Photonics (GFP), Singapore, 28–30 August 2019; pp. 1–2. [CrossRef]
373. Kang, Y.; Xu, S.; Han, K.; Kong, E.Y.-J.; Song, Z.; Luo, S.; Kumar, A.; Wang, C.; Fan, W.; Liang, G.; et al. Ge<sub>0.95</sub>Sn<sub>0.05</sub> gate-all-around p-channel metal-oxide-semiconductor field-effect transistors with Sub-3 nm nanowire width. *Nano Lett.* **2021**, *21*, 5555–5563. [CrossRef] [PubMed]
374. Lin, G.; Cui, P.; Wang, T.; Hickey, R.; Zhang, J.; Zhao, H.; Kolodzey, J.; Zeng, Y. Fabrication of germanium tin microstructures through inductively coupled plasma dry etching. *IEEE Trans. Nanotechnol.* **2021**, *20*, 846–851. [CrossRef]
375. Joo, H.-J.; Kim, Y.; Burt, D.; Jung, Y.; Zhang, L.; Chen, M.; Parluhutan, S.J.; Kang, D.-H.; Lee, C.; Assali, S.; et al. 1D photonic crystal direct bandgap GeSn-on-insulator laser. *Appl. Phys. Lett.* **2021**, *119*, 201101. [CrossRef]

376. Bjelajac, A.; Gromovyi, M.; Sakat, E.; Wang, B.; Patriarche, G.; Pauc, N.; Calvo, V.; Boucaud, P.; Boeuf, F.; Chelnokov, A.; et al. Up to 300 K lasing with GeSn-On-Insulator microdisk resonators. *Opt. Express* **2022**, *30*, 3954–3961. [[CrossRef](#)]
377. Paul, J.; Mondal, C.; Biswas, A. Subthreshold modeling of nanoscale germanium-tin (GeSn)-on-insulator MOSFETs including quantum effects. *Mater. Sci. Semicond. Process.* **2019**, *94*, 128–135. [[CrossRef](#)]
378. Atabaki, A.H.; Moazeni, S.; Pavanello, F.; Gevorgyan, H.; Notaros, J.; Alloatti, L.; Wade, M.T.; Sun, C.; Kruger, S.A.; Meng, H.; et al. Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip. *Nature* **2018**, *556*, 349–354. [[CrossRef](#)]
379. Timurdogan, E.; Su, Z.; Shiue, R.-J.; Byrd, M.J.; Poulton, C.V.; Jabon, K.; DeRose, C.; Moss, B.R.; Hosseini, E.S.; Duzevik, I.; et al. 400G Silicon Photonics Integrated Circuit Transceiver Chipsets for CPO, OBO, and Pluggable Modules. In Proceedings of the 2020 Optical Fiber Communications Conference and Exhibition (OFC), San Diego, CA, USA, 8–12 March 2020; pp. 1–3. [[CrossRef](#)]
380. Chaisakul, P.; Marris-Morini, D.; Frigerio, J.; Chrastina, D.; Rouified, M.-S.; Cecchi, S.; Crozat, P.; Isella, G.; Vivien, L. Integrated germanium optical interconnects on silicon substrates. *Nat. Photonics* **2014**, *8*, 482–488. [[CrossRef](#)]
381. Xu, B.; Wang, G.; Du, Y.; Miao, Y.; Li, B.; Zhao, X.; Lin, H.; Yu, J.; Su, J.; Dong, Y.; et al. Monolithic Integration of O-Band InAs Quantum Dot Lasers with Engineered GaAs Virtual Substrate Based on Silicon. *Nanomaterials* **2022**, *12*, 2704. [[CrossRef](#)] [[PubMed](#)]
382. Du, Y.; Wei, W.; Xu, B.; Wang, G.; Li, B.; Miao, Y.; Zhao, X.; Kong, Z.; Lin, H.; Yu, J.; et al. Reduced Dislocation of GaAs Layer Grown on Ge-Buffered Si (001) Substrate Using Dislocation Filter Layers for an O-Band InAs/GaAs Quantum Dot Narrow-Ridge Laser. *Micromachines* **2022**, *13*, 1579. [[CrossRef](#)] [[PubMed](#)]
383. Zhao, X.; Moeen, M.; Toprak, M.S.; Wang, G.; Luo, J.; Ke, X.; Li, Z.; Liu, D.; Wang, W.; Zhao, C.; et al. Design impact on the performance of Ge PIN photodetectors. *J. Mater. Sci. Mater. Electron.* **2020**, *31*, 18–25. [[CrossRef](#)]
384. Zhao, X.; Wang, G.; Lin, H.; Du, Y.; Luo, X.; Kong, Z.; Su, J.; Li, J.; Xiong, W.; Miao, Y.; et al. High Performance p-i-n Photodetectors on Ge-on-Insulator Platform. *Nanomaterials* **2021**, *11*, 1125. [[CrossRef](#)] [[PubMed](#)]
385. Novack, A.; Streshinsky, M.; Ding, R.; Liu, Y.; Lim, A.E.J.; Lo, G.Q.; Hochberg, M. Progress in silicon platforms for integrated optics. *Nanophotonics* **2014**, *3*, 205–214. [[CrossRef](#)]
386. Won, R.; Paniccia, M. Integrating silicon photonics. *Nat. Photonics* **2010**, *4*, 498–499. [[CrossRef](#)]
387. Kolahdouz, M.; Xu, B.; Nasiri, A.F.; Fathollahzadeh, M.; Manian, M.; Aghababa, H.; Wu, Y.; Radamson, H.H. Carbon-Related Materials: Graphene and Carbon Nanotubes in Semiconductor Applications and Design. *Micromachines* **2022**, *13*, 1257. [[CrossRef](#)]
388. Celano, U. *Electrical Atomic Force Microscopy for Nanoelectronics*; Springer: Berlin/Heidelberg, Germany, 2019. [[CrossRef](#)]
389. Hui, F.; Lanza, M. Scanning probe microscopy for advanced nanoelectronics. *Nat. Electron.* **2019**, *2*, 221–229. [[CrossRef](#)]
390. Lorusso, G.F.; Horiguchi, N.; Bömmels, J.; Wilson, C.J.; den Bosch, G.V.; Kar, G.S.; Ikota, M. Electron beam metrology for advanced technology nodes. *Jpn. J. Appl. Phys.* **2019**, *58*, SD0801. [[CrossRef](#)]
391. Ma, E.; Chou, K.; Ebert, M.; Liu, X.; Ren, W.; Hu, X.; Maassen, M.; Yin, W.; Chen, A.; Wang, F.; et al. Multiple beam inspection (MBI) for 7nm node and beyond: Technologies and applications Frontiers of Characterization and Metrology for Nanoelectronics. In Proceedings of the Metrology, Inspection, and Process Control for Microlithography XXXIII, San Jose, CA, USA, 26 March 2019; Volume 109591R. [[CrossRef](#)]
392. De Goede, M.; Johlin, E.; Sciacca, B.; Boughorbel, F.; Garnett, E.C. 3D multi-energy deconvolution electron microscopy. *Nanoscale* **2017**, *9*, 684–689. [[CrossRef](#)]
393. Warner, J.H.; Rümmele, M.H.; Gemming, T.; Bühner, B.; Briggs, G.A.D. Direct Imaging of Rotational Stacking Faults in Few Layer Graphene. *Nano Lett.* **2009**, *9*, 102–106. [[CrossRef](#)]
394. Radamson, H.H. Graphene. In *Springer Handbook of Electronic and Photonic Materials*; Springer: Berlin/Heidelberg, Germany, 2017. [[CrossRef](#)]
395. Hofmann, T.; Dobisz, E.; Ocko, B.M. Grazing incident small angle X-ray scattering: A metrology to probe nanopatterned surfaces. *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct.* **2009**, *27*, 3238. [[CrossRef](#)]
396. Radamson, H.H.; Hallstedt, J. Application of high-resolution X-ray diffraction for detecting defects in SiGe(C) materials. *J. Phys. Condes. Matter* **2005**, *17*, S2315–S2322. [[CrossRef](#)]
397. Hansson, G.V.; Radamsson, H.H.; Ni, W.X. Strain and relaxation in Si-MBE structures studied by reciprocal space mapping using high-resolution X-ray-diffraction. *J. Mater. Sci. Mater. Electron.* **1995**, *6*, 292–297. [[CrossRef](#)]
398. Radamson, H.H.; Sardela, M.R., Jr.; Hultman, L.; Hansson, G.V. Characterization of highly Sb-doped Si using high-resolution X-ray diffraction and transmission electron microscopy. *J. Appl. Phys.* **1994**, *76*, 763. [[CrossRef](#)]
399. Zhang, J.; Perrin, M.L.; Barba, L. High-speed identification of suspended carbon nanotubes using Raman spectroscopy and deep learning. *Microsyst. Nanoeng.* **2022**, *8*, 19. [[CrossRef](#)]
400. Orji, N.G.; Badaroglu, M.; Barnes, B.M.; Beitia, C.; Bunday, B.D.; Celano, U.; Vladar, A.E. Metrology for the next generation of semiconductor devices. *Nat. Electron.* **2018**, *1*, 532–547. [[CrossRef](#)] [[PubMed](#)]
401. Vaid, A.; Elia, A.; Iddawela, G.; Bozdog, C.; Sendelbach, M.; Kang, B.C.; Wolfling, S. Hybrid metrology: From the lab into the fab. *J. Micro/Nanolithography MEMS MOEMS* **2014**, *13*, 041410. [[CrossRef](#)]
402. Celano, U.; Favia, P.; Drijbooms, C.; Dixon-Luinenburg, O.; Richard, O.; Bender, H.; Vancoille, E.; Paredis, K.; Loo, R.; Schulze, A.; et al. Individual Device Analysis Using Hybrid TEM-Scalpel SSRM Metrology. *Front. Charact. Metrol. Nanoelectron.* **2017**, *11*, 122–126.
403. Radamson, H.H.; Hallen, A.; Sychugov, I.; Azarov, A. *Analytical Methods and Instruments for Micro- and Nanomaterials*; Springer: Berlin/Heidelberg, Germany, 2023. [[CrossRef](#)]

404. *The International Roadmap for Devices and Systems*; Edition Metrology; IEEE: Piscataway, NJ, USA, 2020.
405. Neisser, M.; Orji, N.G.; Levinson, H.J.; Celano, U.; Moyne, J.; Mashiro, S.; Wilcox, D.; Libman, S. How Lithography and Metrology Are Enabling Yield in the Next Generation of Semiconductor Patterning. *Computer* **2024**, *57*, 51–58. [[CrossRef](#)]
406. Grahn, J.V.; Fosshaug, H.; Jargelius, M.; Jönsson, P.; Linder, M.; Malm, B.G.; Mohadjeri, B.; Pejnefors, J.; Radamson, H.H.; Sandén, M.; et al. A low-complexity 62-GHz fT SiGe heterojunction bipolar transistor process using differential epitaxy and in situ phosphorus-doped poly-Si emitter at very low thermal budget. *Solid-State Electron.* **2000**, *44*, 549–554. [[CrossRef](#)]
407. Radamson, H.H.; Sardela, M.R., Jr.; Nur, O.; Willander, M.; Sernelius, B.E.; Ni, W.X.; Hansson, G.V. Electron mobility enhancement in Si using doubly  $\delta$ -doped layers. *Appl. Phys. Lett.* **1994**, *64*, 1842–1844. [[CrossRef](#)]

**Disclaimer/Publisher’s Note:** The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.