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# A Single-Output-Filter Double Dual Ćuk Converter

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**Abstract:** This study introduces an innovative version of a recently studied converter. A Double Dual Ćuk Converter was recently studied with advantages like the possibility of designing it for achieving a low-input current ripple. The proposed converter, called the Improved Double Dual Ćuk Converter, maintains the advantages of the former one, and it is characterized by requiring one less capacitor and inductor than its predecessor. This allows addressing the challenge of optimizing the topology to reduce component count without compromising the operation; this work proposes an efficient design methodology based on theoretical analysis and experimental validation. Results demonstrate that the improved topology not only retains the advantages of the previous version, including high efficiency and robustness, but also enhances power density by reducing the number of components. These advancements open new possibilities for applications requiring compact and efficient power converters, such as renewable energy systems, electric vehicles, and portable power supply systems. This work underscores the importance of continuous innovation in power converter design and lays the groundwork for future research aimed at optimizing converter topologies. A detailed discussion of the operating principles and modeling of the converter is provided. Furthermore, simulation outcomes highlighting differences in steady-state duration, output voltage, input current ripple, and operational efficiency are shared. The results from an experimental test bench are also presented to corroborate the efficacy of the improved converter.

**Keywords:** DC–DC power converter; PWM; double dual Ćuk converter



**Citation:** Robles-Campos, H.R.; Rosas-Caro, J.C.; Valderrabano-Gonzalez, A.; Posada, J. A Single-Output-Filter Double Dual Ćuk Converter. *Electronics* **2022**, *13*, 1838. https://doi.org/10.3390/electronics13101838

Academic Editor: Ibrahim Mohd Alsofyani

Received: 28 March 2024
Revised: 27 April 2024
Accepted: 6 May 2024
Published: 9 May 2024



## 1. Introduction

The contemporary era is marked by the escalating challenges of climate change, which threaten global ecosystems, economies, and societies. The increasing concentration of greenhouse gases in the Earth's atmosphere, primarily due to the combustion of fossil fuels for energy production, has led to unprecedented global warming and climate instability. These environmental challenges have catalyzed the urgent need for sustainable solutions to mitigate the impact of human activities on the planet. Among these solutions, renewable energy emerges as a pivotal alternative, offering a viable pathway to reduce carbon emissions and promote environmental sustainability [1–4].

Particularly in the realm of electric power generation, the transition to renewable energy sources such as solar, wind, hydro, and biomass is critical. This shift not only addresses the pressing environmental concerns but also aligns with the global imperative to secure a sustainable, reliable, and clean energy future. The role of advanced power conversion technologies, including innovative converter topologies, is instrumental in harnessing the full potential of renewable energy sources, therefore contributing to the global effort to combat climate change. In particular, fuel-cell stacks and photovoltaic panels need DC–DC power electronics converters to further boost the voltage of the output port of renewable energy sources. In addition, to efficiently operate, photovoltaic power plants require the design and implementation of real-time algorithms to track and impose the maximum power point of operation [5–9].

Solar power stands out as a viable option for electricity generation, offering a substantial method for minimizing carbon emissions [10,11]. It boasts the advantage of being non-polluting, emitting no greenhouse gases, and being generally benign to the environment. However, the primary drawback associated with renewable energy sources lies in their variable nature, leading to fluctuations in output voltage. To address this variability, a DC–DC power converter that ensures a stable and uniform output voltage is recommended [10].

Therefore, DC–DC power converters are essential for managing and maintaining the output voltage at a predetermined reference level [12–14]. Moreover, it is advantageous to develop a power converter that ensures a steady and minimal input current ripple. This importance stems from the fact that significant input current ripple can lead to elevated RMS current values, causing additional losses and increased temperatures, therefore accelerating the aging of the renewable energy source. In the traditional Ćuk power converter, energy transfer occurs through capacitive means, offering the advantage of integrating a capacitance voltage-divider feature. The Ćuk converter is the focus of several recent research investigations [15–18]. As presented in [15], the topology offers the possibility to handle bidirectional power flow using a voltage-doubler concept. Nonetheless, as compared to the traditional Ćuk, its disadvantage is an increased number of components. In the study presented in [16], the Ćuk converter was compared against the so-called Sheppard–Taylor power converter. To do so, the characteristics of the number of components, voltage gain, and stress over the semiconductors were taken into account. According to the results presented, the selection of either the Ćuk or the Sheppard–Taylor power converter will depend on the specific requirements and trade-offs regarding its application. The findings revealed that both converters exhibited similar behaviors and presented mathematical models of similar complexity. Another investigation presented in [17], the Ćuk converter was compared against the so-called Mahafzah converter that utilizes a coupling capacitor with lower rated voltage. According to the results obtained, the Mahafzah power converter reduces the magnitude of semiconductor currents compared to the traditional Ćuk converter. Although the Mahafzah converter requires the same number of elements as the Ćuk converter, the coupling capacitor provides an advantage to the Mahafzah converter, featuring a small rated voltage. A new proposal presenting a three-switch single-phase Z-source inverter based on a Ćuk converter has been investigated in [18]. The presented topology features buck and boost capabilities, as well as dual grounding. Although the findings are relevant, the proposed topology requires more inductors and capacitors than conventional single-phase Z-source inverters, generating more system losses.

One of the most recent contributions in the study of the Ćuk converter and derived topologies was recently introduced in [19], named an interleaved type of boost converter. Due to its architecture, it may be classified as part of the family of double dual converters [7,20], a kind of converter in which a power structure is repeated twice, one of them in the backward direction of the first one. The converter introduced in [19], called here a Double Dual Ćuk Converter (DDCC), is shown in Figure 1, and with some rearrangements in Figure 2. In the study in [19], it has been shown that the DDCC produces a low current ripple at the input port, which is a desirable feature. It can actually be designed to have a zero current ripple at the input port for a particular operating condition. The DDCC has several advantages. Nevertheless, it requires a setup of two switches, two diodes, four inductors, and four capacitors, as illustrated in Figure 2. This study proposes the design of a modified double dual Ćuk converter, preliminarily presented in [21] and shown in Figure 3. It can be named the Improved Double Dual Ćuk Converter (IDDCC). Compared to the DDCC, the IDDCC boasts several improvements: (i) it utilizes fewer reactive components (merely three inductors and three capacitors), (ii) it maintains the ratio among the output over the input voltage (voltage gain), (iii) it also maintains the low current ripple at the input port, and (iv) it preserves efficiency. Moreover, it presents opportunities for reduction in both size and cost. Nonetheless, the IDDCC still features some disadvantages as well, those are: (i) the input voltage reference is different from the output voltage reference, this

could cause issues in some applications, and (ii) it can be considered a complex circuit, especially when compared to simpler topologies such as the traditional Ćuk [7]. This manuscript is structured as follows: The operational principles and design of the IDDCC converter are detailed in Section 2. Section 3 elaborates on the simulation framework and performance evaluation. Section 4 presents the experimental assessment. Conclusions are drawn in Section 5.

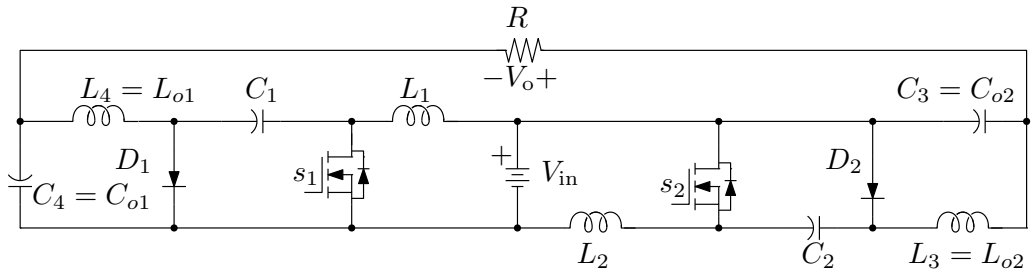


**Figure 1.** The double dual Ćuk converter studied in [12].

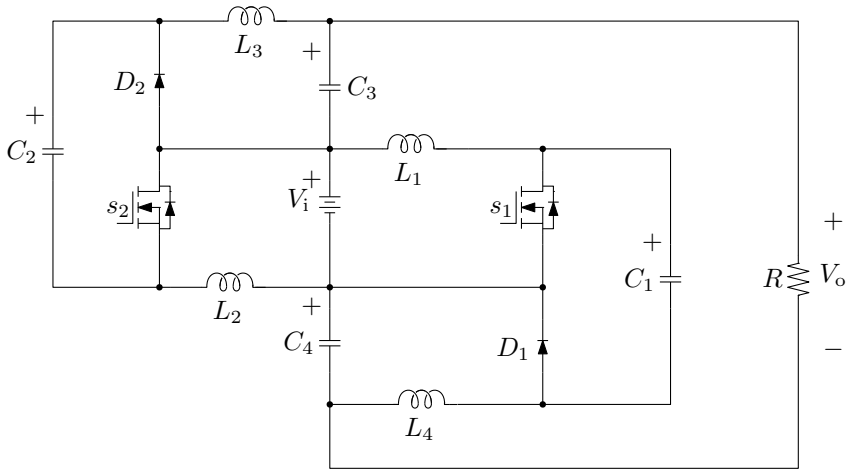


**Figure 2.** The double dual Ćuk converter studied in [12], with some rearrangements.

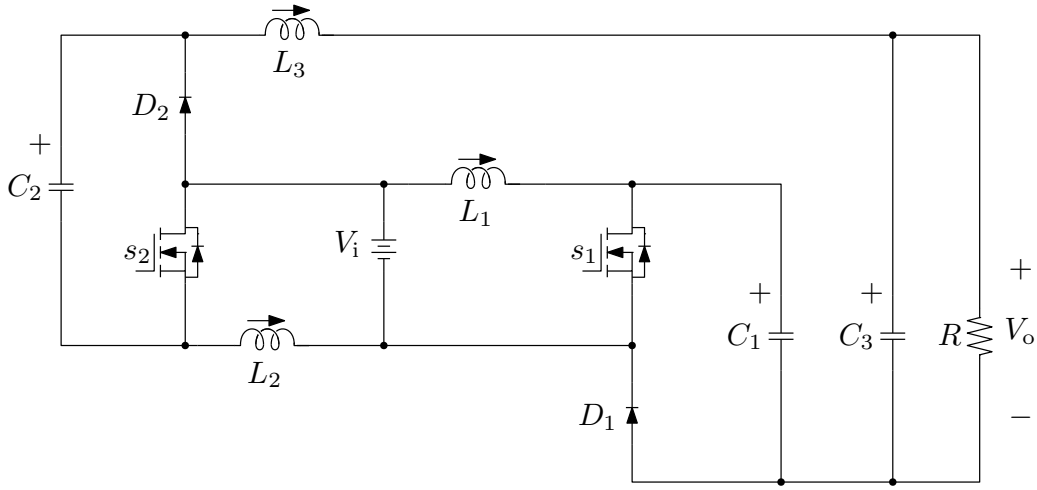


**Figure 3.** The proposed converter topology.

## 2. The Proposed Improved Double Dual Ćuk Converter

The suggested configuration incorporates three inductors, $L_l$ to $L_3$, along with three capacitors, $C_l$ to $C_3$. It also features the switching actions of transistors $s_1$ and $s_2$, which operate in a complementary manner. During operation in the Continuous Conduction

Mode (CCM), an examination of the switching states reveals two potential equivalent circuit diagrams, as depicted in Figures 4 and 5.

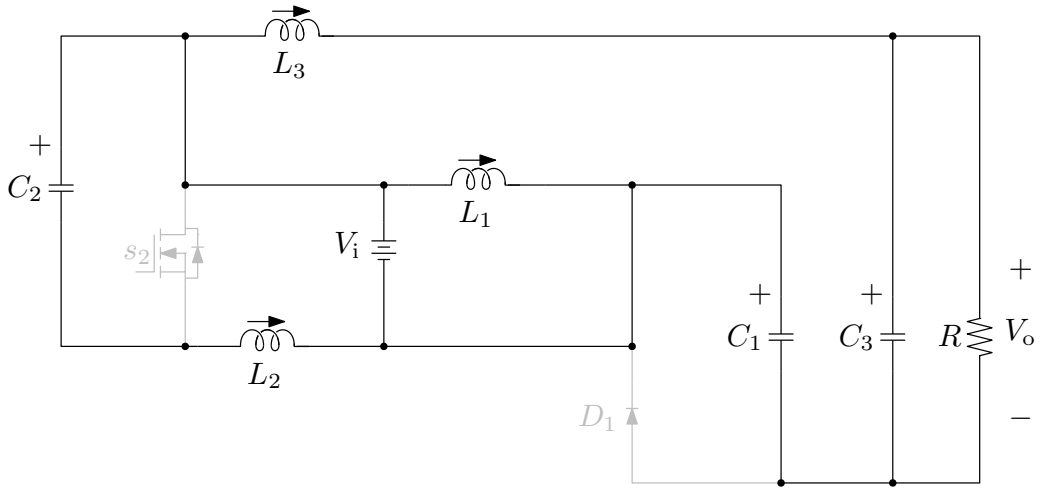


**Figure 4.** Equivalent circuit of state 1.

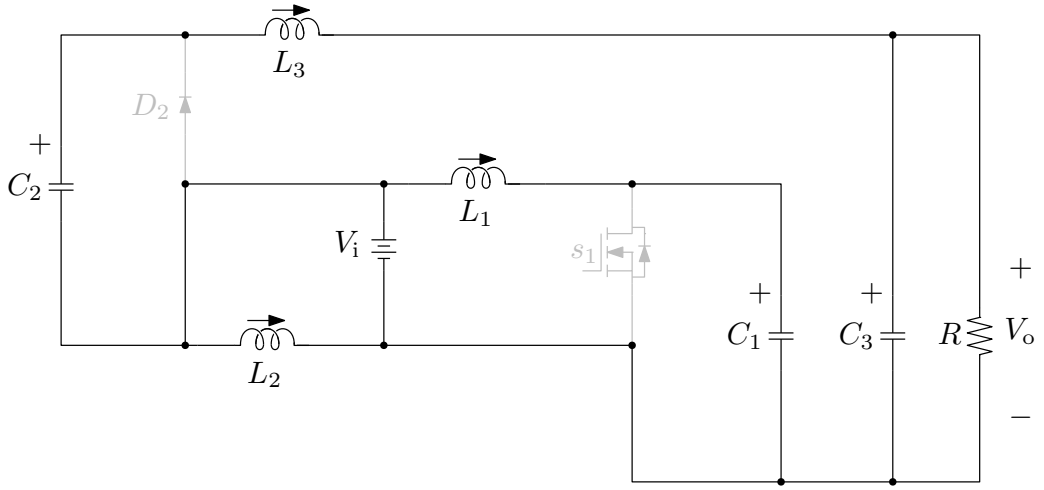


**Figure 5.** Equivalent circuit of state 2.

### *2.1. Converter Mathematical Model*

To derive the mathematical representation of the IDDCC power converter, an analysis of the circuits illustrated in Figures 4 and 5 is required.

Employing the conventional averaging method facilitates the acquisition of the proposed converter's mathematical model. The mean voltage across each of the inductors $L_l$, $L_2$, and $L_3$ over a single switching cycle can be expressed through Equations (1)–(3).

$$L_1 \frac{di_{L_1}}{dt} = d(V_i) + (1-d)(V_i - v_{C_1}) \quad (1)$$

$$L_2 \frac{di_{L_2}}{dt} = d(V_i - v_{C_2}) + (1-d)(V_i) \quad (2)$$

$$L_3 \frac{di_{L_3}}{dt} = d(V_i + v_{C_1} - v_{C_3}) + \ldots \quad (3)$$
$$\ldots + (1-d)(V_i + v_{C_2} - v_{C_3}).$$

Here, $v_{C_1}$, $v_{C_2}$, and $v_{C_3}$ denote the voltage across each capacitor, respectively. In a similar manner, $i_{L_1}$, $i_{L_2}$, and $i_{L_3}$ indicate the current passing through each inductor. It is important to note that the initial term in each of Formula (1)–(3) {a voltage or sum of

voltages times the duty ratio $d$} reflects the inductor voltage when the switch $s_1$ is in the closed position (while $s_2$ is in the open position). On the other hand, the subsequent term in each formula (a voltage or sum of voltages times $(1-d)$) depicts the inductor voltages when the main switch $s_1$ is open while $s_2$ is closed.

The average methodology is similarly applied to determine the current traversing each capacitor, enabling the computation of the mean current across capacitors $C_1$ to $C_3$, delineated by Equations (4)–(6). It is noteworthy that $i_o$ symbolizes the output current, which is determined by the formula ($i_o = V_o/R$).

$$C_1 \frac{dv_{C_1}}{dt} = d(-i_{L_3}) + (1-d)(i_{L_1}) \tag{4}$$

$$C_2 \frac{dv_{C_2}}{dt} = d(i_{L_2}) + (1-d)(-i_{L_3}) \tag{5}$$

$$C_3 \frac{dv_{C_3}}{dt} = d(i_{L_3} - i_o) + (1-d)(i_{L_3} - i_o) \tag{6}$$

The collective set of Equations (1) through (6) forms the average dynamic model for the IDDCC power converter. By undertaking further mathematical manipulations, Equations (1)–(6) are condensed and reformulated into Equations (7)–(12).

$$L_1 \frac{di_{L_1}}{dt} = V_i - (1-d)v_{C_1}, \tag{7}$$

$$L_2 \frac{di_{L_2}}{dt} = V_i - (d)v_{C_2}, \tag{8}$$

$$L_3 \frac{di_{L_3}}{dt} = V_i + d(v_{C_1} - v_{C_2}) + v_{C_2} - v_{C_3}, \tag{9}$$

$$C_1 \frac{dv_{C_1}}{dt} = (1-d)i_{L_1} - di_{L_3}, \tag{10}$$

$$C_2 \frac{dv_{C_2}}{dt} = di_{L_2} - (1-d)i_{L_3}, \tag{11}$$

$$C_3 \frac{dv_{C_3}}{dt} = i_{L_3} - i_o. \tag{12}$$

This average dynamic representation assumes that the IDDCC power converter functions within the continuous conduction mode.

### *2.2. DC Components and Equilibrium Operating Conditions of State Equations*

Within the dynamic model of the IDDCC power converter, as outlined by Equations (7)–(12), the point of equilibrium operation can be deduced. This is achieved by applying the small ripple approximation [22–24], characterized by variables presented in lowercase within Equations (7)–(12), signaling their variable nature. The small ripple approximation assumes minimal changes in state variables throughout a single switching cycle, achievable through careful choice of switching frequency ($f_{sw}$) inversely related to the switching period ($T_{sw}$), as well as the capacitance and inductance of capacitors and inductors. At a steady state, the rate of change of state variables drops to zero. Therefore, analyzing Equations (7)–(12) under the small ripple approximation allows for the identification of the converter's equilibrium state. Notice, the duty cycle variable $d$ becomes now represented by $D$. The voltage across capacitors C1 and C2, as deduced from Equations (7) and (8), is specified as follows:

$$V_{C_1} = \frac{1}{1-D} V_i, \tag{13}$$

$$V_{C_2} = \frac{1}{D} V_i. \tag{14}$$

Subsequently, the output voltage, equal to $V_{C_3}$, can be derived from Equation (9) in the manner described below:

$$V_o = V_i + D(V_{C_1} - V_{C_2}) + V_{C_2},$$
$$V_o = V_i + D\left(\frac{1}{1-D}V_i - \frac{1}{D}V_i\right) + \frac{1}{D}V_i. \quad (15)$$
$$V_o = \left(1 + \frac{D}{1-D} + -1 + \frac{1}{D}\right)V_i,$$
$$V_o = \left(\frac{D}{1-D} + \frac{1}{D}\right)V_i. \quad (16)$$

Ultimately, the equation representing the voltage gain of the IDDCC power converter is derived as follows (17),

$$V_o = \left(\frac{D^2 - D + 1}{D(1-D)}\right)V_i. \quad (17)$$

### 2.3. Voltage-Gain Behavior

As shown in Equation (17), the proposed converter features a quadratic-like voltage gain. To assess the voltage-gain equation of the proposed converter, a figure indicating its behavior is depicted in Figure 6. As can be observed, the minimum gain is obtained when the duty cycle $D = 0.5$. As a matter of fact, if the reader picks a duty cycle $D = 0.5$, then the IDDCC is expected to boost 3 times the input voltage $V_i$.

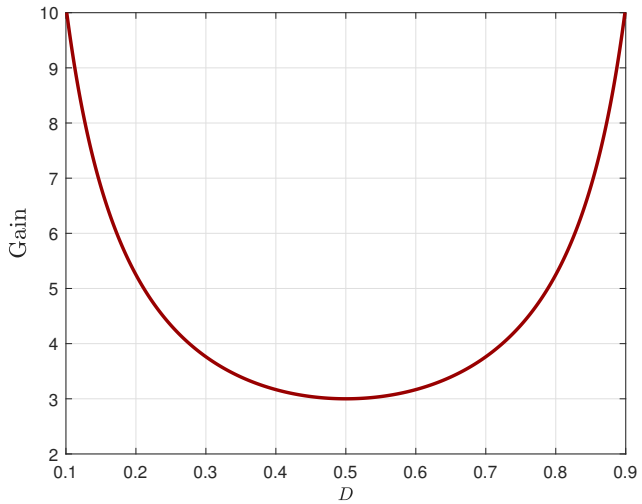


**Figure 6.** IDDCC voltage-gain behavior.

Likewise, through a series of mathematical adjustments, the current passing through each inductor is calculated from Equations (10)–(12) in the following manner.

$$I_{L_3} = I_o. \quad (18)$$
$$I_{L_1} = \frac{D}{1-D}I_o. \quad (19)$$
$$I_{L_2} = \frac{1-D}{D}I_o. \quad (20)$$

### 2.4. Components Selection

The sizing of the reactive components within the IDDCC converter follows the conventional methodology outlined in [22], based on design criteria such as the permissible maximum current ripple in the inductors and the allowable maximum voltage ripple in the

capacitors. Utilizing the equivalent circuits depicted in Figures 4 and 5, inductors $L_1$ and $L_2$ are selected using the equation provided in (21) and (22).

$$L_1 = \frac{V_i}{2\Delta i_{L_1}} DT_{sw}. \tag{21}$$

$$L_2 = \frac{V_i}{2\Delta i_{L_2}} (1-D)T_{sw}. \tag{22}$$

where $\Delta i_{L_1}$ and $\Delta i_{L_2}$ represent the maximum permissible current ripple through inductors $L_1$ and $L_2$, respectively. This can be determined as a fraction of their steady DC current (for example, 10% of their DC current at nominal power). The derivation of Equation (21) is straightforward since inductor $L_1$ links to the input voltage source with transistor $s_1$ in the closed position, and similarly, inductor $L_2$ connects when transistor $s_2$ is closed, please refer to Equation (22). As for $L_3$, it is noted to be connected to the voltage $V_i + V_{C_1} - V_{C_3}$ when transistor $s_1$ is engaged (refer to Figures 4 and 5). Consequently, the value for $L_3$ can be determined using Equation (25).

$$L_3 = \left(V_i + V_{C_1} - V_{C_3}\right) \frac{DT_{sw}}{2\Delta i_{L_3}}, \tag{23}$$

$$L_3 = V_i \left( \frac{1}{1-D} + 1 - \{ \frac{D}{1-D} + \frac{1}{D} \} \right) \frac{DT_{sw}}{2\Delta i_{L_3}}, \tag{24}$$

$$L_3 = V_i \left( \frac{D - 2D^2 - 1}{D(1-D)} \right) \frac{DT_{sw}}{2\Delta i_{L_3}}. \tag{25}$$

where $\Delta i_{L_3}$ denotes the maximum permissible current ripple passing through $L_3$.

Regarding the capacitors, based on the equivalent circuits shown in Figures 4 and 5, the selection of capacitance values for $C_1$ and $C_2$ can be guided by the equations labeled as (25) and (26).

$$C_1 = \frac{I_o}{2\Delta v_{C_1}} DT_{sw}. \tag{26}$$

$$C_2 = \frac{I_o}{2\Delta v_{C_2}} DT_{sw}. \tag{27}$$

where $\Delta v_{C_1}$ and $\Delta v_{C_2}$ represent the highest permissible voltage ripple in capacitors $C_1$ and $C_2$, respectively; akin to the approach for current ripple case in inductors, the allowable voltage ripple can be expressed as a proportion of their DC voltage (such as 0.1% of their DC voltage at nominal power). Since $C_3$ is part of a second-order filter, its current flow remains continuous, mirroring the behavior seen either on the buck or the Ćuk converters. Consequently, the capacitance for $C_3$ can be calculated using Equation (28),

$$C_3 = \frac{\Delta i_{L3} T_{sw}}{8\Delta v_{C_3}}, \tag{28}$$

where $\Delta v_{C_3}$ indicates the maximum permissible switching ripple in the voltage across the capacitor $C_3$, which, in this instance, is the same as the ripple observed in the output port.

## 3. Comparative Evaluation

In this section, an evaluative comparison is conducted between the DDCC and the newly proposed IDDCC power converters. Four principal characteristics are examined and confirmed: (i) time to reach a steady state, (ii) output voltage level, (iii) ripple in input current, and (iv) overall system efficiency.

### 3.1. Considerations

For this analysis, each power converter is energized with an input voltage $V_i$ = 30 V, and both the DDCC and the IDDCC power converters provide power to a resistive load of the same value equal to 81 Ω. This setup results in an electrical power consumption of 100 W ($I_o$ = 1.11 A). The switching frequency was selected as $F_{sw}$ = 40 kHz. The input current ripple is determined to be 0.34 A, which accounts for around 10% of the DC current. In this study, the passive components, inductors, and capacitors are considered using the non-commercial value of components based on the exact ripple equation solutions; however, these values closely align with those of available commercial components. `Matlab-Simscape Simulink` [25], a well-established software platform, is employed for the simulations. A comparative performance evaluation of the DDCC and the IDDCC power converters is presented by utilizing and detailing the same electric components and same properties as well. The reader is referred to Tables 1–3, where the complete list of electric elements and their properties are listed.

**Table 1.** Nominal design parameters both power converters.

| Parameter | Identifier | Value | Unit |
|---|---|---|---|
| Input voltage | $V_i$ | 30 | V |
| Output voltage | $V_o$ | 90 | V |
| Input current ripple | $\Delta i_L$ | 0.34 | A |
| Output voltage ripple | $\Delta V_o$ | 0.8 | V |
| Transistors TP65H070L (GaN) | $R_{on}$ | 85 | mΩ |
| Switching frequency | $f_{sw}$ | 40 | kHz |

**Table 2.** DDCC converter design.

| Parameter | Identifier | Value | Unit |
|---|---|---|---|
| Inductors | $L_1, L_2$ | 1.1 | mH |
| Inductors | $L_3, L_4$ | 560 | µH |
| | ESR | 25 | mΩ |
| Capacitors | $C_1, C_2$ | 47 | µF |
| Capacitors | $C_3, C_4$ | 1 | µF |
| | ESR | 5 | mΩ |

**Table 3.** IDDCC converter design.

| Parameter | Identifier | Value | Unit |
|---|---|---|---|
| Inductors | $L_1, L_2$ | 1.1 | mH |
| Inductors | $L_3$ | 560 | µH |
| | ESR | 25 | mΩ |
| Capacitors | $C_1, C_2$ | 47 | µF |
| Capacitors | $C_3$ | 1 | µF |
| | ESR | 5 | mΩ |

### 3.2. Design Parameters

Reflecting on the design criteria outlined in Table 1, the DDCC requires, for example, an inductor $L_1$ of 1.1 mH to achieve an input current ripple $\Delta i_{L_1}$ = 0.34 A. Table 2 displays a full enumeration of the reactive components for the DDCC.

Similarly, for the IDDCC converter, an inductor $L_1$ = 1.1 mH is needed to accomplish an input current ripple $\Delta i_{L_1}$ = 0.34 A. The detailed listing of reactive components for the IDDCC is provided in Table 3.

The deployment of the IDDCC power converter within the Matlab–Simscape Simulink software environment [25] is depicted in Figure 7.

Derived from it, a collection of targeted simulation outcomes is showcased. The design specifications enumerated in Tables 1–3 were considered during this process.

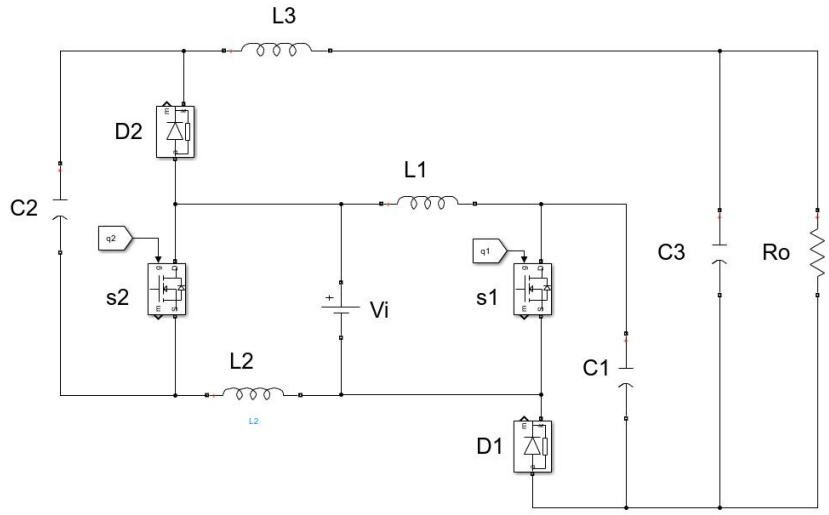


**Figure 7.** IDDCC as shown in Matlab–Simscape Simulink.

### *3.3. Steady-State Time Comparison*

Within this subsection, the time it takes for the DDCC and IDDCC power converters to reach a steady state is evaluated. The following premise is established for this analysis: A power converter is considered to have achieved steady state when its output voltage $V_o$ experiences a fluctuation within ±1%, meaning the output voltage variation is approximately ±9 V. Based on this criterion, recordings of the output voltage $V_o$ are illustrated in both the upper and lower portions of Figure 8. Moreover, the data gathered are concisely summarized in Table 4.

**Table 4.** Steady-state time summary.

| Converter | Overshoot Value (V) | Settling Time (ms) |
|---|---|---|
| DDCC | 156.012 | 10 |
| IDDCC | 166.025 | 10 |

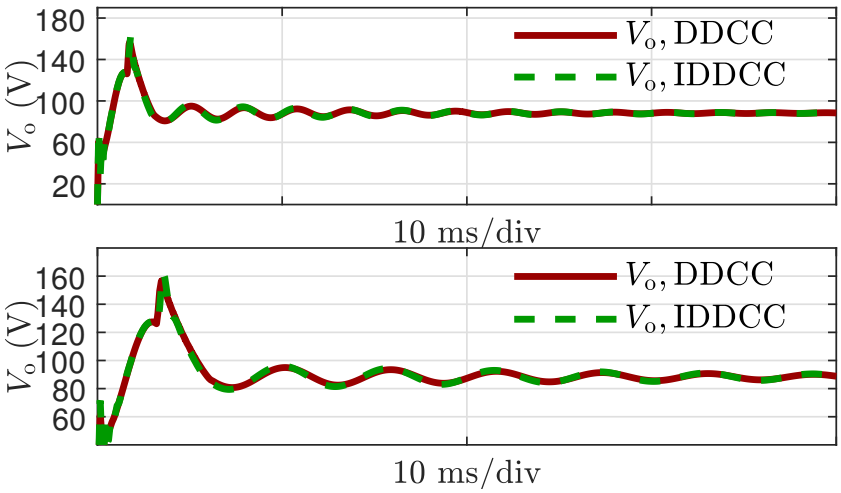


**Figure 8.** Steady state of conventional DDCC and IDDCC.

Based on the data presented in Table 4, the DDCC converter exhibits a lower voltage overshoot. Nonetheless, as illustrated in the lower part of Figure 8, both power converters achieve a steady state simultaneously, in under 10 milliseconds.

### *3.4. Output Voltage Comparison*

In this instance, to confirm the accuracy of the output voltage $V_o$ and output current $I_o$, recordings of both traces are showcased in Figure 9. As seen in the upper portion of Figure 9, the output voltage traces of both the DDCC and IDDCC power converters closely align with the target output voltage $V_o$ = 90 V. It is important to note that achieving a $V_o$ = 90 V requires a duty ratio $D$ = 0.5 for both the DDCC and IDDCC converters. The traces of the output voltage for both converters are virtually indistinguishable, adhering to the design criteria for output voltage ripple. In essence, both converters maintain identical voltage gains while producing the same output voltage.

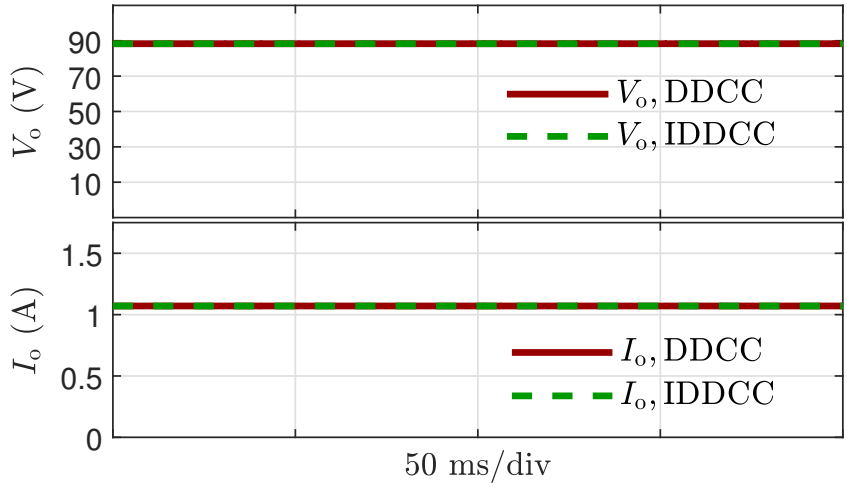


**Figure 9.** Output voltages and currents comparison.

Similarly, as illustrated in the bottom part of Figure 9, an output current value of $I_o$ = 1.11 A is recorded for both power converters. It is noteworthy that the traces of the output current from both devices closely overlay one another when powering a load of 81 Ω.

### *3.5. Input Current Ripple*

As demonstrated, the input current traces of both the DDCC and IDDCC power converters are analyzed side by side, this is shown in Figure 10. It is observable that the input current behaviors, $i_{L_1}$ and $i_{L_2}$, are consistent across both converters. Specifically, it is evident that for each switching cycle, one inductor is in the charging phase (exhibiting a positive slope) while the other is discharging (showing a negative slope). A current ripple of $\Delta i_L$ = 0.34 A, in line with design expectations, is recorded. This cycle of charging and discharging effectively mitigates the input current ripple, marking a significant advantage of the converter that warrants further exploration. Notably, despite the IDDCC topology utilizing fewer reactive components than the DDCC, it still manages to reduce the input current ripple effectively.

### *3.6. Efficiency*

Efficiency stands as a critical element in the development and analysis of power converters, characterized by Formula (29), where $P_i$ represents the input power, and $P_o$ denotes the output power. Moreover, $\Delta P$ signifies the losses of the IDDCC. It can be obtained by Equation (30). Measurements of input and output power for both the DDCC and IDDCC power converters are depicted in Figure 11. Based on the data illustrated in Figure 11, it is apparent that both converters exhibit comparable efficiency levels.

$$\eta = \frac{P_o}{P_i} \times 100, \tag{29}$$

$$\Delta P = P_i - P_o. \tag{30}$$

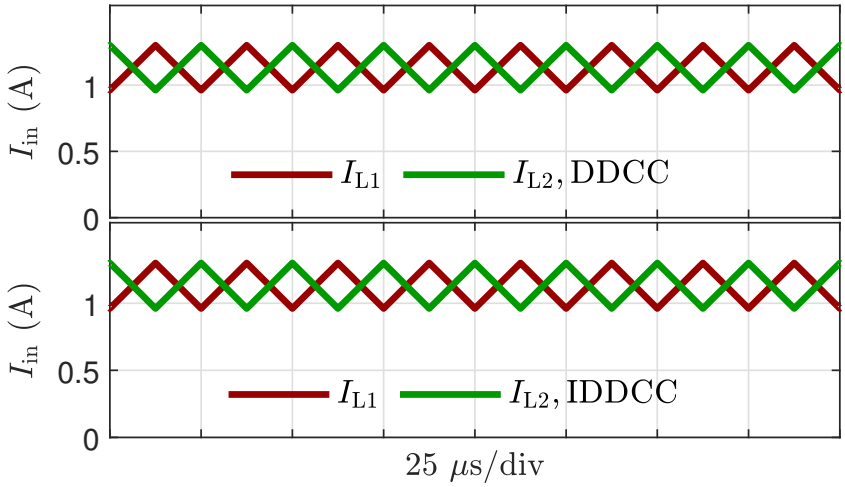


**Figure 10.** Input currents comparison.

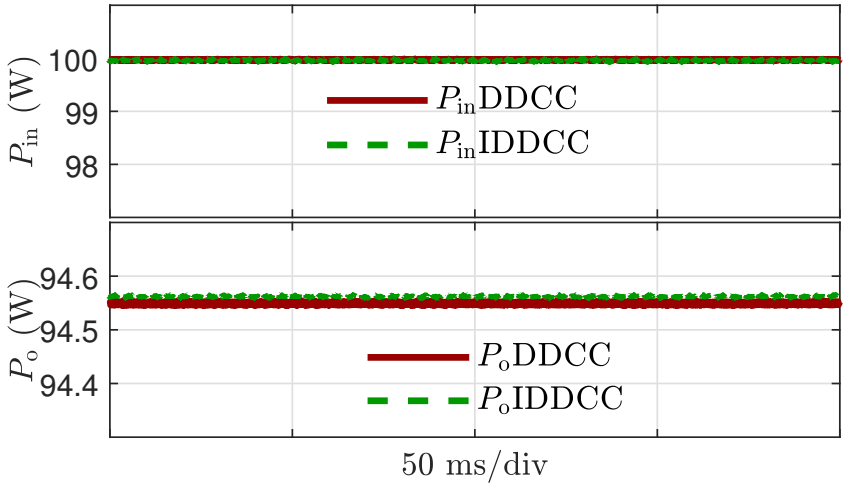


**Figure 11.** Input and output power comparison.

## 4. Experimental Results

To confirm the efficacy of the suggested IDDCC power converter, a set of software simulations was implemented on the `Matlab-Simulink` platform. The proposed converter's performance was verified and contrasted for the scaled-down experiment and the simulations using identical parameters given in Table 5.

**Table 5.** Setup of IDDCC power converter for both simulation and experiment.

| Parameter | Identifier | Value | Unit |
|---|---|---|---|
| Inductors | $L_1, L_2$ | 500 | µH |
| Inductors | $L_3$ | 200 | µH |
| | ESR | 15 | mΩ |
| Capacitors | $C_1, C_2$ | 10 | µF |
| Capacitors | $C_3$ | 10 | µF |
| | ESR | 5 | mΩ |

Several different tests were performed to collect data from the proposed converter. Some of the results obtained are presented below and identified as Test Cases I, II, and III.

### *4.1. Test Case I*

In Test Case I, a switching frequency of $F_{\text{sw}}$ = 50 kHz was employed, with an input voltage $V_{\text{in}}$ = 10 V and a duty cycle of $D$ = 0.5 (equating to 10 µs/20 µs). Simulation results

of this test case are depicted in Figure 12. In the same fashion, experimental observations are presented in Figure 13.

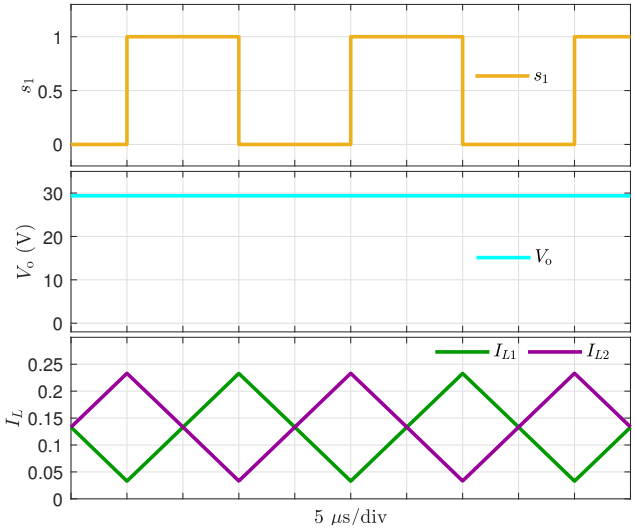


**Figure 12.** Simulation signals, firing signal $s_1$, voltage at the output port $V_o$, current at the inductor $I_{L1}$ and current at the inductor $I_{L2}$.

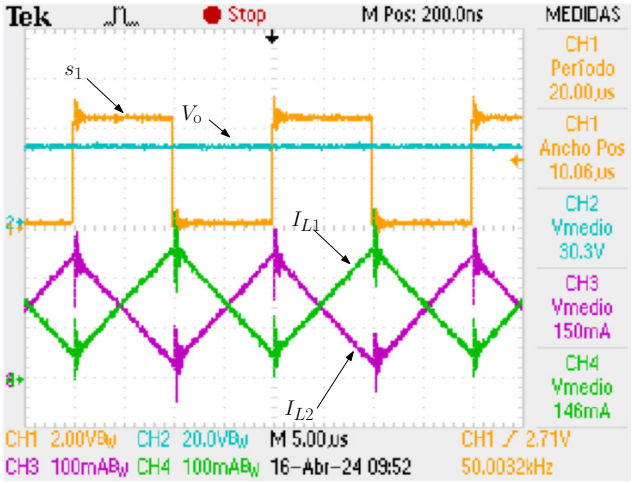


**Figure 13.** Experimental signals, firing signal $s_1$, voltage at the output port $V_o$, current at the inductor $I_{L1}$ and current at the inductor $I_{L2}$.

First, Equation (17) and Figure 6 are validated by observing that $V_i$ = 10 V is boosted 3 times to obtain an output voltage $V_o$ = 30 V. In addition, a good match between the different signals shown in both figures can be observed. A summary of main observations is summarized in Table 6. It seems, and it can be stated, that, based on the measurements and data obtained in Test Case I, the IDDCC converter is performing adequately, showing the same behavior in measurements of frequency, amplitudes, and voltage gain.

**Table 6.** Test Case I: summary of results.

| Parameter | Simulation | Experiment | Units |
|---|---|---|---|
| $D$ | $\frac{10\,\mu s}{20\,\mu s} = 0.5$ | $\frac{10\,\mu s}{20\,\mu s} = 0.5$ | none |
| $V_o$ | 30 | 30.3 | V |
| $I_{L1}$ and $I_{L2}$ | 150 | 150 | mA (average) |
| Frequency | 50 | 50 | kHz |

To further validate the performance of the IDDCC converter under the setup of Test Case I, measurements of current in the input port $I_{\text{in}}$ and current in the output port $I_{\text{o}}$ are depicted in Figures 14 and 15. Notice that due to the fact that $I_{L1}$ and $I_{L2}$ waveforms are complementary to each other, cancelation of its current ripple $\Delta I_L$ is achieved. This feature results in obtaining a ripple-free input current $I_{\text{in}}$. This feature is demonstrated in both simulation and experimental results. Be aware that this feature is only valid when the duty cycle is set to $D = 0.5$. Moreover, as expected, a typical variation in the experimental measurement of input current waveform $I_{\text{in}}$ is observed when the firing signal $s_1$ goes up and down.

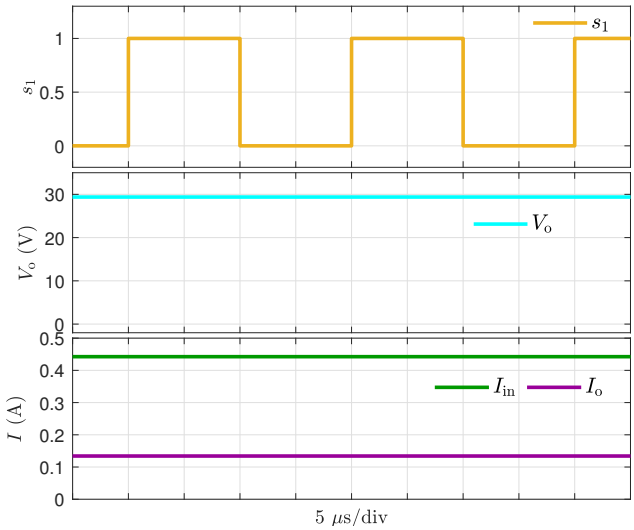


**Figure 14.** Simulation signals, firing signal $s_1$, voltage at the output port $V_{\text{o}}$, current at input port $I_{in}$ and current at the output port $I_o$.

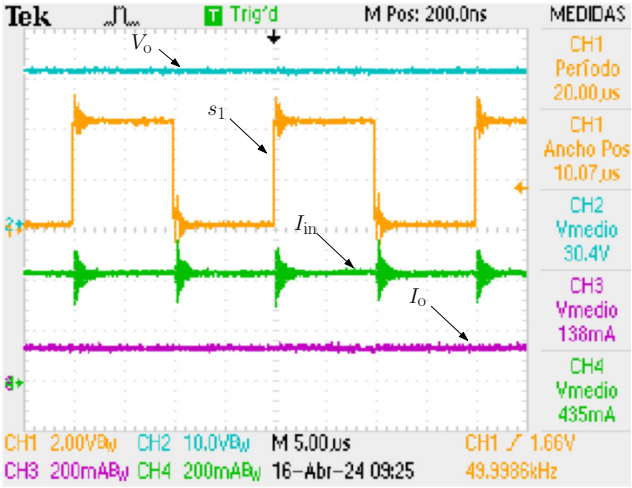


**Figure 15.** Experimental signals, firing signal $s_1$, voltage at the output port $V_{\text{o}}$, current at the input port $I_{in}$ and current at the output port $I_{\text{o}}$.

### *4.2. Test Case II*

The setup of Test Case II is the same as Test Case I. Nonetheless, the only difference is that in this case, a duty cycle $D$ = 0.316 is selected. Simulation and experimental results are depicted in Figures 16 and 17, respectively. Once again, Equation (17) and Figure 6 are validated through the results obtained. Moreover, it is observed that the input voltage $V_{\text{i}}$ = 10 V is boosted 3.66 times by measuring an output voltage $V_{\text{o}}$ = 36.6 V in both simulation and experimental results, respectively.

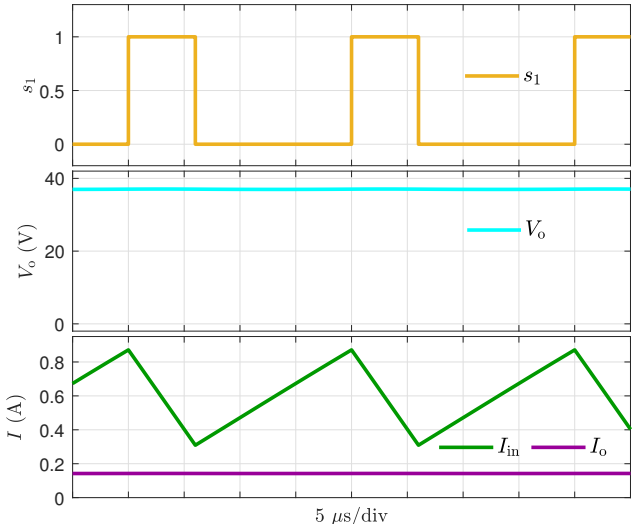


**Figure 16.** Simulation signals, firing signal $s_1$, voltage at the output port $V_o$, current at input port $I_{in}$ and current at the output port $I_o$.

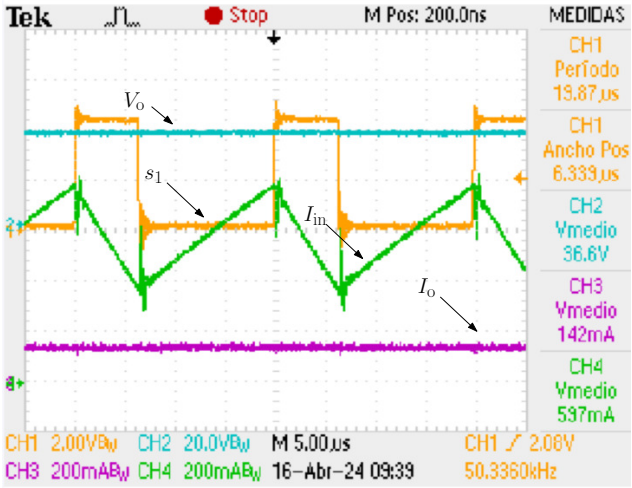


**Figure 17.** Experimental signals, firing signal $s_1$, voltage at the output port $V_o$, current at the input port $I_{in}$ and current at the output port $I_o$.

A summary of findings regarding Test Case II is summarized in Table 7. Based on these simulations and the experimental results of Test Case II, it seems the proposed IDDCC power converter performs as expected. The measurements and data generated indicate that its behavior regarding switching frequency, voltage and current waveforms, and voltage gain of both simulation and experimental results depict a good match.

**Table 7.** Test Case II: summary of results.

| Parameter | Simulation | Experiment | Units |
|---|---|---|---|
| $D$ | $\frac{6.33\ \mu s}{20\ \mu s} = 0.316$ | $\frac{6.33\ \mu s}{20\ \mu s} = 0.316$ | |
| $V_o$ | 36.6 | 36.6 | V |
| $I_o$ | 143 | 142 | mA (average) |
| $I_{in}$ | 600 | 597 | mA (average) |
| frequency | 50 | 50 | kHz |

### *4.3. Test Case III*

To further validate the performance of the IDDCC power converter, the duty cycle was made equal to $D = 0.69$ for both simulation and experiment. All the other parameters are the same as in Test Case I. The results obtained are depicted on Figures 18 and 19, respectively. According to the results obtained, the voltage-gain Equation (17) and Figure 6 are found correct. This time, the input voltage value $V_{\mathrm{i}}$ set equal to 10 V has been boosted to 36.9 V, adequately validating the IDDCC performance. It can be mentioned that a good agreement between simulation and experimental results of the IDDCC regarding switching frequency, input and output voltage waveforms, input and output currents waveforms, and voltage gain is obtained.

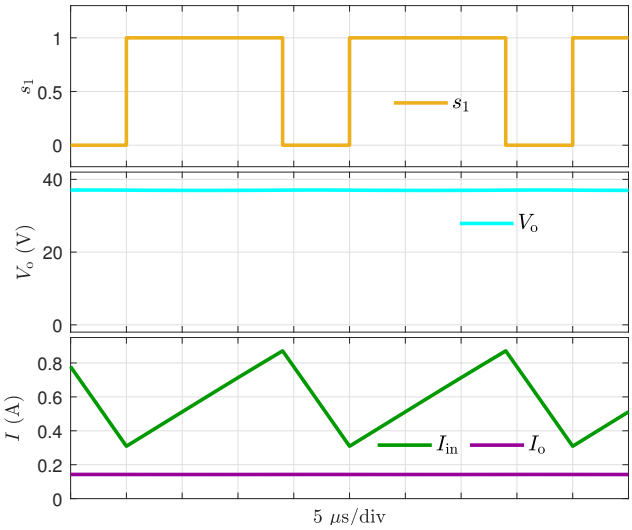


**Figure 18.** Simulation signals, firing signal $s_1$, voltage at the output port $V_{\mathrm{o}}$, current at input port $I_{in}$ and current at the output port $I_o$.

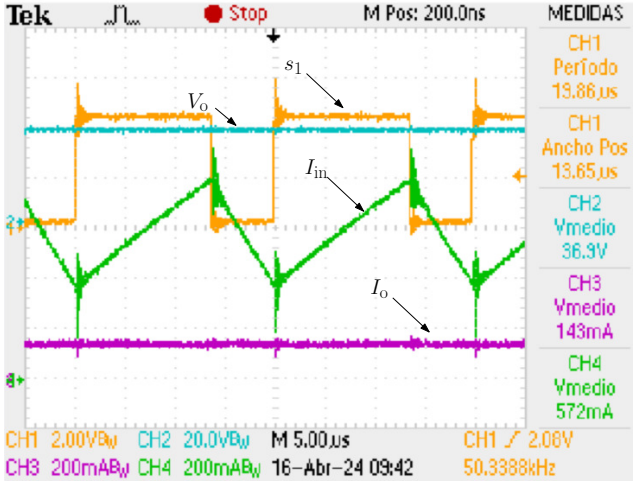


**Figure 19.** Experimental signals, firing signal $s_1$, voltage at the output port $V_{\mathrm{o}}$, current through the inductor $i_{L_1}$ and current at the input port $I_{\mathrm{in}}$.

## 5. Conclusions

This paper introduced enhancements to an existing interleaved-type power converter, briefly referred to as Improved Double Dual Ćuk Converter (IDDCC). The primary aim was to scrutinize the converter known as Double Dual Ćuk Converter (DDCC) with the intent of designing a new improved converter that utilizes fewer reactive components (limited to three capacitors and three inductors), while preserving the identical voltage gain and

achieving equal or superior efficiency. The analysis juxtaposed and validated both converters under equitable scenarios. The findings from the simulations indicate that the IDDCC boasts several benefits: (i) it requires fewer reactive components (merely three inductors and three capacitors), (ii) it maintains the established voltage gain, (iii) it ensures minimal switching ripple at the input port current, and (iv) it sustains its efficiency. Ultimately, this newly proposed converter is projected to diminish both its physical dimensions and financial expenditure. Additionally, experimental data from a scaled-down prototype were presented to demonstrate practical outcomes.

**Author Contributions:** H.R.R.-C. and J.C.R.-C. contributed to the conceptualization of the article; A.V.-G. contributed to the methodology and validation; J.P. contributed with the software; H.R.R.-C. and A.V.-G. contributed to the formal analysis; H.R.R.-C. and J.C.R.-C. wrote the draft and manuscript preparation. All authors have read and agreed to the published version of the manuscript.

**Funding:** The authors would like to thank the founding from Universidad Panamericana through the project UP–CI–2023–GDL–05–ING "Estudio de eliminación de rizo en convertidores DC-DC".

**Data Availability Statement:** Data are contained within the article.

**Acknowledgments:** The authors gratefully acknowledge the support of Universidad Panamericana in México and Universidad Autónoma de Occidente in Colombia.

**Conflicts of Interest:** The authors declare no conflict of interest.

## Abbreviations

The following abbreviations are used in this article:

| | |
|---|---|
| DDCC | Double Dual Ćuk Converter |
| IDDCC | Improved Double Dual Ćuk Converter |
| CCM | Continuous Conduction Mode |

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