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Radiation Detector Front-End Readout Chip with Nonbinary Successive Approximation Register Analog-to-Digital Converter for Wearable Healthcare Monitoring Applications

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Abstract: A 16-channel front-end readout chip for a radiation detector is designed for portable or wearable healthcare monitoring applications. The proposed chip reads the signal of the radiation detector and converts it into digital serial-out data by using a nonbinary successive approximation register (SAR) analog-to-digital converter (ADC) that has a 1-MS/s sampling rate and 10-b resolution. The minimum-to-maximum differential and integral nonlinearity are measured as −0.32 to 0.33 and −0.43 to 0.37 least significant bits, respectively. The signal-to-noise-and-distortion ratio and effective number of bits are 57.41 dB and 9.24 bits, respectively, for an input frequency of 500 kHz and a sampling rate of 1 MS/s. The SAR ADC has a 38.9-fJ/conversion step figure of merit at the sampling rate of 1 MS/s. The proposed chip can read input signals with peak currents ranging from 20 to 750 µA and convert the analog signal into a 10-bit serial-output digital signal. The input dynamic range is 2–75 pC. The resolution of the peak current is 208.3 nA. The chip, which has an area of 1.444 mm × 10.568 mm, is implemented using CMOS 0.18-µm 1P6M technology, and the power consumption of each channel is 19 mW. This design is suitable for wearable devices, especially biomedical devices.

Keywords: bioelectronics; wearable sensors; healthcare monitoring; radiation detector; nonbinary SAR ADC

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1. Introduction

As integrated chip technology has developed, many large and costly machines have become smaller and less expensive. In the biomedical field, progressive wireless technology and modalities such as electroencephalography [1], electrocardiography [2–6], and magnetic resonance imaging [7] are being integrated into wireless body sensor networks [5,6,8]. Wearable devices are becoming even smaller because digital signal processors and data storage can be outsourced to external devices. Technological developments are leading to considerable benefits in terms of wearable healthcare monitoring.

The use of radiation detector devices in medicine [9,10] is limited by the large size of these devices. Integrated chip technology offers a means of scaling down instruments, and smaller radiation detector devices would have a greater scope of application. Communication within the Internet of Things (IoT) is convenient and rapid, and integrated chip technology enables the use of radiation detector devices in wearable healthcare monitoring and the IoT [11–14]. The conversion blocks that have been employed to convert analog signals to digital signals are analog-to-digital converters (ADCs) [11–13], digital delay-locked loop circuits [14], and time-to-digital converters [15].

In designing wearable healthcare monitoring applications, the objectives are a sampling rate of several megasamples per second and low power consumption.

Pipeline ADCs have high speed, with high sampling rates (~100 MS/s), medium resolution (8–12 b), and high power consumption (dozens of milliwatts). Delta-sigma

ADCs have low speed, with sampling rates in the dozens of kilosamples per second, high resolution (12–20 b), and moderate power consumption (several milliwatts). SAR ADCs have medium speed, with sampling rates of several megasamples per second, moderate resolution (8–12 b), and low power consumption (dozens of microwatts). SAR ADCs are thus more suitable than pipelined ADCs or delta-sigma ADCs for wearable healthcare monitoring applications.

This study proposes a front-end readout circuit for a radiation detector; this circuit contains a nonbinary successive approximation register (SAR) ADC [16]. In radiation applications, a particle can cause bit flips in digital circuits and voltage spikes in analog circuits. These flips and spikes can be considered a noise effect. Because of its nonbinary structure, the SAR ADC has a correction mechanism that can minimize the effect of the digital-to-analog converter (DAC), settling incomplete errors and the effects of noise from the DAC and comparator [17]. The results of simulations are depicted in Figures 1 and 2. Figure 1 presents a comparison of the effective number of bits (ENOB) for a binary SAR ADC versus a nonbinary SAR ADC when some noise is present in the comparator input. The ENOB of the nonbinary SAR ADC is 0.17 b higher than that of the binary SAR ADC with an 8-least-significant-bit (LSB) noise effect. Figure 2 presents a comparison of the ENOB for binary and nonbinary SAR ADCs for various settling ratios. The settling ratio means that the ratio of DAC voltage settles to the correct value. The ENOB of the nonbinary SAR is still 9 b when the DAC settling ratio is 80%. The ENOB of the binary SAR ADC is 9 b at a settling ratio of 97.5%, whereas at an 80% settling ratio, it is only 5.12 b.

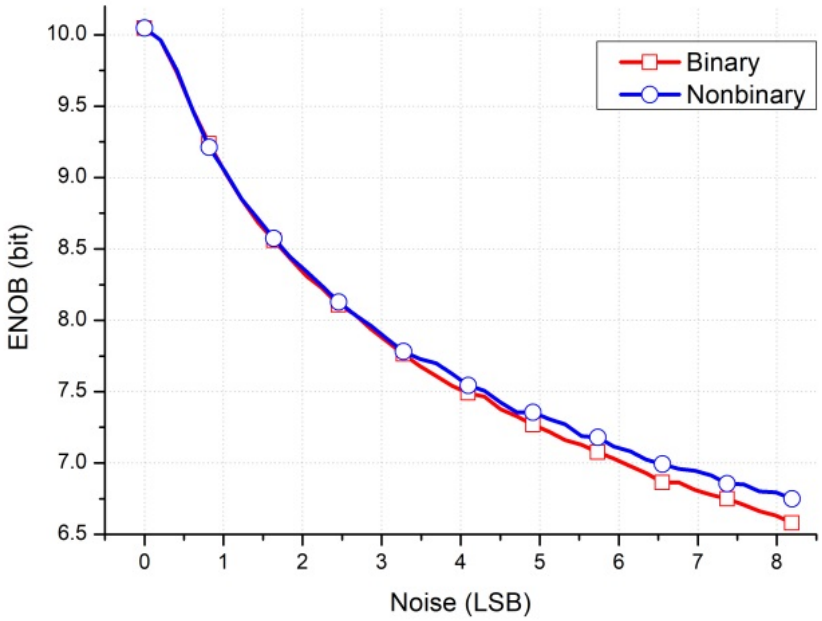


Figure 1. ENOB of binary and nonbinary SAR ADCs with a noise effect in Matlab R2017b simulations.

Figures 3 and 4 present the results of Matlab simulations quantifying the performance of a radiation detection front-end circuit using a nonbinary SAR ADC versus that using a binary SAR ADC. The ideal conversion code count in this simulation is 552, and the result for the binary SAR ADC case is a 1-LSB error, even when the noise effect is only at 0.25 LSB. Conversely, for the nonbinary SAR ADC case, correct conversion results are obtained with up to a 1.5-LSB noise effect. With up to a 7.5-LSB noise effect, the conversion errors for the binary and nonbinary SAR ADCs are 10 and 2 LSB, respectively. With incomplete DAC settling, no conversion errors are found to occur for the binary and nonbinary SAR ADC cases until the settling ratios of 87.5% and 83.8%, respectively, are reached. For the binary SAR ADC case, a 1-LSB conversion error occurs until a settling ratio of 72% is reached, at which point the error increases to an 11-LSB conversion error. By contrast, the nonbinary SAR ADC continues to have a conversion error of only 1 LSB.

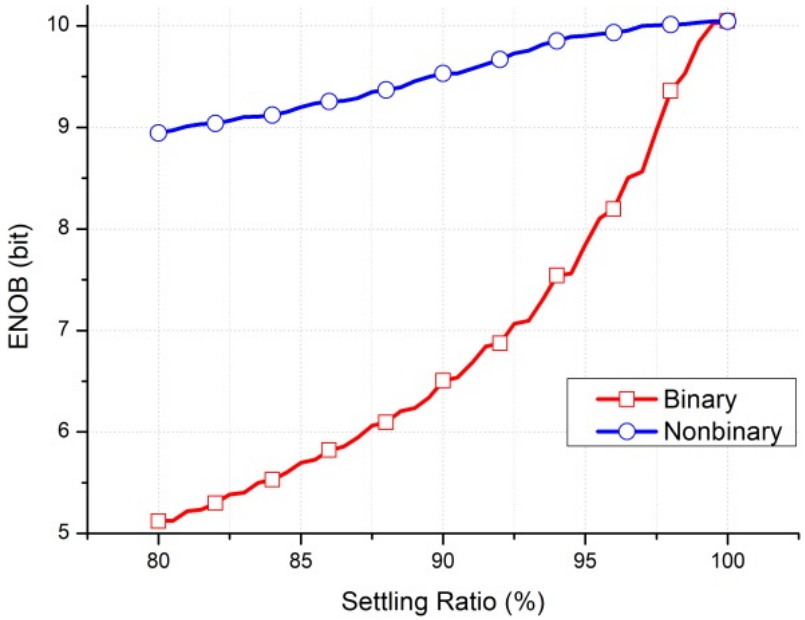


Figure 2. ENOB of binary and nonbinary SAR ADCs versus DAC settling ratio in Matlab simulations.

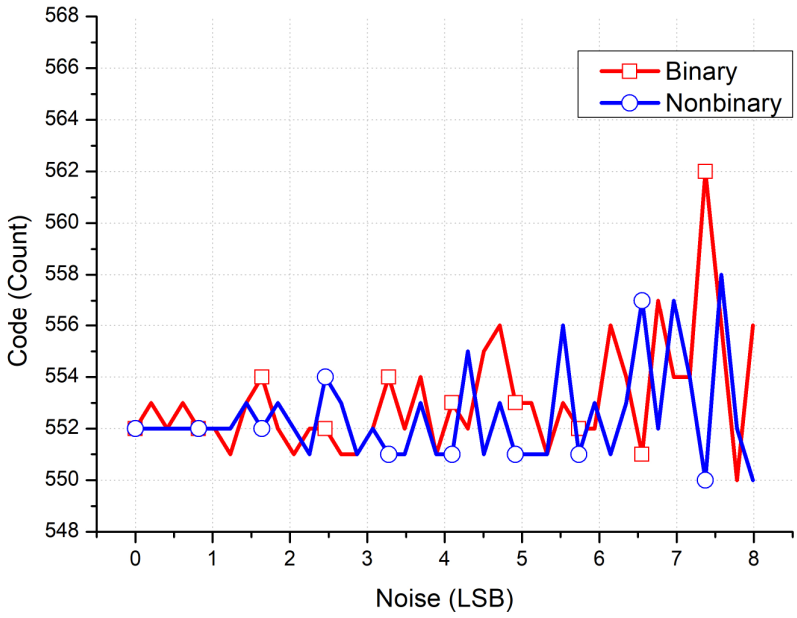


Figure 3. Conversion error versus noise for a radiation detector front-end readout chip containing a binary versus nonbinary SAR ADC with DAC incomplete settling in Matlab simulations.

Because most applications of radiation detector front-end readout chips require multiple channels, the chip proposed in the present study is a 16-channel front-end readout chip. The use of multiple channels causes a cross-talk effect and reduces the accuracy of an SAR ADC. The cross-talk signal is noise to the SAR ADC, and the SAR ADC thus requires a correction mechanism to reduce the effect of this noise. Section 2 of this paper describes the block diagram of the proposed chip. Section 3 describes how the chip is implemented. Section 4 discusses the chip's performance in tests. Finally, Section 5 concludes the paper.

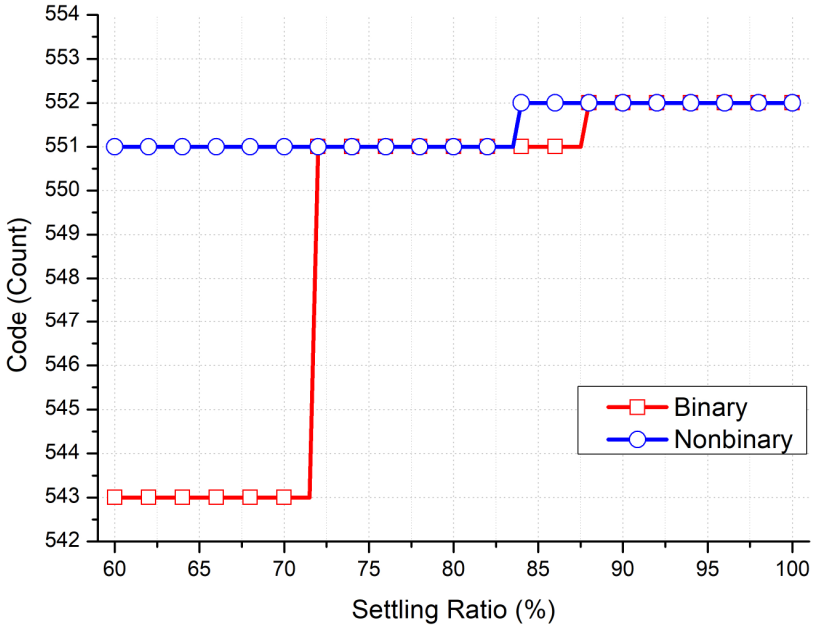


Figure 4. Conversion error versus settling ratio for a radiation detector front-end readout chip containing a binary versus nonbinary SAR ADC with DAC incomplete settling in Matlab simulations.

2. Proposed Structure

The block diagram of a 16-channel front-end readout circuit for a radiation detector is depicted in Figure 5. The circuit comprises an amplifier, a trigger generator, an integrator, an ADC, a reset signal generator (RSG), a parallel-in serial-out shifter register (PSSR), and a bias circuit. When the radiation detector responds to radiation, a current signal is generated and sent to the amplifier. The amplifier converts the current signal into a voltage signal and transfers this signal to the trigger generator and integrator. The integrator then begins integration, and simultaneously, the ADC begins tracking the integrator's output signal. The trigger generator is a differential difference comparator and thus has two differential inputs and a single output. The trigger signal is high when the input signal is higher than the reference voltage and low otherwise. When the radiation detector turns off, the trigger generator's output signal ceases. The ADC then stops its signal tracking and conversion. After it has converted an analog signal, the ADC transfers the parallel digital data to the PSSR and sends a reset signal to the RSG. The RSG resets the integrator after turning off the signal of the trigger generator and the reset signal of the ADC. The amplifier, trigger generator, ADC, and RSG enter into sleep mode until the radiation detector responds again. A flowchart of this process is depicted in Figure 6. The input signal's CLK periodically controls the PSSR's renewal of parallel-in digital data from the ADC and transferal of serial-out data, a serial-out clock, and a sampling clock. The sampling clock is the time at which parallel-in digital data should be renewed, whereas the serial-out clock is the time at which serial digital data are read out. Each serial-out datum follows each trigger signal.

The integrator comprises an amplifier, an input resistor, and multiple-integrated-slope switched capacitors. The multiple integrated slopes of these switched capacitors are changed by switches S_1 and S_2. The original integrated slope works with one capacitor when the control signals s_1 and s_2 are low. The integrated slope works with two capacitors when the control signals s_1 and s_2 are high and low, respectively. When the control signals s_1 and s_2 are respectively low and high or are both high, the integrated slope works with three or four capacitors. The multiple integrated slopes can cover a substantial input-signal-to-digital-output conversion range and thus support numerous applications.

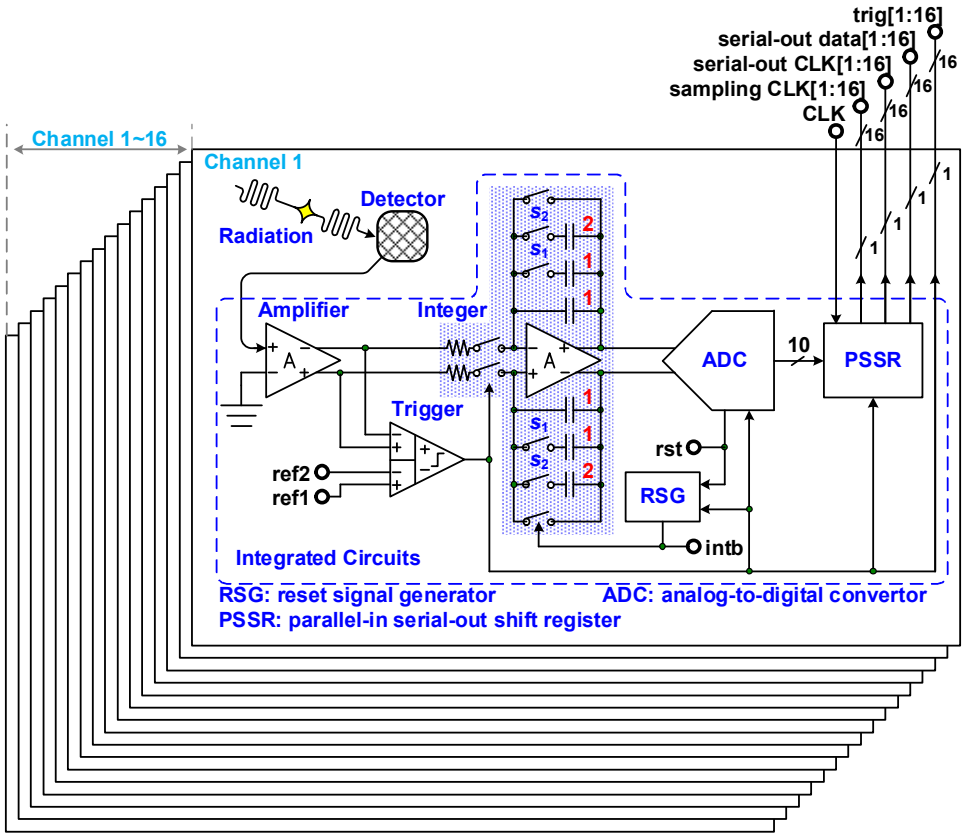


Figure 5. Block diagram of 16-channel front-end readout circuit for a radiation detector.

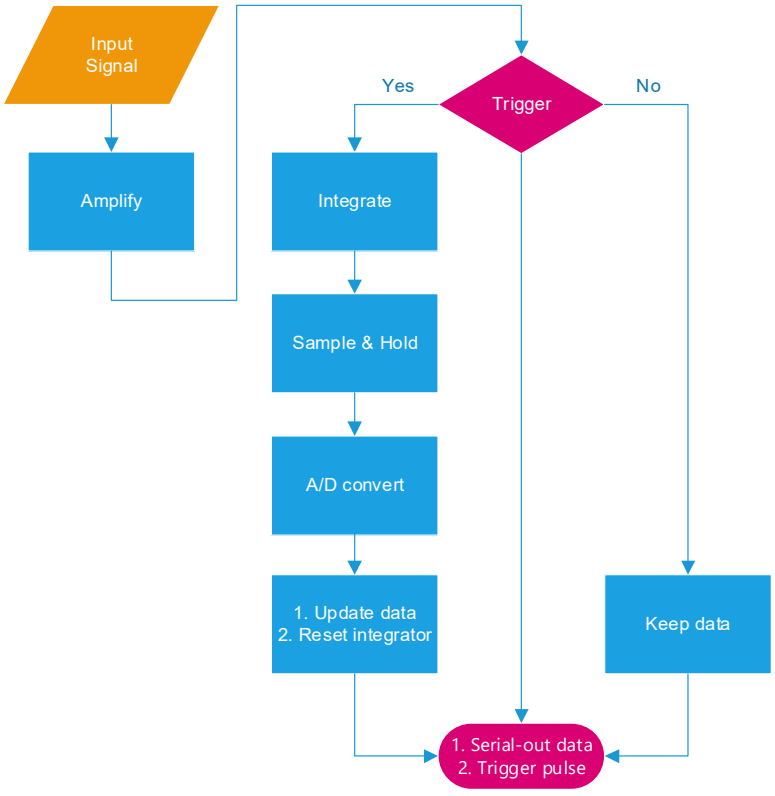


Figure 6. Function flowchart of proposed circuit.

A 4-bit binary SAR ADC with a split capacitor DAC [18] is depicted in Figure 7. The power efficiency of the SAR ADC with split capacitor technology is greater than that of a conventional SAR ADC. The capacitors in a conventional 4-bit SAR ADC are denoted C_2, C_1, C_0, and C_D, and the weighted sizes are 8, 4, 2, and 2. By contrast, in the SAR ADC with split capacitor technology, the DAC structure contains C_2 and C_{2b} instead of C_2, C_1 and C_{1b} instead of C_1, and C_0 and C_{0b} instead of C_0. The normal conversion process of a binary SAR ADC with split capacitors is depicted in Figure 8a, and the conversion process with most significant bit (MSB) error decisions is illustrated in Figure 8b. The digital outputs of the 4-bit binary SAR ADC with split capacitors are b_3, b_2, b_1, and b_0, and the mapping code weights are 8, 4, 2, and 1, respectively. Thus, the digital result is $8 \times b_3 + 4 \times b_2 + 2 \times b_1 + 1 \times b_0$. The correction results of conversion—b_3, b_2, b_1, and b_0—are 1, 0, 0, and 1, respectively, leading to a calculation result of 9. If an MSB error decision occurs, however, the conversion results are 0, 1, 1, and 1, and the calculation result is 7. The MSB error decision causes an incorrect conversion result.

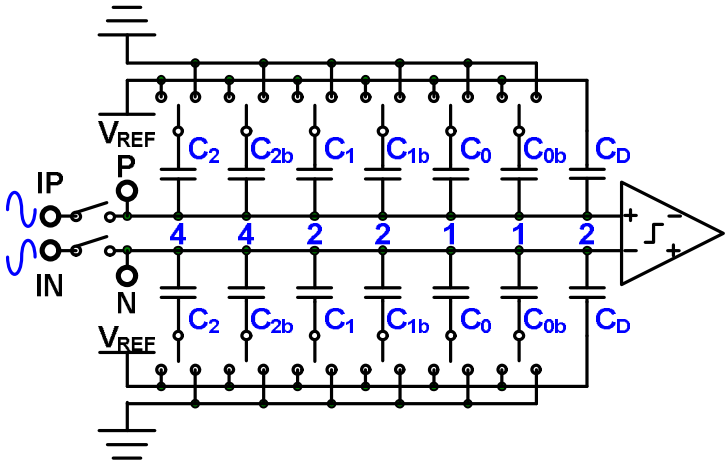
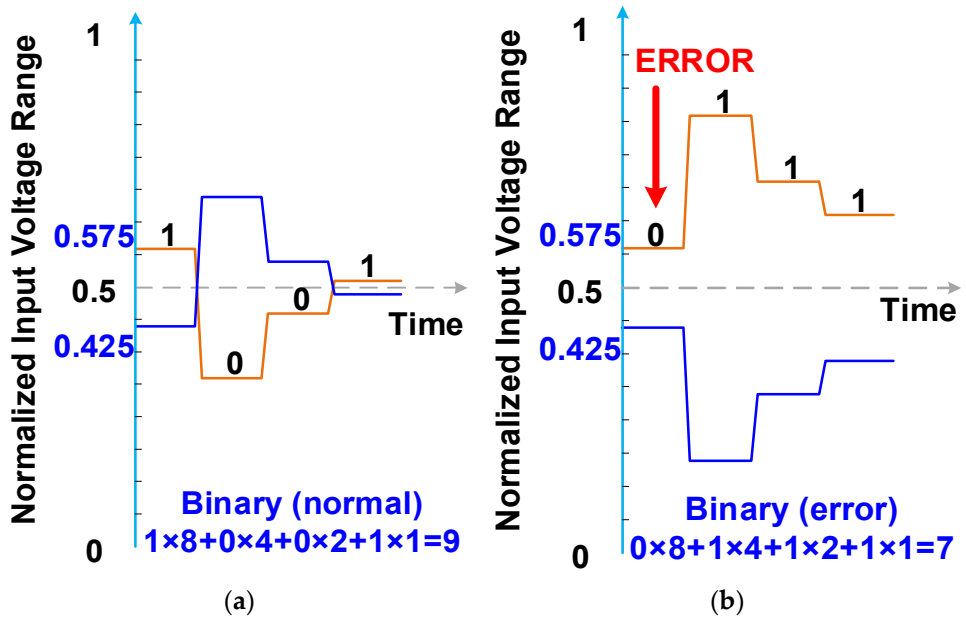


Figure 7. Four-bit binary SAR ADC with split capacitors.



(**a**) (**b**)

Figure 8. (**a**) Normal conversion process and (**b**) conversion process with MSB error decisions in a 4-bit binary SAR ADC.

A 4-bit nonbinary SAR ADC with split capacitors is depicted in Figure 9. The DAC structure splits two redundant capacitors, C_3 and C_{3b}, to obtain more redundancy code

for error correction. The capacitors of the 4-bit nonbinary SAR ADC with split capacitors are C_3, C_{3b}, C_2, C_{2b}, C_1, C_{1b}, C_0, C_{0b}, and C_D, and their respective weight sizes are 3, 3, 2, 2, 1, 1, 1, 1, and 2. The digital outputs of the 4-bit nonbinary SAR ADC with split capacitors are b_4, b_3, b_2, b_1, and b_0, and the respective mapping code weights are 6, 4, 2, 2, and 1. Thus, the digital result is $6 \times b_4 + 4 \times b_3 + 2 \times b_2 + 2 \times b_1 + 1 \times b_0$. The redundant code weight of b_4 is the summation of the other code weights minus the code weight of b_4 ($4 + 2 + 2 + 1 + 1 - 6 = 4$). The other redundant code weights are 2, 2, and 0 (calculations: $2 + 2 + 1 + 1 - 2 = 2$; $2 + 1 + 1 - 2 = 2$; and $1 + 1 - 2 = 0$). Because the binary SAR ADC with split capacitors has no redundant capacitors, it has no redundant code weights. The normal conversion process of a 4-bit nonbinary SAR ADC with split capacitors is depicted in Figure 10a. The correction conversion results are 1, 0, 1, 0, and 1, and the calculation result is 9. The conversion process of a 4-bit nonbinary SAR ADC with split capacitors and MSB error decisions is presented in Figure 10b. The conversion results are 0, 1, 1, 1, and 1, and the calculation result is 9. The MSB error decision can be corrected with redundant code weights.

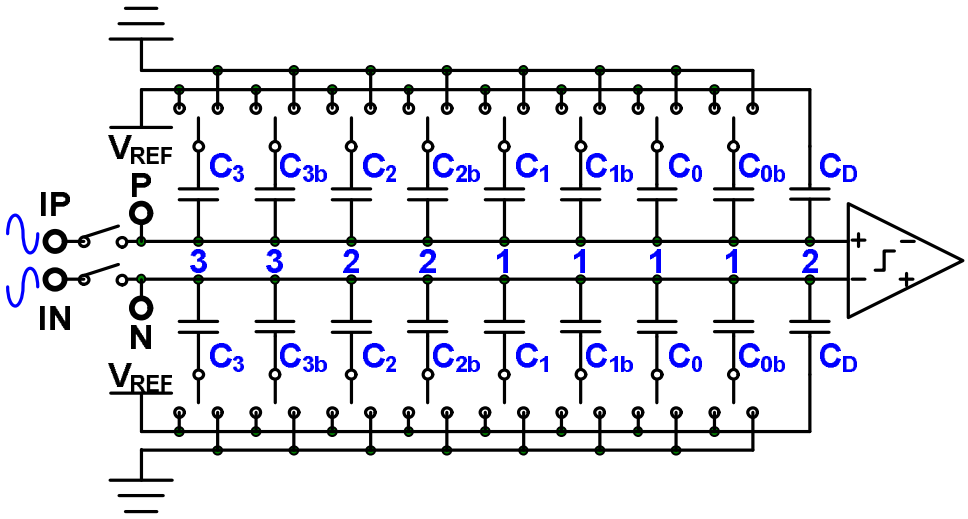
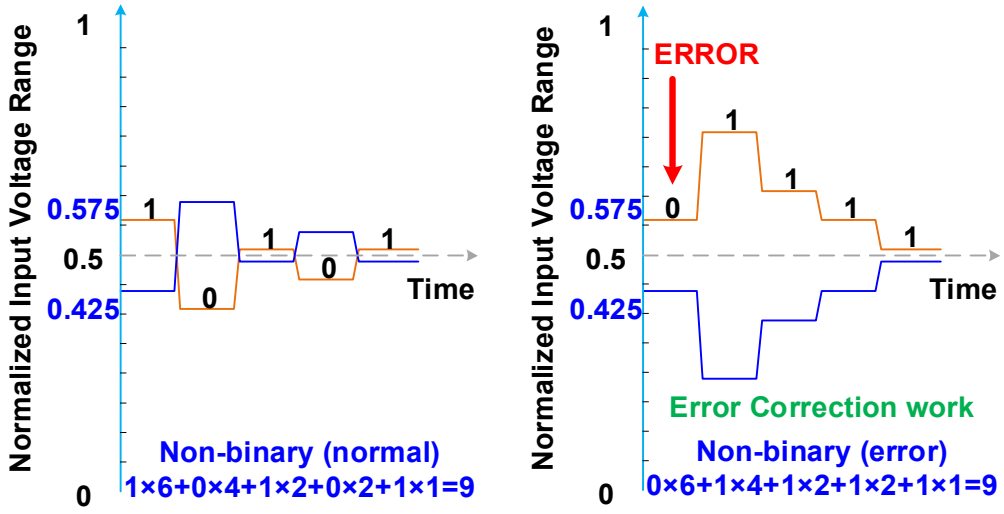


Figure 9. Four-bit nonbinary SAR ADC with split capacitors.



(**a**) (**b**)

Figure 10. (**a**) Normal conversion process and (**b**) conversion process with MSB error decisions of a 4-bit nonbinary SAR ADC.

The code weights and redundant code weights of 10-bit binary and nonbinary SAR ADCs are listed in Table 1. When redundant code weights are larger, more redundant bits must be added in the conversion process. In the case of the 10-bit SAR ADC, adding two redundant bits leads to a 20% gain in redundant code weights available for correcting error decisions. The large values of the redundant code weights listed in Table 1 can guarantee larger error correction ranges. Series capacitor technology is employed in this study to reduce the capacitor array of the DAC, which is depicted in Figure 11. The capacitors C_0 and C_{0b} comprise two series unit capacitors; this means that the size of the capacitor array in the DAC is halved because the equivalent capacitance of this array with two series unit capacitors is a half-unit capacitor [17,19].

Table 1. Bit weights of binary and nonbinary SAR ADCs.

Bit	Binary Code Weight	Redundant Code Weight	Nonbinary Code Weight	Redundant Code Weight
b_{11}	-	-	404	216
b_{10}	-	-	248	124
b_9	512	0	152	68
b_8	256	0	88	44
b_7	128	0	52	28
b_6	64	0	32	16
b_5	32	0	20	8
b_4	16	0	12	4
b_3	8	0	8	0
b_2	4	0	4	0
b_1	2	0	2	0
b_0	1	0	1	0
Dummy	1	0	1	0

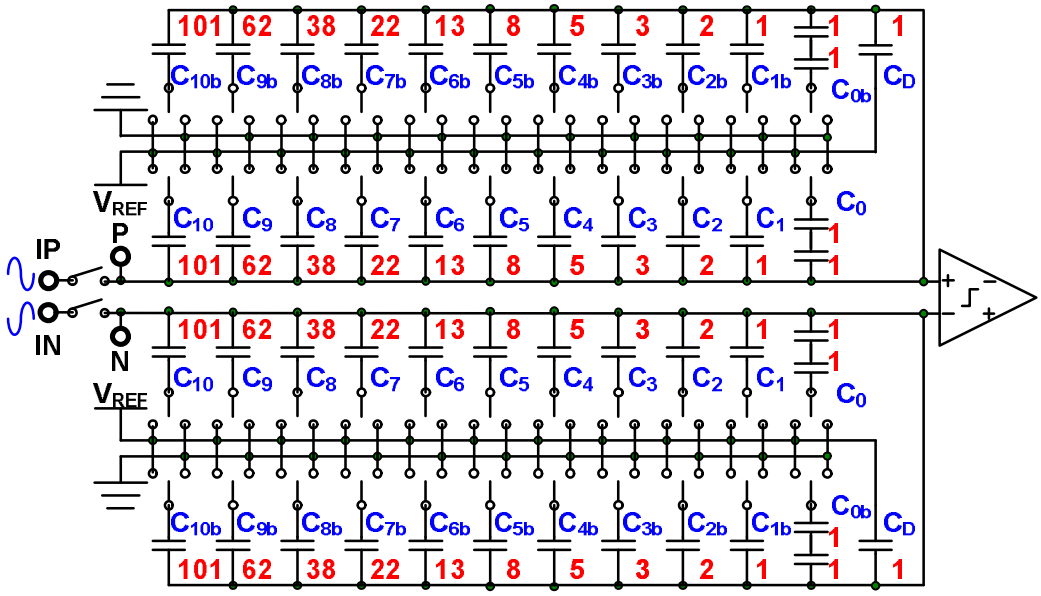


Figure 11. DAC of a nonbinary SAR ADC.

3. Circuit Design and Implementation

This section describes the circuit structure and how each stage of the block diagram is designed and implemented, from the input signal to the first stage to the output signal from the last stage.

3.1. Amplifier

The amplifier, which is the signal-receiving stage in the proposed block diagram, has the circuit structure depicted in Figure 12. It comprises input resistors R_i and R_d, a fully differential amplifier M_1–M_5, and common feedback resistors R_1 and R_2. The current signal is converted into a voltage signal by input resistor R_i, and the voltage signal is amplified by the amplifier. A trade-off is made between the noise contributed by the input resistance and the range over which the received current signal is converted into the voltage signal. When the input resistance is 1 kΩ, it contributes noise of 13 μV_{rms} when the operating frequency is 10 MHz, as revealed in Equation (1) [20]. Because the converted voltage range for an input current signal of 1 μA to 1 mA is 0.1–1.0 V, the noise contribution of the input resistor can be ignored. In the 16-channel design, the offset between channels must be considered. The large mismatch contribution in the amplifier is the threshold voltage (denoted V_{TH}) difference between the input pair M_2 and M_3. To ensure that the offset tolerance between each channel is acceptable, $1\sigma < 0.5\ mV_{rms}$, the width and length of the input pair must be sufficiently large, as expressed in Equation (2) [20]. Figure 13 depicts the results of an Hspice Monte Carlo simulation of the amplifier with 1000 samples. The input-referred offset voltage is 0.265 mV_{rms}, and the input signal has a voltage of 20 mV.

$$\sqrt{\overline{v^2}} = \sqrt{4kTR\Delta f} = \sqrt{1.66 \times 10^{-20} \times 1 \times 10^3 \cdot 10 \times 10^6} \approx 13\,\mu V_{rms} \quad (1)$$

$$\Delta V_{TH} = \frac{A_{ATH}}{\sqrt{WL}} \quad (2)$$

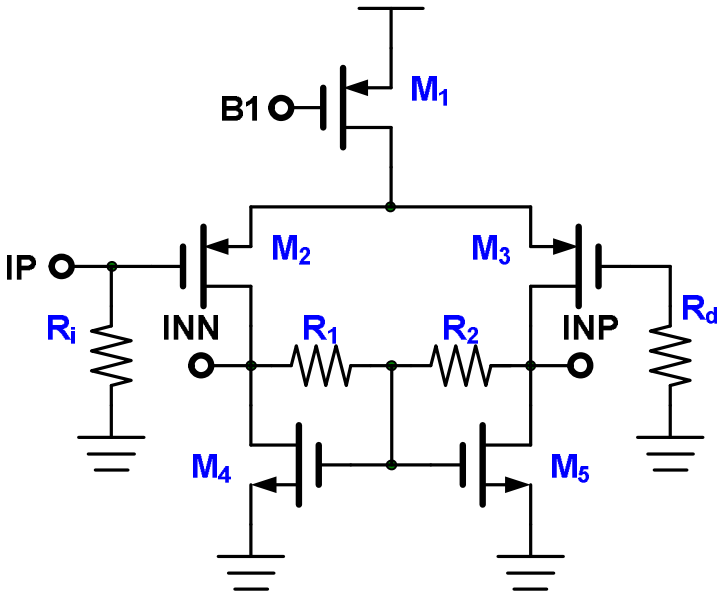


Figure 12. Amplifier.

3.2. Integrator

The integrator (illustrated in Figure 14) comprises the input resistors R_3 and R_4, which are switched by M_6 and M_7, respectively; a fully differential amplifier M_8–M_{12}; the common feedback resistors R_5 and R_6; the reset switches M_{13} and M_{14}; and multiple slopes integrated by capacitors C_1–C_6 and switches M_{15}–M_{20}. The integrator integrates when M_6 and M_7 turn on and M_{13} and M_{14} turn off, whereas it stops integrating when M_6, M_7, M_{13}, and M_{14} turn off. Integration is reset when M_6 and M_7 turn off and M_{13} and M_{14} turn on. The output voltage of the integrator is integrated by input signal V_{IN}, switched capacitors C_{int}, and input resistors R_4 and R_6, as shown in Equation (3). C_{int} comprises C_1–C_6. The multiple integrated slopes switch to different integrated slopes when M_{15}–M_{20} work in a different mode. When M_{15} and M_{18} always turn on and M_{16}, M_{17}, M_{19}, and M_{20} turn off,

the integrated slope is the largest of the multiple integrated slopes. Under this condition, C_{int} is C_1. For the design, each switched capacitor in the integrator has the same turn-on resistance. In the device, the design size ratio of M_{17}:M_{16}:M_{15} is 2:1:1. The second integrated slope occurs when M_{16} and M_{19} turn on and M_{17} and M_{20} turn off. C_{int} is then $C_1 + C_2$. The third occurs when M_{16} and M_{19} turn off and M_{17} and M_{20} turn on, in which case C_{int} is $C_1 + C_3$. The last occurs when M_{16}–M_{17} and M_{19}–M_{20} turn on, resulting in C_{int} being $C_1 + C_2 + C_3$. Because the capacitance ratio of C_1 to ($C_1 + C_2$) to ($C_1 + C_3$) to ($C_1 + C_2 + C_3$) is 1:2:3:4, the ratio between integrated slopes is 12:6:4:3.

$$V_{OUT} = V_{OUTP} - V_{OUTN} = -\frac{1}{R_4 C_{int}} \int V_{INN} dt + \frac{1}{R_6 C_{int}} \int V_{INP} dt = \frac{1}{R_4 C_{int}} \int V_{IN} dt \quad (3)$$

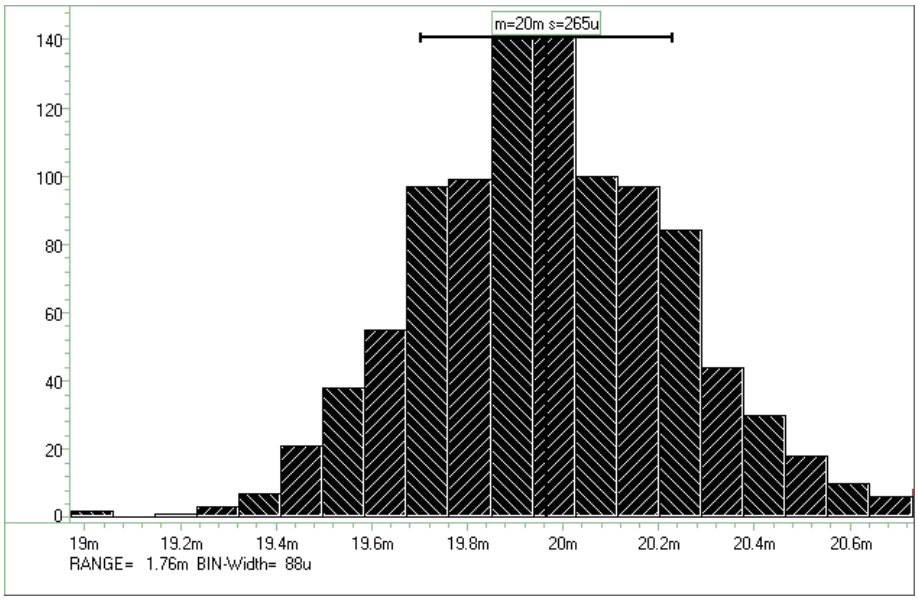


Figure 13. Hspice Monte Carlo simulation of the amplifier with 1000 samples.

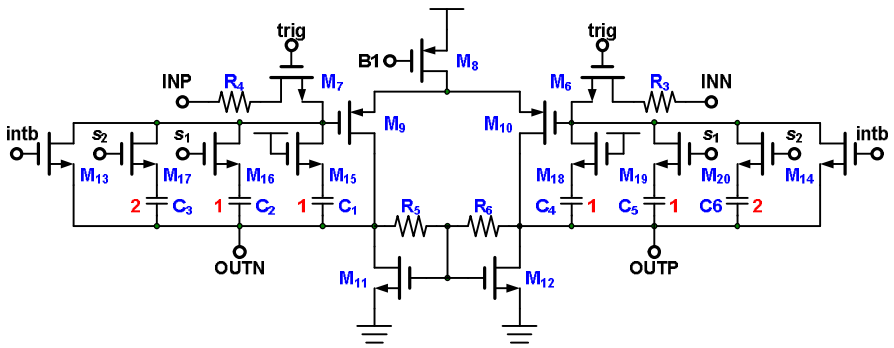


Figure 14. Integrator with multiple switched capacitors.

3.3. Trigger Generator

The trigger generator comprises a differential difference amplifier M_{21}–M_{28}, R_7 [21], R_8, and a comparator M_{29}–M_{41}, as illustrated in Figure 15. The positive output terminal of the differential difference amplifier is the gate of M_{30}, and the negative output terminal is the gate of M_{31}. The voltage of the positive output terminal is expressed in Equation (4), the voltage of the negative output terminal is expressed in Equation (5), and the differential voltage of the output terminal is expressed in Equation (6). Using the result of the differential difference amplifier, the comparator generates a trigger signal.

$$v_{op} = -\left(v_{INN} \times g_{mp} + v_{ref1} \times g_{mp}\right) \times r_{on} \quad (4)$$

$$v_{on} = -\left(v_{INP} \times g_{mp} + v_{ref2} \times g_{mp}\right) \times r_{on} \quad (5)$$

$$v_{op} - v_{on} = \left[\left(v_{INP} - v_{INN}\right) - \left(v_{ref1} - v_{ref2}\right)\right] \times g_{mp} \times r_{on} \quad (6)$$

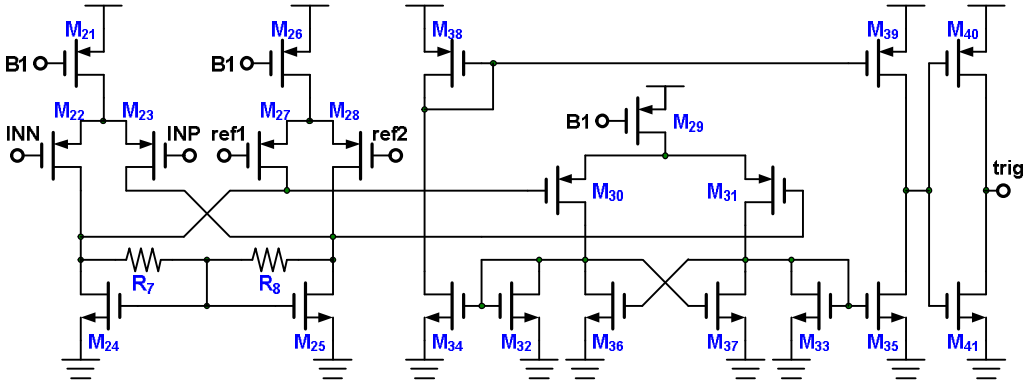


Figure 15. Differential difference input trigger generator.

The comparator comprises differential inputs (M_{30} and M_{31}), a cross-coupled latch (M_{36} and M_{37}), a diode-connected load (M_{33} and M_{34}), a current summary (M_{34}, M_{35}, M_{38}, and M_{39}), and an inverter-based output buffer (M_{40} and M_{41}). When the gate voltage of M_{30} is higher than that of M_{31}, the drain current of M_{30} is lower than that of M_{31}; the cross-coupled latch then reduces the drain voltage of M_{30} and increases the drain voltage of M_{31}. The current summary part summarizes the drain currents of the diode-connected loads M_{32} and M_{33}, and the inverter-based output buffer increases the level of the output voltage to the supply voltage level. If the gate voltage of M_{30} is lower than that of M_{31}, the level of the output voltage of the comparator decreases to the ground voltage level.

3.4. Bias Circuit

The bias circuit, depicted in Figure 16 [20], has a bias part and a start-up part. Because the bias part comprises P-type and N-type current mirror structures of M_{b1}–M_{b6} and R_b, the circuit operates in two static states. One static state involves current, whereas the other does not. The circuit requires a start-up circuit to push the bias part into the correct operation mode. When the supply voltage turns on and the bias part is in the incorrect operation mode, the voltages V_{B2} and V_{B3} are low. When V_{B3} is low, M_{s5} turns off, the diode-connected M_{s1} turns on M_{s2}, and M_{s2} and the diode-connected M_{s3} turn on M_{s4} to increase V_{B2} and V_{B3} to the correct operation voltage. Because V_{B3} is in the correct operation mode, M_{s5} turns on and M_{s2} turns off, and M_{s4} turns off. The start-up part turns off, and the bias part is then operating in the correct mode. The bias circuit biases the amplifier depicted in Figure 12, the integrator displayed in Figure 14, and the trigger generator illustrated in Figure 15. To ensure favorable matching of the bias device M_{b2}, the amplifier's M_1, the integrator's M_8, and the trigger generator's M_{21}, M_{26}, and M_{29} must have the same width, length, symmetry, and device layout direction, but the device multiple can be different. Without using resistor R_b, the current mirror loop involving M_{b1}–M_{b6} gives positive feedback. Adding the resistor R_b and the multiple M_{b6} results in the loop giving negative feedback. The bias current I_{b2} is determined by the resistance R_b and the size of M_{b5}–M_{b6}, as expressed in Equation (7) [20]. The bias current I_{b2} has extremely low sensitivity to supply voltage variation and noise.

$$I_{b2} = \frac{2}{\mu_n C_{ox}(W/L)_{b5}} \cdot \frac{1}{R_b}\left(1 - \frac{1}{\sqrt{(W/L)_{b6}/(W/L)_{b5}}}\right) \quad (7)$$

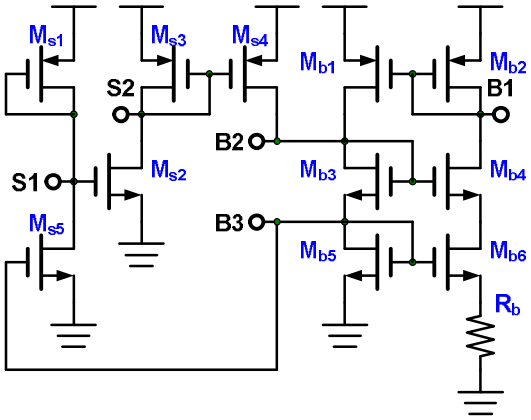


Figure 16. Bias circuit.

3.5. Reset Circuit

The integrator illustrated in Figure 14 starts to integrate when it receives the trigger signal and retains the result until the SAR ADC has completed its conversion. The reset circuit displayed in Figure 17 combines the trigger signal from the trigger circuit with the reset signal from the SAR ADC and then generates the reset signals int and intb, which reset the integrator. The reset circuit operates in four states: reset, hold after reset, trigger, and hold after trigger. In the reset state, a reset signal pulse enters node rst. And the node trig is 0. M_{43}, M_{44}, M_{46}, and M_{49} turn on, and the others turn off. The node int changes to 0, and the node intb changes to 1. In the hold after reset state, the nodes rst and trig are 0, and M_{46}–M_{47} turn off. M_{42}–M_{45} and M_{48}–M_{49} comprise a latch circuit and keep the int and intb voltage levels at 0 and 1, respectively. In the trigger state, a trigger signal pulse is sent to the node trig. In the meantime, the node rst is 0. M_{42}, M_{45}, M_{47}, and M_{48} turn on, and the others turn off. The node int changes to 1, and the node intb changes to 0. In the hold after trigger state, the latch circuit keeps the int and intb voltage levels at 1 and 0, respectively.

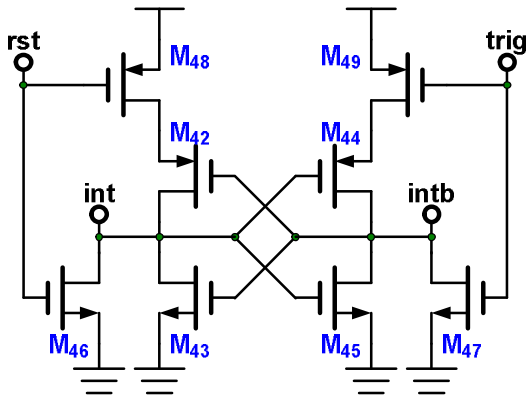


Figure 17. Reset circuit.

3.6. Nonbinary SAR ADC

The block diagram of the SAR ADC is presented in Figure 18. The SAR ADC comprises a comparator, a clock generator, a capacitor array DAC (CDAC), and a nonbinary-to-binary converter (NBC). The clock generator is initiated when the falling edge of the trigger signal is reached and generates the timing clock that controls the CDAC, comparator, and

NBC. The comparator detects the difference in voltage between the positive terminal and negative terminal of the CDAC. The CDAC follows the signal from the clock generator and comparator to switch the capacitors; the weight size of the capacitors is depicted in Figure 11. The data output from the ADC to the PSSR input are 10b binary code, which is depicted in Equation (8).

$$\begin{aligned} ADC_{OUT} = \quad & 512 \cdot d_9 + 256 \cdot d_8 + 128 \cdot d_7 + 64 \cdot d_6 + 32 \cdot d_5 \\ & +16 \cdot d_4 + 8 \cdot d_3 + 4 \cdot d_2 + 2 \cdot d_1 + 1 \cdot d_0 \end{aligned} \tag{8}$$

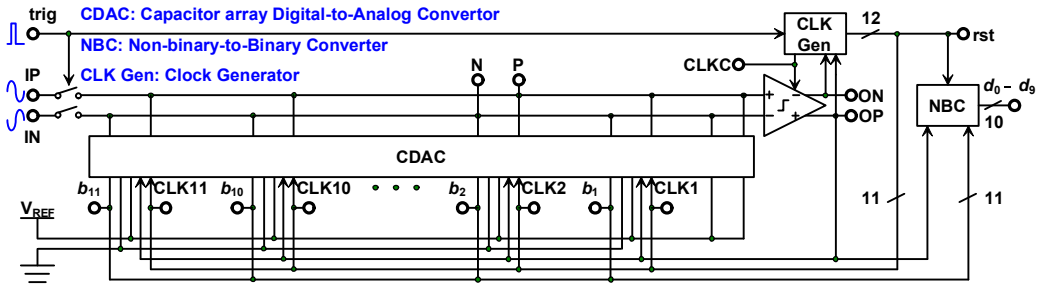


Figure 18. Nonbinary SAR ADC block diagram.

3.7. NBC

The NBC, illustrated in Figure 19, comprises many counters that convert the nonbinary comparator results into binary digital code. The input of the NBC is depicted in Equation (9). Each piece of nonbinary code can be split into binary parts; for example, $404 \times b_{11}$, $248 \times b_{10}$, $152 \times b_9$, $88 \times b_8$, $52 \times b_7$, $20 \times b_5$, and $12 \times b_4$ can be split into $(256 + 128 + 16 + 4) \times b_{11}$, $(128 + 64 + 32 + 16 + 8) \times b_{10}$, $(128 + 16 + 8) \times b_9$, $(64 + 16 + 8) \times b_8$, $(32 + 16 + 4) \times b_7$, $(16 + 4) \times b_5$, and $(8 + 4) \times b_4$, respectively. The nonbinary code is split into binary parts. Counters are then employed to summarize the same-order binary parts. The results of the counter are a binary result and carry-out data. The carry-out data must be summarized with the next-order binary code. Because the comparator results for b_0 and b_1 are binary, they do not need to be converted. In the last stage, an OR gate is used to obtain a summary of the carry-out data (denoted c_{72}) and the carry-out data of the full adder [17].

$$\begin{aligned} NBC_{IN} = \quad & 404 \cdot b_{11} + 248 \cdot b_{10} + 152 \cdot b_9 + 88 \cdot b_8 + 52 \cdot b_7 + 32 \cdot b_6 \\ & +20 \cdot b_5 + 12 \cdot b_4 + 8 \cdot b_3 + 4 \cdot b_2 + 2 \cdot b_1 + 1 \cdot b_0 \end{aligned} \tag{9}$$

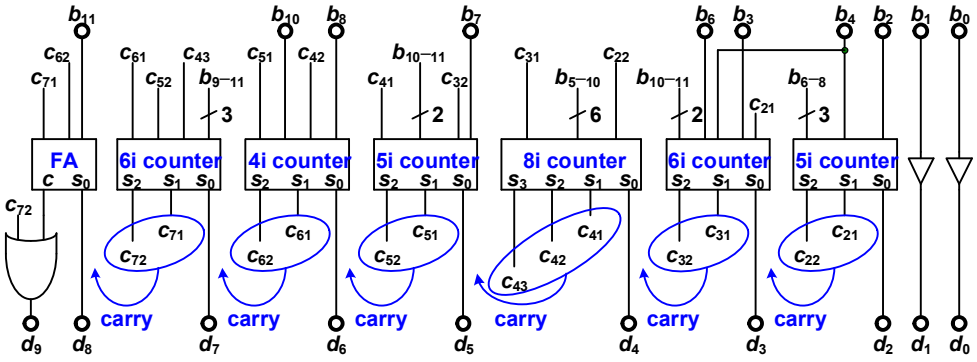


Figure 19. NBC of nonbinary SAR ADC.

3.8. PSSR

Because the application has 16 channels, the area cost of the parallel-out data solution is enormous, and the data transmission line is overly large. This study employs serial-out data to prevent those problems. The PSSR illustrated in Figure 20 is used to convert the data from the parallel-in to the serial-out form. An off-chip clock is required to control the

PSSR. An AND gate and the D-flip-flops (DFFs) DF_{20}–DF_{23} divide the input clock by 12, and DF_{24} generates the sampling clock for loading parallel data. The NOR gate generates the serial-out clock for off-chip digital I/O reception of serial-out data. The PSSR stores data in parallel by using DFFs DF_0–DF_9 and transfers the serial-out data by using multiplexes and DFFs DF_{10}–DF_{19}.

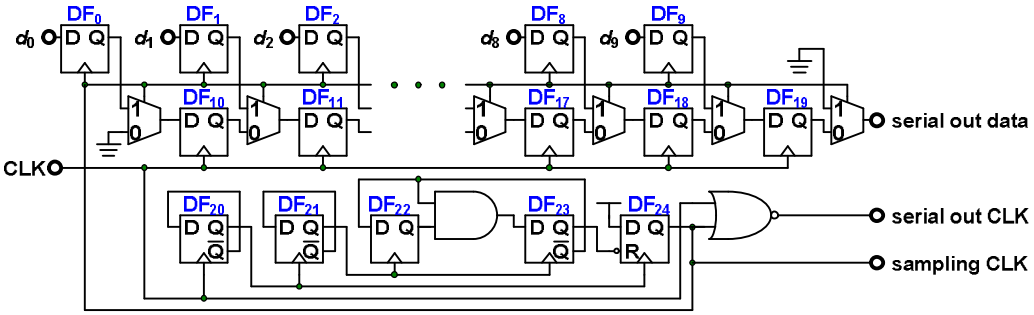


Figure 20. PSSR.

4. Measurement Results

The designed chip is implemented with CMOS 0.18 µm 1P6M technology. A photograph of the die is presented in Figure 21. The chip is 1.444 mm × 10.568 mm and contains a 16-channel front-end readout circuit for a radiation detector. Regarding the chip's static-state performance, the minimum differential nonlinearity (DNL) and integral nonlinearity (INL) of the nonbinary SAR ADC are −0.32 and −0.43 LSB, whereas the maxima of these indicators are 0.33 and 0.37 LSB, respectively, as revealed in Figure 22. Regarding the chip's dynamic performance, the spurious-free dynamic range, signal-to-noise ratio, signal-to-noise-and-distortion ratio, and effective number of bits (ENOB) of the nonbinary SAR ADC when a 500-KHz sine signal with a 1 MS/s sampling rate is input are 68.8 dB, 57.41 dB, 57.41 dB, and 9.24 b, respectively, as detailed in Figure 23. The power consumption of the SAR ADC is 23.5 µW. The figure of merit (FoM) is calculated using Equation (10) from [22]. The FoM of the SRA ADC is 38.9 fJ/conversion step.

$$FoM_W = \frac{Power}{2^{ENOB} \times f_{Sampling}} \, J/conv. - step \tag{10}$$

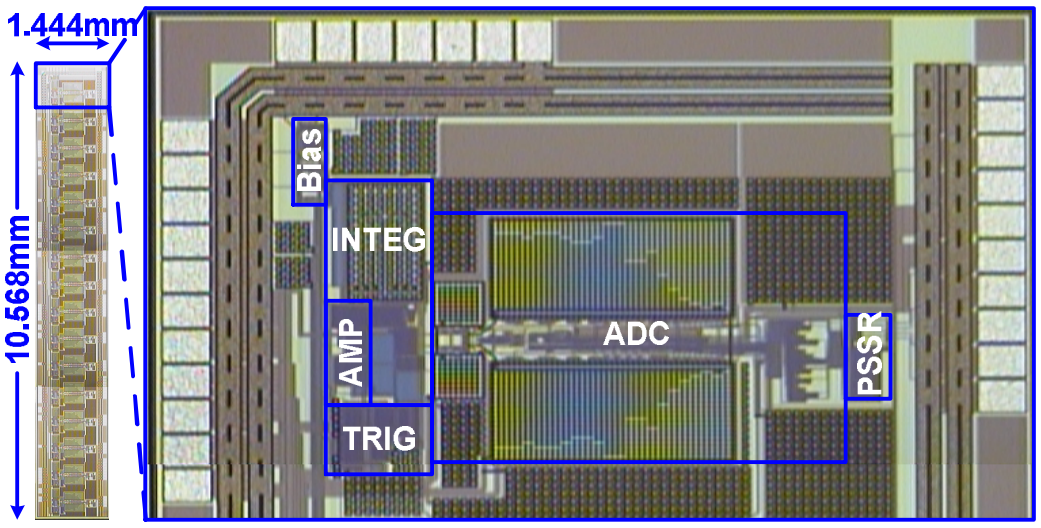


Figure 21. Die photograph.

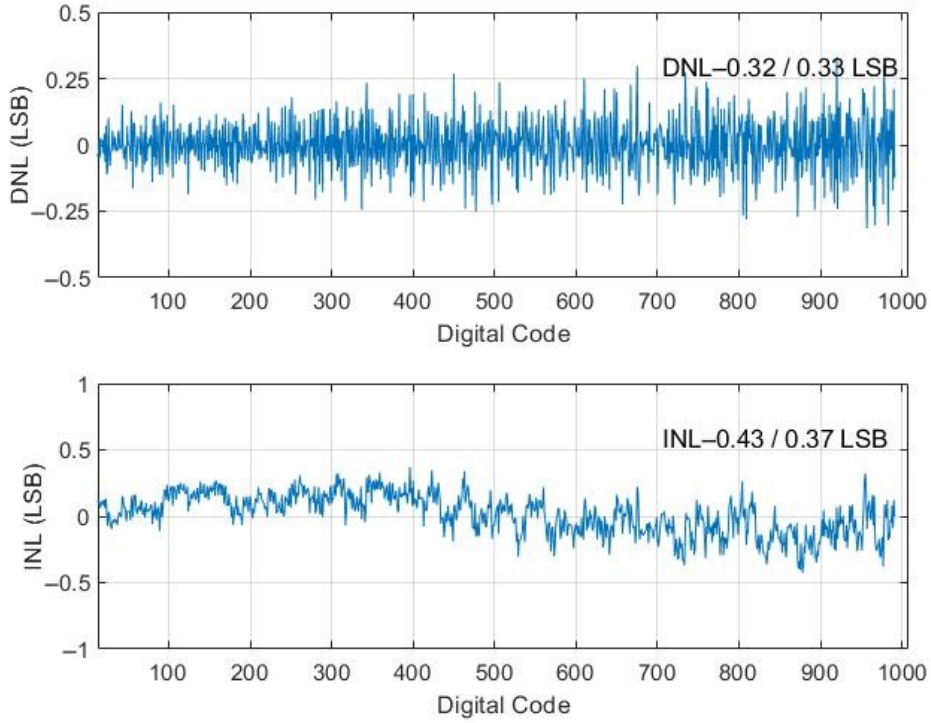


Figure 22. Static-state performance of nonbinary SAR ADC.

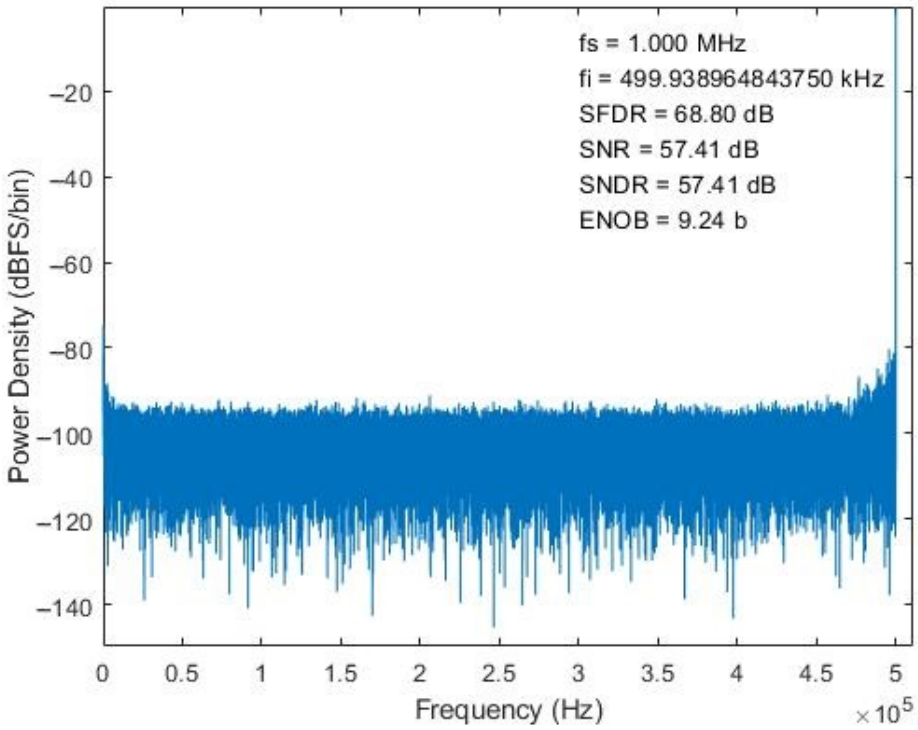


Figure 23. Dynamic performance of nonbinary SAR ADC.

The environment used for measurement in this study is depicted in Figure 24. The input signal of the chip on board device under test is provided by a function generator. The output signal is input to an oscilloscope. Analog power and digital power are supplied by respective power supplies.

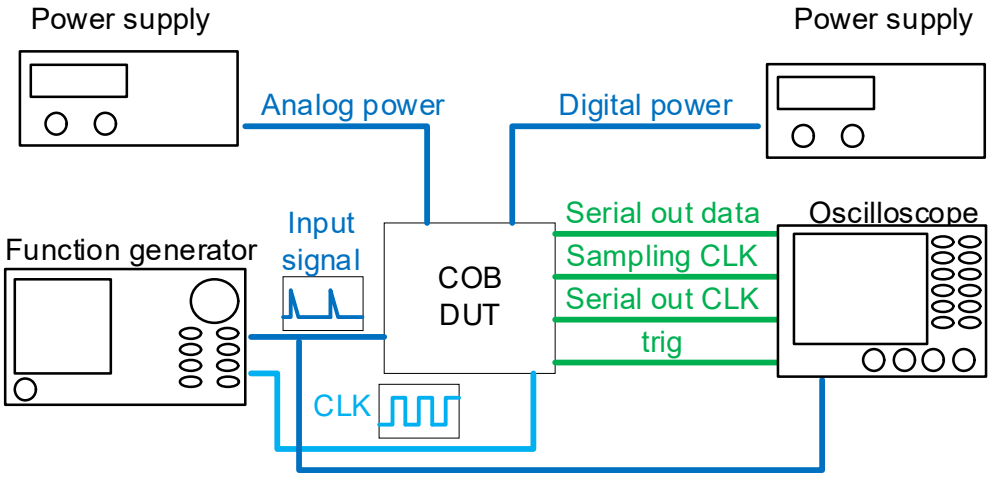


Figure 24. Measurement environment.

The entire chip test is depicted in Figure 25. When the input signal rises and falls, the trigger signal turns on and off, respectively. The serial-out data transfer the detection result with the sampling clock and the serial-out clock. Conversion curves with different integrated slopes are displayed in Figure 26. The maximum cover range of the peak-to-peak current pulse is 750 µA. The resolution of the conversion curve and the minimum coverage of testing, described in Figure 27, are 208.3 nA and 20 µA, respectively. When the shaping time is 200 ns, the input dynamic is 2–75 pC. The nonlinearity of the conversion curve versus the peak current in the digital output is depicted in Figure 28; the maximum nonlinearity is 1.8%. The conversion curves of 16 channels from the input peak current to the digital output are depicted in Figure 29. Because of the process variation of resistors and capacitors in the integrator, the slope for each channel is different. The nonlinearity of the aforementioned conversion curves is depicted in Figure 30. The maximum nonlinearity is found to be 1.8%.

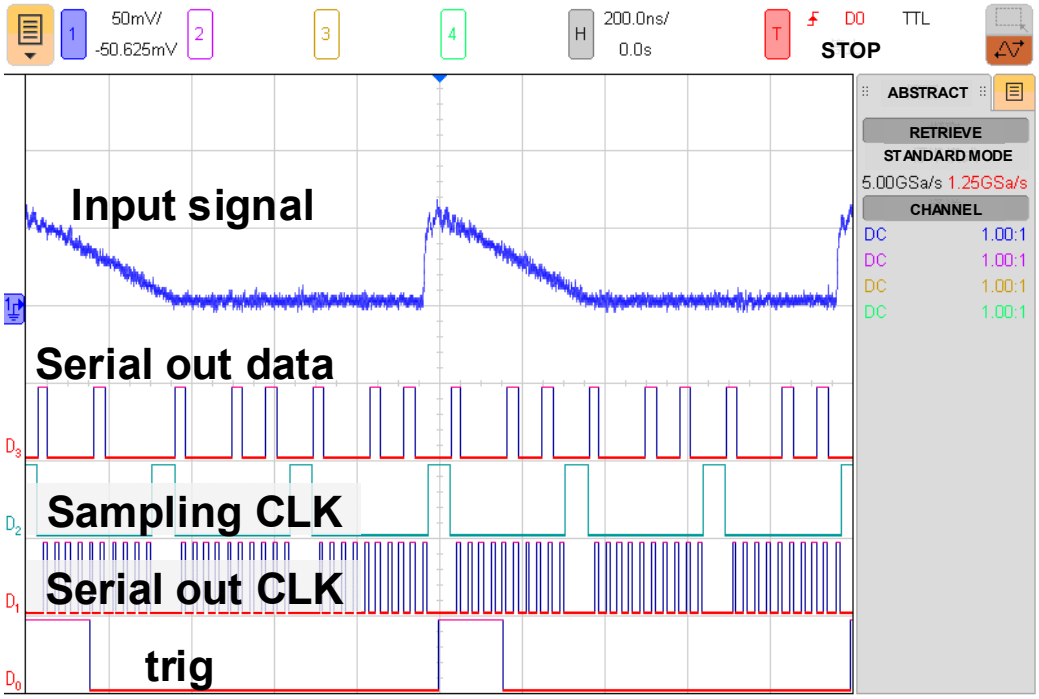


Figure 25. Output signal on an oscilloscope.

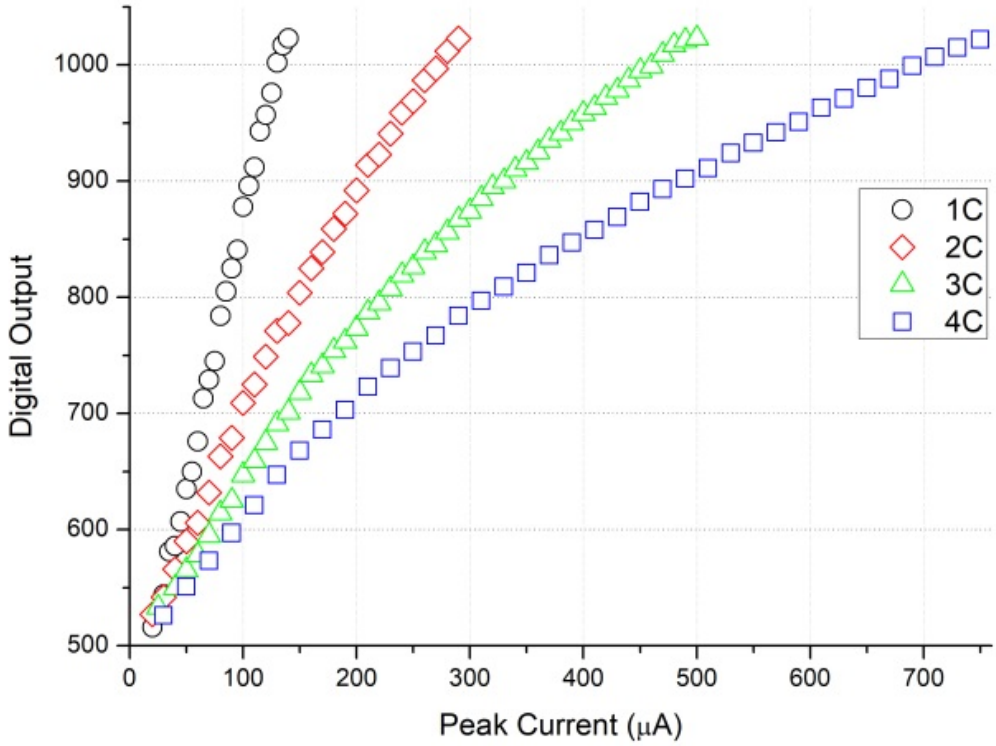


Figure 26. Peak current to digital data with different integration coefficients.

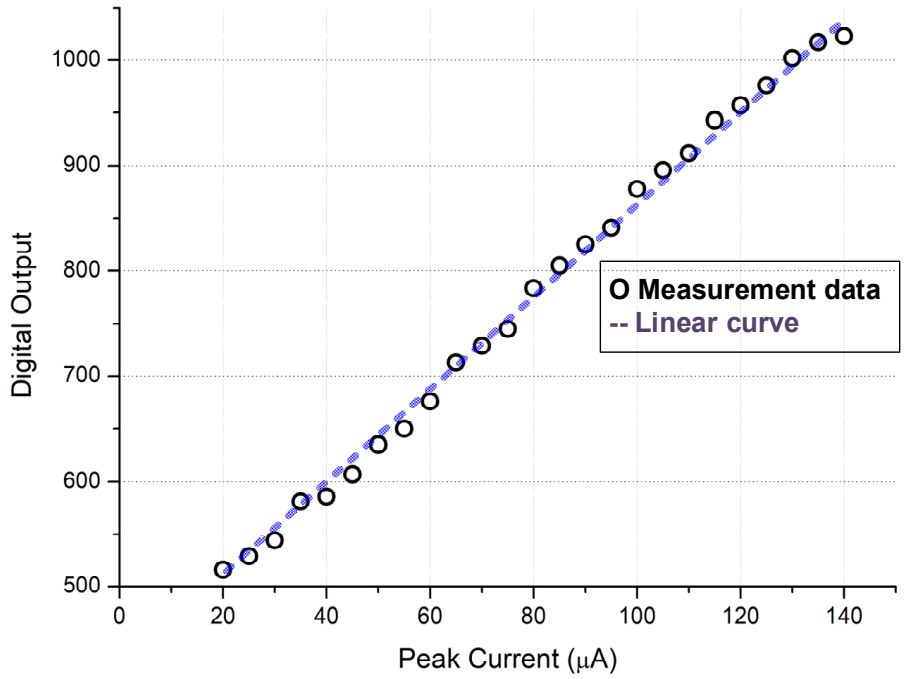


Figure 27. Conversion curve from input peak current to the digital output.

The power consumption is 19 mW/channel for a 3-V supply voltage. The power consumption of the amplifier, integrator, trigger, ADC, and PSSR is 3.14, 4.98, 8.20, 0.03, and 0.1 mW, respectively. The proportion of power consumed by each block is depicted in Figure 31.

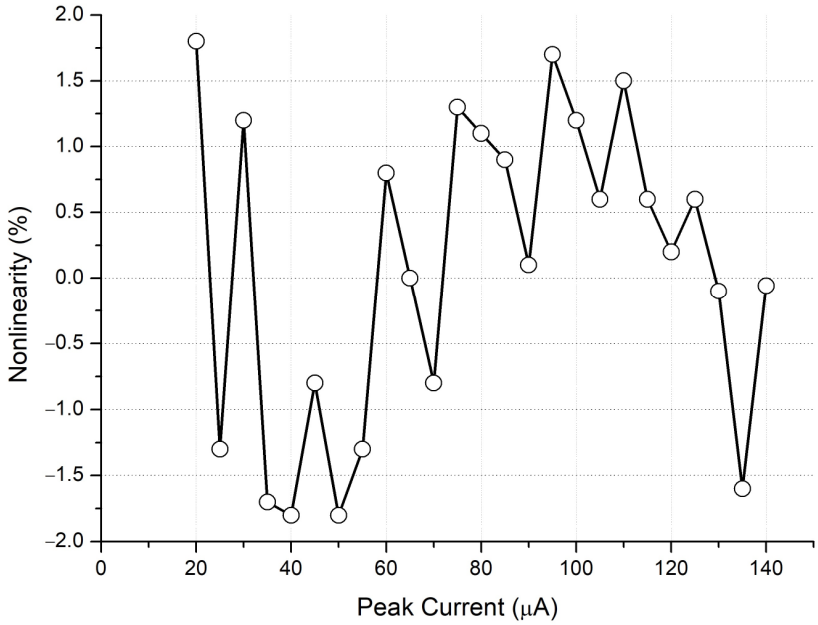


Figure 28. Nonlinearity of conversion curve from input peak current to digital output.

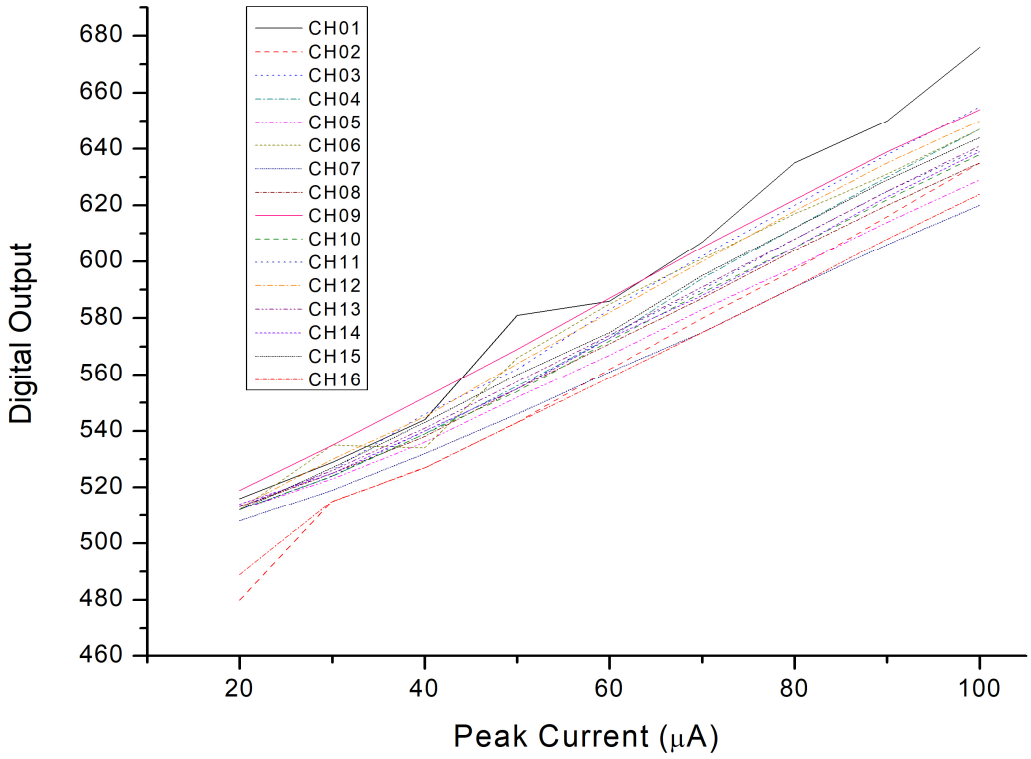


Figure 29. Conversion curves of 16 channels from input peak current to digital output.

The performance of the proposed design and that of other designs [11–13,23,24] are summarized in Table 2. The number of channels in the proposed design is 16, which is higher than the number in the previously reported designs [11,13,23,24]. The input charge range, 2/75 pC, is larger than that in three other designs [13,23,24]. The nonlinearity of the conversion curve, 1.8%, is smaller than that in two other designs [11,23] and close to that in another [13]. The sampling rate per channel, 1 MS/s, is better than that in two other designs [12,23] and the same as that in another [13]. The DNL and INL in the present study—in the ranges −0.32 to 0.33 and −0.43 to 0.37, respectively—are better than those in two other designs [11–13]. The resolution of the ADC, 10 b, is better than that in

two other designs [12,13]. The ENOB, 9.24 b, is better than that in one other design [12]. The ADC power consumption per channel, 23.5 µW, is better than that in one other design [12] and close to that in another [13]. The FoM of the proposed ADC, 0.0389 pJ/conversion step, is better than that in another design [12].

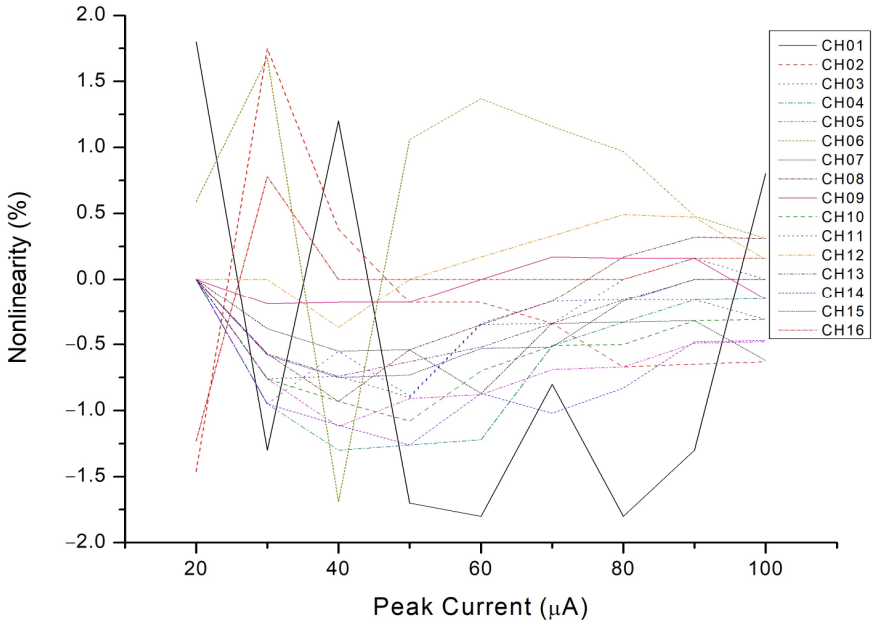


Figure 30. Nonlinearity of conversion curves of 16 channels from input peak current to digital output.

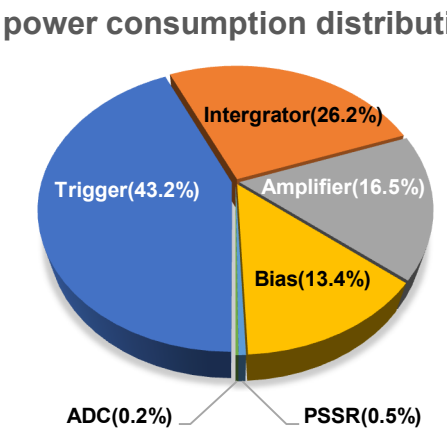


Figure 31. Power consumption distribution.

Table 2. Summary of performance of proposed and other designs.

	This Work	[11]	[12]	[13]	[23]	[24]
Technology	0.18 µM	0.35 µM	0.18 µM	0.18 µM	-	0.35 µM
Supply voltage (V)	3/1 V	3.3	3.3	1.8	±15/3 V	5/1 V
Power per channel (mW)	19	15	15	0.02	-	30
Number of channels (unit)	16	10	64	1	1	8
Shaping time (ns)	200	280	300	100	10,000	5/10
Input charge range (pC)	2/75	2.4/104	0.48/520	0.25/17	0.01/33	0/3
Nonlinearity of converting curve (%)	1.8	<3		1.7	5	-
ADC type	SAR	-	Pipeline	Integrated	SAR	TDC
Sampling rate per channel (MS/s)	1	-	0.39	1	20 k	
DNL of ADC (LSB)	−0.32/0.33	-	−0.62/0.67	−0.36/0.12	-	

Table 2. *Cont.*

	This Work	[11]	[12]	[13]	[23]	[24]
INL of ADC (LSB)	−0.43/0.37	-	−0.39/0.72	−0.38/0.5	-	
Resolution of ADC (b)	10	-	8	8	12	40 psec
ENOB of ADC (b)	9.24	-	6.03	-	-	
ADC power per channel (μW)	23.5	-	390.63	20	-	-
FoM of ADC (pJ/conversion step)	0.0389	-	15.303	-	-	-

5. Conclusions

To scale down a radiation detector such that it can be incorporated into a wearable device, in this study, integrated circuit technology was employed to fabricate a 16-channel front-end readout chip for such a detector, and chip performance tests were conducted. The DNL, INL, ENOB, and power consumption of the proposed ADC are −0.32 to 0.33, −0.43 to 0.37, 9.24 b, and 23.5 μW, respectively. The resolution is 208.3 nA, and the cover range of the input current pulse from peak to peak is 20–750 μA with multiple integrated slopes. The equal input dynamic range is 2–75 pC, and the maximum nonlinearity is 1.8%. This chip is suitable for use in radiation detection, the IoT, and wearable biomedical applications.

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