electronics

MDPI

Article

Investigation of Trap Density Effect in Gate-All-Around Field Effect Transistors Using the Finite Element Method

Maissa Belkhiria [1], Fatma Aouaini [2,*], Shatha A. Aldaghfag [2], Fraj Echouchene [1] and Hafedh Belmabrouk [3]

[1] Laboratory of Electronics and Microelectronics, Faculty of Science of Monastir, University of Monastir, Monastir 5019, Tunisia; maissabelkhiria@gmail.com (M.B.); frchouchne@yahoo.fr (F.E.)
[2] Department of Physics, College of Science, Princess Nourah bint Abdulrahman University, P.O. Box 84428, Riyadh 11671, Saudi Arabia; saaldaghfaq@pnu.edu.sa
[3] Department of Physics, College of Science at Zulfi, Majmaah University, P.O. Box 1712, Zulfi 11932, Saudi Arabia; ha.belmabrouk@mu.edu.sa
* Correspondence: fasaidi@pnu.edu.sa

Abstract: Trap density refers to the density of electronic trap states within dielectric materials that can capture and release charge carriers (electrons or holes) in a semiconductor channel, affecting the transistor's performance. This study aims to investigate the influence of trap density on the electrothermal behavior of nanowire gate-all-around GAAFET devices. The numerical solution of Poisson's equations and continuity equations, coupled with the heat conduction model, has been used to predict the temperature inside the GAAFET device. The finite element method has been used to discretize the semiconductor equations. Investigations have been carried out on a number of physical and geometric parameters, such as oxide thickness, nanowire radius, and gate length. Their effects on output characteristics and device temperature have been discussed. A thinner oxide thickness, lower device radius, and longer channel length led to a higher current flow. Results also reveal that high trap densities can have significant impacts on the degradation of electronic devices, particularly in the context of semiconductor devices like transistors.

Keywords: semiconductor equation; finite element method; GAAFET; simulation; trap density

check for updates

Citation: Belkhiria, M.; Aouaini, F.; A. Aldaghfag, S.; Echouchene, F.; Belmabrouk, H. Investigation of Trap Density Effect in Gate-All-Around Field Effect Transistors Using the Finite Element Method. *Electronics* **2023**, *12*, 3673. https://doi.org/10.3390/electronics12173673

Academic Editors: Gerard Ghibaudo and Elias Stathatos

Received: 12 July 2023
Revised: 23 August 2023
Accepted: 29 August 2023
Published: 31 August 2023

Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

In search of higher device performance and lower power consumption, new structures such as FinFETs [1] and Pi-gate [2], tri-gate [3], Omega-gated [4], and gate-all-around (GAA) MOSFETs [5] have been reported [6,7]. GAAFET structures are seen as the near-term future of integrated circuits as they provide highly electrostatic gate control [8]. GAAFET transistors have a gate-all-around structure, where the gate surrounds the semiconductor channel. This structure demonstrates an enhancement in gate control that reduces SCEs, with lower leakage currents and operational voltages [9–11]. This results in improved performance and reduced power consumption. A comparative electrothermal study of GAAFETs and FinFETs has been proposed by Zhao et al. [12]. A higher I_{on} current and a lower I_{off} current are obtained for the GAAFET structure at V_d = 0.7 V and V_d = 0.05 V. The electric properties, including transfer characteristics, output characteristics, gain, mobility roll-off, subthreshold slope, and drain-induced barrier lowering (DIBL), in GAAFET structures have been analyzed by Mohan et al. [13]. The selection of adequate gate material and architecture has been proposed by several authors to improve the device's performance [14–18]. The various technology nodes and their limitations have been presented by Narula et al. [19] (Table 1). A comparative study by Kumar et al. [20] reveals that the GS-GAA structure shows the most improved results. However, the thermal resistance of GAAFETs [21] compared with planar transistors [22,23] and FinFETs [24–27] shows that GAAFETs have significantly higher thermal resistance (Figure 1). This parameter has a direct influence on the device performance and overall functionality.

Table 1. Node issues and solutions of the different technologies.

Node	Best Device	Issue	Solution
<0.1 µm	Bulk MOSFET	SCE, low drive current	- Strained SiGe - Metal gate - High-k dielectric
0.1 µm–32 µm	SOI MOSFET	Power leakage current	- Ultra-thin body SOI MOSFET
32 µm–10 nm	FinFET	SCE are prominent	- Use of multi-gate material - Stacked oxide
<10 nm	GAA	Power, cost	- Vertically stacked GAA - Work function engineering - High–k dielectric

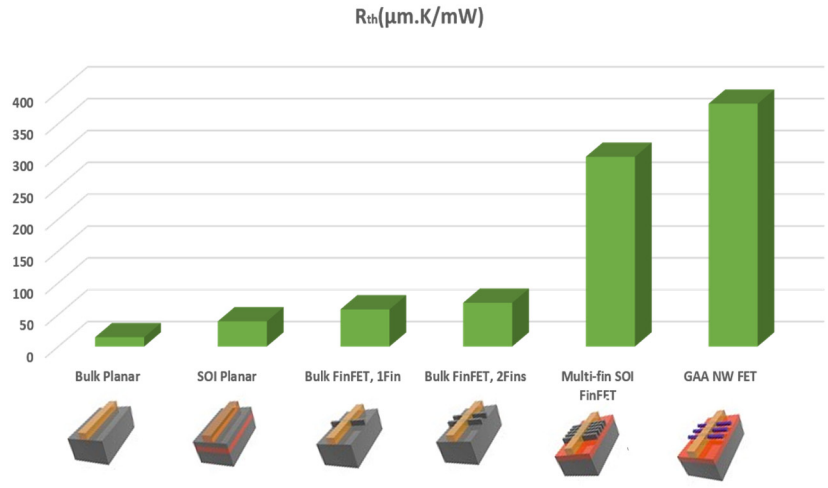

Figure 1. Thermal resistance of Bulk planar, SOI planar, FinFETs, and GAAFET devices.

This effect is mainly due to the intensive scaling down of field-effect transistors. As a result, this higher thermal resistance could induce many issues that cause degradation of device performance, including a tunnel effect, increased power consumption, and excess heat production [28–33]. When the oxide SiO_2 is scaled down, gate current leakage occurs as a result of carriers being able to tunnel through the gate dielectric [34]. Therefore, since SiO_2 is inappropriate for nanodevices, the use of high-k materials is essential for overcoming the limitations of SiO_2, which faces challenges in maintaining sufficient gate control in modern nanoscale transistors. In our previous work [35], we have compared the behavior of several high-k materials such as HfO_2, ZrO_2,La_2O_3, and Al_2O_3. We have shown that Al_2O_3 as a substitute produces significant reductions in thermal effects and can be used as a potential candidate in transistor devices. While high-k materials offer advantages in improving device performance, they tend to have higher trap densities compared to SiO_2. The presence of traps in the dielectric can lead to charge trapping, affecting the overall charge control in the transistor channel. In fact, the traps are defined as energy levels in the bandgap of the semiconductor. These traps can capture and release charge carriers. This phenomenon can cause several reliability problems that affect the device's electrical and thermal characteristics. When trapped carriers are later released back into the channel, it leads to a change in the device's threshold voltage and electrical characteristics. For that reason, it is crucial to account for trap density and its effects in order to accurately model and simulate the electrothermal behavior of GAAFET devices.

Device designers and researchers often use advanced simulation techniques, which include trap models, to study the impact of traps on a device's performance under different operating conditions [36–39]. The effects of interface trap charges (ITCs) on doping-less

NW-based devices were addressed for the first time by Kumar et al. [40]. The proposed device performed better in the presence of positive ITCs. The influence of interface traps on the I–V characteristics of InAs-nanowire-FETs and MOSFETs has been investigated by Pala et al. [41]. They demonstrated that traps have a significant impact on subthreshold slopes and that even a single trap can deteriorate the subthreshold reverse-slope of an InAs nanowire.

The simulation of nanoscale devices is computationally intensive due to the fine mesh needed to accurately capture the intricacies of small-scale structures. Several mesh-free methods have been developed to solve physical and engineering problems [42–46]. The finite element method has gained extensive attention due to its ability to solve partial differential equations for difficult problems with irregular geometries [47,48]. This method is based on the discretization of partial differential equations (PDEs) [49], which describe space-and-time-dependent physical problems. The solution of the equation is an approach to the real solution. Previously, we analyzed the self-heating effect in GAAFETs [50] using the finite element method. The finite element discretization has been used to tackle the effect of Joule heating in a conductive-bridge random-access memory (CBRAM) for the single-phase-lag heat conduction model [51].

This paper aims to contribute to the investigation of the trap density effect on the electro-thermal behavior of GAAFETs. High-k dielectric Al_2O_3 has been used as the gate dielectric, and the finite element method has been used for modeling semiconductor equations, coupled with the heat conduction model. The device's structure and the numerical method are developed in Section 2. The results are discussed in Section 3. In Section 4, the conclusions of this work are presented.

2. Device Structure and Simulation Approach

2.1. Device Structure and Flow Process

Figure 2a shows the entire 3D GAAFET structure. Between the two outer gates, a thin oxide layer Al_2O_3 surrounds the silicon channel region. The fabrication processes of the GAAFET structure are illustrated in Figure 2b. More details about the process flow is reported with [52]. A 2D axial-symmetry schematic cross-sectional view of the structure is seen in Figure 2c.

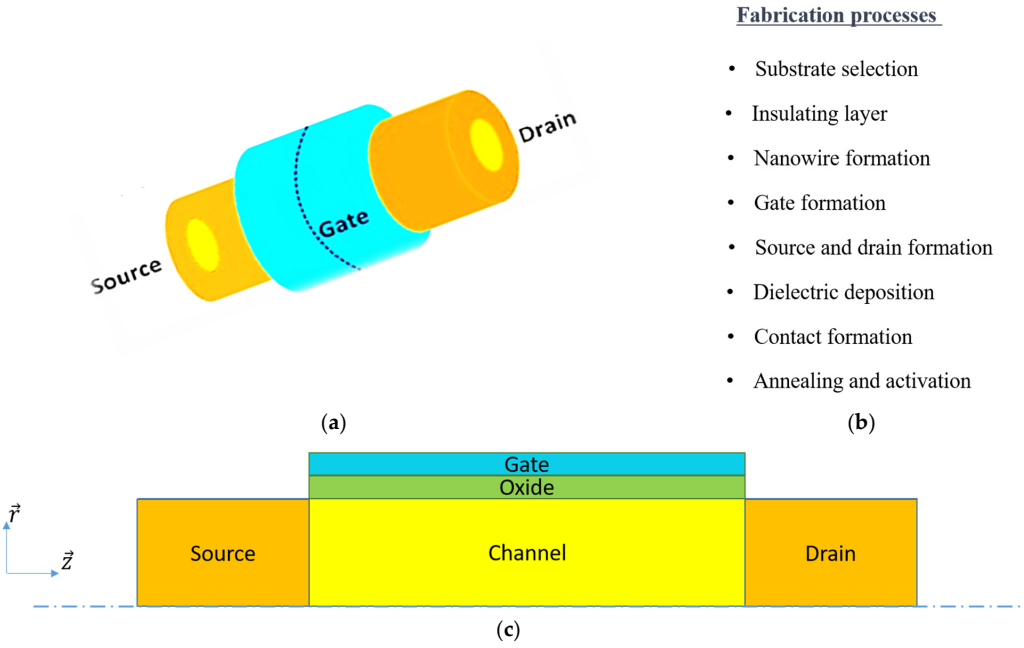

Figure 2. GAAFET 3D geometry structure (**a**), fabrication processes (**b**) and 2D axial-symmetry schematic cross-sectional view (**c**).

As the 3D structure presents an axial symmetry around the z-axis, a 2D axial-symmetry structure is considered in this work. The supply voltage to the device is 0.5 V and the oxide thickness is 2 nm. The source/drain doping concentration is 1×10^{17} cm^{-3}, the channel doping is 1×10^{20} cm^{-3}, the device radius, R, is 5 nm, and the length of the gate, L_g, is 100 nm. Table 2 displays other physical and thermal parameters.

Table 2. Physical and thermal parameters.

Materials	λ (Wm^{-3}K^{-1})	C (MJm^{-3}K^{-1})	ε
Si	150	15	11.8
Al_2O_3	35	2.89	10

- For the semiconductor equations, as boundary conditions, a constant electrostatic potential equal to V_d is applied at the drain contact and a potential equal to V_G at the gate contact $n = n_0$, $p = p_0$, and $\varphi = V_0$ at the source and drain regions, and $\nabla n = \nabla p = \nabla \varphi = 0$ at the other boundary sides.
- For the heat conduction equation, we suppose that the devices are completely isolated. The right side, as well as the top and bottom boundaries in the GAAFET, are assumed to be adiabatic ($\nabla T = 0$). A Dirichlet boundary condition ($T_0 = 300$ K) is adopted at the gate, implicitly assuming that the heat rapidly dissipates in metallic contacts.
- A symmetric boundary is used at the symmetry axis for the electrothermal simulation.

2.2. Model Description

Semiconductor equations are based on Poisson's equation and the continuity equation of electrons and holes. The main equations are expressed as follows:

$$\nabla^2 V = -\frac{q}{\varepsilon}\left(p - n + N_D^+ - N_A^-\right) \tag{1}$$

$$\nabla . J_p + q\frac{\partial p}{\partial t} = -qR_p \tag{2}$$

$$\nabla . J_n - q\frac{\partial n}{\partial t} = qR_n \tag{3}$$

$$C\frac{\partial T}{\partial t} = \nabla(\lambda \nabla T) + H \tag{4}$$

where $[V, J_n, J_p]$ are determined from auxiliary equations:

$$\vec{E} = -\nabla V \tag{5}$$

$$\vec{J}_p = q\left(p\vec{v}_p - D_p \nabla p\right) \tag{6}$$

$$\vec{J}_n = -q\left(n\vec{v}_n - D_n \nabla n\right) \tag{7}$$

$$H = \vec{J} \cdot \vec{E} \tag{8}$$

The parameter descriptions are illustrated in Table 3.

Table 3. Parameters description.

Parameters	Description
V	Voltage
q	Electron charge
E	Semiconductor permittivity
p	Hole concentration
n	Electron concentration
T	Temperature
C	Volumetric heat capacity
λ	Thermal conductivity
H	Heat source
$J_{n,p}$	Electron and hole current densities
$D_{n,p}$	Electron and hole diffusion coefficients
$\overrightarrow{v}_{n,p}$	Electron and hole drift velocities

Spatial discretization of the semiconductor Equations (1)–(3) and heat conduction Equation (4) is carried out by the finite element method. The principle of the finite element method is to approximate an unknown to an expression with a shape function; an appropriate function interpolates the solution at the mesh nodes between the discrete values, and a function Ψ can be approximated by:

$$\psi(r,t) = \phi(r) \times \Psi_i(t) \tag{9}$$

where Ψi is the value of Ψ at the nodes i, and $\phi(r)$ is the line vector of the shape functions, which is given by:

$$\phi_i(r) = \prod_{j \neq i} \frac{r - r_j}{r_i - r_j} \tag{10}$$

The disruption of the function is defined by:

$$\delta\psi(r) = \phi^T(r)\delta\psi_i^T \tag{11}$$

where T is the transposed.

For a rectangular element with eight nodes, the desired function, ϕ, is interpolated by a quadratic polynomial (Figure 1), which depends on the variables x and y.

$$\Psi(x,y) = \mathrm{C}_1 + \mathrm{C}_2 x + \mathrm{C}_3 y + \mathrm{C}_4 x^2 + \mathrm{C}_5 xy + \mathrm{C}_6 y^2 + \mathrm{C}_7 x^2 y + \mathrm{C}_8 xy^2 \tag{12}$$

$$\phi_1(x,y) = (1-x)(1-y)(1-2y-2x) \tag{13}$$

$$\phi_2(x,y) = (1-x)(1-y)(1-2y-2x) \tag{14}$$

In our case, the approximation of the function, $\Phi = [V, p, n, T]$, can be expanded in terms of the shape function into:

$$\Phi(r,t) = \sum_{\mathrm{i}=1}^{\mathrm{N}} \Phi_i(t)\phi_i(r) \tag{15}$$

We introduced a shape function, ϕ_j, in the disturbance of the unknown function Φ, expressed as follows:

$$\phi_j = \delta\Phi(t,r) = \sum_{\mathrm{i}=1}^{\mathrm{N}} \left(\delta\Phi_i^e(t)\right)^{T_r} \left(\phi_i(r)\right)^{T_r} \tag{16}$$

where T_r is the transpose matrix. The function distribution $\Phi(r)$ inside an element $d\Omega$ is an interpolation between its nodal.

The integral form is obtained by multiplying (1–3) by ϕ_j and integrating over Ω, the region occupied by the device. After applying the divergence theorem, we find:

$$\int_{\Omega} \nabla\phi_j \left[\varepsilon\vec{\nabla}V\right]\partial\Omega - \int_{\Omega} \phi_j[q(p-n+N_A-N_D)]\partial\Omega = \int_{\Gamma} \phi_j \left[\varepsilon\vec{\nabla}V\right]\partial\Gamma \tag{17}$$

$$\int_{\Omega} \phi_j \left[\frac{\partial p}{\partial t}\right]\partial\Omega + \int_{\Omega} \nabla\phi_j \left[D_p\vec{\nabla}p - p\vec{\nu_p}\right]\partial\Omega + \int_{\Omega} \phi_j[R_p]\partial\Omega = \int_{\Gamma} \phi_j \left[D_p\vec{\nabla}p - p\vec{\nu_p}\right]\partial\Gamma \tag{18}$$

$$\int_{\Omega} \phi_j \left[\frac{\partial n}{\partial t}\right]\partial\Omega - \int_{\Omega} \nabla\phi_j \left[D_n\vec{\nabla}n + n\vec{\nu_n}\right]\partial\Omega + \int_{\Omega} \phi_j[R_n]\partial\Omega = -\int_{\Gamma} \phi_j \left[D_n\vec{\nabla}n + n\vec{\nu_n}\right]\partial\Gamma \tag{19}$$

The left terms of Equations (17)–(19) represent the boundary conditions which make the integrals over Γ vanish. After development, using Equation (4), the system of Equation (1) can be written as:

$$\begin{aligned}\int_{\Omega} \nabla\phi_j \Bigg[\varepsilon\vec{\nabla}\Bigg(\sum_{i=1}^{N} V_i(t)\phi_i(r)\Bigg)\Bigg]\partial\Omega \\ -\int_{\Omega} \phi_j \Bigg[q\Bigg(\Bigg(\sum_{i=1}^{N} p_i(t)\phi_i(r)\Bigg) - \Bigg(\sum_{i=1}^{N} n_i(t)\phi_i(r)\Bigg) + N_A - N_D\Bigg)\Bigg]\partial\Omega \\ = \int_{\Gamma} \phi_j \Bigg[\varepsilon\vec{\nabla}\Bigg(\sum_{i=1}^{N} V_i(t)\phi_i(r)\Bigg)\Bigg]\partial\Gamma\end{aligned} \tag{20}$$

Similar developments of Equations (2) and (3) give the following equation:

$$\sum_{i=1}^{N} \alpha M_{ij}\dot{\Phi}_i + \left(\beta K_{ij} + \gamma L_{ij}\right)\Phi_i + F_j = 0 \tag{21}$$

where:

$$M_{ij} = \int_{\Omega} \phi_i\phi_j\partial\Omega \tag{22}$$

$$L_{ij} = \int_{\Omega} \phi_i\nabla\phi_j\partial\Omega \tag{23}$$

$$K_{ij} = \int_{\Omega} \nabla\phi_i\nabla\phi_j\partial\Omega \tag{24}$$

$$F_j = \int_{\Gamma} \delta_{\Phi}\phi_j\partial\Gamma \tag{25}$$

$$\alpha = \begin{pmatrix} 0 \\ 1 \\ 1 \\ C \end{pmatrix}, \beta = \begin{pmatrix} 0 \\ D_p \\ -D_n \\ \lambda \end{pmatrix}, \gamma = \begin{pmatrix} 0 \\ -1 \\ -1 \\ 0 \end{pmatrix}, \text{ and } \delta_{\Phi} = \begin{pmatrix} q/\varepsilon(N_D - N_A) \\ R \\ R \\ -H \end{pmatrix} \tag{26}$$

After assembling the elementary matrices, we obtain the global matrix form:

$$[M]\alpha\dot{\Phi} + (\beta[K] + \gamma[L])\Phi + [F] = 0 \tag{27}$$

where Φ is the vector of an unknown nodal transportable quantity, M is the damping matrix, (β[K] + γ[L]) is the stiffness matrix, and F is the external flux vector.

The discretization of the ordinary differential equation gives:

$$\Phi_{n+1} = \Phi_{n-1} - \frac{2\Delta t}{\alpha M}[(\beta[K] + \gamma[L])\Phi_n + [F]] \quad (28)$$

2.3. Simulation Setup

As nanoscale devices often exhibit size-dependent behavior, it is essential to understand and accurately model size effects to predict device performance. The FEM consists of dividing the domain of interest into smaller elements (mesh) with particular attention to interfaces and contacts in order to approximate the behavior of the device. The FEM assumes that:

- The physical domain is continuous and can be represented by a finite number of elements.
- A linear relationship between stresses, strains, and displacements exists.
- The material properties are isotropic and homogeneous.

However, there could be some limitations to the application of FEM at the nanoscale. Among these, we mention the extremely small size of the structures, which requires a very fine mesh grid to capture the details. This could lead to computationally expensive models in terms of computational resources and calculation time. In such cases, careful consideration and mesh refinement are necessary. Therefore, finding a trade-off between computational time and accuracy is required for simulation problems. In our study, we use an adequate mesh, more refined at the interfaces and contacts. In addition, FEM is not ideal for accounting for quantum behaviors and often requires specialized methods based on quantum mechanics. Furthermore, FEM can face challenges in correctly dealing with boundary and interface properties that can be difficult to model accurately. In this study, the mesh has been refined so that it will be close to the positions of the atoms, meaning that the oxide–semiconductor interface is assumed to be smooth and that we do not hold the interface roughness. A linear shape function is adopted for potential, electron, and hole densities, with a relative tolerance of 10^{-6} as convergence criteria [53,54].

The numerical resolution of the electrothermal model follows the following steps:

i. The Poisson equation and the continuity equations are solved iteratively, with convergence achieved.
ii. The heat conduction equation is solved using a 300 K initial temperature assumption for the device to determine the temperature profile.

The parts of (i) and (ii) are solved iteratively to reach the convergent solution.

For ensuring the accuracy and reliability of the simulations, we have compared our numerical simulation using the finite element method with existing experimental data from the literature, reported in [55,56]. Figure 3a depicts the log scale drain current versus the gate voltage at V_d = 1 V. Hafnium dioxide (HfO_2) is considered as the gate dielectric; the other parameters are shown in the figure. Figure 3b exhibits the drain current versus the drain voltage at V_G = 0.6 V. The simulation was considered for a cylindrical GAAFET structure having a channel length of 180 and a diameter of 5 nm for a gate voltage of 0.6 V. Figure 4 illustrates a good agreement in output characteristics.

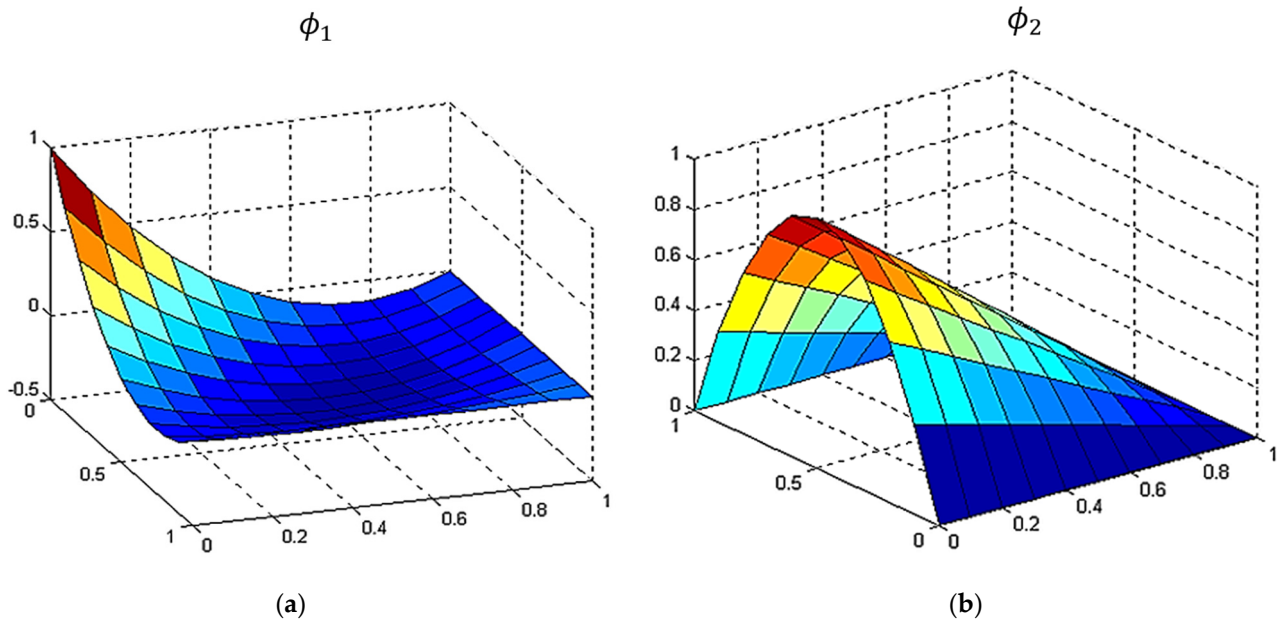

Figure 3. Quadratic interpolation of shape function in rectangular element.

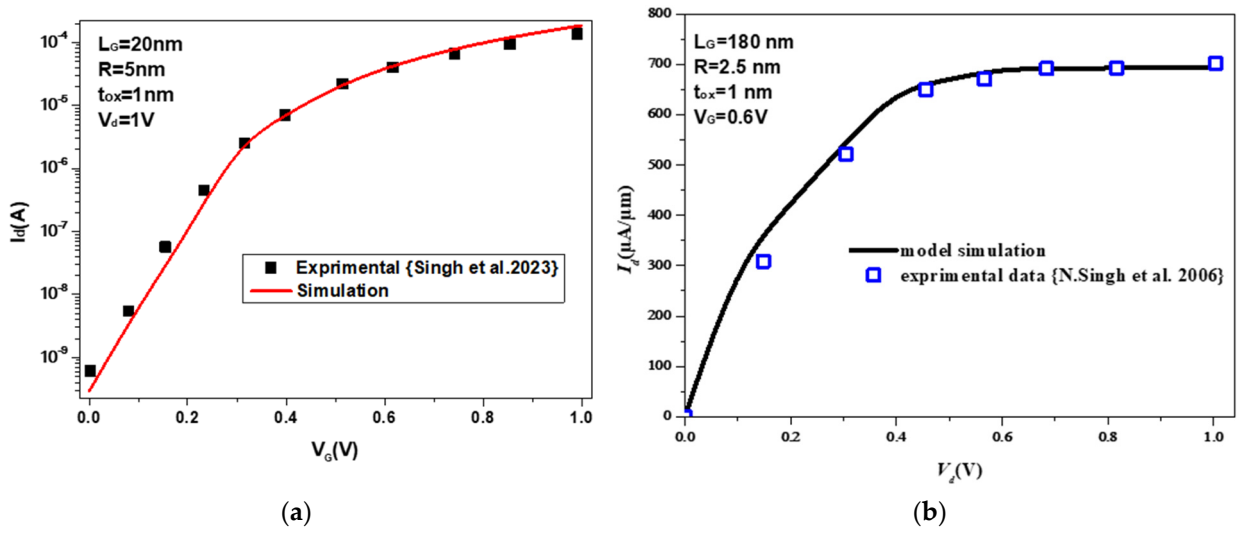

Figure 4. Log scale output characteristics of numerical simulation and experimental data [55] (**a**) and drain current versus the drain voltage compared to experimental data [56] (**b**).

3. Results and Discussion

Figure 5 depicts the output characteristics of the GAAFET in linear and logarithmic views at V_d = 0.5 V. The results are evaluated for different high-k dielectric materials with and without trap density. The drain current is enhanced with higher-k dielectric materials (ZrO_2). This improvement in the device characteristics for higher permittivity is due to better electrostatic control of the channel region, which can both enhance I_{ON} at higher gate biases and reduce I_{OFF} at low gate voltages. It is observed from this figure that the oxide SiO_2 causes one order of reduction in I_{OFF} and about 350 μA enhancement of drive current at V_D =0.5 V and V_G = 1.5 V compared to Al_2O_3. The effect of trap density is more significant for dielectric materials with lower permittivity. In the following, the investigation is carried out on the GAAFET with Al_2O_3 due to its improvement in drain current compared to SiO_2.

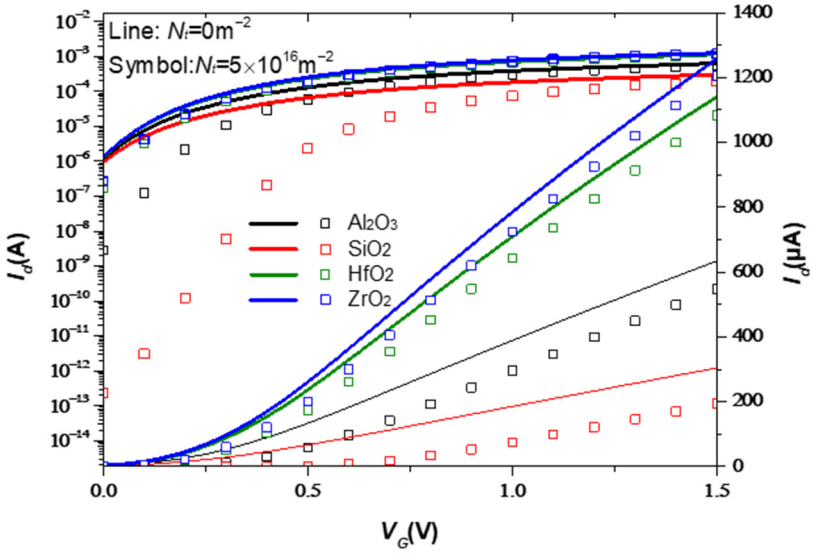

Figure 5. Logarithmic (**left** axis) and linear (**right** axis) output characteristics for different high-k dielectric materials.

In this section, we propose to investigate the effect of the trap density on the electric characteristics of the GAAFET device. Figure 6 shows the electric potential along the channel at the central cross-section of the channel for different values of N_t. The results are simulated for a constant drain value, V_d =1 V, and gate voltages V_G = 1.5 V. The relevant results show that the electric potential decreases with an increase in surface trap concentrations. The electric potential profile is similar along the channel and is higher near the drain region.

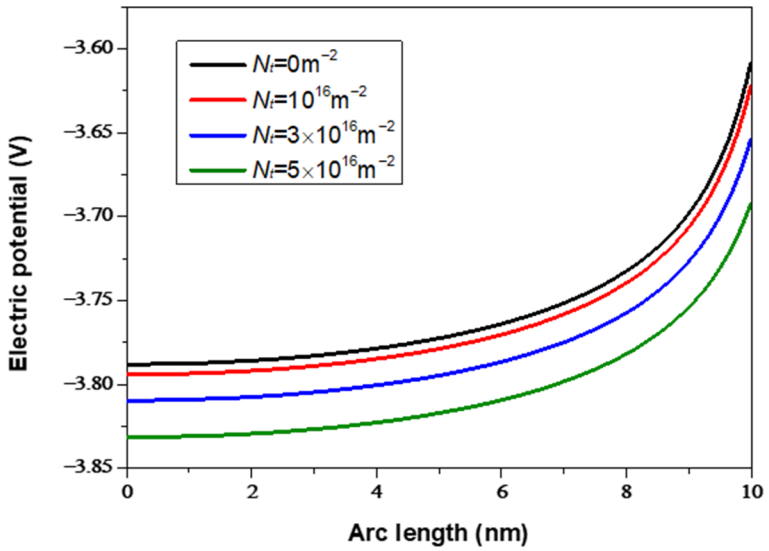

Figure 6. Trap density effect on the electric potential.

The output characteristic of the GAAFET is illustrated in Figure 7 with different trap density values at V_d = 0.5 V. It is clear from the figure that the higher drain current is obtained with a higher trap density, and the effect of the trap density is more intensive, especially for a higher value of the gate voltage. Furthermore, it can be observed that as the trap density ratio increases, the turn-on voltage decreases. Similar results are proven in [57].

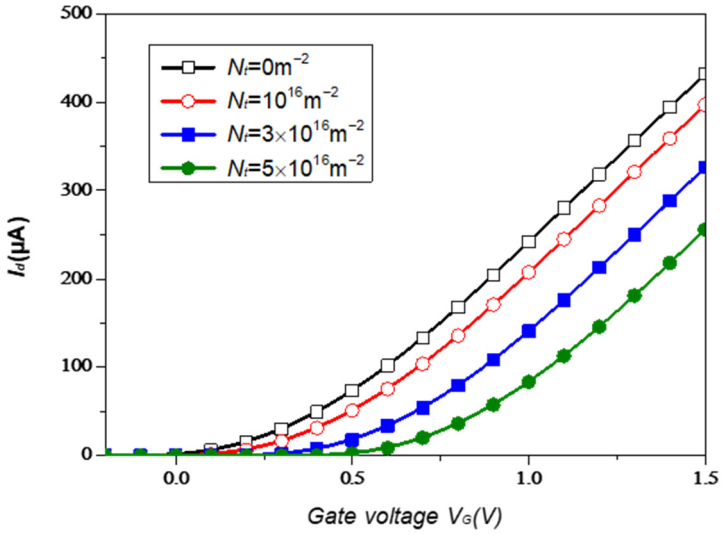

Figure 7. Trap density effect on the output characteristics.

Figure 8a shows the threshold voltage of the GAAFET as a function of the trap density for different drain currents, V_d. As can be seen from the figure, the threshold voltage versus the trap density is almost linear with trap density. These traps cause shifts in the device's performance. Over time, the shifts in threshold voltage can result in device degradation and reduced reliability. Furthermore, continuous capture and release of charge carriers can cause physical damage and defects in the channel and the gate oxide, leading to a decrease in the device's performance over time. Figure 8b depicts the transductance versus the gate voltage for different values of N_t. It is noticeable that a higher transductance value means a faster transistor. Results reveal that a higher g_m is obtained for $N_t = 0$ m^{-2}. It can also be noted that the value is illustrated for $V_G = 1$ V.

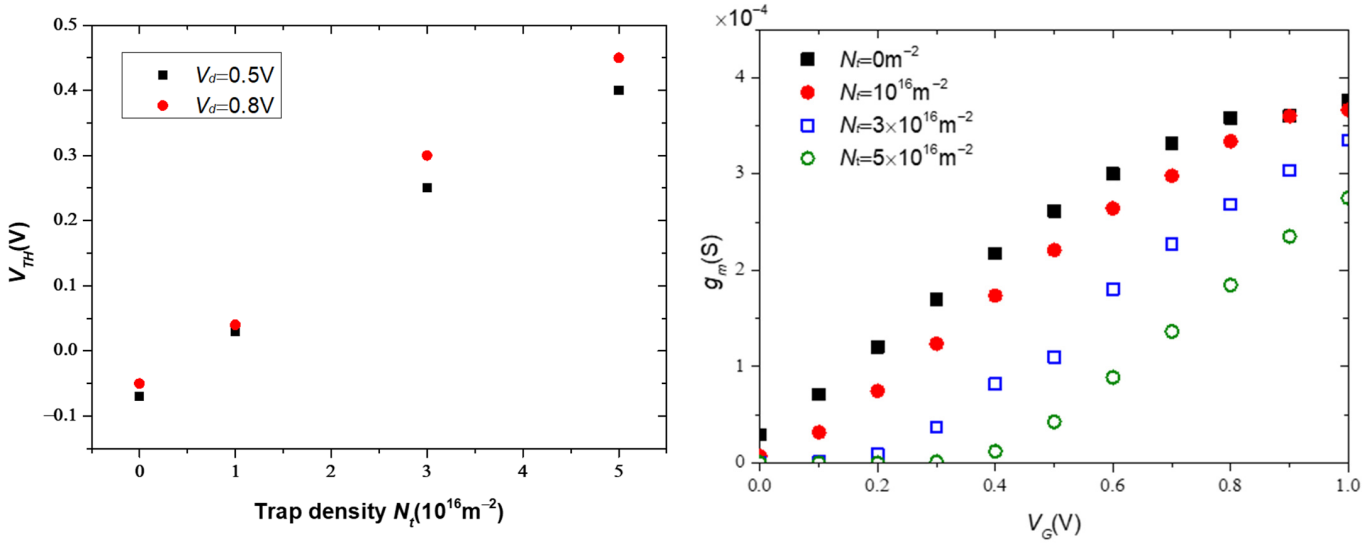

Figure 8. Trap density effects on threshold voltage with different drain voltages (**a**) and a transconductance-versus-gate-voltage plot in the ON state (**b**).

Figure 9 shows the I_{on}/I_{off} ratio in the left axis and the subthreshold slop in the right axis at V_d = 0.5 V. A higher on/off-state current ratio is provided for a lower trap density. A higher I_{on}/I_{off} ratio indicates a larger difference between the current levels when the transistor is in the on-state and off-state, so the transistor can switch more efficiently. The sub-threshold slope in (mV/decade) is an important parameter that indicates how the

drain current changes with the gate-source voltage when the transistor operates in the subthreshold region. A lower subthreshold slope is desirable because it indicates that the transistor can be turned off and on more efficiently with smaller gate voltage changes. In such cases, to achieve the best possible subthreshold slope performance in GAAFET transistors, it is important to minimize the trap density, as shown in the figure.

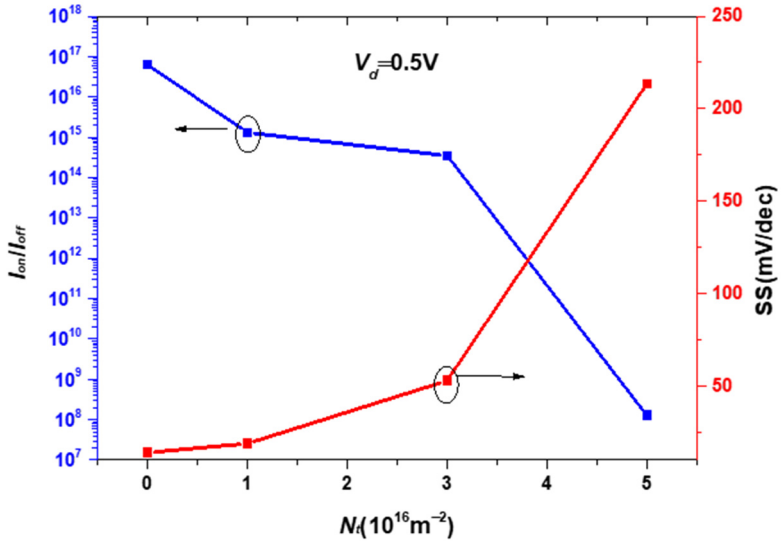

Figure 9. On-state current over off-state current ratio (**left** axis) and subthreshold slope (SS) (**right** axis) variations with different trap density.

Figure 10 shows the effect of trap density on the log scale output characteristics I_d-V_G of the GAAFET. This study is carried out for different geometric parameters such as the oxide thickness, the radius, and the gate length of the device. Figure 10a shows that the drain current varies with the gate voltage for different trap density values of N_t = 0, 10^{16} m^{-2} and 5 × 10^{16} m^{-2}. It is clear from the figure that the drain current is higher in the case where the trap density is not taken into account. For V_G = 0, the drain current is 10^{-11}, 2 × 10^{-7}, and 10^{-6} A and for N_t = 5 × 10^{16}, 10^{16}, and 0 m^{-2}, respectively. Figure 10b depicts the impact of the trap density on the drain current with different oxide thickness values. Results indicate that, especially at higher gate voltages, the drain current is higher with a lower oxide thickness. Likewise, it is apparent that the trap density reduces the drain current, in particular at lower gate voltages for the same oxide thickness. Similarly, the radius effect on the output characteristics of GAAFET devices is illustrated in Figure 10c. The lower radius gives a higher drain current. Figure 10d shows how the log scale I_d-V_G behaves with different gate lengths. When channel length increases, the drain current of the GAAFET decreases. This behavior is associated with the impact of short channel effects. The simulation's results agree with those previously reported by [34].

Although the electrical study shows that reducing oxide thickness can enhance gate control and raise the on-state current of the transistor, shorter gate lengths can amplify short channel effects. They also increase the gate leakage current, which increases the device's off-state power consumption and causes reliability issues. In what follows, we propose to investigate the effect of trap density on the thermal behavior of the device.

Figure 11 shows the temperature distribution in a 3D GAAFET structure for V_G = 1 V, V_d = 2 V without trap density. It is noted from the figure that the maximum temperature, T_{max} = 324 K, is localized near the drain region at the center of the device. The temperature decreases at the drain zone, where it is about 310 K. It is seen that the temperature significantly decreases from the hot spot ($T = T_{max}$) to the source region. On the source side, the temperature is equal to T_0 = 300 K.

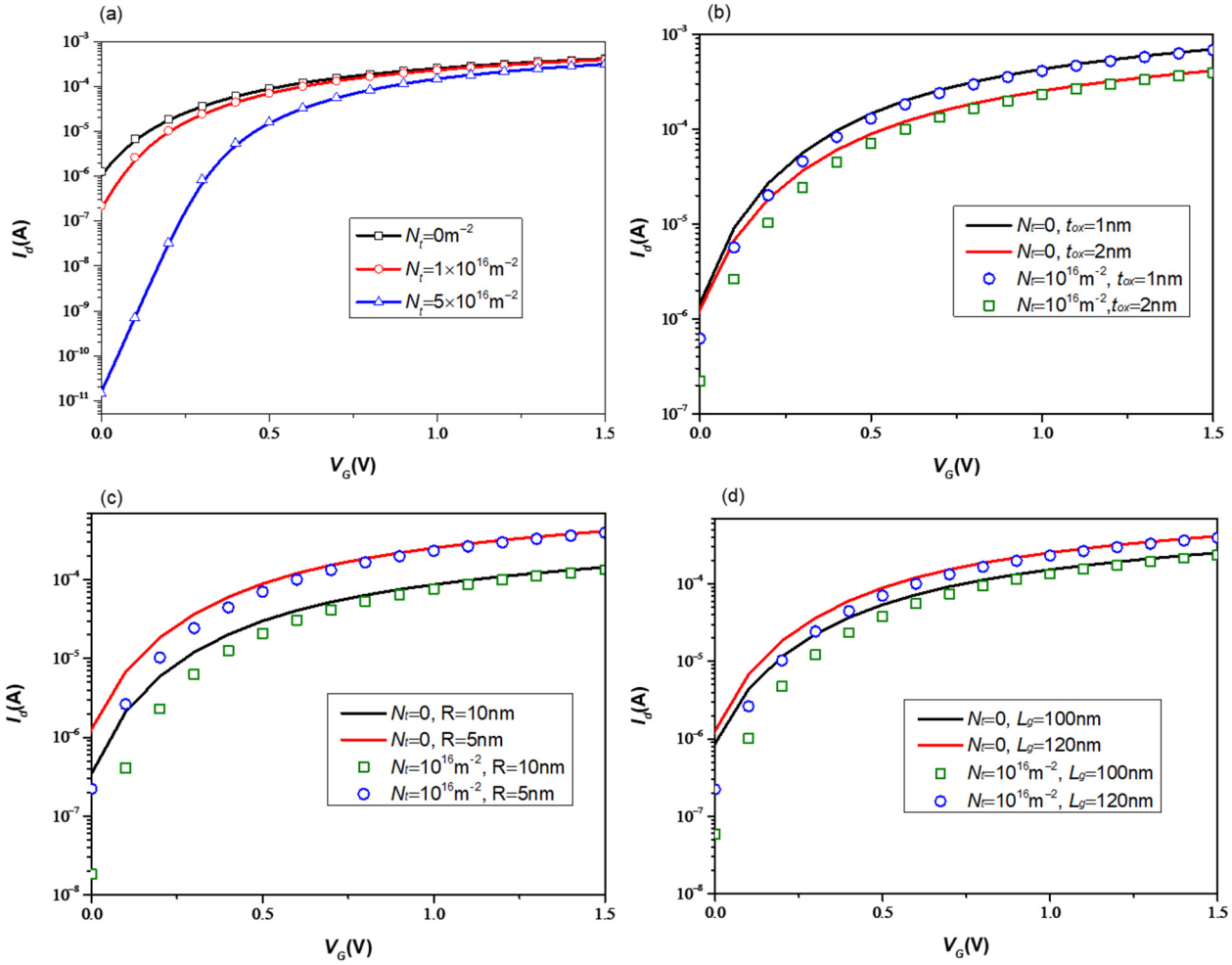

Figure 10. Output characteristics of GAAFET with different (**a**) trap density, (**b**) oxide thickness, (**c**) radius, and (**d**) gate length.

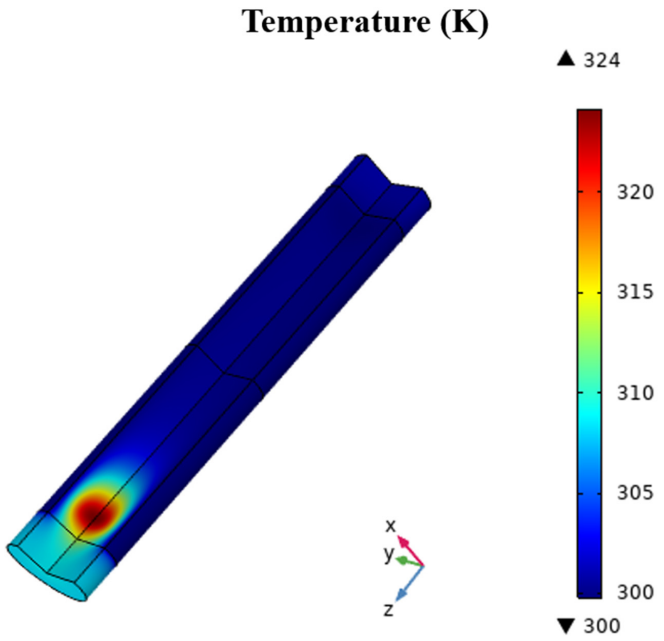

Figure 11. Temperature distribution For V_d = 2 V.

To study the impact of the trap density, the temperature distribution in the GAAFET structure is evaluated for the different gate voltages $N_t = 10^{16}$ m^{-2} and $N_t = 5 \times 10^{16}$ m^{-2}. Figure 12 shows the surface distribution of the temperature for $V_d = 2$ V. Relevant results indicate that for a lower value of V_g ($V_g = 0.5$ V), the maximum temperature decreases from 311 K for $N_t = 10^{16}$ m^{-2} to 303 K for $N_t = 5 \times 10^{16}$ m^{-2}, and for $V_G = 1$ V, the decrease is about 5 K between the two values of trap density. For a high value of V_G ($V_G = 1.5$), the maximum temperature increases from 323 K to 325 K. Additional to these results, as it can be seen from the figure, the temperature distribution is not uniform for the different values, especially in the drain region. For that reason, the temperature profile along the z-axis, from the source to the drain side, is investigated and presented in Figure 13. As can be seen, the effect of the trap density is more noticeable in the hot spot region, where the temperature is at maximum. On the other hand, the results are evaluated along the symmetric axis of the GAAFET structure ($R = 0$) and at the oxide–semiconductor interface ($R = 5$ nm). For a constant value of N_t, (the dashed line in the figure), the temperature is more significant at the center of the device than at the oxide–semiconductor interface. The heat dissipation is evacuated forward into the drain region.

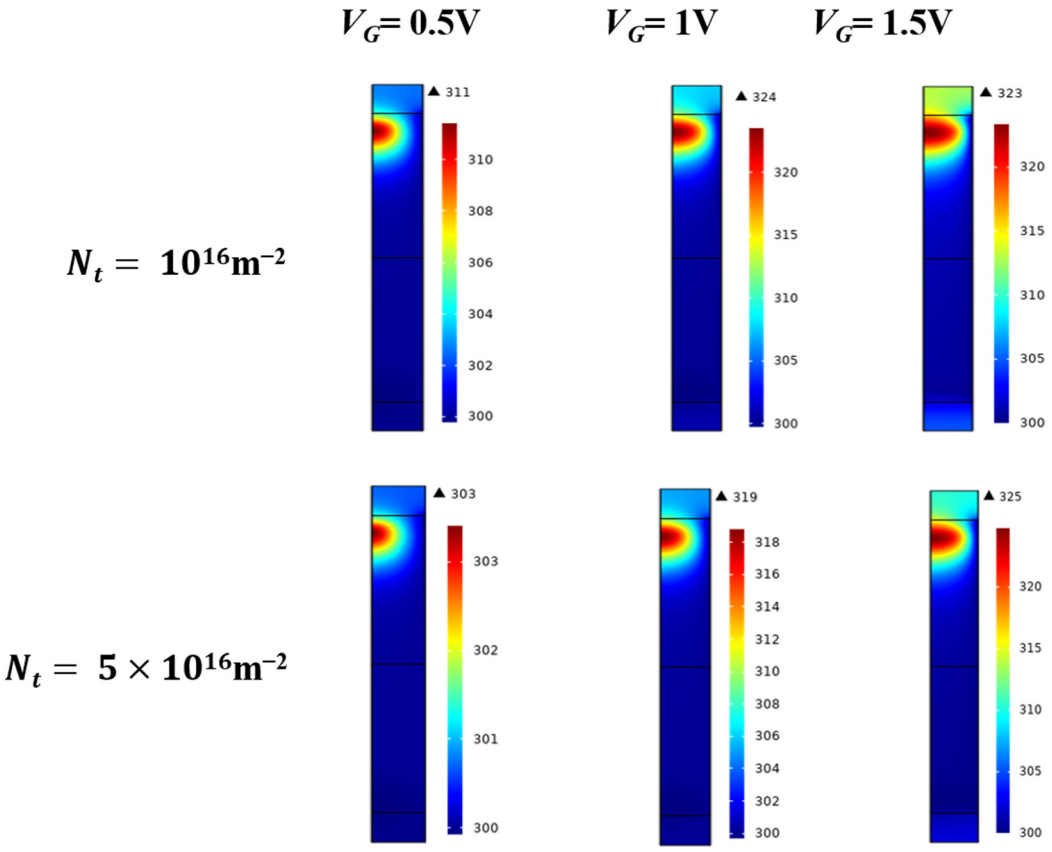

Figure 12. Temperature distribution for different gate voltages at $N_t = 10^{16}$ m^{-2} and $N_t = 5 \times 10^{16}$ m^{-2}.

The impact of reducing oxide thickness and gate length on the device temperature is illustrated in Figure 14. The temperature profile along the z-axis is evaluated at $V_g = 0.5$ V and $V_d = 1$ V for $L_g = 100$ nm (a) and for $L_g = 50$ nm (b) with different oxide thicknesses. While reduced oxide thickness and gate length can enhance performance, they can also lead to increased device temperature. The results revealed that reducing oxide thickness results in higher standby temperature and, therefore, power consumption. This trade-off becomes more pronounced at smaller scales. For $t_{ox} = 1$ nm, the maximum temperature increases from 323.17 K to 350.24 K when L_g decreases from 100 nm to 50 nm. The temperature increase is about 16 K for $t_{ox} = 2$ nm.

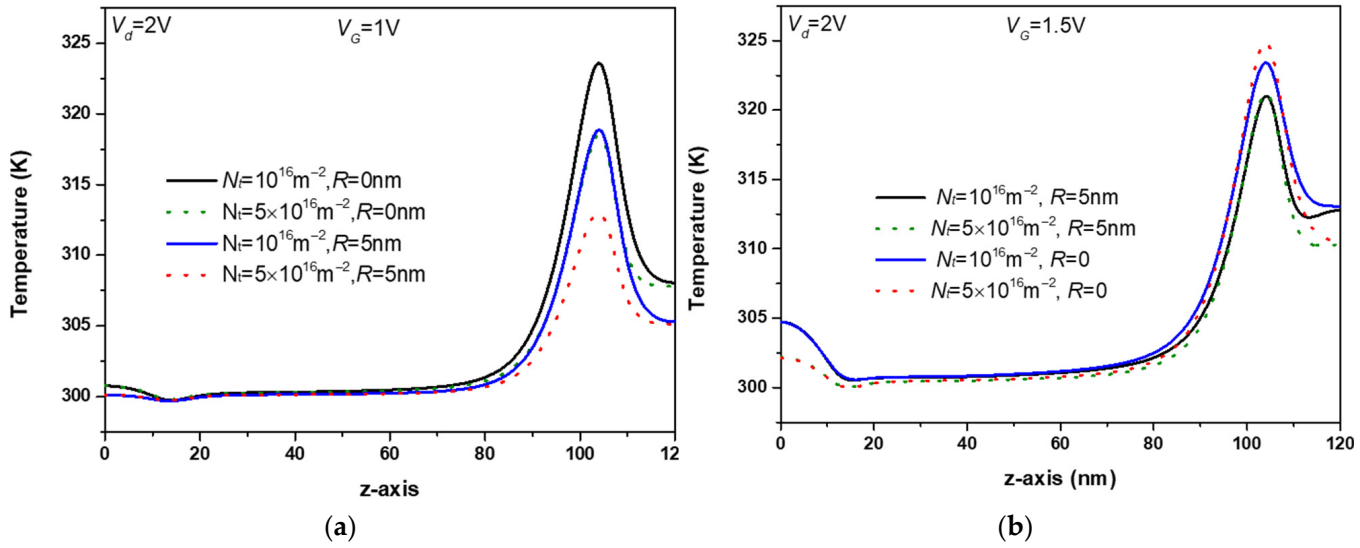

Figure 13. Temperature profile along z-axis for V_g = 1 V (**a**) and V_g = 1.5 V (**b**) for different radius positions and trap density values.

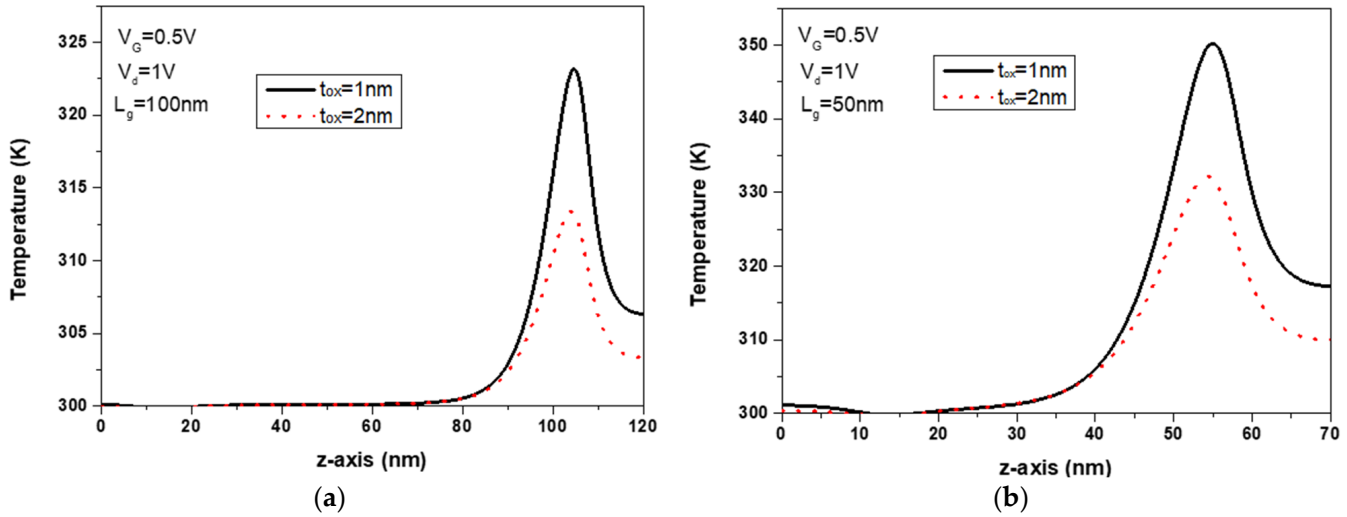

Figure 14. Temperature profile along z-axis at V_g = 0.5 V and V_d = 1 V for L_g = 100 nm (**a**) and L_g = 50 nm (**b**) with different oxide thicknesses.

The heat flux and temperature profile, in the middle of the structure (r = 2 nm) along the channel from the source side to the drain, are presented in Figure 15. Obtained results are evaluated at V_g = 0.8 V and V_d = 1 V. The profiles are presented for r = 0.5 nm, near the symmetry axis, where the hot spot is confined. The peak temperature is T_{max} = 324 K and the maximum heat flux is about 2.2 × 10^{20} Wm^{-3}. We observe that the hot spot is localized, particularly at the channel and drain contact.

Figure 16 shows the effect of the trap density on the temperature rise profile versus the drain voltage V_d. The outcomes are shown when V_d ranges from 0 to 1.8 V and V_g is 0.5 V. The temperature rise is found to increase quadratically with drain voltage according to the results. Without taking the trap density into account, the maximum temperature rise is noted for higher drain voltage values. For a constant drain voltage, the temperature rise becomes smaller as the trap density increases.

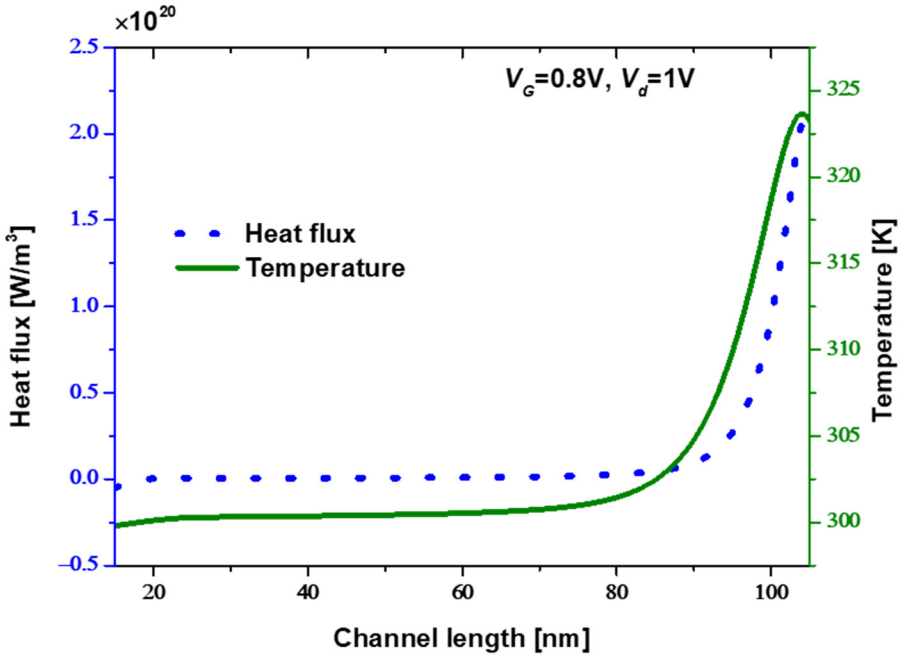

Figure 15. Heat flux (**left**) and temperature (**right**) profiles along the arc length for r = 2 nm.

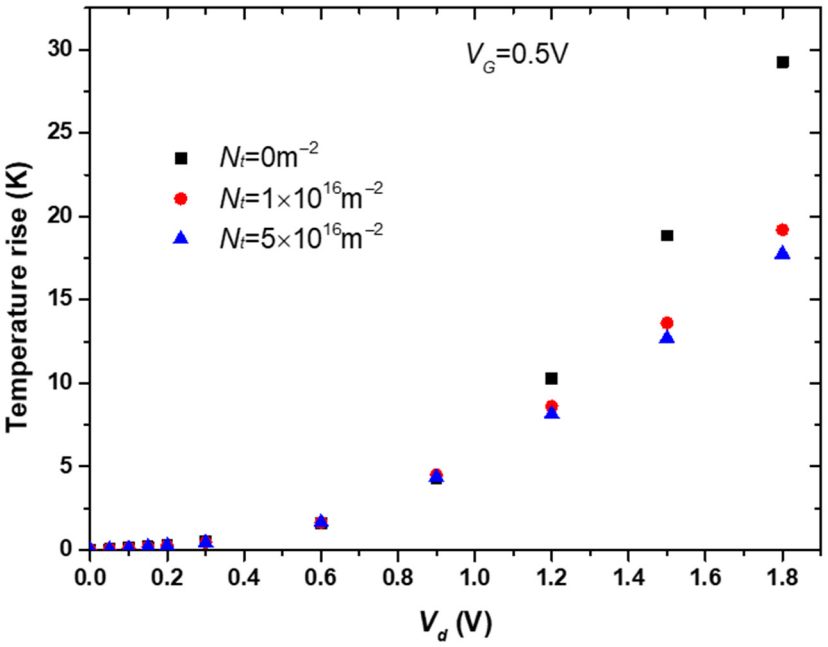

Figure 16. Temperature rise profile as a function of the drain voltages for V_g = 0.5 V.

4. Conclusions

GAAFETs have the potential to be used for various applications due to their unique advantages over traditional MOSFETs and FinFETs. The electrothermal behavior of GAAFETs has been analyzed in this work. This study demonstrates how the trap density can affect the electrical responses and thermal behavior of GAAFETs. The numerical simulation has been investigated in a 2D axis-symmetry structure, the finite element method has been used in the discretization of the semiconductor equations, and the impact of the trap density on the output characteristics has been discussed. Moreover, the effect of the geometric parameters is investigated, taking into account the trap density on the output characteristics of the GAAFET. It has been shown that reducing the oxide thickness can improve gate control and increase the transistor's on-state current. However, it also increases the gate leakage

current, which increases the power consumption of the device in the off state. On the other hand, shorter gate lengths can increase short channel effects, reducing control over the channel and leading to potential reliability issues. Following that, the thermal behavior was analyzed. The results reveal that the electrical and thermal responses of transistors are significantly influenced by trap density. An enhancement of the output characteristics in the device is obtained using lower geometric dimensions such as oxide thickness, gate length, and device radius. In summary, comprehending and controlling trap density will enable researchers to produce more efficient, dependable, and high-performance GAAFET transistors in the future.

Author Contributions: M.B. contributed to the simulation and implementation of the research and to the writing of the relevant subsection of the manuscript. F.A. contributed to the analysis of the results and the writing of the manuscript. S.A.A. and F.E. contributed to the correction and organization of the manuscript. H.B. is the supervisor of the work presented in this manuscript. All authors have read and agreed to the published version of the manuscript.

Funding: The authors extend their appreciation to the Deputyship for Research & Innovation, Ministry of Education in Saudi Arabia for funding this research work through the project number RI-44-0327.

Data Availability Statement: No new data were created.

Acknowledgments: The authors extend their appreciation to the Deputyship for Research & Innovation, Ministry of Education in Saudi Arabia for funding this research work through the project number RI-44-0327.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Hisamoto, D.; Lee, W.-C.; Kedzierski, J.; Takeuchi, H.; Asano, K.; Kuo, C.; Anderson, E.; King, T.-J.; Bokor, J.; Hu, C. FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. *IEEE Trans. Electron Devices* **2000**, *47*, 2320–2325.
2. Park, J.-T.; Colinge, J.-P.; Diaz, C.H. Pi-gate soi mosfet. *IEEE Electron Device Lett.* **2001**, *22*, 405–406. [CrossRef]
3. Doyle, B.; Datta, S.; Doczy, M.; Hareland, S.; Jin, B.; Kavalieros, J.; Linton, T.; Murthy, A.; Rios, R.; Chau, R. High performance fully-depleted tri-gate CMOS transistors. *IEEE Electron Device Lett.* **2003**, *24*, 263–265. [CrossRef]
4. Yang, F.-L.; Chen, H.-Y.; Chen, F.-C.; Huang, C.-C.; Chang, C.-Y.; Chiu, H.-K.; Lee, C.-C.; Chen, C.-C.; Huang, H.-T.; Chen, C.-J. 25 nm CMOS omega FETs. In Proceedings of the Digest International Electron Devices Meeting, San Francisco, CA, USA, 8–11 December 2002; pp. 255–258.
5. Monfray, S.; Skotnicki, T.; Morand, Y.; Descombes, S.; Coronel, P.; Mazoyer, P.; Harrison, S.; Ribot, P.; Talbot, A.; Dutartre, D. 50 nm-gate all around (GAA)-silicon on nothing (SON)-devices: A simple way to co-integration of GAA transistors within bulk MOSFET process. In Proceedings of the 2002 Symposium on VLSI Technology, Kyoto, Japan, 10 June 2022; Digest of Technical Papers (Cat. No. 01CH37303). pp. 108–109.
6. Kumar, M.J.; Orouji, A.A.; Dhakad, H. New dual-material SG nanoscale MOSFET: Analytical threshold-voltage model. *IEEE Trans. Electron Devices* **2006**, *53*, 920–922. [CrossRef]
7. Wang, H.-K.; Wu, S.; Chiang, T.-K.; Lee, M.-S. A new two-dimensional analytical threshold voltage model for short-channel triple-material surrounding-gate metal–oxide–semiconductor field-effect transistors. *Jpn. J. Appl. Phys.* **2012**, *51*, 054301. [CrossRef]
8. Mo, F.; Spano, C.E.; Ardesi, Y.; Ruo Roch, M.; Piccinini, G.; Vacca, M. NS-GAAFET Compact Modeling: Technological Challenges in Sub-3-nm Circuit Performance. *Electronics* **2023**, *12*, 1487. [CrossRef]
9. Karbalaei, M.; Dideban, D.; Heidari, H. A sectorial scheme of gate-all-around field effect transistor with improved electrical characteristics. *Ain Shams Eng. J.* **2021**, *12*, 755–760. [CrossRef]
10. Lee, C.-C.; Huang, P.-C.; Hsiang, T.-P. Interactive Lattice and Process-Stress Responses in the Sub-7 nm Germanium-Based Three-Dimensional Transistor Architecture of FinFET and Nanowire GAAFET. *IEEE Trans. Electron Devices* **2022**, *69*, 6552–6560. [CrossRef]
11. Min, J.; Shin, C. Study of line edge roughness on various types of gate-all-around field effect transistor. *Semicond. Sci. Technol.* **2019**, *35*, 015004. [CrossRef]
12. Zhao, P.; Zhao, S.-H.; He, Y.-D.; Du, G. A comparative study of self-heating effects in 3nm node GAAFETs and FinFETs. In Proceedings of the 2022 IEEE 16th International Conference on Solid-State & Integrated Circuit Technology (ICSICT), Nanjing, China, 25–28 October 2022; pp. 1–3.
13. Mohan, C.; Choudhary, S.; Prasad, B. Gate All Around FET: An Alternative of FinFET for Future Technology Nodes. *Int. J. Adv. Res. Sci. Eng.* **2017**, *6*, 563–569.

14. Barraud, S.; Berthome, M.; Coquand, R.; Cassé, M.; Ernst, T.; Samson, M.-P.; Perreau, P.; Bourdelle, K.; Faynot, O.; Poiroux, T. Scaling of trigate junctionless nanowire MOSFET with gate length down to 13 nm. *IEEE Electron Device Lett.* **2012**, *33*, 1225–1227. [CrossRef]
15. Sallese, J.-M.; Chevillon, N.; Lallement, C.; Iniguez, B.; Prégaldiny, F. Charge-based modeling of junctionless double-gate field-effect transistors. *IEEE Trans. Electron Devices* **2011**, *58*, 2628–2637. [CrossRef]
16. Yeo, K.H.; Suk, S.D.; Li, M.; Yeoh, Y.-Y.; Cho, K.H.; Hong, K.-H.; Yun, S.; Lee, M.S.; Cho, N.; Lee, K. Gate-all-around (GAA) twin silicon nanowire MOSFET (TSNWFET) with 15 nm length gate and 4 nm radius nanowires. In Proceedings of the 2006 International Electron Devices Meeting, San Francisco, CA, USA, 11–13 December 2006; pp. 1–4.
17. Dhanaselvam, P.S.; Balamurugan, N. Analytical approach of a nanoscale triple-material surrounding gate (TMSG) MOSFETs for reduced short-channel effects. *Microelectron. J.* **2013**, *44*, 400–404. [CrossRef]
18. Pravin, J.C.; Nirmal, D.; Prajoon, P.; Ajayan, J. Implementation of nanoscale circuits using dual metal gate engineered nanowire MOSFET with high-k dielectrics for low power applications. *Phys. E Low-Dimens. Syst. Nanostructures* **2016**, *83*, 95–100. [CrossRef]
19. Narula, M.S.; Pandey, A. A Comprehensive Review on FinFET, Gate All Around, Tunnel FET: Concept, Performance and Challenges. In Proceedings of the 2022 8th International Conference on Signal Processing and Communication (ICSC), Noida, India, 1–3 December 2022.
20. Kumar, B.; Kumar, A.; Chaujar, R. The effect of gate stack and high-κ spacer on device performance of a Junctionless GAA FinFET. In *2020 IEEE vlsi Device Circuit and System (vlsi dcs)*; IEEE: Piscataway, NJ, USA, 2020; pp. 159–163.
21. Alam, M.A.; Mahajan, B.K.; Chen, Y.-P.; Ahn, W.; Jiang, H.; Shin, S.H. A device-to-system perspective regarding self-heating enhanced hot carrier degradation in modern field-effect transistors: A topical review. *IEEE Trans. Electron Devices* **2019**, *66*, 4556–4565. [CrossRef]
22. Bury, E.; Kaczer, B.; Roussel, P.; Ritzenthaler, R.; Raleva, K.; Vasileska, D.; Groeseneken, G. Experimental validation of self-heating simulations and projections for transistors in deeply scaled nodes. In Proceedings of the 2014 IEEE International Reliability Physics Symposium, Waikoloa, HI, USA, 1–5 June 2014; pp. XT. 8.1–XT. 8.6.
23. Takahashi, T.; Matsuki, T.; Shinada, T.; Inoue, Y.; Uchida, K. Direct evaluation of self-heating effects in bulk and ultra-thin BOX SOI MOSFETs using four-terminal gate resistance technique. *IEEE J. Electron Devices Soc.* **2016**, *4*, 365–373. [CrossRef]
24. Scholten, A.; Smit, G.; Pijper, R.; Tiemeijer, L.; Tuinhout, H.; Van der Steen, J.-L.; Mercha, A.; Braccioli, M.; Klaassen, D. Experimental assessment of self-heating in SOI FinFETs. In Proceedings of the 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009; pp. 1–4.
25. Jang, D.; Bury, E.; Ritzenthaler, R.; Bardon, M.G.; Chiarella, T.; Miyaguchi, K.; Raghavan, P.; Mocuta, A.; Groeseneken, G.; Mercha, A. Self-heating on bulk FinFET from 14nm down to 7nm node. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015; pp. 11.16. 11–11.16. 14.
26. Ahn, W.; Shin, S.H.; Jiang, C.; Jiang, H.; Wahab, M.; Alam, M.A. Integrated modeling of self-heating of confined geometry (FinFET, NWFET, and NSHFET) transistors and its implications for the reliability of sub-20 nm modern integrated circuits. *Microelectron. Reliab.* **2018**, *81*, 262–273. [CrossRef]
27. Jiang, H.; Shin, S.; Liu, X.; Zhang, X.; Alam, M.A. The impact of self-heating on HCI reliability in high-performance digital circuits. *IEEE Electron Device Lett.* **2017**, *38*, 430–433. [CrossRef]
28. Koh, M.; Mizubayashi, W.; Iwamoto, K.; Murakami, H.; Ono, T.; Tsuno, M.; Mihara, T.; Shibahara, K.; Miyazaki, S.; Hirose, M. Limit of gate oxide thickness scaling in MOSFETs due to apparent threshold voltage fluctuation induced by tunnel leakage current. *IEEE Trans. Electron Devices* **2001**, *48*, 259–264. [CrossRef]
29. Pimbley, J.M.; Meindl, J.D. MOSFET scaling limits determined by subthreshold conduction. *IEEE Trans. Electron Devices* **1989**, *36*, 1711–1721. [CrossRef]
30. Seo, K.-I.; Haran, B.; Gupta, D.; Guo, D.; Standaert, T.; Xie, R.; Shang, H.; Alptekin, E.; Bae, D.-I.; Bae, G. A 10nm platform technology for low power and high performance application featuring FINFET devices with multi workfunction gate stack on bulk and SOI. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, USA, 9–12 June 2014.
31. Zeitzoff, P.M. MOSFET scaling trends and challenges through the end of the roadmap. In Proceedings of the IEEE 2004 Custom Integrated Circuits Conference (IEEE Cat. No. 04CH37571), Orlando, FL, USA, 3–6 October 2004; pp. 233–240.
32. Echouchene, F.; Belmabrouk, H. Effect of Temperature Jump on Nonequilibrium Entropy Generation in a MOSFET Transistor Using Dual-Phase-Lagging Model. *J. Heat Transf.* **2017**, *139*, 122007. [CrossRef]
33. Echouchene, F.; Mabrouk, H.B. Non equilibrium entropy generation in nano scale MOSFET transistor based a nonlinear DPL heat conduction model. In Proceedings of the 2018 9th International Renewable Energy Congress (IREC), Hammamet, Tunisia, 20–22 March 2018; pp. 1–6.
34. Junior, N.G.; Costa, F.J.; Trevisoli, R.; Barraud, S.; Doria, R.T. Influence of interface traps density and temperature variation on the NBTI effect in p-Type junctionless nanowire transistors. *Solid-State Electron.* **2021**, *186*, 108097.
35. Belkhiria, M.; Echouchene, F.; Jaba, N.; Bajahzar, A.; Belmabrouk, H. Impact of high-k gate dielectric on self-heating effects in PiFETs structure. *IEEE Trans. Electron Devices* **2020**, *67*, 3522–3529. [CrossRef]
36. Li, J.; Pud, S.; Petrychuk, M.; Offenhausser, A.; Vitusevich, S. Sensitivity enhancement of Si nanowire field effect transistor biosensors using single trap phenomena. *Nano Lett.* **2014**, *14*, 3504–3509. [CrossRef]
37. Yoon, J.-S.; Kim, K.; Rim, T.; Baek, C.-K. Performance and variations induced by single interface trap of nanowire FETs at 7-nm node. *IEEE Trans. Electron Devices* **2016**, *64*, 339–345. [CrossRef]

38. Kalb, W.L.; Batlogg, B. Calculating the trap density of states in organic field-effect transistors from experiment: A comparison of different methods. *Phys. Rev. B* **2010**, *81*, 035327. [CrossRef]
39. Sai, P.; Jorudas, J.; Dub, M.; Sakowicz, M.; Jakštas, V.; But, D.; Prystawko, P.; Cywinski, G.; Kašalynas, I.; Knap, W. Low frequency noise and trap density in GaN/AlGaN field effect transistors. *Appl. Phys. Lett.* **2019**, *115*, 183501. [CrossRef]
40. Kumar, N.; Raman, A. Performance assessment of the charge-plasma-based cylindrical GAA vertical nanowire TFET with impact of interface trap charges. *IEEE Trans. Electron Devices* **2019**, *66*, 4453–4460. [CrossRef]
41. Pala, M.G.; Esseni, D. Interface traps in InAs nanowire tunnel-FETs and MOSFETs—Part I: Model description and single trap analysis in tunnel-FETs. *IEEE Trans. Electron Devices* **2013**, *60*, 2795–2801. [CrossRef]
42. Zienkiewicz, O.C.; Taylor, R.L.; Nithiarasu, P.; Zhu, J. *The Finite Element Method*; McGraw-hill London: London, UK, 1977; Volume 3.
43. Sewell, G. *Analysis of a Finite Element Method: PDE/PROTRAN*; Springer Science & Business Media: Berlin/Heidelberg, Germany, 2012.
44. Pratap, Y.; Ghosh, P.; Haldar, S.; Gupta, R.; Gupta, M. An analytical subthreshold current modeling of cylindrical gate all around (CGAA) MOSFET incorporating the influence of device design engineering. *Microelectron. J.* **2014**, *45*, 408–415. [CrossRef]
45. Ajay, B.; Gadicha, V.B.G. Om Prakash Jena Mechanism to protect Decentralized Transaction Using Blockchain Technology. In *Machine Learning Adoption in Blockchain-Based Intelligent Manufacturing: Theoretical Basics, Applications, and Challenges*; Taylor & Francis Publication: Abingdon, UK, 2021.
46. Sibabrata Mohanty, K.C.R.a.O.P.J. Implementation of Total Productive Maintenance (TPM) in Manufacturing Industry for Improving Production Effectiveness. In *Industrial Transformation: Implementation and Essential Components and Processes of Digital Systems*; Taylor & Francis Publication: Abingdon, UK, 2021.
47. Reddy, J.N. *Introduction to the Finite Element Method*; McGraw-Hill Education: London, UK, 2019.
48. Zlámal, M. Finite element solution of the fundamental equations of semiconductor devices. I. *Math. Comput.* **1986**, *46*, 27–43. [CrossRef]
49. Lin, P.T.; Shadid, J.N.; Sala, M.; Tuminaro, R.S.; Hennigan, G.L.; Hoekstra, R.J. Performance of a parallel algebraic multilevel preconditioner for stabilized finite element semiconductor device modeling. *J. Comput. Phys.* **2009**, *228*, 6250–6267. [CrossRef]
50. Belkhiria, M.; Echouchene, F.; Jaba, N.; Bajahzar, A.; Belmabrouk, H. 2-D-Nonlinear Electrothermal Model for Investigating the Self-Heating Effect in GAAFET Transistors. *IEEE Trans. Electron Devices* **2021**, *68*, 954–961. [CrossRef]
51. Jemii, E.; Belkhiria, M.; Aouaini, F.; Echouchene, F.; Alyousef, H. Electrothermal analyses in Cu/ZrO_2/Pt CBRAM memory using a dual-phase-lag model. *J. Comput. Electron.* **2022**, *21*, 792–801. [CrossRef]
52. Han, K.; Long, S.; Deng, Z.; Zhang, Y.; Li, J. A novel germanium-around-source gate-all-around tunnelling field-effect transistor for low-power applications. *Micromachines* **2020**, *11*, 164. [CrossRef]
53. Jagota, V.; Sethi, A.P.S.; Kumar, K. Finite element method: An overview. *Walailak J. Sci. Technol. (WJST)* **2013**, *10*, 1–8.
54. de Arantes e Oliveira, E.R. The patch test and the general convergence criteria of the finite element method. *Int. J. Solids Struct.* **1977**, *13*, 159–178. [CrossRef]
55. Singh, S.; Solay, L.R.; Anand, S.; Kumar, N.; Ranjan, R.; Singh, A. Implementation of Gate-All-Around Gate-Engineered Charge Plasma Nanowire FET-Based Common Source Amplifier. *Micromachines* **2023**, *14*, 1357. [CrossRef]
56. Singh, N.; Agarwal, A.; Bera, L.; Liow, T.; Yang, R.; Rustagi, S.; Tung, C.; Kumar, R.; Lo, G.; Balasubramanian, N. High-performance fully depleted silicon nanowire (diameter/spl les/5 nm) gate-all-around CMOS devices. *IEEE Electron Device Lett.* **2006**, *27*, 383–386. [CrossRef]
57. Zaini, M.; Mohd Sarjidan, M.; Abd, W. The effect of trap density on the trapping and de-trapping processes in determining the turn-on voltage of double-carrier organic light-emitting devices (OLEDs). *J. Electron. Mater.* **2021**, *50*, 4511–4523. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.