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Comparative Analysis of Thermal Properties in Molybdenum Substrate to Silicon and Glass for a System-on-Foil Integration

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Abstract: Advanced electronics technology is moving towards smaller footprints and higher computational power. In order to achieve this, advanced packaging techniques are currently being considered, including organic, glass, and semiconductor-based substrates that allow for 2.5D or 3D integration of chips and devices. Metal-core substrates are a new alternative with similar properties to those of semiconductor-based substrates but with the added benefits of higher flexibility and metal ductility. This work comprehensively compares the thermal properties of a novel metal-based substrate, molybdenum, and silicon and fused silica glass substrates in the context of system-on-foil (SoF) integration. A simple electronic technique is used to simulate the heat generated by a typical CPU and to measure the heat dissipation properties of the substrates. The results indicate that molybdenum and silicon are able to effectively dissipate a continuous power density of 2.3 W/mm^2 as the surface temperature only increases by ~15 °C. In contrast, the surface temperature of fused silica glass substrates increases by >140 °C for the same applied power. These simple techniques and measurements were validated with infrared camera measurements as well as through finite element analysis via COMSOL simulation. The results validate the use of molybdenum as an advanced packaging substrate and can be used to characterize new substrates and approaches for advanced packaging.

Keywords: glass; heat capacity; molybdenum; printed circuit board; silicon; system-on-foil; thermal conductivity

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1. Introduction

Moore's law has been the fundamental driving force in the semiconductor industry, continuously pushing the fabrication of electrical devices to achieve smaller footprints, increased device density, and enhanced computational power. With the constant advance of these industry limits, new challenges arise. Heat management has become a critical challenge when it comes to the structure, fabrication, and packaging of such devices. A new approach for device packaging is being developed to manage heat dissipation through the introduction of a system-on-foil (SoF) technology. SoF is an alternative to traditional printed circuit boards (PCBs), typically used in system-on-chip applications, and is able to provide improved heat management and dissipation. SoF provides a platform for either packaged chips to be surface-mounted or active/passive devices to be fabricated on the foil substrate directly, similar to on a silicon substrate. This technology provides high-speed interconnected and high-density integrated circuits, allowing for a class of electronics that can include a full system integrated onto a flexible substrate. Consequently, this class of electronics can achieve reduced size, weight, cost, and power consumption when compared to conventional PCB approaches [1].

The progression from 2D to 2.5D to 3D packaging is crucial for the future trajectory of the advanced packaging industry, which is expected to reach $70 billion by 2032, up from $29 billion in 2022 [2]. One of the main motivations for thinned substrates is to reduce electrical resistance, which then allows for more efficient heat removal from active circuitry to a heat sink or other heating solutions [3,4]. Measuring the thermal conductivity of thin electronic substrates has previously been studied using SiC Schottky diodes, which, in their most basic form, are metal-semiconductor junctions, creating an electron barrier [5].

Glass, or SiO_2, is another category of advanced packaging substrate material often utilized in the optics and display industries [6]. However, this often requires a copper-based heat sink/heat spreader to be incorporated between the devices and the interposer [6]. Gold and copper are known to be a source of device contamination for front-end-of-line (FEOL) device fabrication [7]. This results in significant incompatibilities if future work requires device fabrication directly on substrates. Glass-based substrate materials for advanced packaging have been demonstrated by Shorey et al. [7]. Ultra-high resistivity and low electrical loss, along with an adjustable coefficient of thermal expansion, make glass one of the many ideal substrates for interposer developments [7–11]. The work presented by Shorey et al. utilized through-glass vias (TGVs) filled with copper for thermal management. This alleviates the effect of the fused silica glass's poor thermal properties in comparison to silicon or metal-based interposers.

Metal-based or metal-core interposers have been suggested as a possible substrate for advanced packaging. Although metal-based interposers are not suitable for active devices, they have the advantage of increased flexibility, ductility, and malleability so that 3D structures can be implemented. As shown in a study presented by Zweben et al. [12], molybdenum has been commonly used in alloys with copper for constraining layers of PCBs to obtain low coefficient of thermal expansions (CTEs) and thermal management while serving as heat sinks. In addition, the thermal conductivity of molybdenum, 138 W/m·K [13], is on par with that of silicon, 124–130 W/m·K [14], and provides a similar thermal dissipation characteristic. Work presented by Singh et al. and Reiser et al. also demonstrated the application of molybdenum and copper alloys through different fabrication processes to achieve an optimized alloy composition ratio of Cu and Mo for thermal management applications [15,16]. However, there are not many reports where integrated heating elements, which more closely mimic the heat generated by a circuit on the substrate than other measurement methods, are used to characterize the thermal properties of molybdenum in an electronic packaging configuration. In addition to thermal properties, the rigidity of the molybdenum substrate, while being flexible enough to withstand high stress impacts, illustrates further material benefits over that of conventional silicon and glass substrates.

As such, there is a need to study the thermal properties of molybdenum as an advanced packaging material with in situ resistors. This paper describes the design of in situ heater and sense resistors fabricated on three different substrates: (1) molybdenum, (2) silicon, and (3) fused silica glass in order to compare its performance to established interposer substrate materials. The presented work illustrates the feasibility of molybdenum substrate-based technology for advanced packaging applications through test structure fabrication and analysis of electrical testing results, subsequently confirmed by infrared camera measurements and heat transfer modeling in COMSOL Multiphysics™. Simple structures are modeled and fabricated on each substrate, where resistors will mimic chip-lets on substrates. The presented results demonstrate the feasibility for molybdenum substrate-based technology to be adopted for advanced packaging as well as presenting test techniques that can be adopted by others for characterizing advanced packaging substrates.

2. Materials and Methods

2.1. Device Design

Illustrated below in Figure 1 is a two-dimensional figurative device layout design for the presented work, along with thermal length in both the x and y directions. Individual serpentine lines are patterned resistors, where gray thermal sensors (Rsense) with a total

number of 2933 squares are on either side of a red heating resistor (Rheat) with a total number of 800 squares in the center. The Rheat resistor in the center of the design simulates heating circuitry or a CPU operating at high clock rates, which typically generates heat flux densities of 1.12–2.5 W/mm^2 [17]. The temperature sensors were placed at a different distance to experimentally understand the lateral heat dissipation. The sheet resistance for 180 nm of aluminum was calculated to be 0.15 Ω with expected Rheat and Rsense resistances of 120 and 440 Ω, respectively.

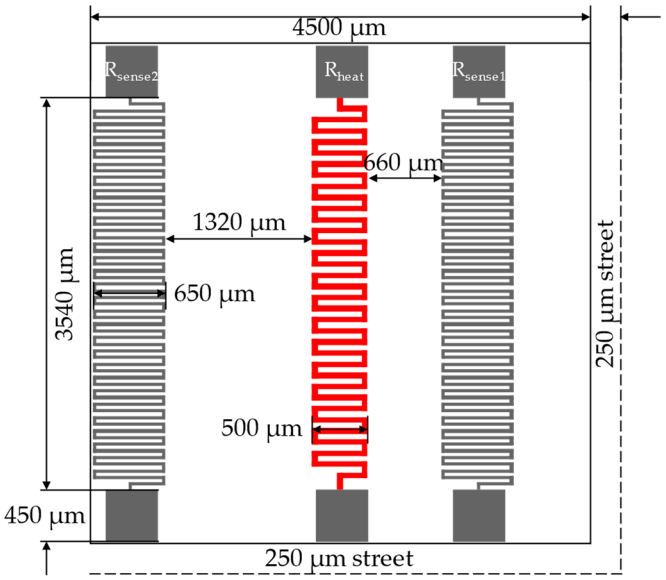


Figure 1. Layout and dimensions of the heating (Rheat) and sense (Rsense1 and Rsense2) resistors used to characterize the thermal properties of silicon, molybdenum, and glass substrates.

2.2. Device Fabrication

The presented devices were fabricated on three different substrates in order to compare the thermal performance of molybdenum to a typical material, such as silicon, as well as to an alternative material, such as fused silica glass. All three substrates have a nominal diameter of 4 inches and a thickness of 250 µm. Molybdenum, silicon <100>, and fused silica glass wafers were procured from Lux Semiconductors (Albany, NY, USA), Virginia Semiconductors (Fredericksburg, VA, USA), and Precision Micro-Optics (Burlington, MA, USA), respectively.

Shown in Figure 2 is a simplified process diagram for the fabrication of the test structures. The fabrication process starts with a standard RCA clean for the silicon substrates and an acetone/isopropyl alcohol (IPA) ultrasonic clean for both molybdenum and glass substrates. A 5 µm film of tetraethoxysilane (TEOS) was deposited onto molybdenum and silicon substrates using an Applied Materials P5000 PECVD. Subsequently, a negative photoresist, Futurrex NR9g-1500-PY, was applied onto a hexamethyldisilazane (HMDS) primed wafer surface with a manual photoresist spin coater at 5000 rpm for a thickness that was approximately 1 µm. A contact lithography, SUSS MA-150, with an i-line filter, was used to transfer the pattern of the temperature heating and sensing resistor patterns with a clear field mask. Next, 180 nm of aluminum (Al/Si, 98/2 wt%) was DC sputtered in a CVC601 Sputter system and patterned for thermal heating and sensing resistors via a lift-off process in an acetone bath with ultrasonication for approximately 5 min. Figure S2 illustrates a not-to-scale cross-sectional view of the fabricated structures comparing the three substrates.

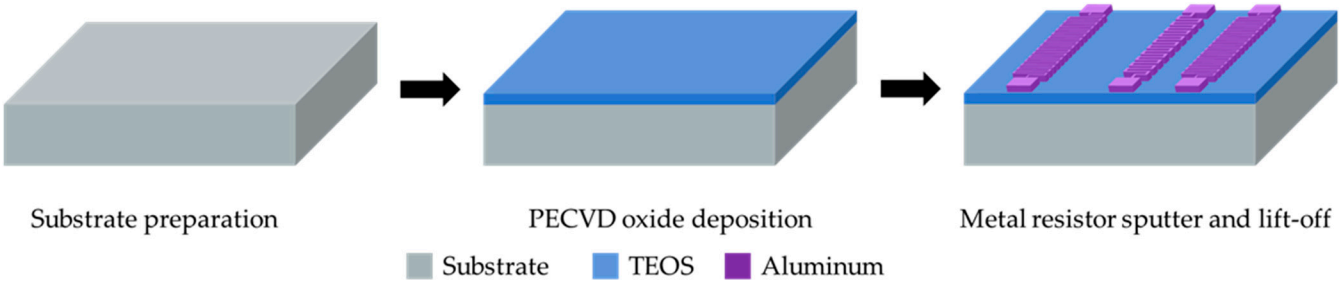


Figure 2. Schematic representation of the process flow indicating the main fabrication steps and resultant structure. The same process was used to fabricate structures on silicon and molybdenum substrates. The fused silica glass substrate did not have TEOS deposited.

2.3. Temperature Coefficient of Resistance Measurements and Calibration

The temperature coefficient of resistance (TCR) of the fabricated resistors was measured to calibrate the fabricated changes in resistance of the thin film resistor to temperature changes. Individual chips were diced using an ADT Dicing Saw 7120, epoxied to an FR4 PCB board, and ultrasonically wire bonded with a 75-µm diameter Al/Si wire to copper pads on the PCB board. Copper pins were then soldered to the copper pads, and extension wires were connected. The resistance of the aluminum resistors was monitored using a 4-wire resistance method with an Agilent 34401A digital multimeter as the temperature was changed in a temperature-controlled convection oven. The temperature was allowed to stabilize for 10 min before the resistance measurements were taken. A total of 5 structures were measured to ascertain the measurement error.

2.4. Thermal Characterization of the Substrates

Substrate characterization through electrical testing was carried out on whole wafers (4-inch) using a Cascade Microtech RF-1 manual probe station, HP 6207B DC power supply, Agilent 34401A digital multimeter and Digilent Analog Discovery board 2. An amplifying circuit, illustrated in Figure 3a, was built with an IRLZ24 power MOSFET driven by a waveform generator (Digilent AD2). A control resistor Rc of known resistance was placed in series with Rheat in order to measure the current flowing through Rheat. The oscilloscope channels of the Digilent Analog Discovery board 2 were used to measure the voltage drop V_C across R_C ($V_C = V_C^+ - V_C^-$) to accurately obtain the current (I_C) going through Rheat. Current (I_C) was obtained by taking the ratio of V_C over R_C. Real-time resistance of Rheat was then obtained by the ratio of I_C over V_h (the voltage drop between node V_h^+ and V_h^-). The power applied to the heating resistor (Rheat) was calculated using $P = I_C \times V_h$. With the real-time resistance of Rheat, the temperature of the Rheat resistor could be calculated from the measured TCR.

A separate circuit was used to simultaneously monitor the resistance and temperature of the sense resistors Rsense, which were located some distance away from the heat resistors, as presented in Figure 1. As shown in Figure 3b, similarly to the Rheat circuit, a control resistor Rc was placed in series with Rsense in order to measure the current flowing through Rsense. The oscilloscope channels of a separate Digilent Analog Discovery board 2 were used to measure the voltage drop V_C across R_C ($V_C = V_C^+ - V_C^-$) to accurately obtain the current (I_C) going through Rsense. The current (I_C) was obtained by taking the ratio of V_C over R_C. Real-time resistance of Rsense was obtained by the ratio of I_C over vs. (the voltage drop between node V_S^+ and V_S^-). With the real-time resistance of Rsense, the temperature of the Rsense resistor could be calculated from the measured TCR.

A schematic representation of the test setup is shown in Figure 4. The schematic shows a representation of the wafer being tested on a probe station with micro manipulators connected to the heat and sense resistors of a particular structure, as seen in the inset. The wafers were held to the 6-inch metal chuck of the probe station with a vacuum. The driving and sense circuitry allowed for real-time monitoring of the power that was being

applied as well as the resistance changes of the resistors being tested through four different oscilloscope channels. A function generator and a voltage supply were adjusted to supply the required power through the heat resistor as well as the desired waveform.

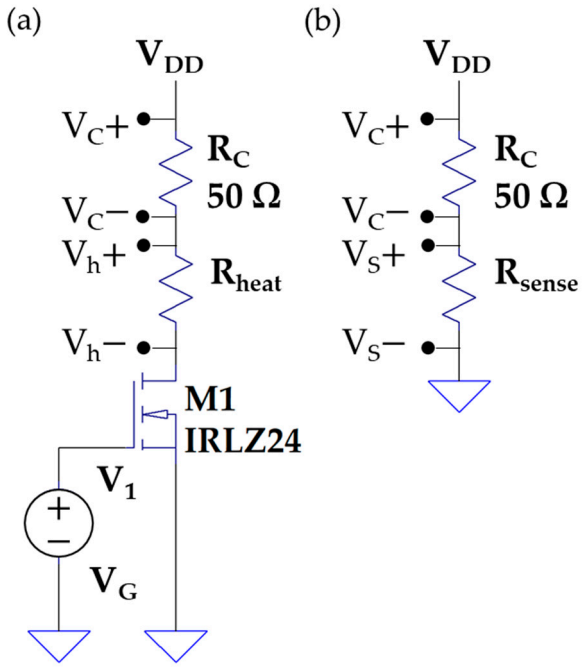


Figure 3. Schematics of the circuits used to measure the real-time resistance of (**a**) Rheat and (**b**) Rsense. The instantaneous power applied to Rheat was also measured. TCR was used to calculate the temperature of the heat and sense resistors.

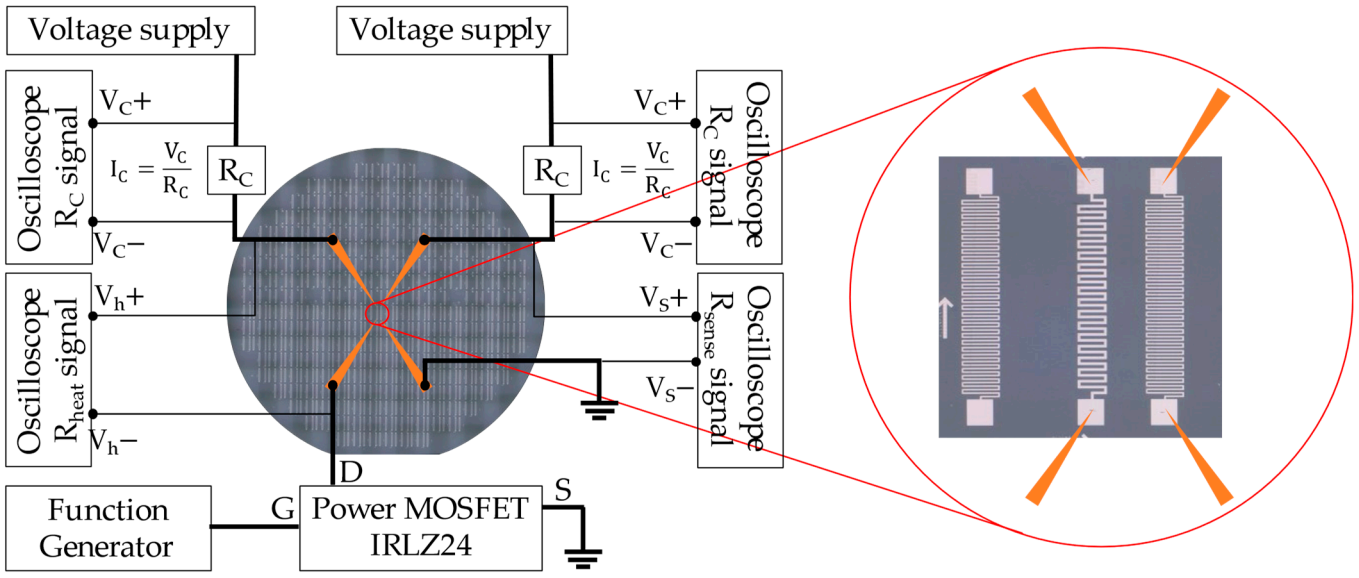


Figure 4. Schematic representation of the test setup showing the probes that connected to the heat and sense resistors and were connected to the driving and measuring circuits shown in the magnified image. Additional microscope images of the test structures on molybdenum, silicon, and fused silica glass substrates are shown in Figure S1a–c, respectively. The wafers were held with a vacuum to a 6-inch wafer chunk that acted as a heat sink.

A FLIR AX5 high-resolution thermal camera was used to measure the temperature of the devices and explore lateral thermal dissipation under steady state conditions. The

IR camera was calibrated by measuring the emissivity of each of the surface material according to the recommended procedure by the manufacturer. Emissivity values of 0.75 and 0.65 were found for TEOS and aluminum, respectively.

2.5. Finite Element Analysis

The finite element analysis software COMSOL Multiphysics™, version 5.6, was used to simulate a simplified heated structure and explore the theoretical thermal characteristics of the fabricated structures. A 3D model exploring heat transfer in solids was used. The governing equation of this model is:

$$Q + Q_{ted} = \rho C_p u \cdot \nabla T + \nabla \cdot q \quad (1)$$

where Q represents the heat source (W/m^3), Q_{ted} is the thermoelastic damping (W/m^3), ρ is the density (kg/m^3), C_p is the specific heat capacity at constant pressure (J/(kg·K)), u is the fluid velocity vector (m/s), ∇T is the temperature gradient (K), ∇ is the gradient operator, and q is the conductive heat flux (W/m^2).

The geometry created to represent the heated structure was composed of three stacked components: the substrate, TEOS layer, and an aluminum-heating element on top. The relevant material parameters for this study are listed in Table 1. The substrate was a block feature with dimensions of 10 mm × 10 mm × 250 µm (L × W × H). The oxide layer was a block feature with dimensions of 10 mm × 10 mm × 5 µm. In order to simplify the simulations, the heating element was represented as a rectangular feature with dimensions of 4 mm × 0.5 mm × 180 nm located directly in the top center of the substrate-oxide stack. These dimensions were intended to replicate the feature dimensions fabricated on the wafers tested.

Table 1. Material properties in solid phase.

Material	Density (kg m^{-3})	Specific Heat Capacity (J kg^{-1} K^{-1})	Thermal Conductivity (W m^{-1} K^{-1})
Molybdenum [18]	1.020×10^4	250	138
Silicon [14]	2.329×10^3	700	130
Fused silica glass [19]	2.203×10^3	703	1.38

The boundary conditions of the thermal model geometry can be described as follows. The entirety of the geometry, apart from the bottom-most boundary, was thermally isolated with an initial temperature of 298 K to neglect the minimal radiation losses. The bottom-most boundary of the geometry was set to be a constant temperature of 298 K, to emulate a chip mounted to a heat sink. Within the scope of the simulations performed, all solid materials experienced conductive heat transfer, while the air gap implemented in other simulations experienced minor radiation and convective heat transfer from the solid substrate above. It can be noted that the air gap modeled was merely microns thick to emulate the existence of debris and surface roughness-induced gaps and thus did not experience significant natural or forced convection. Further details on the simulation conditions are presented in the Supplementary Information.

3. Results and Discussion

3.1. Temperature Coefficient of Resistance Measurements

Figure 5a shows the resistance of Rheat and Rsense resistors of packaged devices in a convection oven as the temperature of the oven is increased. The temperature coefficient of resistance (TCR) α can be then extracted from the normalized slope as shown in Figure 5b according to Equations (2) and (3):

$$R_T = R_o(1 + \alpha \Delta T) \quad (2)$$

$$\alpha = \frac{(R_T - R_o)/R_o}{(T_T - T_o)} \quad (3)$$

where α is TCR, R_T represents the resistance at the temperature of interest, R_o is the resistance at a reference temperature, and $T_T - T_o$ is the change in temperature. As shown in Figure 5, the slope is 0.25%/°C for Rheat and 0.27%/°C for Rsense for a representative measurement. The estimated error of this value was based on the measurement of five different test structures and is indicated on the plot. These values are comparable to published work thin film (<200 nm) aluminum TCR ranging from 0.24 to 0.39%/°C [20–24] whereas a 0.4%/°C of TCR is typical for bulk aluminum films [25]. Thin film metals generally have a lower TCR in comparison to their bulk counterparts. This is due to material imperfections in the method of thin film deposition, such as vacancies, dislocations, foreign atoms, and refractory oxides [20]. As such, a TCR value of 0.26%/°C was used to convert the change in resistance to a temperature change from room temperature for the remainder of the experiment.

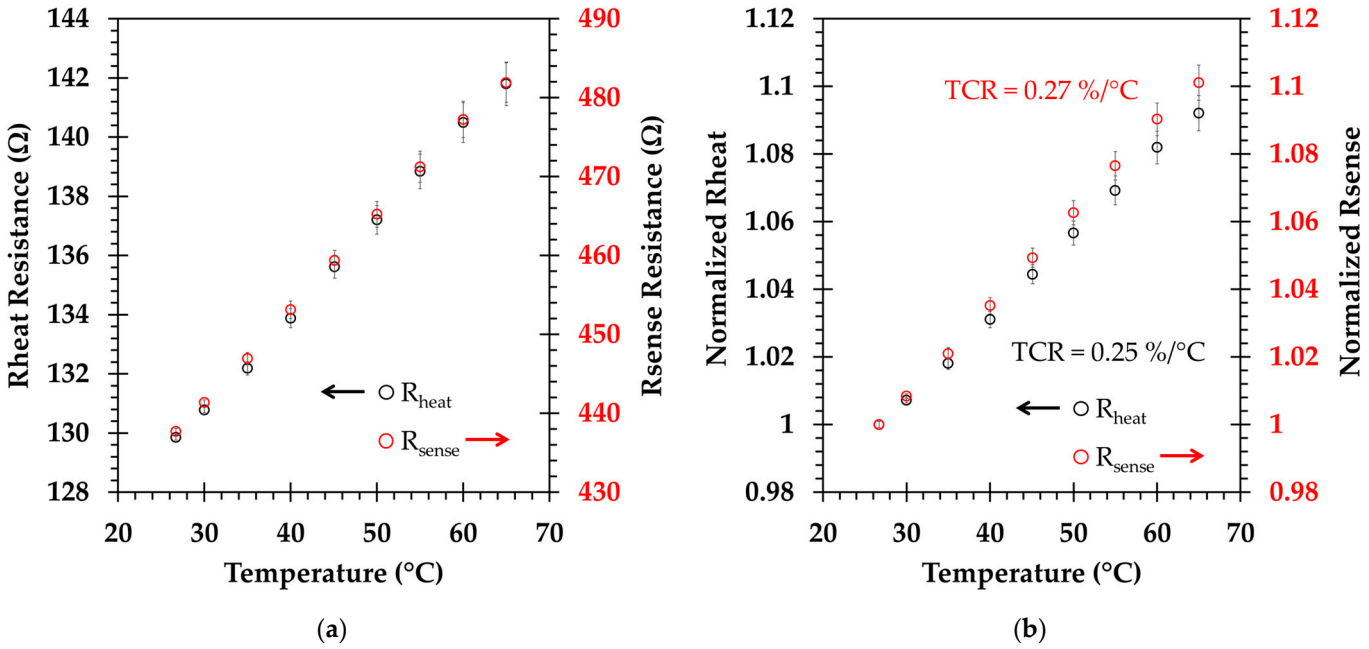


Figure 5. (**a**) Representative measured resistance of Rheat and Rsense as a function to temperature. (**b**) Normalized resistance as a function of temperature. The TCR value extracted from the slope is 0.25%/°C for Rheat and 0.26%/°C for Rsense.

3.2. Static Temperature Measurements

Electrical testing was performed on the fabricated devices as described in the Methods sections. Figure 6 shows the temperature increase of the heating resistor Rheat when 2 Watts of power is applied on the silicon and molybdenum substrate. The temperature increased rapidly from room temperature 25 °C to 40.6 °C and 39.9 °C (15 °C increase) for silicon and molybdenum, respectively, and remained at that temperature after ~200 ms. Only Rsense1 was monitored as the temperature of Rsense2 was too low to be measured in most cases. Rsense will describe Rsense1 from now on in this paper. The final temperature on the molybdenum substrate was slightly lower than on the silicon substrate. As such, the temperature of Rsense was slightly lower and only increased to 34.1 °C and 33.9 °C (~10 °C increase), respectively, as shown in Figure 7. Figure 6b shows that the temperature of the heating resistor on the fused silica glass substrates starts to reach steady-state around 500 ms and increases to a much higher temperature of 142.5 °C. On the other hand, the temperature of the sense resistors on the glass substrates only increases to 34.6 °C within that time period, which is slightly higher than that of the silicon and molybdenum substrates.

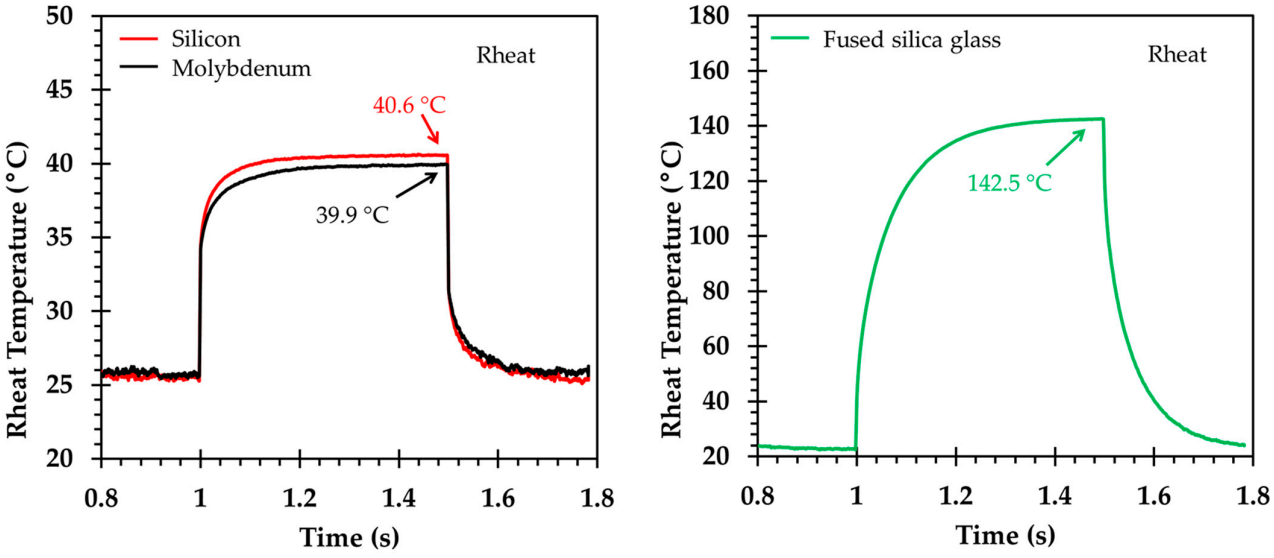


Figure 6. (**a**) Calculated temperature of the Rheat as function of time when 2 Watts of power are applied to Rheat for 0.5 s on the molybdenum and silicon substrates. (**b**) Calculated temperature of Rheat as function of time when 2 Watts of power are applied to Rheat for 0.5 s on the fused silica glass substrate.

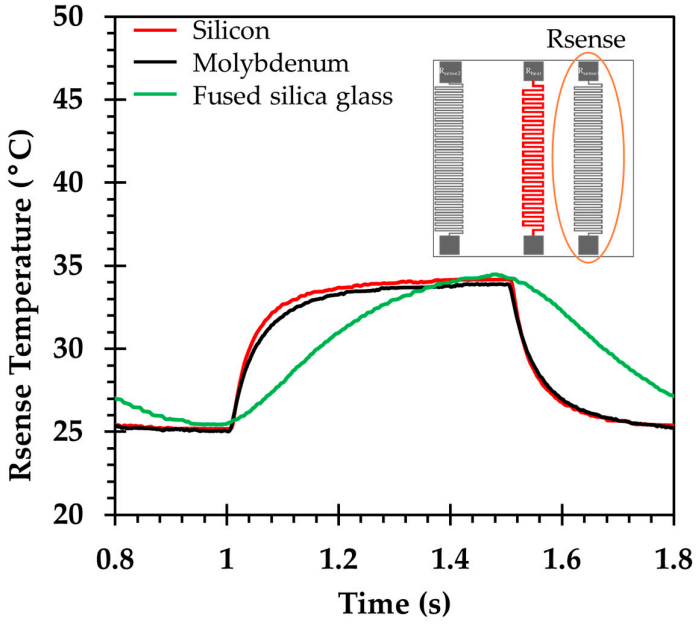
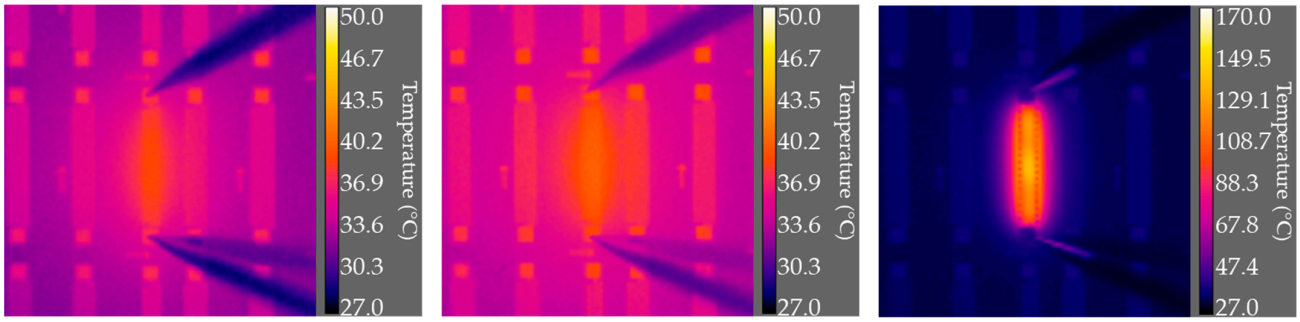


Figure 7. Calculated temperature of Rsense as function of time when 2 Watts of power are applied to Rheat for 0.5 s for all three substrates. Rsense is 0.6 mm away from the heat source as indicated in the inset. Only Rsense 1 (orange circled) was monitored as the temperature of Rsense2 was too low to be measured in most cases.

In addition, a FLIR AX5 high-resolution thermal camera was used to measure the temperature of the devices and explore lateral thermal dissipation. An emissivity value of 0.65, determined through calibration for the aluminum regions, was used in all the measurements since the temperature of the areas with aluminum was of most interest. Shown in Figure 8 are the static temperature measurements for (a) molybdenum, (b) silicon, and (c) fused silica glass substrates with power applied and under steady-state conditions. Table 2 summarizes the peak temperature of the heating resistor at each given power

output, 1 W, 2 W, and 2.7 W. The temperatures observed for an applied power of 2 Watts closely match those observed through electrical measurements of the resistance of the heater and sense resistors. It is also worth noting that molybdenum and silicon have almost the same temperature readout at identical power input to Rheat, with molybdenum being slightly lower than silicon. In addition, the lateral heat dissipation was observed to be higher for the silicon and molybdenum substrates, such that they increased in temperature at a similar rate as the heating resistors but decreased at a much faster rate on the fused silica glass substrates. This can be observed in better detail in Figure 9 where it is shown that the temperature on the fused silica glass substrate decays much faster laterally, reaching room temperature within 1 mm of the heat source, whereas the temperature of the silicon and molybdenum substrates remain elevated even at 3 mm away. It should also be noted that the discontinuities observed as the temperature was measured over the aluminum resistors, correspond to the different emissivity values of the surface materials (i.e., TEOS vs. aluminum). Complete thermal imaging for molybdenum, silicon, and fused silica glass substrates for Rheat at 0 W, 1 W, 2 W, and 2.7 W are shown in Supplementary Material Figure S3.



(**a**) (**b**) (**c**)

Figure 8. Static temperature measurement with a FLIR AX5 thermal camera for (**a**) molybdenum, (**b**) silicon, and (**c**) fused silica glass substrates with 2 W power applied to the heating resistor.

Table 2. Maximum temperature measurement at 1 W, 2 W, and 2.7 W power applied to Rheat.

Substrate	Power (W)		
	1 W	2 W	2.7 W
Molybdenum	36.7 °C	38.6 °C	40.3 °C
Silicon	37.1 °C	39.1 °C	40.9 °C
Fused silica glass	82.8 °C	136.0 °C	166.0 °C

3.3. Varied Pulse and Power Temperature Measurements

The thermal response to heat pulses of different frequencies and power was studied for the three different substrates. The applied power was introduced as a ½ sine wave in order to prevent any switching signal discontinuities on the monitoring signals, which follows a similar approach as Damcevska et al. [5]. For each substrate, signals were applied with peak powers of 1 W, 2 W, and 2.7 W—corresponding to 1.13 W/mm^2, 2.26 W/mm^2, and 3.05 W/mm^2 respectively, for pulses of 5, 10, 20, 50, and 100 ms.

As described in the methods section, the resistance of both the heat and sense resistors were calculated by measuring their voltage drop and the current flowing through a control resistor, which was in series with the resistors measured and was kept at room temperature. Figure 10 presents the data collected for a 1-W-5-ms pulse in a silicon substrate heating resistor, which is a representative set of the data collected at each of the test conditions. To provide an accurate measurement of the change in resistance, the heat and sense resistors were initially biased at around 1.2 V, which corresponds to about 0.05 W and should result in negligible heating. As shown in Figure 10a, a ½ sine wave was then applied which results in a voltage peak of ~4.5 V and a peak power of 1 W. The real-time resistance of

both the heat and sense resistors was monitored by measuring the voltage drop across each of them as well as the current flowing through a control resistor in series. As shown in Figure 10b, the measured resistance increases as the heating or sense resistor is heated and the temperature can be calculated by applying the previously measured TCR. The temperature response of the resistor corresponds to the temperature of the surface of the substrate and depends on the substrate's thermal characteristics. The peak temperature can also be extracted for each pulse condition.

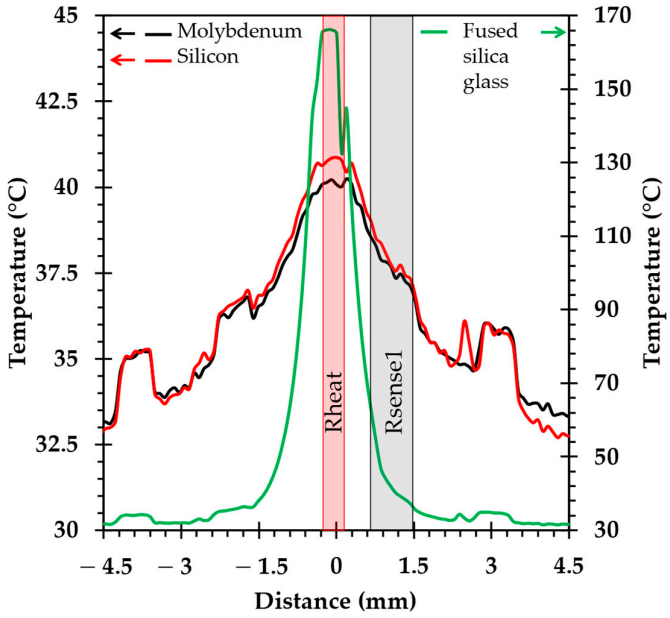
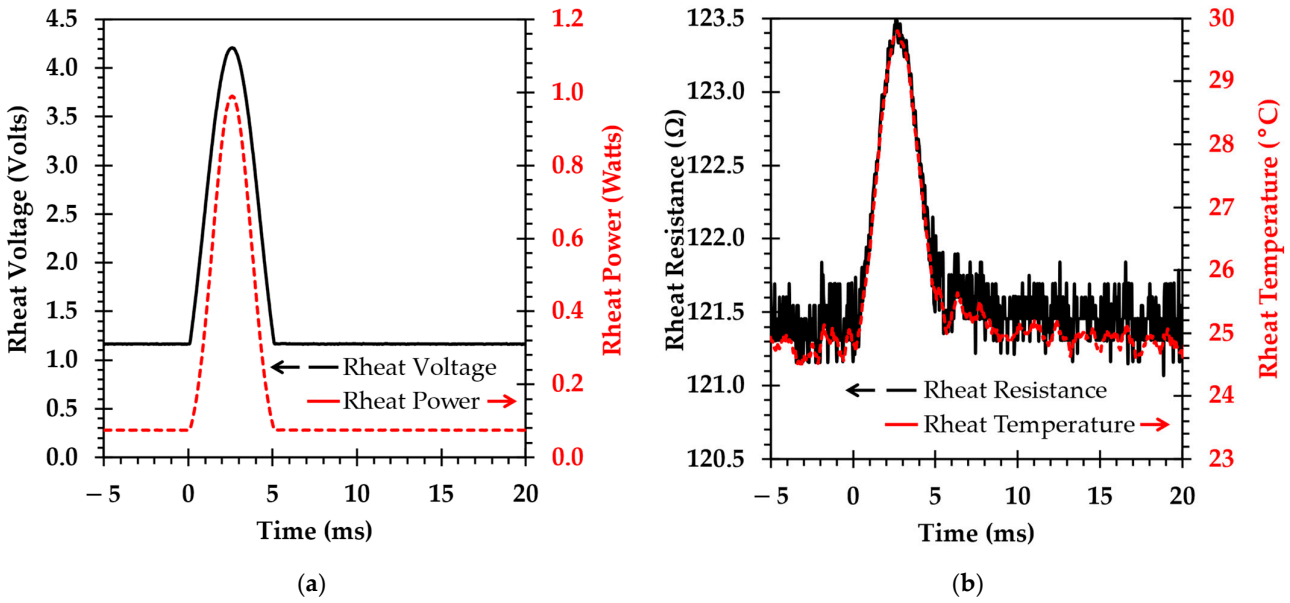


Figure 9. Temperature profile taken with a FLIR AX5 thermal camera for molybdenum, silicon, and fused silica glass substrates with 2 W of power as a function of the distance from the heating resistor. Shaded areas indicate the approximate locations of Rheat and Rsense resistors.



(**a**) (**b**)

Figure 10. Representative test conditions and resultant measured values when a 1 W-5 ms-½ sine pulse is applied to the heat resistor. (**a**) Voltage measured across the heat resistor (left *y*-axis) and corresponding power calculated (right *y*-axis). (**b**) Measured resistance of the heat resistor (Rheat) (left *y*-axis), and corresponding calculated temperature from the measured TCR (right *y*-axis).

Figure 11a–f shows the calculated temperature responses of the heat resistors fabricated on silicon and molybdenum substrates for pulses of different frequencies and powers. The thermal response increases with respect to increasing power as expected, but also with increasing pulse time, which would indicate that a steady-state condition has not been reached. The thermal response of the silicon and molybdenum substrates is very similar for all power conditions as expected since the thermal conductivity of silicon and molybdenum are similar to one another at 130 W/m·K and 138 W/m·K, respectively. On the other hand, no major differences were observed in the time response even though the heat capacitance of silicon and molybdenum are significantly different at 700 J/kg·K and 250 J/kg·K, respectively. These results indicate that the thermal conductivity dominates under these particular dimensions of the substrates and the difference in specific heat capacitance is not observed.

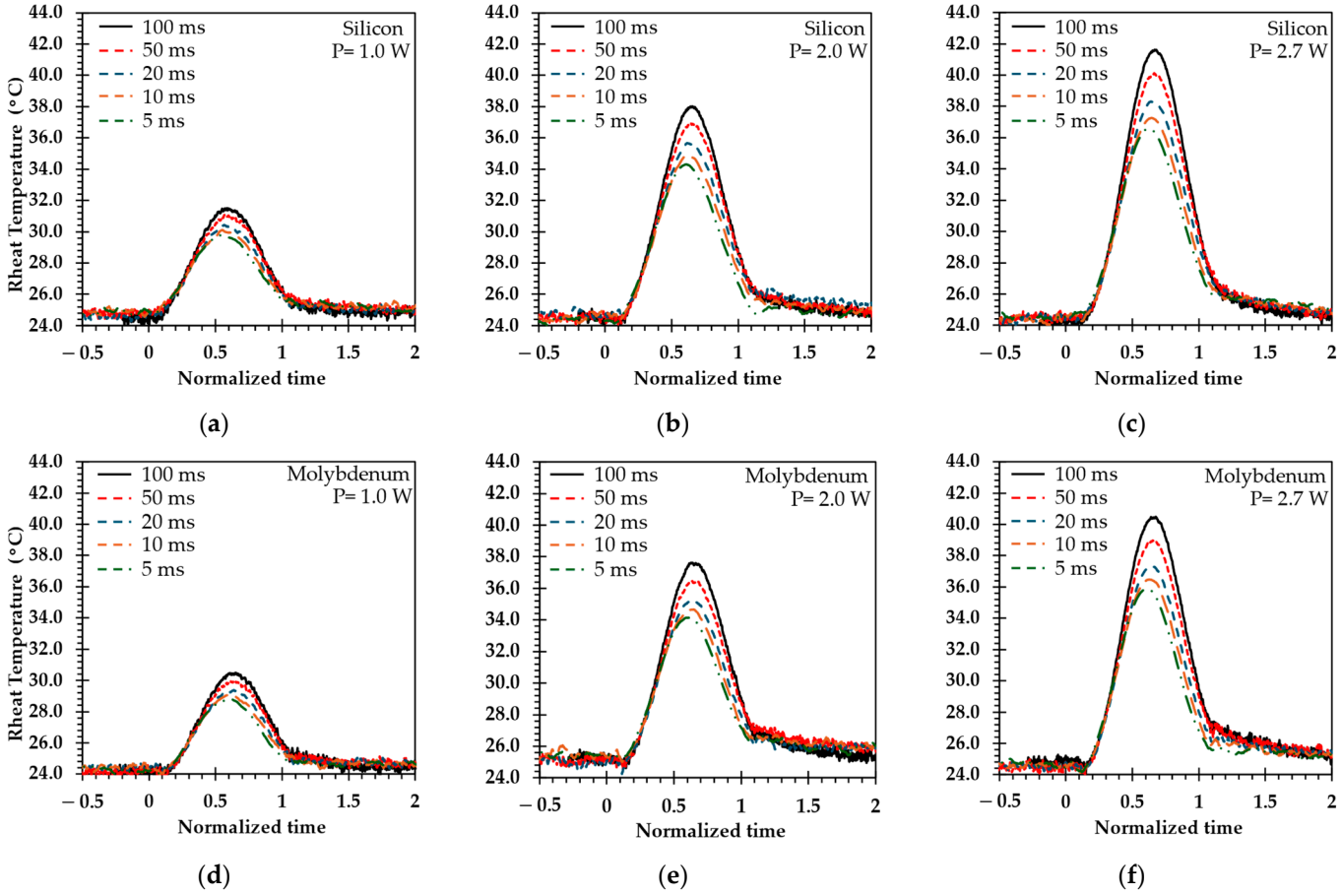


Figure 11. Temperature of the heat resistors fabricated on a silicon substrate when (**a**) 1 W peak pulse at five different pulse times is applied, (**b**,**c**) show the response for 2 W and 2.7 W peak pulses, respectively. (**d**–**f**) show the temperature of the heat resistors fabricated on molybdenum substrates for the indicated pulse conditions.

Figure 12a–c shows the measured temperature responses of the heat resistors fabricated on fused silica glass substrates for pulses of different frequencies and powers. Unlike Si and Mo, glass substrates experience a noticeable increase in the time it takes for the temperature to return to its initial value. In addition, the peak temperature is significantly higher for glass substrates, indicating that the glass substrate does not dissipate the heat away as effectively as the silicon and molybdenum substrates as expected, due to the thermal conductivity of glass being 1.38 W/m·K, magnitudes lower than silicon and molybdenum.

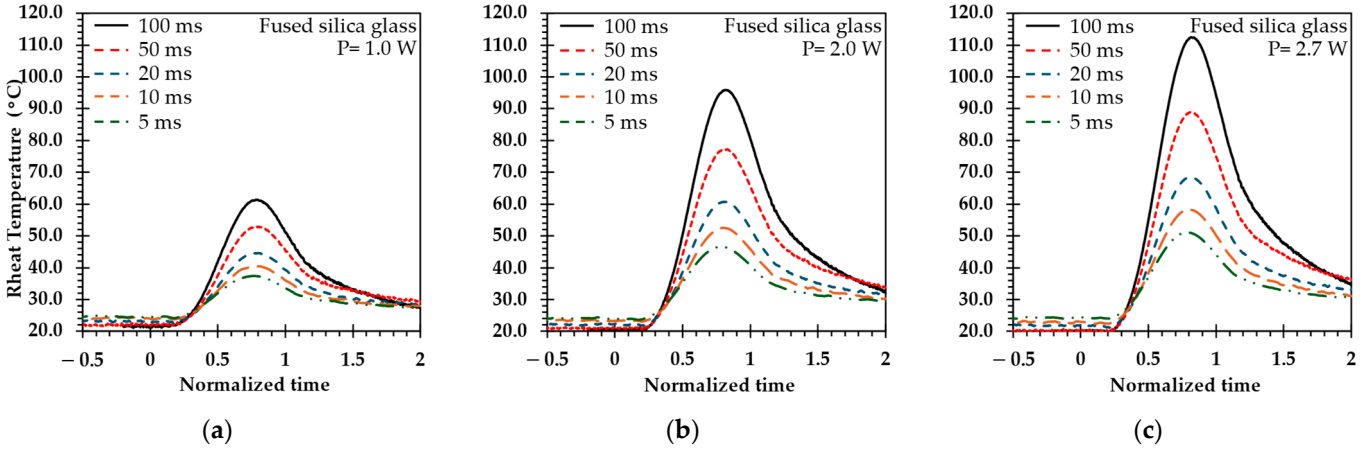


Figure 12. Plot (**a**) shows temperature of the heat resistors fabricated on a fused silica glass substrate for 1 W peak pulse at five different pulse times, graphs (**b**,**c**) show 2 W and 2.7 W peak pulses, respectively.

Peak temperature values were extracted from each of the pulses for silicon, molybdenum, and glass as shown in Figure 13. In Figure 13a, the peak temperatures of silicon and molybdenum have a similar trend and fall close to one another, with molybdenum being slightly lower. In Figure 13b the maximum temperature of glass was significantly higher than that of silicon and molybdenum. The peak temperatures continue to increase over the pulse times studied, indicating that a steady-state temperature has not been achieved. This is consistent with the data presented in Figures 6 and 7 where it is shown that silicon and molybdenum reached steady-state for t > 200 ms and the fused silica glass for t > 500 ms.

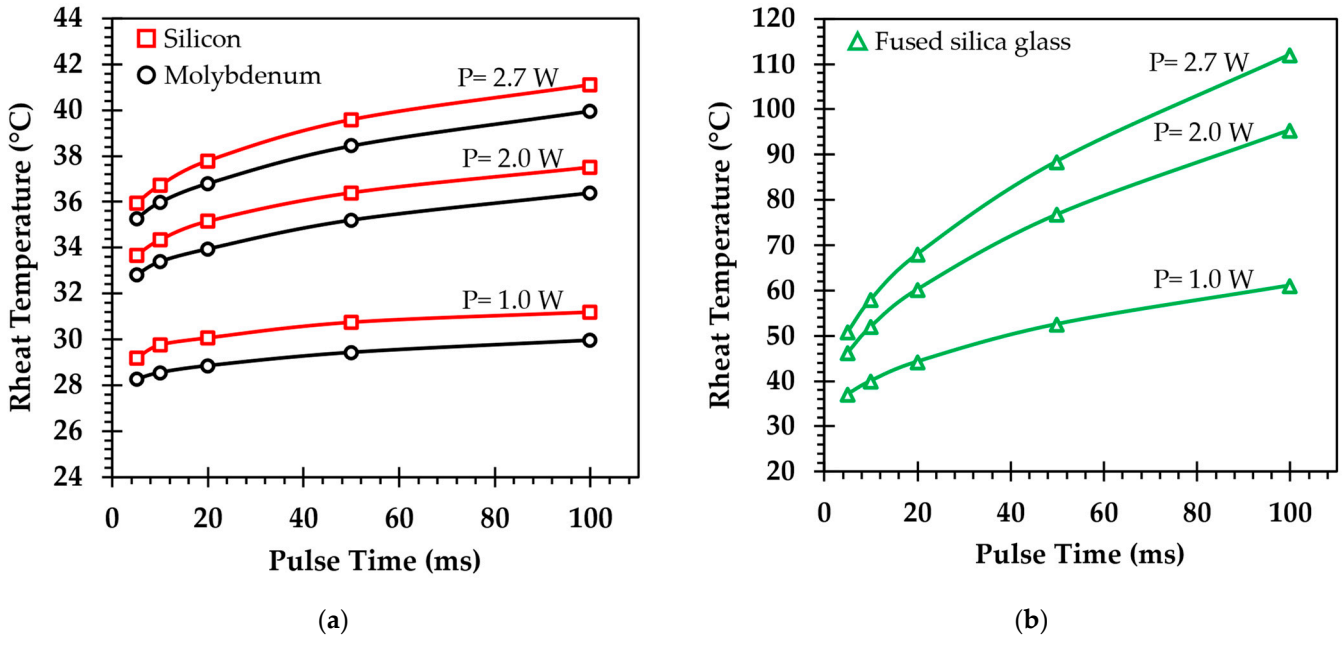


Figure 13. Measured peak temperature of the heat resistors for different pulse duration and power levels for (**a**) silicon and molybdenum substrates; (**b**) fused silica glass substrate.

3.4. Finite Element Analysis Modeling

As described in the test methods, the temperatures of the sense resistors described in Figure 1 were simultaneously monitored as the power and pulse time were varied. This was performed in order to analyze the heat dissipation properties of the substrates in the lateral direction. Only Rsense1 was monitored as the temperature of Rsense2 was too low to be measured in most cases. Rsense will describe Rsense1 from now on in this paper.

Figure 14 shows the peak temperature of the sense resistors when a ½ sine wave signal with a power peak of 2.7 W and different pulse times were applied to the heat resistors. As seen in Figure 14, the temperature of the heat resistors for silicon and molybdenum was similar and about 4 °C lower than that of the heat resistor for the shown bias conditions. On the other hand, the sense resistors built on the fused silica glass substrates were lower than those built on silicon and molybdenum and about 50 to 100 °C lower than its heat resistors. These results indicate that the high thermal conductivity of silicon and molybdenum allows the heat to easily spread laterally. In contrast, for a fused silica glass substrate, the heat is concentrated around where it is generated. These results agree with the observations made with the infrared camera and presented in Figure 9, where the temperature of the glass substrates decreased to room temperature in a shorter lateral distance than that of silicon or molybdenum.

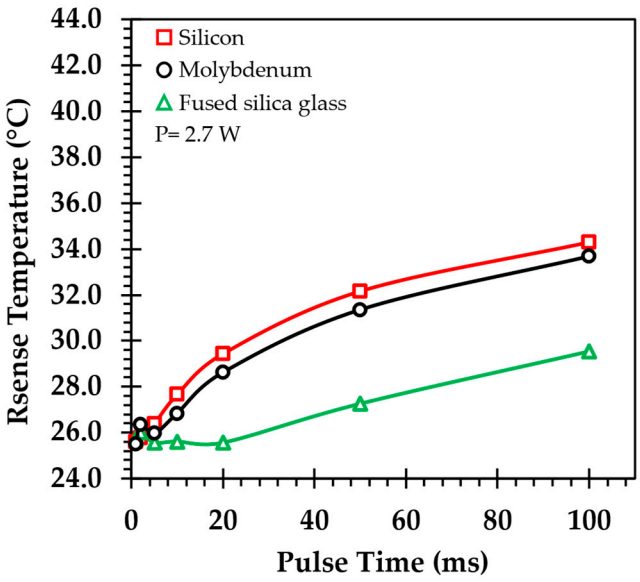
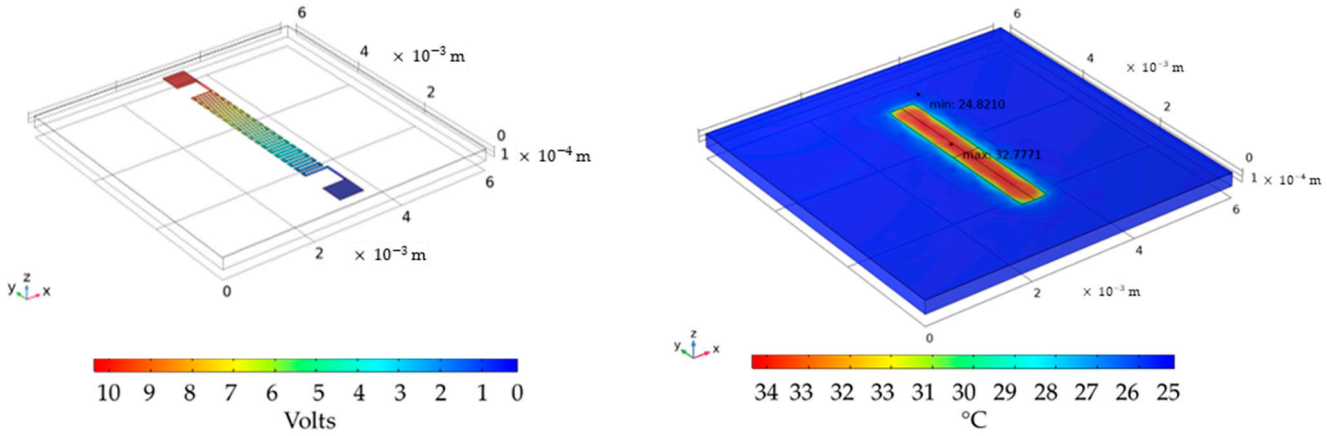


Figure 14. Measured peak temperature of the sense resistors for different pulse duration and power levels, indicating that heat dissipates laterally at a lower rate on the fused silica glass substrates.

Finite element analysis was performed to evaluate the validity of the test results and to investigate other test conditions. A model in COMSOL Multiphysics™ software was used, indicated in the methods sections and described in more detail in the Supplementary Information. The arrangement illustrated in Figure 15a was initially constructed to investigate the heat generated with a serpentine heating element. The material stack matches are presented in Figure 2. The bottom of the substrate was set to a room temperature of 25 °C to match the test conditions. Figure 15a shows a uniform 10 V drop along the length of the serpentine resistor which results in a uniform thermal power generation along its length. As such, a simplified model of the heating resistor was used as shown in Figure 15b. Figure 15b shows a typical output obtained through these simulations where the maximum surface temperature is at the center of the heating resistor.

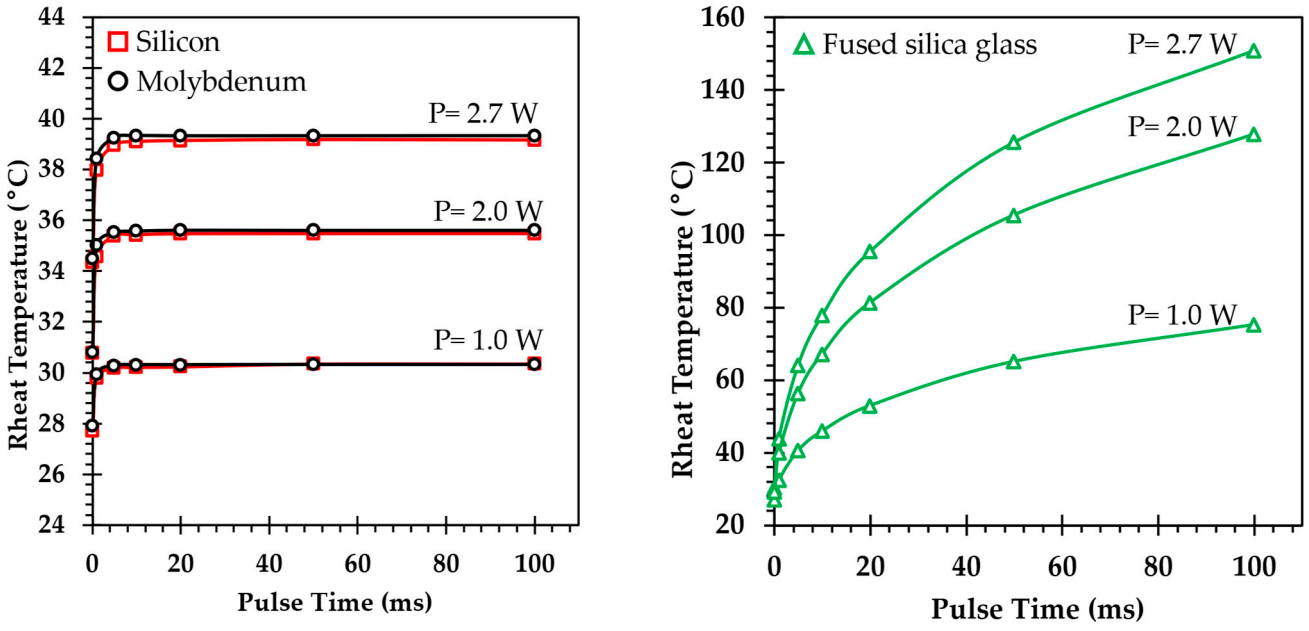
In order to match the experimental test conditions, the application of different frequencies and peak powers was studied for the three different substrates. The applied power was introduced as a squared ½ sine wave to account for the fact that power instead of voltage was applied. Figure 16 shows the peak temperatures of the different substrates for the applied peak powers and pulse durations. Additional pulse times of shorter duration of 1 ms and 0.1 ms were also simulated. The results indicate that temperature values were in the same range as those obtained experimentally both through electrical measurements and using the infrared camera. This validates our methodology since the simulation model was based on the physical phenomena and included the thermal properties of the materials. In contrast to the experimental data, the peak temperature of the silicon and molybdenum

substrates seemed to plateau after 5 ms, indicating that the system reached steady-state at that time. The experimental results indicated that steady-state was not reached until later at t > 200 ms. The temperature of the fused silica substrate did not reach steady state in the time interval studied, indicating that the lower thermal conductivity contributes to the continuous accumulation of heat and a longer time to reach steady-state.



(**a**) (**b**)

Figure 15. Finite element model of (**a**) serpentine heater with 10 Volts applied and (**b**) 2 Watts of power applied to a rectangular prism that represents the heating structure while simplifying the computational resources.



(**a**) (**b**)

Figure 16. Simulated measured peak temperature of the heat resistors for different pulse duration and power levels for (**a**) silicon and molybdenum substrates; (**b**) fused silica glass substrate.

To investigate the discrepancy between the experimental and simulated results, the bottom surface of the silicon and molybdenum was modified and a low thermal conductivity layer, consisting of a 5 µm air gap, was added. The existence of any gaps of air at the substrate–heat sink interface was expected to drastically effect the heat management of the system, such that the only heat transfer that occurs through air is through radiation, as

opposed to the ideal solid thermal conduction. These gaps are typically caused by surface roughness and non-uniformity at the substrate–heat sink interface. Experimentally, the substrates were held down to the 6 inch chuck probe station, which acted as a large heat sink, with a vacuum of ~14.7 psi, and air gaps were expected.

The additional simulation results, containing a layer of air, shown in Figure 17, indicated that with a non-ideal thermal contact to the back of the silicon and molybdenum substrates, heat was dissipated much less efficiently, and a steady state was not reached until a much later time. The effect of this poor thermal connection in the simulation results more closely resembles the experimental results. A direct comparison of the simulated and experimental data is presented in Figure S5 of the Supplementary Information. Even with the addition of a low thermal conductive layer, a perfect match between the experimental and simulated data was not observed. This illustrates the difficulties of matching real-life conditions to a simulation model and validates the need for real-life techniques and measurements in thermal analysis.

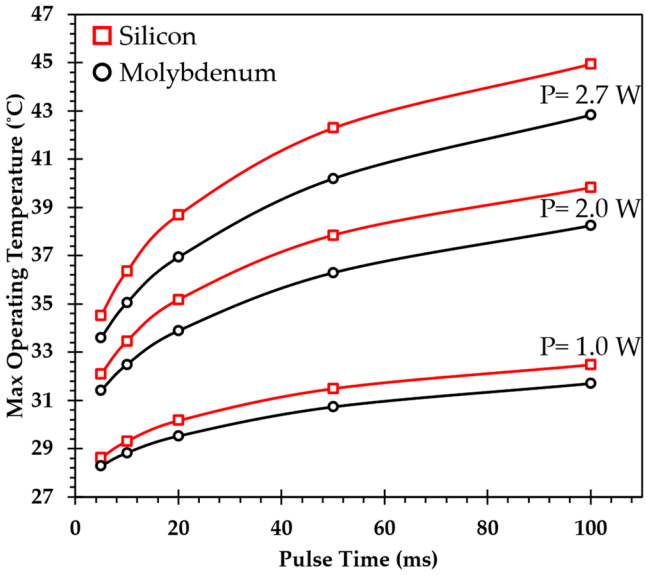


Figure 17. Simulated measured peak temperature of the heat resistors for different pulse durations and power levels for silicon and molybdenum substrates with an additional 5 μm air gap between the substrate and the room temperature heat sink with the purpose of emulating a bad thermal connection due to debris and non-uniform substrate geometry.

These observations illustrate that while it is still critical to utilize substrates and heat sinks comprised of materials with high thermal conductivity, it is just as important to maintain a good thermal connection at the substrate–heat sink interface. To accomplish this, various methods and materials can be used. These can range from basic thermal management supplies, such as thermal paste/grease, thermal pads, and solder bonds [26,27], to advanced micro-scale thermal management developments, such as carbon/metal microtubes, microchannel cooling, and wicking structures depending on specific device and heat management needs [28,29]. Some of these micro-structures can even be fabricated in conjunction with each other to form pseudo-heat pipes at a micro-scale, allowing for increased heat dissipation rates while maintaining device scaling and performance [30].

The data presented in this work demonstrate the feasibility of the proposed system-on-foil technology as an advanced packaging solution for improved heat management and device operation. Metal-based substrates, such as molybdenum, with much higher thermal conductivities, provide lower maximum operating temperatures and can be made thinner than traditional substrates for a lower thermal resistance [5]. Glass substrates, with a much lower thermal conductivity, are much slower to reach maximum steady-state temperatures and can be used to thermally isolate specific areas of a chip. Work presented by Lei et al. on parylene-filled trenches utilized a similar approach of incorporating a low thermal conductiv-

ity material (parylene) to isolate heat from areas of the fabricated silicon chip [31]. However, the approach of the work suffers from material delamination and a limited temperature range of operation, which has to be constrained below the melting temperature of parylene. Lastly, the presented simulation and experimental data can support silicon oxide-based materials to be used as an insulating trench around the perimeter of a chip or device, allowing multiple chips to be placed in much closer proximity while preventing heat transfer from one chip to another for future advanced 3D packaging architecture approaches.

4. Conclusions

This work shows a comprehensive comparison of the thermal properties between molybdenum, silicon, and fused silica glass substrates through the fabrication of heating and sensing thin-film resistors on 250 μm thick wafer substrates. The temperature coefficient of resistance of the fabricated resistors was measured and used to calculate the temperature of the surface of the substrates when different power conditions were applied. The results indicate that molybdenum and silicon vertically dissipate heat effectively as the surface temperature only increases by ~10–20 °C when continuous 1.2–3.1 W/mm^2 of heat is applied. In contrast, the surface temperature of fused silica glass substrates increases by >140 °C for the same applied power. On the other hand, fused silica glass substrate is more effective at laterally insulating heat as the surface temperature decreases to room temperature within a lateral distance of 1.5mm. In contrast, the temperature of silicon and molybdenum substrates only decreases slightly at an equal distance. These measurements and observations were validated with infrared camera measurements as well as through finite element analysis via COMSOL simulation. The importance of a good thermal connection is also presented and discussed. Finally, a hybrid approach that combines the high and low thermal conduction of these materials is discussed. Overall, the presented work and analysis provides guidance on the electrical characterization of the thermal properties of materials for advanced electronics packaging as well as future directions.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/electronics13101818/s1, Figure S1: Microscope image of test structures on (a) molybdenum, (b) silicon, and (c) fused silica glass substrates; Figure S2: Microscope image of test structures on (a) molybdenum, (b) silicon, and (c) fused silica glass substrates; Figure S3: Static temperature measurement with a FLIR AX5 thermal camera for (a–d) molybdenum, (e–h) silicon, and (i–l) fused silica glass substrates with 0 W, 1 W, 2 W, and 2.7 W power from heating resistor (Rheat); Figure S4: 3D isometric and 2D cross-sectional views of test structures modeled in component thickness correspond to dimensions referenced in Figure 3. Figure S5. Superimposed simulation (dotted line) and experimental (solid line) measured peak temperature.

Author Contributions: Conceptualization, T.-J.H., C.M., G.H., S.M. and I.P.; methodology, T.-J.H.; software, T.K. and I.P.; validation, T.-J.H., T.K. and I.P.; formal analysis, T.-J.H. and I.P.; investigation, T.-J.H., T.K. and I.P.; resources, T.-J.H., C.M., G.H., S.M. and I.P.; data curation, T.-J.H., T.K. and I.P.; writing—original draft preparation, T.-J.H., T.K., P.S. and I.P.; writing—review and editing, T.-J.H., T.K., P.S. and I.P.; visualization, T.-J.H. and I.P.; supervision, I.P.; project administration, C.M., G.H., S.M. and I.P.; funding acquisition, C.M., G.H., S.M. and I.P. All authors have read and agreed to the published version of the manuscript.

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