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A 55 nm CMOS RF Transmitter Front-End with an Active Mixer and a Class-E Power Amplifier for 433 MHz ISM Band Applications

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Abstract: In order to meet the increasing demands of wireless communication for ISM bands, a 433 MHz transmitter RF front-end is designed using a 55 nm low-power CMOS technology. The circuits consist of an active mixer, a driver amplifier and a class-E power amplifier (PA). A double-balanced Gilbert active mixer is designed to realize binary phase-shift keying (BPSK) modulation. The driver is used to preamplify the modulated RF signals. The class-E PA adopts a parallel four-branch cascode structure to control the output power level. The load network of the PA is implemented through an off-chip circuit, in which a finite DC-feed inductance load network is selected to reduce the power loss. The mixer and driver are designed with a 1.2 V supply voltage, while the PA is operated at a 1.8 V supply voltage. The area of the chip is 0.206 mm × 0.089 mm, and the measured results show that it achieves a maximum output power of 2.7 dBm, with a total power consumption of 6.72 mW. At a drain efficiency (DE) of 34.5%, an S_{22} less than −10 dB over the frequency ranges from 393.79 MHz to 455.70 MHz can be measured for the PA. With 192 kbps BPSK data modulated at 433 MHz, the measured EVM is about 0.83% rms.

Keywords: transmitter front-end; active mixer; driver; class-E power amplifier (PA); BPSK modulation

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1. Introduction

Wireless communication devices play a crucial role in the modern electronic market [1–6]. The direct conversion transceiver architecture is widely used, having the advantage of lower complexity [6]. For a direct upconversion transmitter, the baseband signals must be upconverted to RF band by a mixer and then amplified by a power amplifier (PA) before they are transmitted by an antenna. To improve the output power level, a driver is always needed to preamplify the RF signals before the PA [2,5]. Generally, the performances of the mixer and the PA are of vital importance to wireless transmitters [7].

The spectral purity and error vector magnitude (EVM) of the transmitted signals are mainly restricted by the mixer [6]. A passive or an active mixer can be used to realize upconversion in transmitters. Passive mixers exhibit higher switching speed, high linearity and lower noise, but they often bring about conversion loss and require high local oscillating signal power. In the meantime, active mixers can provide higher conversion gain and higher port isolation with lower local oscillating signal power requirements. However, the active mixers have higher noise than their passive counterparts [5,8]. Considering both advantage and disadvantage of passive and active mixers, the active mixers with Gilbert topology are the most common choice, owing to their high conversion gain and high reverse isolation [6,9].

As class-E PAs can theoretically achieve a drain efficiency (DE) of 100%, they stand out from various kinds of PAs and are the first choice for many transmitters [10–16]. However, it is noted that class-E PAs often could not achieve the theoretical efficiency due

to nonidealities in their circuit implementations [1,10–16]. One of the reasons is that a finite on-resistance causes a significant drop in DE and output power [1,17]. To decrease the power loss, a finite DC-feed inductance load network is proposed and is widely used in class-E PAs [18,19].

To meet the short-range wireless communication requirements for the 433 MHz ISM band, this paper presents a transmitter RF front-end fabricated in a 55 nm low-power (LP) CMOS technology. The main contributions of this work are summarized below:

1. A standard transmitter RF front-end is designed, and the block diagram is shown in Figure 1. The circuits consist of an active mixer, a driver and a class-E PA. A double-balanced Gilbert active mixer is designed to realize BPSK modulation. The driver is used to preamplifiy the RF signal, and the PA adopts a parallel four-branch cascode structure to control the output power level.
2. Since the transmitter RF front-end is mainly used in the transmission of digitized low-frequency signals such as voice signals, a 192 kbps data rate is selected for the transmitters. The experimental results show that the transmitter RF front-end can achieve a better error vector magnitude (EVM) when compared with similar works.

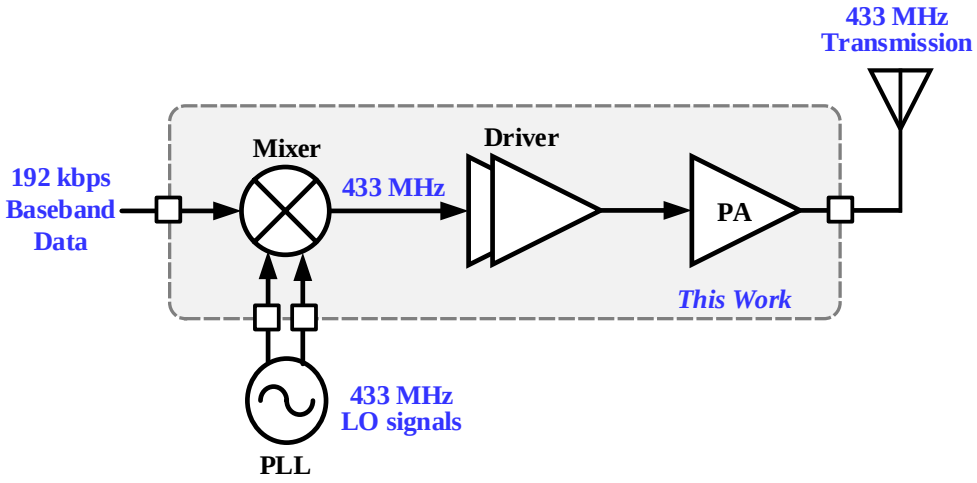

Figure 1. The block diagram of the transmitter RF front-end.

This paper is arranged as follows: Section 2 presents the principles and analysis for the circuits. Section 3 gives the circuit design of the transmitter RF front-end. Section 4 shows the experimental results. Section 5 discusses the limitation and potential future work. Finally, conclusions are drawn in Section 6.

2. Analysis of Circuits

2.1. Analysis of the Gilbert Mixer

Figure 2 illustrates a simplified schematic of a double-balanced Gilbert mixer, which converts the baseband and local oscillating voltage signals to currents, mixes the currents together as RF currents and converts the RF currents to output voltages via load resistors. Since the input transconductance and output transresistance can be designed as large values, the mixer can theoretically yield an arbitrarily high gain.

LOP and LON are the differential local oscillating signals, and DP and DN are the baseband signals, which are "1" or "0". Therefore, the transistors $M_1 \sim M_6$ operate in switching mode. Assume the waveform of the local oscillating signal is a sinusoidal signal and can be expressed as

$$V_{LO}(t) = V_{LO} \sin(\omega_{LO} t + \theta) \quad (1)$$

where V_{LO}, ω_{LO} and θ are the magnitude, frequency and initial phase of the local oscillating signal, respectively. The baseband signal is the differential square signal and can be

regarded as the superposition of sinusoidal waves with multiple frequency components. The baseband signal can be expressed as

$$V_{BB}(t) = \frac{4}{\pi}(sin\omega_{BB}(t) + \frac{1}{3}sin3\omega_{BB}(t) + \frac{1}{5}sin5\omega_{BB}(t) + ...) \tag{2}$$

where ω_{BB} represents the frequency of the baseband signal.

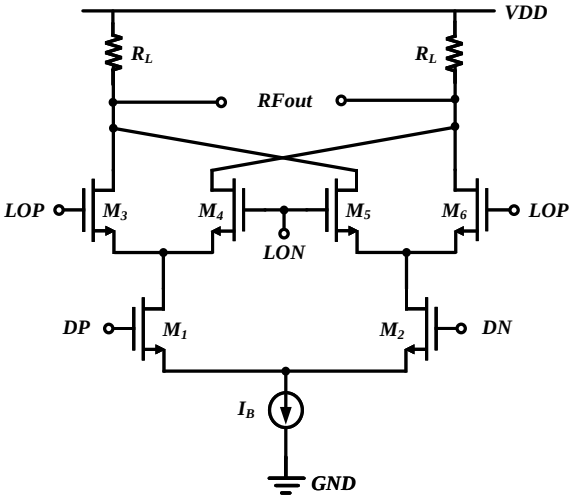

Figure 2. The schematic of a simplified Gilbert mixer.

When M_1 turns on, the current passing through M_3 can be written as

$$I_D(t) = g_m V_{LO} \sin(\omega_{LO} t + \theta) \tag{3}$$

where g_m is the transconductance of M_{3-6}. Because M_1 and M_2 are driven by baseband square signals, they can be regarded as ideal switches. The currents passing through M_1 and M_3 are mixed together and converted to voltage signal via load resistor R_L. The voltage signal can be written as

$$\begin{aligned} V_{RF}(t) &= g_m V_{LO}(t) V_{BB}(t) R_L \\ &= \frac{2}{\pi} g_m V_{LO} R_L [cos(\omega_{LO} + \omega_{BB})t + cos(\omega_{LO} - \omega_{BB})t + ...] \end{aligned} \tag{4}$$

Therefore, the conversion gain of the mixer can be calculated as

$$CG_{Mixer} = \frac{V_{RF}}{V_{LO}} \approx \frac{2}{\pi} g_m R_L \tag{5}$$

where V_{RF} is the magnitude of the modulated signal. It can be seen from (5) that the modulated signal includes neither the baseband nor the local frequency components. Hence, the ideal double-balanced Gilbert mixer can effectively suppress the baseband and local signal feedthrough.

2.2. Analysis of the Class-E PA

The simplified schematic of a class-E PA is shown in Figure 3a, which consists of a transistor M_1 operating in switching mode, a choke inductor L_0 to isolate AC and DC signals, a shunt capacitor C_p and a compensation inductor L_x to adjust the current and voltage waveform, as well as a resonant circuit including L_s and C_s to select the fundamental frequency signal. The equivalent circuit diagram of Class-E PA is shown in Figure 3b, in which M_1 is replaced by an ideal switch. Assuming the switch is driven by a square wave with a duty cycle of 50%, the circuit can be divided into two modes. When the switch is closed (i.e., $0 \leq \omega t < \pi$), the voltage across the switch is 0 and the current is not 0. When

the switch is open (i.e., $\pi \leq \omega t < 2\pi$), the current through the switch is 0 and the voltage is not 0. The current flowing through LC resonant circuit i_L can be derived by

$$i_L = I_L \sin(\omega t + \varphi) \tag{6}$$

where ω and φ are the frequency and initial phase of the driving signal. I_L is the magnitude of the current flowing through LC resonant. The total currents of the switch i_{SW} and shunt capacitor i_{Cp} can be written as

$$i_{SW} + i_{Cp} = I_0 - i_L = I_0 - I_L \sin(\omega t + \varphi) \tag{7}$$

where I_0 is the current flowing the choke inductor. When $\omega t \in [0,\pi)$, the switch is closed, and the currents of the switch and shunt capacitor can be derived by

$$\begin{cases} i_{SW} = I_0 - I_L \sin(\omega t + \phi) \\ i_{Cp} = 0 \end{cases} \tag{8}$$

where ϕ is the initial phase of the current flowing through LC resonant. The voltage of the switch can be written as

$$v_{SW} = 0 \tag{9}$$

When $\omega t \in [\pi,2\pi)$, the switch is open, and the current of the switch and shunt capacitor can be derived by

$$\begin{cases} i_{SW} = 0 \\ i_{Cp} = i_0 - I_L \sin(\omega t + \phi) \end{cases} \tag{10}$$

and the voltage of the switch can be written as

$$v_{SW} = v_{Cp} = \frac{1}{\omega C_p} \int_{\pi}^{\omega t} i_{Cp} d(\omega t) = \frac{1}{\omega C_p} \int_{\pi}^{\omega t} (I_0 - I_L \sin(\omega t + \phi)) d(\omega t) \tag{11}$$

The driver signal, current waveform and voltage waveform of the switch are shown in Figure 4. It can be seen from the figure that the current and voltage of the switch do not overlap in the time domain. As a result, the circuit has no power consumption and its efficiency can ideally be up to 100%. The ideal operating conditions for Class-E PAs are ZVS (Zero Voltage Switch) and ZVDS (Zero Voltage Derivative Switch), which can be written as

$$\begin{cases} v(\omega t) = 0 & \omega t \in (2n\pi, (2n+1)\pi], n = 0, 1, 2, 3\ldots \\ \frac{dv(\omega t)}{d\omega t} = 0 & \omega t = 2n\pi, n = 1, 2, 3\ldots \end{cases} \tag{12}$$

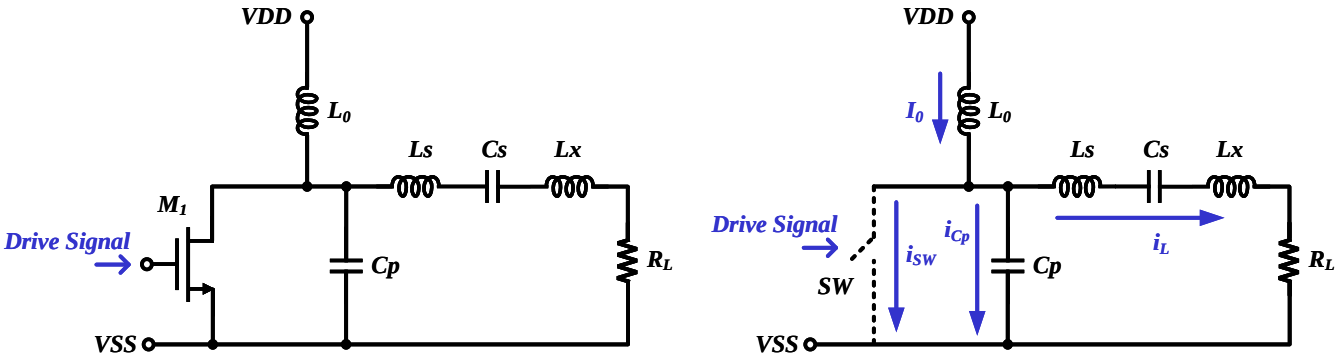

Figure 3. (**a**) The simplified schematic of class-E PA. (**b**) Equivalent circuit diagram of class-E PA.

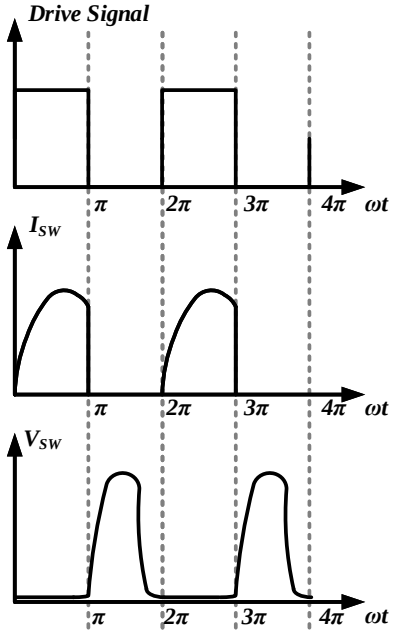

Figure 4. The driver signal, current waveform and voltage waveform of the switch.

3. Circuit Design

As shown in Figure 1, the overall architecture includes a double-balanced Gilbert mixer, a driver and a class-E PA. The circuits are designed in a 55 nm LP CMOS process, and the supply voltage of the mixer and the driver is 1.2 V. To obtain an RF signal with a high power level, the PA adopts 1.8 V supply voltage. The design targets are listed in Table 1.

Table 1. The design targets.

Design Parameter	Value
Technology	55 nm
Supply Voltage	1.2/1.8 V
Operating Frequency	433.92 MHz
Data Rate	192 kbps
Overall Conversion Gain	>40 dB
Power Consumption	<6 mW
Maximum Output Power	>3 dBm

With the above design targets, this section illustrates the detailed circuits and design procedures.

3.1. Mixer and Driver Stage Circuit Design

The baseband signals need to be upconverted to RF signals by a mixer and then preamplified by a driver before they arrive at a PA. The schematic of the mixer and the driver is shown in Figure 5.

To achieve a better isolation performance, a double-balanced Gilbert mixing topology is selected. $M_1 \sim M_2$ are the input transistors for the baseband signals. $M_3 \sim M_6$ are the input transistors for the local oscillating signals. The signals are converted to currents, and then the currents are mixed together to form RF currents. Finally, the the RF currents are converted to output RF voltage signals via load current mirrors $M_7 \sim M_8$. M_9 provides the tail current for the Gilbert cell. $M_{10} \sim M_{12}$ and R_4 provide bias for $M_3 \sim M_6$. DP and DN are the baseband signals, which are sequences of "1" or "0", and LOP and LON are the differential local oscillating signals. With a baseband frequency of f_{BB} and a local frequency of f_{LO}, an output frequency $f_{RF} = f_{LO} \pm f_{BB}$ can be achieved.

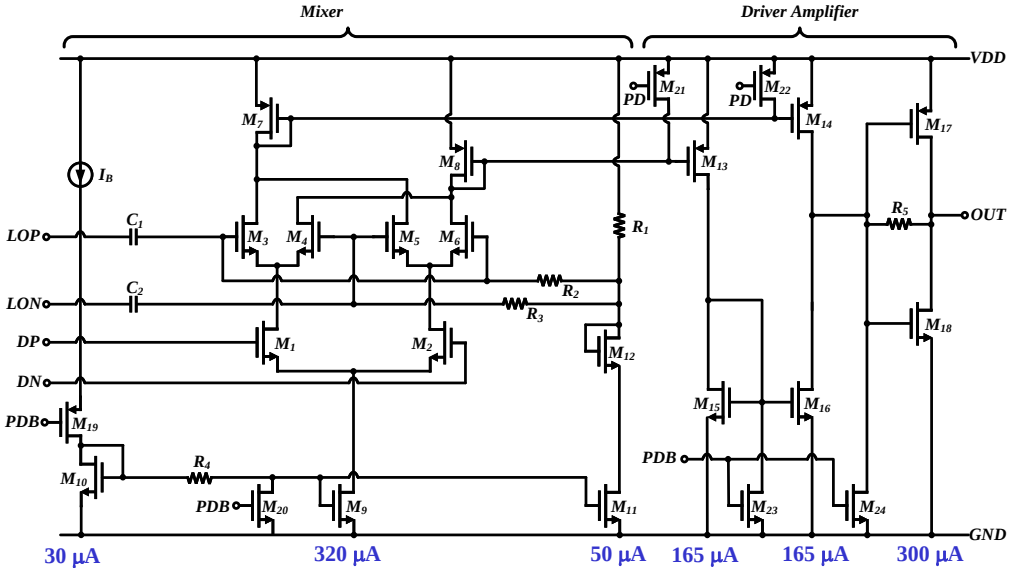

Figure 5. The schematic of the active mixer and driver.

The driver stage includes a differential to single-ended transformation circuit, which is composed of transistors M_{13}∼M_{16}, and a driving buffer consisting of M_{17}∼M_{18} and R_5. Meanwhile, several switching transistors, including M_{19}∼M_{24}, are used to reduce power consumption when the system is idle. PD and PDB are control signals which turn on or off the corresponding transistors. When $PD = 0$ and $PDB = 1$, the corresponding branches are turned off.

To meet the design specification, the conversion gain of the mixer and the voltage gain of the driver are set to about 15 dB and more than 10 dB, respectively. Their power consumption is set to less than 1.3 mW. Based on Equation (5), the conversion gain of the mixer is

$$CG_{Mixer} = \frac{2}{\pi} \frac{g_{m3}}{g_{m7}} \tag{13}$$

Therefore, $g_{m3} \approx 6 \cdot g_{m7}$. The bias current of each branch is allocated as Figure 5 shows, and the initial size of each transistor can be calculated by $I - V$ equations of the transistor. After adjusting the parameters to meet the PVT variation, the final component parameters are listed in Table 2.

Table 2. Component Values.

Component	Value	Component	Value
M_{1-2}	16 μm/0.06 μm	M_{3-6}	2 × (16 μm/0.06 μm)
M_{7-8}	4 × (32 μm/0.5 μm)	M_9	12 × (12 μm/1 μm)
M_{10}	12 μm/1 μm	M_{11}	2 × (12 μm/1 μm)
M_{12}	4 × (4 μm/0.1 μm)	M_{13-14}	20 μm/0.1 μm
M_{15-16}	4 × (32 μm/0.5 μm)	M_{17}	2 × (64 μm/0.06 μm)
M_{18}	2 × (16 μm/0.06 μm)	R_{1-2}	10 kΩ
R_3	10 kΩ	R_4	6 kΩ
R_5	10 kΩ	C_{1-2}	800 fF

3.2. Class-E PA Circuit Design

The schematic of the class-E PA is shown in Figure 6, in which four parallel cascode branches are used to control the output power level of the PA [20,21]. Common source transistors M_1∼M_4 with a thin oxide layer are driven by the signal from the driver stage and operate in switching mode. Common gate transistors M_5∼M_8 with a thick oxide layer are employed to improve reliability at high voltages. To control the level of output power, the common gate transistors are controlled by a four-bit power control word (PCW). $PAIN$

is the driving signal from the previous driver, and its waveform is similar to square wave, as shown in Figure 4. PDB is the switching signal for the PA. When $PDB = 1$, all the currents will be set to 0 and the PA will turn off. The design procedure of the PA includes two phases, which are circuit stage design and resonant and matching network design. Since the output power range is set to be from -6 dBm to 3 dBm, the currents of the four branches are set to 100 µA, 50 µA, 50 µA and 100 µA, respectively. The sizes of the transistors are listed in Table 3.

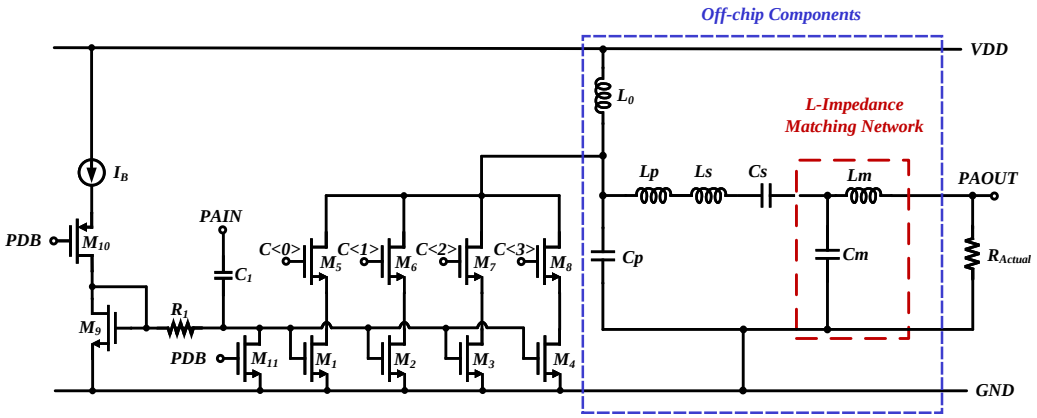

Figure 6. The gain-controlled PA circuit.

Table 3. Transistor sizes of the class-E PA.

Component	Value
M_{1-4}	2 × (20 µm/0.2 µm)
M_5	5 × (5 µm/0.3 µm)
M_6	2 × (2 µm/0.3 µm)
M_7	4 × (2 µm/0.3 µm)
M_8	9 × (2 µm/0.3 µm)
M_9	2 × (20 µm/0.2 µm)

As the PA operates in 433 MHz frequency, the resonant and matching network is realized by off-chip components. The output network includes an off-chip choke inductor L_0 to isolate AC and DC signals and a shunt capacitor C_p and a compensation inductor L_x to adjust the current and voltage waveform, as well as a resonant circuit including L_s and C_s to select the fundamental frequency signal.

To reduce power loss, a load network with a 500 nH finite DC-feed inductor is employed in the Class-E PA. Calculated parameters of the passive devices are shown in Table 4, where R_L is an ideal load of 250 Ω. To match the actual load of a 50 Ω antenna and achieve the maximum power transmission, an L-type impedance matching network, as shown in Figure 6, is employed, and Figure 7 illustrates the matching process using a Smith Chart. As Figure 7a shows, the load–pull simulation scans out the transmitted power for multiple impedance values of the actual load. Each circle represents an equal power level, where the star-shaped point ($P1$) is the impedance point of maximum power transmission. Relevant studies have proven that conjugate matching is a condition for maximum power transmission [22–25]. The matching procedure is shown in Figure 7b. First, a capacitor is paralleled in the circuit to lead the matching path following the black line ($Path1$). Second, an inductor is connected in series, and the matching path is the red line ($Path2$).

Finally, since the mixer and the driver work with a 1.2 V supply voltage and the class-E PA operates with a 1.8 V supply voltage, they are integrated into a single chip but are separated to two voltage domains by Deep Nwells [26,27].

Table 4. The calculated results of passive devices.

Component	Value
C_p	437 fF
R_L	250 Ω
L_p	74.8 nH

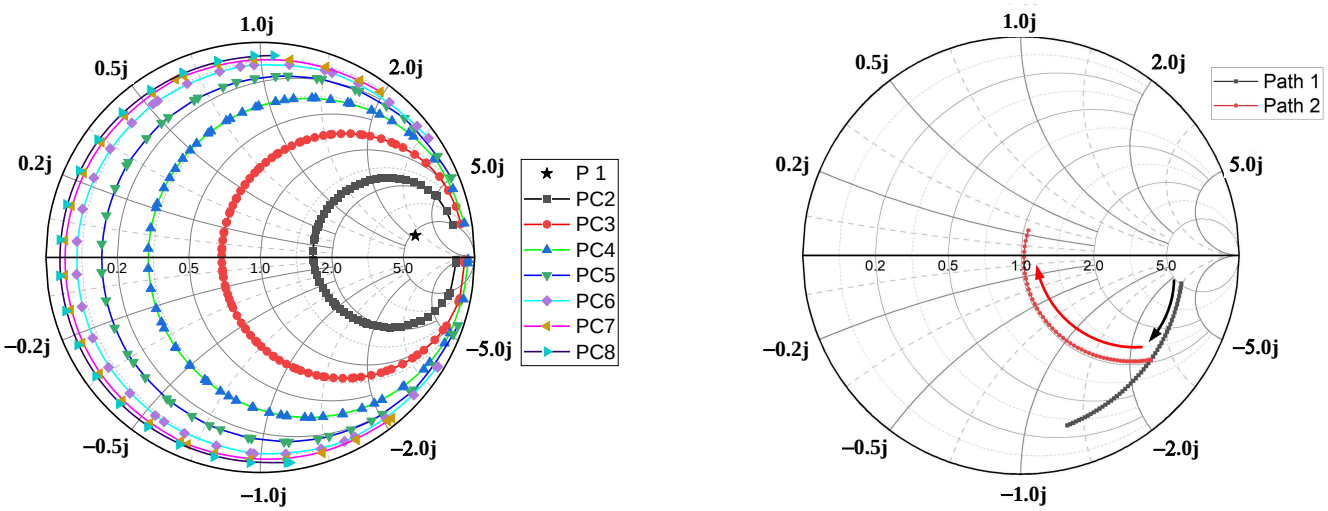

Figure 7. (**a**) The power circle chart of load-pull simulation. (**b**) The impedance matching process.

4. Experimental Results

The transmitter RF front-end is fabricated in a 55 nm CMOS LP process. The chip microphotograph and the corresponding layout are shown in Figure 8. The area of the chip is about 0.018 mm^2. To guarantee the function the proposed transmitter RF front-end, a postlayout simulation is performed. Figure 9 gives the conversion gain of the circuits. With a local oscillating signal whose power is −20 dBm, it can be seen from this figure that the mixer and the driver provide a conversion gain of about 28.5 dB, and the transmitter RF front-end has a total conversion gain of about 41.3 dB at the 433.92 MHz frequency. The output powers with different PCW are shown in Figure 10. The maximum output power is more than 3.2 dBm over a power range from −26 dBm to −15 dBm. Additionally, the postlayout simulated stability factors B_{1f} and K_f are shown in Figure 11. It can be seen from the figure that $B_{1f} > 0$ and $K_f > 1$ at 433 MHz frequency, which means that the PA is stable.

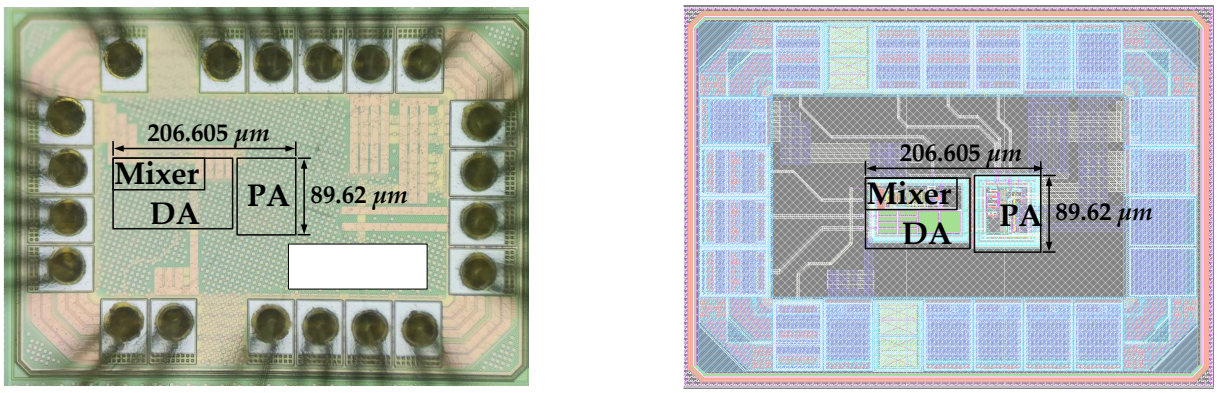

Figure 8. (**a**) The chip microphotograph. (**b**) The corresponding layout.

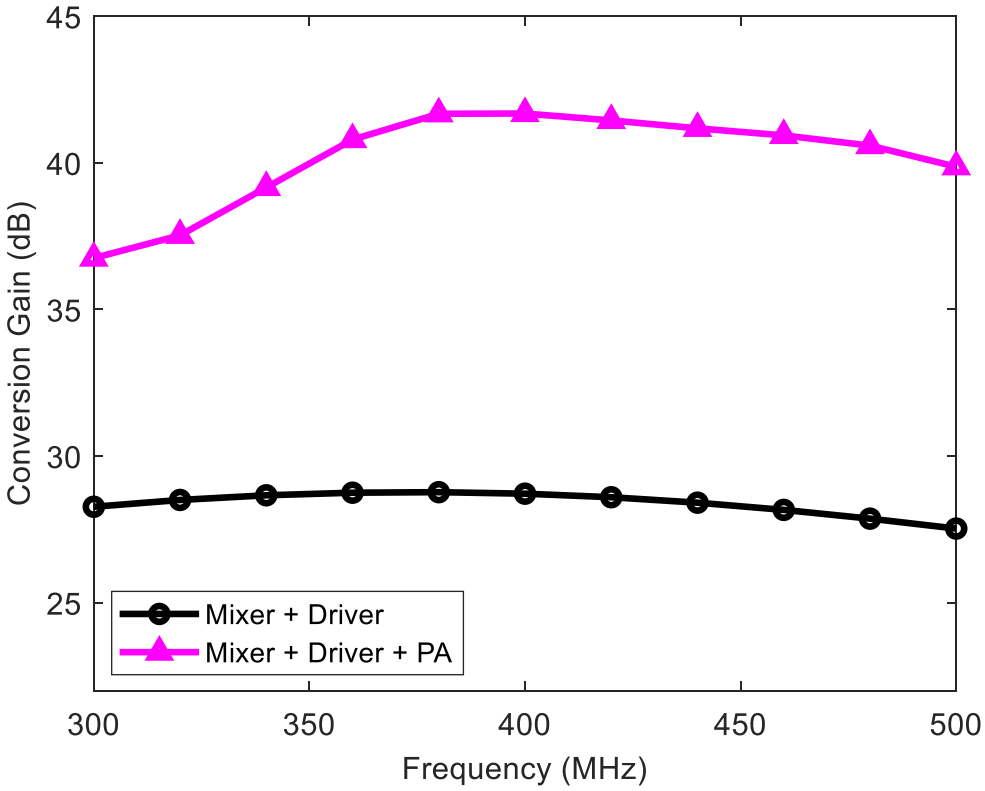

Figure 9. The postlayout simulated conversion gain.

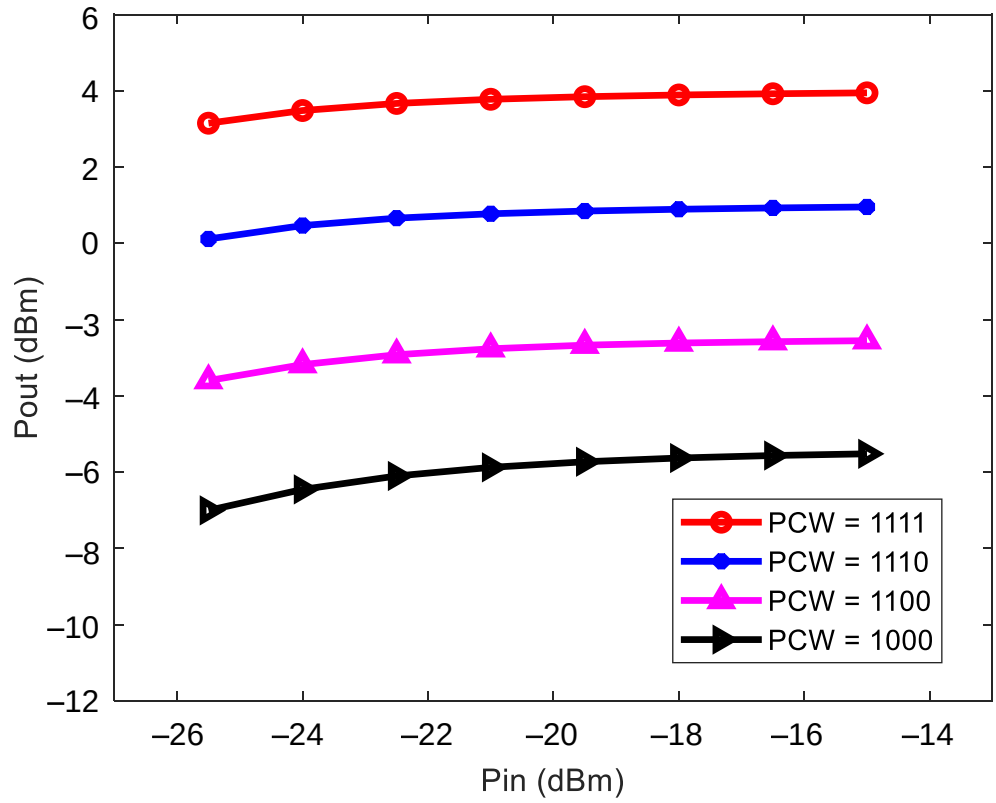

Figure 10. The postlayout simulated output powers of PA with different power control words.

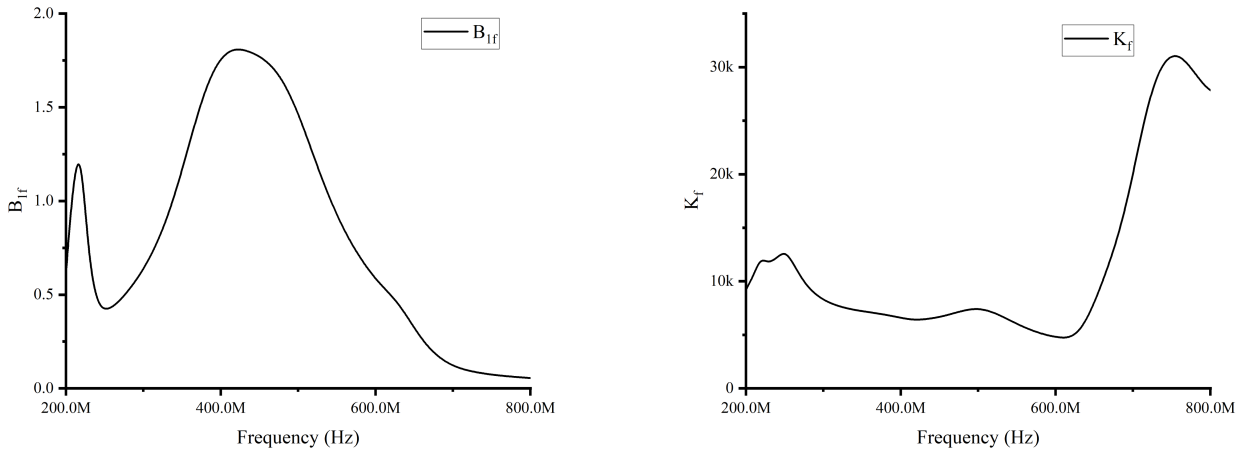

Figure 11. (**a**) The postlayout simulation result of B_{1f}. (**b**) The postlayout simulation result of K_f.

After tapeout and packaging, the chip is bonded to a PCB board and tested. With a 200 mVpp and 433.92 MHz frequency sinusoidal signal at the local oscillating signal port, as well as a 1.2 V DC signal at the baseband port, the output spectrum with maximum output power level is shown in Figure 12. It can be seen from the figure that the maximum output power is 2.7 dBm.

The performance DE reflects the efficiency of the PA, and it is defined as

$$DE = \frac{P_{out}}{P_{supply}} \tag{14}$$

Figure 13 plots the postlayout simulated and measured maximum output power and DE of the class-E PA over the frequency range of 400 MHz∼500 MHz. We can find that the postlayout simulated maximum output power and DE at 433.92 MHz frequency are 3.7 dBm and 40.1%, respectively, while the measured maximum output power and DE at 433.92 MHz frequency are 2.7 dBm and 34.5%, respectively.

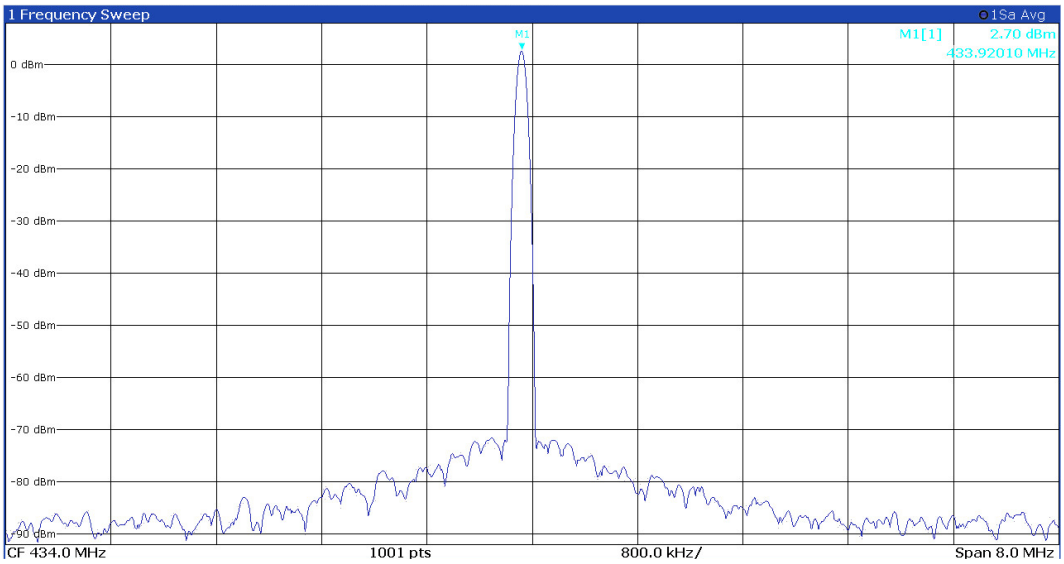

Figure 12. The measured output signal power spectrum.

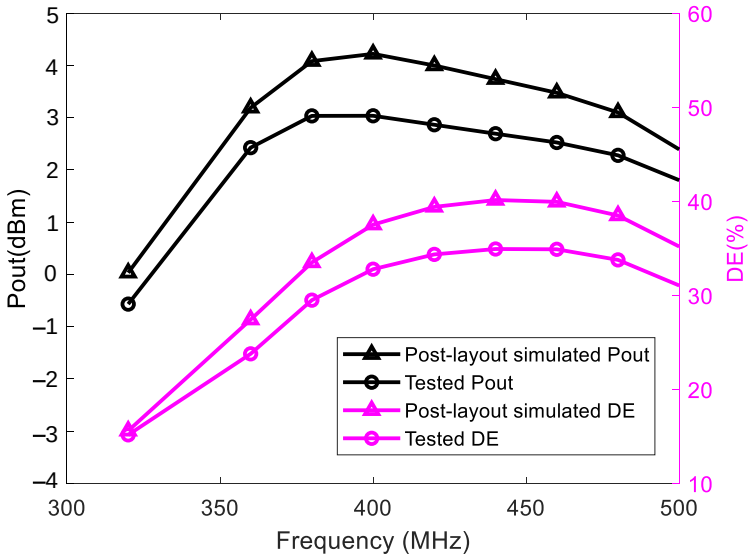

Figure 13. The postlayout simulated and measured output power and DE.

We also tested the S_{22} of the output port, and the measured result is shown in Figure 14. We can find that S_{22} is less than −10 dB in the 393.79 MHz∼455.70 MHz frequency range.

With a 192 kbps input signal, the output BPSK spectrum is shown in Figure 15. The bandwidth of the output signal is about 384 kHz. The measured EVM is shown in Figure 16. We can find that the measured EVM is about 0.83% rms, and the magnitude error and the phase error are 0.23% and 0.46°, respectively.

Furthermore, the measured power consumption of the whole chip is about 6.72 mW, among which the mixer and driver consume about 1.32 mW, and the class-E PA consumes about 5.4 mW.

We summarized the measurement results, and the performance comparison is shown in Table 5. It can be seen from the table that the proposed transmitter RF front-end can achieve a better EVM when compared with similar works.

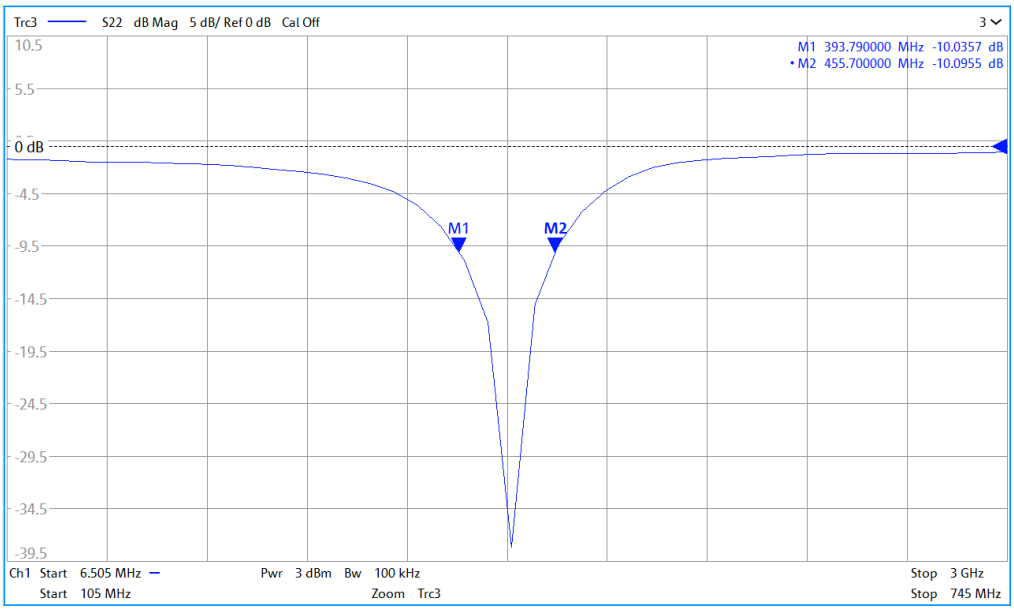

Figure 14. The measured S_{22} of the output port.

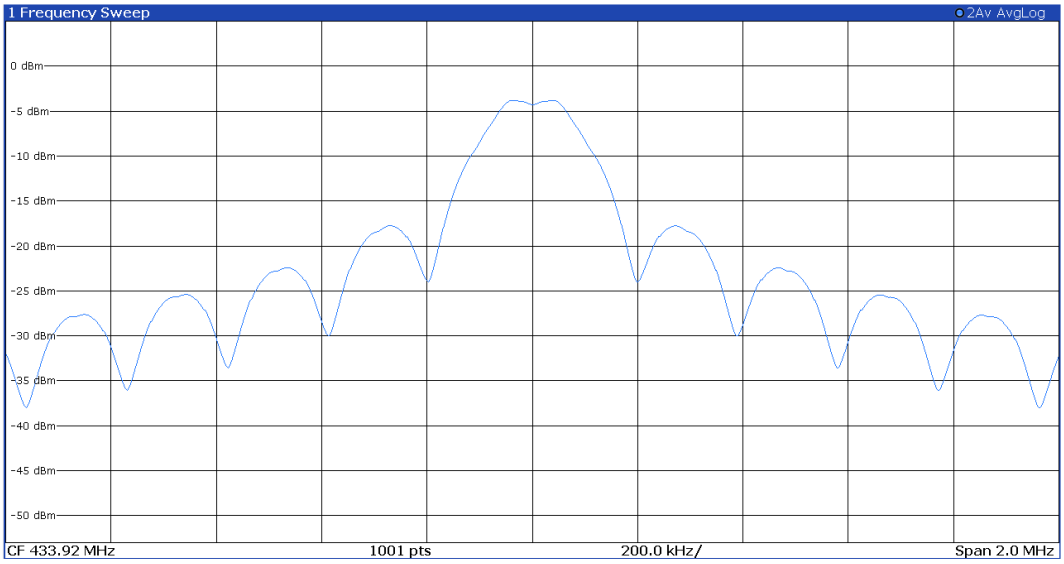

Figure 15. The measured power spectrum with 192 kbps BPSK modulation.

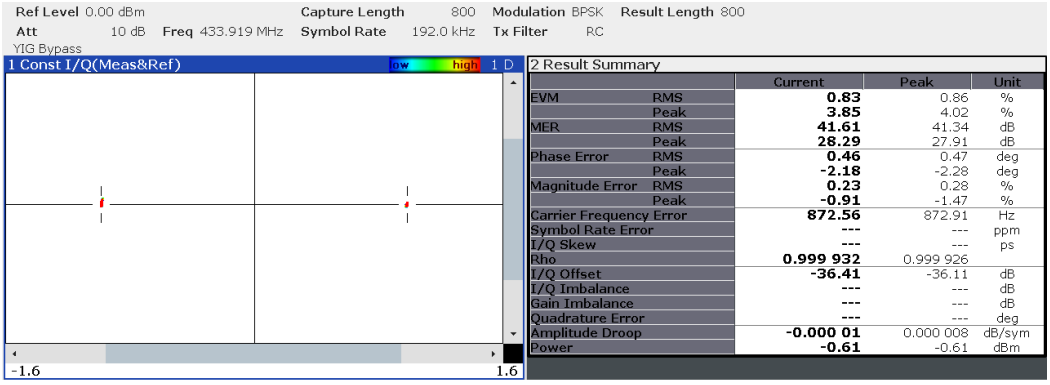

Figure 16. The measured 192 kbps BPSK modulation EVM.

Table 5. Performance summary and comparison.

Performance	[2]	[28] *	[29]	This Work
Year	2020	2019	2020	2023
Architecture	AMP + ADC + PLL + Mixer + PA	Ring Oscillator	SRAM + DAC + PLL + Mixer + Driver	Mixer + Driver + PA
Modulation Type	BPSK	FSK	64-QAM	BPSK
Technology (nm)	350	180	65	55
Operating Frequency (MHz)	433	433	1000	433
VDD (V)	1.8/2.5	1.8	N.A.	1.2/1.8
DE (%)	N.A.	N.A.	N.A.	34.5
Maximum Pout (dBm)	5.7	−28	9.5	2.7
Area (mm^2)	1.71	0.0018	0.5	0.018
Power (mW)	25.1 (PA 9.8)	0.58	45	6.72
Bandwidth (MHz)	0.384	N.A.	20	0.384
EVM (%)	17.06	N.A.	7.33	0.83

* Postlayout simulation.

5. Discussion

Since the main purpose of this work is to verify the feasibility of utilizing a low-power digital process for a potential mixed-signal design, only a few key analog/RF blocks were

integrated to form the backbone of the transmitter. Other blocks, such as a phase lock loop, amplifiers and an analog-to-digital converter, which are needed for a standalone transmitter with sensing function, are omitted in this version of the design. Meanwhile, each block of this work is a standard implementation of corresponding architecture without the latest performance improvement techniques. Additionally, to suppress the local oscillating feedthrough, various methods are proposed by integrating an upsample filter and designing calibration schemes [30–32]. All of the above points could be improved in future works.

6. Conclusions

This paper presented a 433 MHz transmitter TX front-end with a double-balanced active mixer and a class-E PA using a 55 nm CMOS LP process. A driver was designed to preamplify the RF signal before the PA. The chip occupies an area of 0.018 mm^2, and the total power consumption is about 6.72 mW. The measured results show that the performances of the transmitter TX front-end can meet the requirements of BPSK transmitters with moderate data rates.

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