electronics

MDPI

Article

A Compact Model of Carbon Nanotube Field-Effect Transistors for Various Sizes with Bipolar Characteristics

Wentao Huang [1,2] and Lan Chen [1,2,*]

[1] Institute of Microelectronics of the Chinese Academy of Sciences, Beijing 100029, China; huangwentao@ime.ac.cn
[2] University of Chinese Academy of Sciences, Beijing 101408, China
* Correspondence: chenlan@ime.ac.cn; Tel.: +86-139-1150-8171

Abstract: Carbon nanotubes have excellent electrical properties and can be used as a new generation of semiconductor materials. This paper presents a compact model for carbon nanotube field-effect transistors (CNTFETs). The model uses a semi-empirical approach to model the current–voltage properties of CNTFETs with gate lengths exceeding 100 nm. This study introduces an innovative approach by proposing physical parametric reference lengths (L_{ref}), which facilitate the integration of devices of varying sizes into a unified modeling framework. Furthermore, this paper develops models for the bipolar properties of carbon nanotube devices, employing two distinct sets of model parameters for enhanced accuracy. The model offers a comprehensive analysis of the different capacitances occurring between the electrodes within the device. The simulation of the model shows good agreement with the experimental measurements, confirming the model's validity. The model is implemented in the Verilog-A hardware description language, with the circuit being subsequently constructed and subjected to simulations via the HSPICE tool. The CNTFET-based inverter exhibits a gain of 7.022 and a delay time of 16.23 ps when operated at a voltage of 1.2 V.

Keywords: carbon nanotube transistor; compact model; virtual source model

Citation: Huang, W.; Chen, L. A Compact Model of Carbon Nanotube Field-Effect Transistors for Various Sizes with Bipolar Characteristics. *Electronics* **2024**, *13*, 1355. https://doi.org/10.3390/electronics13071355

Academic Editors: Ana-Maria Lepadatu, Andrei Avram, Florin Nastase and Martino Aldrigo

Received: 14 March 2024
Revised: 28 March 2024
Accepted: 1 April 2024
Published: 3 April 2024

1. Introduction

As Moore's Law progresses, typical planar MOS devices encounter parasitic effects such as the short-channel effect, DIBL effect, and tunneling effect when they reach a size of 22 nm. Consequently, the development of technologies like high-k metal gates, ultrathin bodies, and FinFETs enabled the continuation of Moore's Law. Simultaneously, there is a search for novel semiconductor materials that possess exceptional features in order to substitute them for silicon. Carbon nanotubes have several advantages, including exceptionally fast carrier mobility, high saturation speed, extended carrier mean free range, an ultrathin body structure, and a flawless lattice structure. Consequently, it is anticipated that it will be referred to as the fundamental substance for the upcoming era of energy-efficient microchips.

In 1991, Sumio Iijima made the initial discovery of carbon nanotubes, a novel type of semiconductor material [1]. During the following decade, researchers at the laboratory developed more advanced and reliable methods for manufacturing carbon nanotubes, which were then utilized in the production of field-effect transistors. Then, the production of integrated circuits utilizing CNTFETs was successfully achieved. The investigation of high-performance CNTFETs also utilized top-gate structures, gate-all-around structures, and other methodologies to enhance gate control and reduce the negative effects caused by parasitic phenomena that occur as the device is scaled down in size [2,3]. Currently, the preparation of CNTFETs with dimensions smaller than 10 nm is ongoing. These CNTFETs have a subthreshold swing of 70 mV/dec. Scandium (Sc) metal with a low figure of merit has been utilized as a material for the source and drain in the fabrication of N-type CNTFETs [4,5]. This choice of material has resulted in good ohmic contact. Additionally, arrays

of carbon nanotubes with a density of 200 CNTs/μm have been employed to effectively enhance the performance of individual devices [6]. Carbon nanotubes exhibit excellent thermal conductivity, particularly in their longitudinal direction, which aids in the efficient dissipation of heat in CNTFETs. CNTFETs are utilized in high-performance circuits, including 3D monolithic integrated systems and Risc-V, because of this characteristic [7–9].

The advancement of CNTFETs in devices and circuits has been significant. Accurate and efficient CNTFET device models are crucial, as they serve as a link between real devices and simulation analysis. Deji Akinwande from Stanford employs a tight-binding model to analyze the energy band structure of carbon nanotube devices. The energy band structure is utilized to determine the physical characteristics of chiral carbon nanotubes, including the density of states, effective mass, and density of non-simple carriers [10,11]. Additionally, the traditional drift-diffusion model is employed to simulate CNTFETs. Deng conducted an investigation into the issue of band-tunneling currents in small-sized CNTFET devices and developed the Stanford CNFET model based on this research [12,13]. Natori discovers that the current in the channel closest to the source, namely at the virtual source, has the greatest amount of potential energy [14]. Furthermore, the current in the channel can be described by the carrier current at the virtual source. Natori suggests the utilization of Landauer's formula, which serves as a framework for future modeling efforts on CNTFET devices. Fedawy introduces a ballistic transport model, which proposes that carriers experience little scattering within the channel of a small-sized CNTFET device [15]. The carriers produced from the source can traverse the channel and reach the drain without any obstruction. Mark Lundstrom conducts research on the interaction of carriers in carbon nanotube devices with acoustic and optical phonons and explains the resulting scattering effects using transmission coefficients [16,17]. Lang Zeng examines the Schottky barrier and constructs a model to analyze the carrier projection at the barrier [18]. However, the models that rely on the physical properties of carbon nanotube material do not accurately correspond to the measured data of real devices, mostly due to the immature fabrication process and variations in CNTFET devices.

In order to tackle the problem of the physically based model not being accurate enough, Khakifirooz presents a virtual source model (VS) based on experimental parameter extraction [19]. This semi-empirical model pulls a portion of the physical and empirical parameters in the model from experimental data on the basis of keeping a part of the physical design parameters of the device so that it can match the experimental measurement data well. The main formula of the VS model is succinct, thus it has the features of a quick modeling cycle and low model complexity and is ideal for large-scale circuit simulation work. Lee uses the VS model to examine and model CNTFETs and offers the VS-CNFET model [20,21]. Different characteristics relating to device fabrication are covered in the VS-CNFET model, which permits the study of CNTFET devices with different architectures. Based on this concept, CNTFETs can be employed in the simulation of various circuit designs.

Due to its reliance on the ballistic transport assumption, the VS model is not effective at accurately modeling CNTFETs with long gates. Hence, this study presents a virtual source expansion model (VSEX) that may be utilized for CNTFETs of different dimensions. The parameter L_{ref} in VSEX allows the model to switch to a drift-diffusion model when simulating devices of considerable scale. L_{ref} also accounts for the influence of the gate voltage on the threshold voltage in long channel CNTFETs.

CNTFETs also exhibit bipolar properties, leading to a degradation in the subthreshold coefficient and a decrease in the I_{on}/I_{off} ratio of the device [22]. The bipolar characteristic of the CNTFET results in a significant leakage current, leading to higher power consumption in the CNTFET's circuit. Hence, this article also includes the modeling of the bipolar properties of CNTFETs at a low gate bias using the VSEX model.

This article compares the VSEX model with experimental data of CNTFETs with gate lengths of 200 nm and 2 μm. The purpose is to confirm that the VSEX model is more accurate in larger CNTFETs and accurately reflects the bipolar properties of the transfer characteristic curve. Ultimately, a complete version of the CNTFET, which incorporates the

capacitance model, is constructed using Verilog-A. This model is then applied in circuit simulations to demonstrate the dynamic and static capabilities of the CNTFET, as well as the feasibility of the model.

2. Virtual Source Extend Model

2.1. Concept of L_{ref}

Figure 1 reveals that the energy band structure of the carbon nanotube exhibits a peak around the source electrode, referred to as the virtual source. This peak is also observed in the cross-section of the nanotube. The physical properties associated with the current in the VSEX correspond to the electrical parameters at the virtual source.

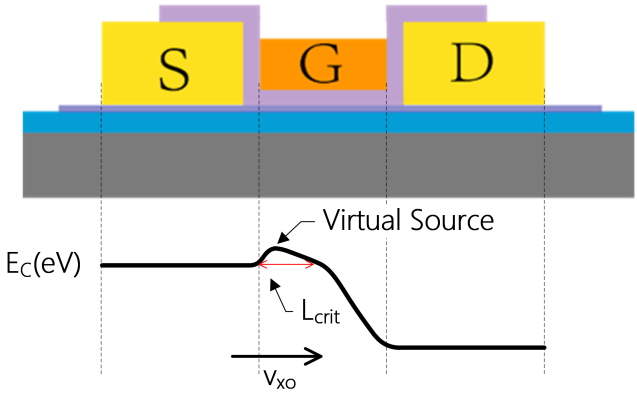


Figure 1. Schematic diagram of the energy band structure of a CNTFET.

In large-sized CNTFETs, the carriers in the channel experience significant scattering, resulting in the reduced saturation velocity of the carriers. The impact of device size on the current characteristics of the channel can be divided into two components. First, the length of the channel has a direct impact on the intensity of the scattering effect on the carriers. The VS model describes the electrical properties of a device in the short channel limit by considering it as an ideal ballistic transport device. In the VS model, carriers are emitted from the source and experience no scattering effects from the carbon nanotubes as they traverse the channel. In contrast, the carriers emitted from the source into the channel in the traditional drift-diffusion model experience continuous scattering within the channel. Eventually, due to the combined influence of the electric field and lattice scattering, the velocity of carriers stabilizes at a certain rate. This velocity can be described using the concept of carrier mobility. However, when the size of the device falls under a certain range, the carriers experience modest dispersion effects in the channel, which causes a decrease in their speed. Hence, in a CNTFET with a gate length over 100 nm, its current will display attributes in both the virtual source model and the drift-diffusion model.

Furthermore, when the gate length is progressively extended, the reason for the device reaching current saturation transitions from carrier velocity saturation to channel pinch-off. Carrier velocity saturation, as described in the ideal ballistic transport theory, leads to the saturation of the device current, regardless of the gate voltage. In the context of drift-diffusion theory, the rise in source-drain voltage leads to the contraction of the conducting channel on the drain side. Eventually, the channel pinch-off occurs when the condition $(V_{gs} - V_{th}) < V_{ds}$ is fulfilled, causing the current to reach saturation. Therefore, the length of the device also has an impact on how much the gate voltage influences the saturation voltage. In CNTFETs with short channels, the saturation voltage is unaffected by the gate voltage, whereas in devices with long channels, the two are closely associated.

The VESX model suggests that both effects can be characterized simultaneously by using L_{ref}, a parameter that is associated with the properties of the carbon nanotube material. Since L_{ref} is influenced by the scattering effect on the carriers, it can be inferred that there is a strong correlation between L_{ref} and the mean-free-path (MFP). Devices

with equal channel lengths but different carrier MFPs exhibit varying scattering effects on carriers. Devices with longer MFPs experience weaker scattering effects, resulting in current characteristics that closely resemble the short-channel approximation. Conversely, devices with shorter MFPs encounter more frequent scattering effects, leading to current characteristics that closely resemble the drift-diffusion model. The L_{ref} and carrier MFP of CNTFETs are directly influenced by characteristics such as the chirality, diameter, and integrity of the lattice structure of the channel carbon nanotube material.

The energy bands in the channel of the CNTFET change as the electrode bias is altered. This leads to a scattering effect in specific regions of the channel, which can be described in terms of the critical length (L_{crit}) [23]:

$$L_{crit} = \int_0^{L_G} \exp(-\frac{V(x) - V(0)}{kT})dx, \tag{1}$$

where L_G represents the gate length of the CNTFET device, $V(0)$ represents the potential at the virtual source, and $V(x)$ represents the potential at different positions along the channel's length.

$$\gamma = \frac{L_{crit}/L_{ref}}{\left[1 + \left(L_{crit}/L_{ref}\right)^{\beta_1}\right]^{1/\beta_1}}. \tag{2}$$

Equation (2) can establish a relationship between L_{crit} and L_{ref}, as well as the size of the device and the material parameters of the device. The value γ, referred to as the ballistic-drift parameter, quantifies the combined influence of ballistic transport and drift-diffusion transport in devices with gate lengths on the order of hundreds of nanometers.

2.2. Current Model

Equation (3) provides a straightforward expression for the channel current in a CNTFET.

$$I_D = v_{xo} \cdot Q_{xo} \cdot F_S. \tag{3}$$

The carrier saturation velocity, known as v_{xo}, refers to the upper limit of velocity that carriers can attain within a carbon nanotube channel. The carrier density at the virtual source, denoted as Q_{xo}, can be determined by the gate oxide capacitance C_{ox} between the gate electrode and the channel in a carbon nanotube field-effect transistor (CNTFET):

$$Q_{xo} = C_{ox} \cdot (1 + \gamma) \cdot n_{ss} \cdot \phi_t \cdot \ln(1 + \exp\frac{V_{gsi} - [V_t - \alpha \cdot \phi_t \cdot F_f]}{(1 + \gamma) \cdot n_{ss} \cdot \phi_t}), \tag{4}$$

where n_{ss} is the subthreshold coefficient of the CNTFET and V_t is the threshold voltage of the device, both of which can be extracted from the subthreshold region of the transfer characteristic curve. $\phi_t = kB/T$ is the electron thermal voltage, and α is an empirical parameter used to fine-tune the model.

The transition function from a high gate voltage to low gate voltage is denoted by F_f:

$$F_f = \frac{1}{1 + \exp(\frac{V_{gsi} - [V_t - \alpha \cdot \phi_t/2]}{\alpha \cdot \phi_t})}. \tag{5}$$

V_{gsi} and V_{dsi} represent the voltages of the internal electrodes of the CNTFET:

$$V_{dsi} = V_{ds} - 2I_D R_{S/D} \quad V_{gsi} = V_{gs} - I_D R_{S/D}. \tag{6}$$

The empirical function F_S in (3) characterizes the current non-saturation attributes of the VSEX model at low source-drain voltages.

$$F_S = \frac{V_{dsi}/V_{DSAT}}{\left[1+\left(\frac{V_{dsi}/V_{DSAT}}{\eta}\right)^{\beta}\right]^{1/\beta}}, \tag{7}$$

$$\eta = (\frac{V_{gs,eff}}{V_{DSAT}})^{\gamma}, \tag{8}$$

$$V_{gs,eff} = \frac{1}{2}\cdot(1+\gamma)\cdot n_{ss}\cdot\phi_t\cdot\ln(1+\exp\frac{V_{gsi}-[V_t-\alpha\cdot\phi_t\cdot F_f]}{(1+\gamma)\cdot n_{ss}\cdot\phi_t}). \tag{9}$$

β is another empirical parameter in the VSEX model used to adjust the shape of the saturation function. V_{DSAT} is the voltage at which carriers reach velocity saturation under ideal ballistic transport assumptions:

$$V_{DSAT} = V_{DSATs}(1-F_f)+\phi_t F_f, \tag{10}$$

$$V_{DSATs} = \frac{v_{x0}L_G}{\mu}. \tag{11}$$

With the above equations, the VSEX model incorporates CNTFETs of various sizes into a unified framework, and the VSEX model can accurately model the device from the subthreshold region to the turn-on region.

2.3. Bipolar Characteristic Modeling

The bipolar properties of CNTFETs are evident in the low gate voltage region of the transfer characteristic curve. In this region, the current decrease of CNTFETs in the subthreshold region decelerates and eventually begins to gradually increase. The carbon nanotube material, which is of the semiconductor type, possesses a symmetrical energy band structure. By employing metals with varying work functions as electrodes, it is possible to create CNTFETs with distinct features by manipulating the energy band structure. When applying a sufficiently high positive voltage to the gate of P-type CNTFETs, the energy bands bend downward, causing the P-type CNTFETs to exhibit the properties of N-type CNTFETs.

Hence, when representing this bipolar attribute, the current can be observed in the low gate voltage region as being influenced by the combination of both the P-type CNTFET and the N-type CNTFET. Therefore, the overall channel current can be represented as

$$I_D = I_{DS,P} + I_{DS,N}. \tag{12}$$

Two sets of VSEX model parameters can be used for $I_{DS,P}$ and $I_{DS,N}$, respectively. These two sets of model parameters can be extracted from regions that satisfy the P-type CNTFET and N-type CNTFET on-state conditions, respectively. The parameters associated with the size of the device, such as L_G and L_{ref}, remain unchanged, while the parameters associated with the material of the device, such as μ, v_{xo}, and n_{ss}, are extracted individually. This not only decreases the quantity of the parameter extraction but also guarantees the consistency of the model parameters.

In the on-state region of a P-type CNTFET, the $I_{DS,P}$ section operates in the conventional on-state region, while the $I_{DS,N}$ component operates in the deep subthreshold region of an N-type CNTFET. This N-type region supplies very little current to the CNTFET, resulting in the typical operating characteristics of a P-type CNTFET being exhibited by the I_D. This modeling technique is both intuitive and rational, and it retains the advantage of the simplicity of the VSEX model.

2.4. Capacitance Model

Furthermore, the SPICE model must incorporate the device's capacitance in addition to the current model. The structure of the CNTFET is illustrated in Figure 2. It is important to mention that there is an additional layer called the stop layer which is constructed of high-k material and is located below the gate oxide layer. This layer is used to improve the control of the etching process.

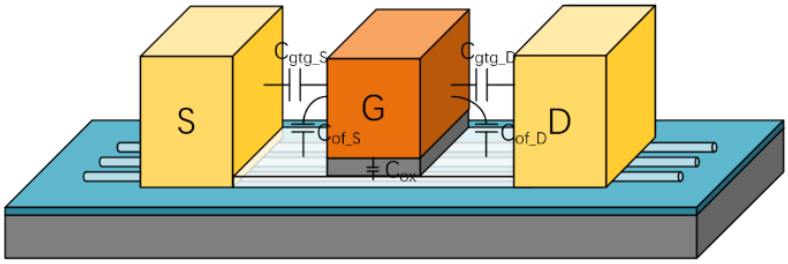
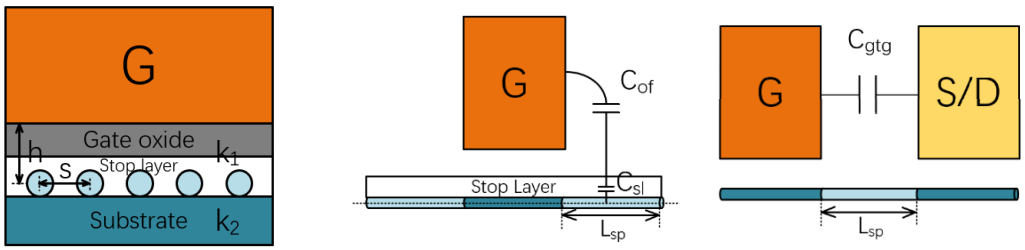


Figure 2. Capacitance in CNTFETs.

Figure 3 illustrates the capacitance of the gate electrode, which may be categorized into three components: C_{ox} between gate and channel, C_{of} between gate and the expansion region, and C_{gtg} between gate and the adjacent source or drain electrodes [24].



(**a**) (**b**) (**c**)

Figure 3. Capacitance structure schematic. (**a**) Oxide capacitance. (**b**) Expansion region capacitance. (**c**) Capacitance between gate and adjacent electrodes.

As shown in Figure 3a, the capacitance of a single carbon nanotube in the gate and channel can be expressed after taking into account the effect of the mirror charge generated by the substrate:

$$C_{gc\_\inf} = \frac{2\pi k_1 \varepsilon_0}{\cosh^{-1}(\frac{2h}{d}) + \lambda_1 \cdot \ln(\frac{2h+2d}{3d})}, \tag{13}$$

$$h = t_{ox} + t_{sl} + r, \quad \lambda_1 = \frac{k_1 - k_2}{k_1 + k_2}, \tag{14}$$

where t_{ox} and t_{sl} are the thickness of the gate oxide layer and stop layer, respectively. r and d are the radius and diameter of the carbon nanotube, respectively. k_1 represents the relative permittivity of high-k materials, specifically gate oxide and stop layer. On the other hand, k_2 represents the relative permittivity of the substrate.

The analysis additionally considers the shielding effect between the aligned rows of carbon nanotubes, incorporating an equivalent capacitance value:

$$C_{gc\_sr} = \frac{4\pi k_1 \varepsilon_0}{\ln(\frac{s^2+2(h-r)\cdot[h+\sqrt{h^2-r^2}]}{s^2+2(h-r)\cdot[h-\sqrt{h^2-r^2}]}) + \lambda_1 \cdot \ln(\frac{(h+d)^2+s^2}{9r^2+s^2}) \cdot \tanh(\frac{h+r}{s-d})}, \tag{15}$$

where s is the spacing between carbon nanotubes. Depending on whether the carbon nanotubes are located at the edge or in the middle of the array, their capacitance is

$$C_{gc\_e} = \frac{C_{gc\_\inf} \cdot C_{gc\_sr}}{C_{gc\_\inf} + C_{gc\_sr}}, \tag{16}$$

$$C_{gc\_m} = 2C_{gc\_e} - C_{gc\_\inf}. \tag{17}$$

In a CNTFET with carbon nanotube number N, the C_{ox} of the entire carbon nanotube array is

$$C_{gc\_total} = 2C_{gc\_e} + (N-2)C_{gc\_m}. \tag{18}$$

As shown in Figure 3b, the capacitance C_{of_total} between the gate and the expansion region can be regarded as the C_{of} of gate oxide to the upper surface of stop layer in series with the C_{sl} of the stop layer:

$$C_{of\_total} = C_{of}C_{sl}/(C_{of} + C_{sl}). \tag{19}$$

The capacitance between the gate and a single carbon nanotube in the expansion region is

$$C_{of\_\inf} = \frac{\pi k_2 \varepsilon_0 L_{sd}}{\cosh^{-1}(\frac{2H_{eff}}{d})}. \tag{20}$$

$$H_{eff} = \sqrt{{t_{ox}}^2 + (0.28L_{sp})^2} \tag{21}$$

H_{eff} is the equivalent distance between the sidewall of the gate and carbon nanotube. The equivalent capacitance resulting from the shielding effect, taking into account the interaction between adjacent carbon tubes, is calculated in a manner similar to gate oxide capacitance:

$$C_{of\_sr} = \frac{\pi k_2 \varepsilon_0 L_{sd}}{\ln(\frac{\sqrt{(2H_{eff})^2+s^2}}{s})}, \tag{22}$$

$$C_{of\_e} = \frac{(\frac{1}{\eta_1}C_{of\_\inf}) \cdot C_{of\_sr}}{(\frac{1}{\eta_1}C_{of\_\inf}) + C_{of\_sr}}, \tag{23}$$

$$C_{of\_m} = \frac{2\alpha}{\eta_1} \cdot C_{of\_e} + (1 - \frac{2\alpha}{\eta_1}) \cdot C_{of\_\inf}, \tag{24}$$

where α and η_1 are empirical parameters:

$$\eta_1 = \exp(\frac{\sqrt{N^2-2N}+N-2}{2.5N}), \quad \alpha = \exp(\frac{N-3}{2N}). \tag{25}$$

The capacitance of the carbon nanotubes at the edge or in the middle can be calculated using the same method as (18):

$$C_{of} = 2C_{of\_e} + (N-2)C_{of\_m}. \tag{26}$$

C_{sl} can be thought of as the capacitance of a parallel capacitor plate:

$$C_{sl} = \frac{k_1 \varepsilon_0 L_{sp} W}{t_{sl}}. \tag{27}$$

In Figure 3c, C_{gtg} of the gate electrode and adjacent electrodes is partitioned into two components, with the two adjacent surfaces being treated as parallel capacitors:

$$C_{gtg\_nr} = \frac{k_2 \varepsilon_0 H_{gate}}{L_{sd}}. \tag{28}$$

The remaining three non-adjacent surfaces can be represented as two cylindrical capacitors with the following radius:

$$R_{eff} = \frac{2L_G + \tau_{bk} H_{gate}}{2\pi} \quad \tau_{bk} = \exp(2 - 2\sqrt{1 + \frac{2(H_{gate} + L_G)}{L_{sp}}}). \tag{29}$$

Assuming that the heights of the source/drain electrodes and the gate electrode are equivalent,

$$C_{gtg} = \frac{k_2 \varepsilon_0 H_{gate}}{L_{sp}} + 0.7 \frac{\pi k_2 \varepsilon_0}{\ln(\frac{L_{sp} + L_G}{R_{eff}})}. \tag{30}$$

As shown in Figure 4, a CNTFET can be represented as a circuit consisting of a current source, resistors, and capacitors.

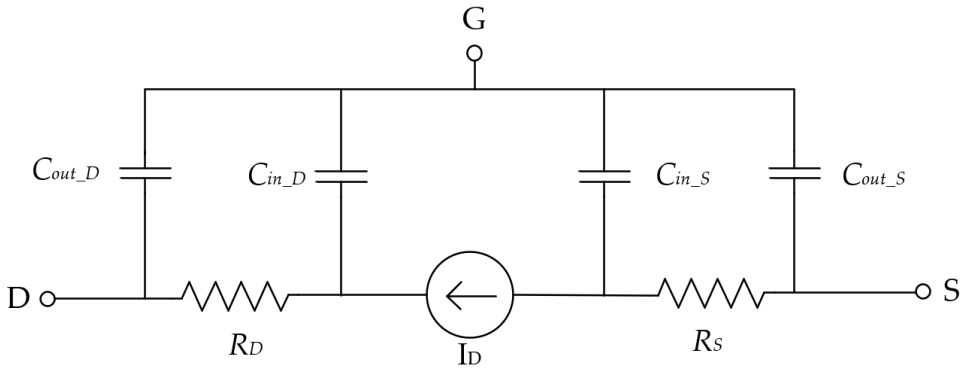


Figure 4. Equivalent circuit of the VSEX model.

$$C_{in} = \frac{1}{2} L_G C_{gc\_total}, \tag{31}$$

$$C_{out} = C_{of\_total} + W \cdot C_{gtg}. \tag{32}$$

C_{out} and C_{in} are the capacitances from the gate to the outer and inner electrodes, respectively.

3. Results

This section compares the present model with experimental data in order to validate the benefits of the VSEX model for large-sized CNTFETs. Furthermore, it has been demonstrated that using bipolar characteristic modeling results in enhanced model accuracy. Ultimately, circuit simulations are conducted using CNTFETs with $L_G = 150$ nm to showcase the practicality of the model in circuit simulation.

3.1. Validation of VSEX Model

Peking University researchers wrap CNTs with conjugated polymers and obtain high-purity semiconductor-type carbon nanotubes via dispersion and gradient density centrifugation methods. Then, they deposit CNTs onto silicon wafers and obtain an aligned CNT via the method of withdrawing silicon wafers [6]. The SEM image of the device, which has a gate length of 200 nm, is depicted in Figure 5. This research extracts the VSEX model parameters from experimental data and simulates the current output characteristics of the CNTFET using the MATLAB tool. Figure 6a demonstrates that the saturation current in the p-type CNTFET with $L_G = 200$ nm exhibits a linear correlation with the gate voltage [6,25]. This behavior is indicative of ballistic transport devices. Both the VSEX model and the VS model exhibit a strong correlation with the experimental results, confirming that the VSEX model can accurately represent the behavior of the VS model in short-channel CNTFETs.

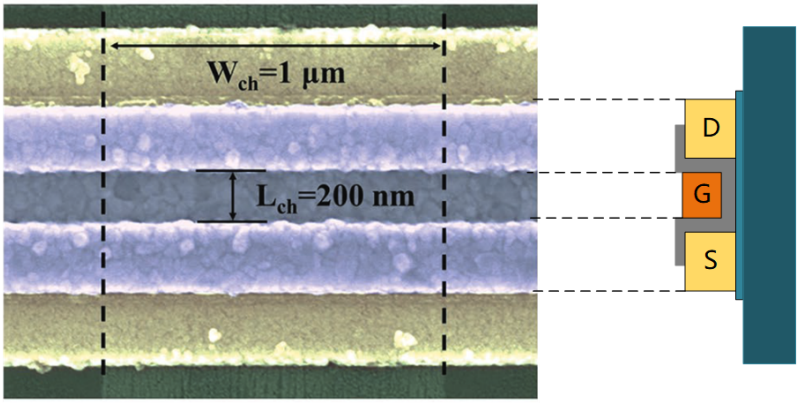
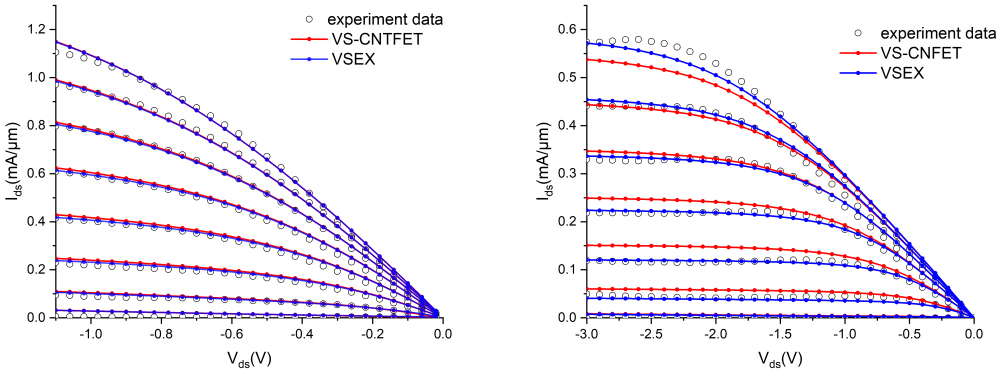


Figure 5. SEM image of the top-view structure of a CNTFET with $L_G = 200$ nm [6].



(**a**) (**b**)

Figure 6. P-type CNTFET output characteristic. (**a**) $L_G = 200$ nm; (**b**) $L_G = 2$ µm.

The saturation current of the CNTFET with $L_G = 2000$ nm, as shown in Figure 6b, follows a power relationship, indicating that it is not a device that displays ballistic transport. The VSEX model accurately represents this characteristic in comparison with the VS model. To provide a clearer understanding of the enhanced impact of the VSEX model, this research additionally employs (33) to analyze the error computation of CNTFET data with varying dimensions. Based on the data in Table 1, it is evident that the accuracy of both models is similar for small-size devices. However, the VSEX model demonstrates an advantage when the size of the CNTFET increases. The VSEX model possesses the capability to accurately represent a broader spectrum of CNTFET sizes.

$$\mathrm{RMS} = \sqrt{\sum_{i=1}^{n} \frac{\sum_{j=1}^{m} \left(\frac{I_{test}(V_{gs}(i),V_{ds}(j)) - I_{sim}(V_{gs}(i),V_{ds}(j))}{I_{test,\max}(i)} \right)^2}{n \times m}} \tag{33}$$

Table 1. The root mean squared error of model.

L_G (nm)	70	150	200	930	200
VSEX	6.94%	4.32%	3.26%	3.04%	5.65%
VS-CNFET	6.87%	3.68%	4.55%	8.78%	13.41%

This research also includes simulations of the present transfer characteristics. Based on the information shown in Figure 7, it is evident that the VSEX model effectively represents the turn-on region of the CNTFET. Bipolar characteristics are observed in CNTFETs [26]. The P-type characteristic leads to a drop in $I_{ds,P}$ as V_{ds} increases, whereas the N-type

characteristic results in an increase in $I_{ds,N}$ as V_{ds} increases. When subjected to a negative V_{ds}, the CNTFET exhibits the dominance of the P-type characteristic, resulting in a decrease in the current. Conversely, when V_{ds} approaches zero, the two characteristics become comparable, leading to a slower rate of current decrease. Conversely, when V_{ds} is positive, the N-type characteristic becomes dominant, causing a gradual increase in the current. Therefore, the transfer characteristic curve of the CNTFET with bipolar characteristics exhibits a V-shaped trend. The utilization of bipolar description theory can enhance the precision of the VSEX model in the deep subthreshold region of the CNTFET.

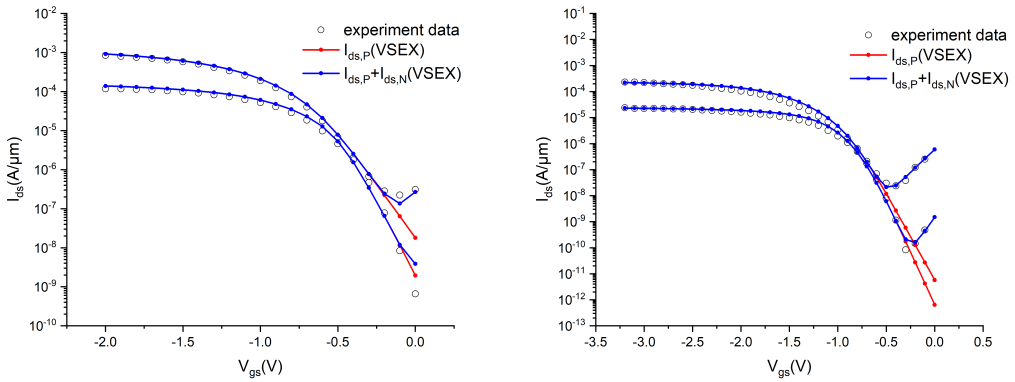


Figure 7. P-type CNTFET transfer characteristic. (**a**) $L_G = 200$ nm; (**b**) $L_G = 2$ µm.

3.2. Circuit Implementation

In the design of CNTFET-based circuits, it is assumed that both P-type and N-type CNTFETs have symmetrical properties. This simplifies the process of extracting parameters and accurately represents the performance of CNTFETs.

Figure 8a illustrates the construction of an inverter utilizing a symmetric CNTFET with a gate length of 150 nm. The parameters in the circuit simulation are decided by the results of parameter extraction and the construction of the device, as indicated in Table 2. The simulation allows for the obtaining of the inverter output waveform and gain by adjusting the operating voltage. As shown in Figure 8b, the gain can reach a maximum value of 7.022 when $V_{dd} = 1.2$ V.

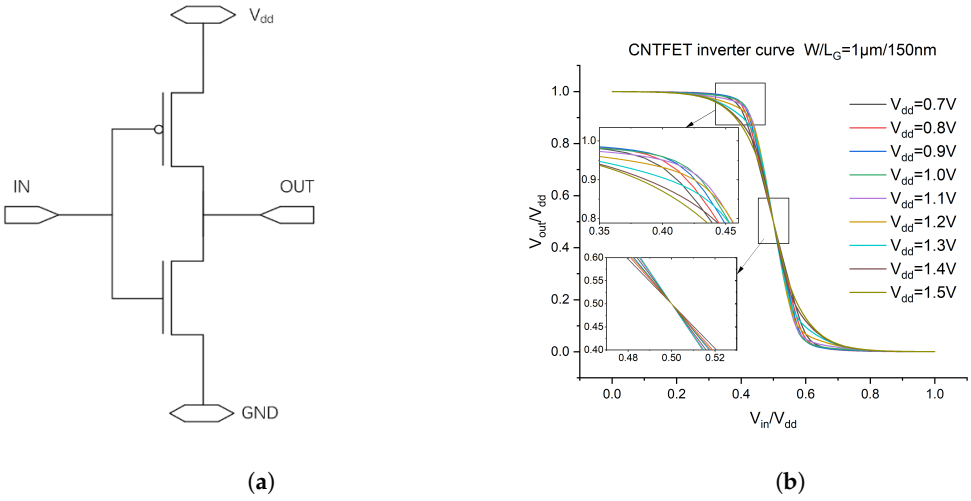
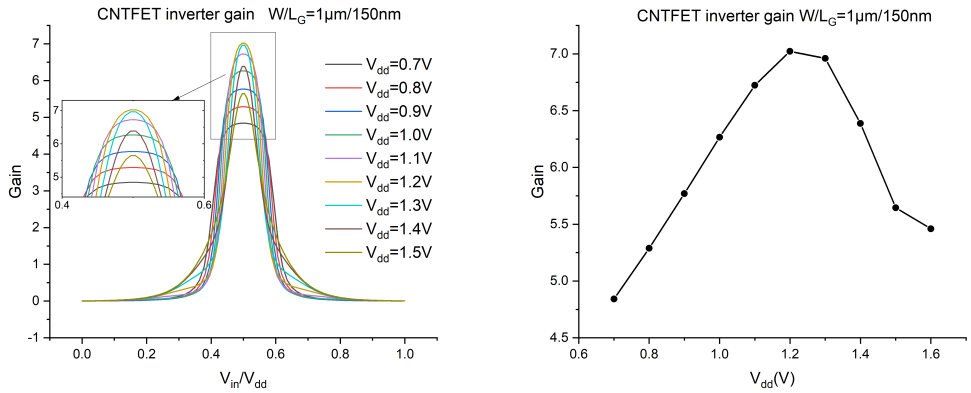


Figure 8. *Cont.*



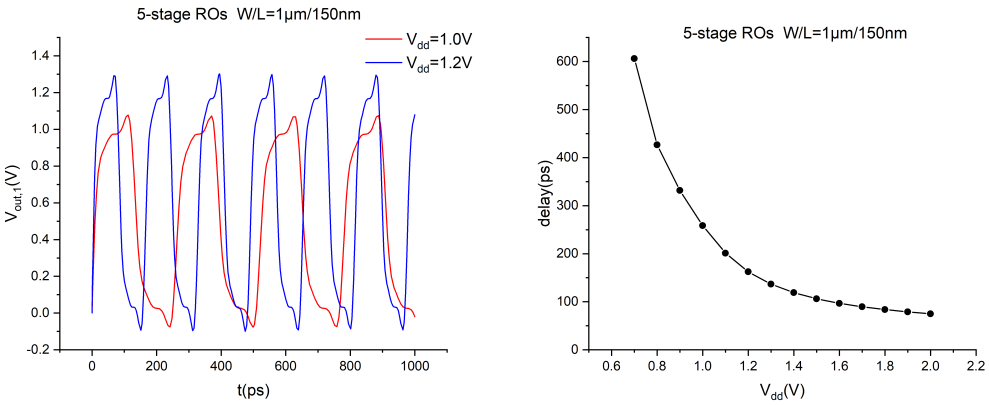
(**c**) (**d**)

Figure 8. Inverter based on CNTFETs with $L_G = 150$ nm. (**a**) The structure of inverter; (**b**) inverter output curves; (**c**) gain of inverter; (**d**) gain versus V_{dd}.

Table 2. Parameters used in the circuit simulation of CNTFETs with $L_G = 150$ nm.

L_G (nm)	W (nm)	L_{ref} (nm)	L_{sp} (nm)	t_{ox} (nm)	t_{sl} (nm)
150	1000	250	60	4.8	3
s (nm)	**d (nm)**	**H_{gate} (nm)**	**k_1**	**k_2**	
5	1.5	15	13	3.9	

As shown in Figure 9, a five-stage ring oscillator is constructed using a device with a gate length of 150 nm. According to Figure 9b, the frequency of the ring oscillator is 6.16 GHz when $V_{dd} = 1.2$ V. The simulation results closely align with the experimental test results in reference [6], suggesting that the model accurately represents the dynamic characteristics of the CNTFET.



(**a**) (**b**)

Figure 9. 5-stage ring oscillator based on CNTFETs with $L_G = 150$ nm. (**a**) Output curves; (**b**) ro5 delay versus V_{dd}.

4. Conclusions

This work proposes a compact model based on the virtual source concept to appropriately characterize CNTFETs. The model primarily examines the impact of scattering on the current behavior in large-scale CNTFETs and visually illustrates this effect using Lref. This research additionally examines the impact of bipolar effects on the current features

and represents the bipolar characteristics using an intuitive approach derived from the VSEX model. Ultimately, the paper presents a comprehensive model that can be utilized for circuit design through the examination of the parasitic capacitance within the device. This paper utilizes the test results of the CNTFET to extract the VSEX model parameters and conduct an error analysis. The circuit is constructed to verify the feasibility and validity of the model in integrated circuit simulation.

Author Contributions: Conceptualization, W.H.; methodology, W.H.; software, W.H.; validation, W.H.; formal analysis, W.H.; investigation, W.H.; resources, L.C.; data curation, W.H.; writing—original draft preparation, W.H.; writing—review and editing, W.H. and L.C.; visualization, W.H.; supervision, L.C.; project administration, L.C.; funding acquisition, L.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Key R & D Program of China under Grant 2022YFB4400400.

Data Availability Statement: All the data are reported/cited in the paper.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Iijima, S. Helical microtubules of graphitic carbon. *Nature* **1991**, *354*, 56–58. [CrossRef]
2. Wind, S.J.; Appenzeller, J.; Avouris, P. Lateral Scaling in Carbon-Nanotube Field-Effect Transistors. *Phys. Rev. Lett.* **2003**, *91*, 58301. [CrossRef] [PubMed]
3. Chen, Z.; Farmer, D.; Xu, S.; Gordon, R.; Avouris, P.; Appenzeller, J. Externally Assembled Gate-All-Around Carbon Nanotube Field-Effect Transistor. *IEEE Electron. Device Lett.* **2008**, *29*, 183–185. [CrossRef]
4. Zhang, Z.; Liang, X.; Wang, S.; Yao, K.; Hu, Y.; Zhu, Y.; Chen, Q.; Zhou, W.; Li, Y.; Yao, Y.; et al. Doping-Free Fabrication of Carbon Nanotube Based Ballistic CMOS Devices and Circuits. *Nano Lett.* **2007**, *7*, 3603–3607. [CrossRef]
5. Qiu, C.; Zhang, Z.; Xiao, M.; Yang, Y.; Zhong, D.; Peng, L.M. Scaling carbon nanotube complementary transistors to 5-nm gate lengths. *Science* **2017**, *355*, 271–276. [CrossRef] [PubMed]
6. Lin, Y.; Liang, S.; Xu, L.; Liu, L.; Hu, Q.; Fan, C.; Liu, Y.; Han, J.; Zhang, Z.; Peng, L.M. Enhancement-Mode Field-Effect Transistors and High-Speed Integrated Circuits Based on Aligned Carbon Nanotube Films. *Adv. Funct. Mater.* **2022**, *32*, 2104539. [CrossRef]
7. Shulaker, M.M.; Wu, T.F.; Pal, A.; Zhao, L.; Nishi, Y.; Saraswat, K.; Wong, H.S.P.; Mitra, S. Monolithic 3D integration of logic and memory: Carbon nanotube FETs, resistive RAM, and silicon FETs. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014. [CrossRef]
8. Shulaker, M.M.; Hills, G.; Park, R.S.; Howe, R.T.; Saraswat, K.; Wong, H.S.P.; Mitra, S.; Shulaker, M.M.; Hills, G.; Park, R.S.; et al. Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. *Nature* **2017**, *547*, 74–78. [CrossRef] [PubMed]
9. Bishop, M.D.; Hills, G.; Srimani, T.; Lau, C.; Murphy, D.; Fuller, S.; Humes, J.; Ratkovich, A.; Nelson, M.; Shulaker, M.M.; et al. Fabrication of carbon nanotube field-effect transistors in commercial silicon manufacturing facilities. *Nat. Electron.* **2020**, *3*, 492–501. [CrossRef]
10. Akinwande, D.; Nishi, Y.; Wong, H.S.P. An Analytical Derivation of the Density of States, Effective Mass, and Carrier Density for Achiral Carbon Nanotubes. *IEEE Trans. Electron. Devices* **2007**, *55*, 289–297. [CrossRef]
11. Akinwande, D.; Liang, J.; Wong, H.S.P. Analytical Degenerate Carrier Density and Quantum Capacitance for Semiconducting Carbon Nanotubes. In Proceedings of the 2008 Device Research Conference, Santa Barbara, CA, USA, 23–25 June 2008. [CrossRef]
12. Deng, J.; Wong, H.S.P. A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region. *IEEE Trans. Electron. Devices* **2007**, *54*, 3186–3194. [CrossRef]
13. Deng, J.; Wong, H.S.P. A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking. *IEEE Trans. Electron. Devices* **2007**, *54*, 3195–3205. [CrossRef]
14. Natori, K.; Kimura, Y.; Shimizu, T. Characteristics of a carbon nanotube field-effect transistor analyzed as a ballistic nanowire field-effect transistor. *J. Appl. Phys.* **2005**, *97*, 34306. [CrossRef]
15. Fedawy, M.; Fikry, W.; Alhenawy, A.; Hassan, H. I-V characteristics model for ballistic Single Wall Carbon Nanotube Field Effect Transistors (SW-CNTFET). In Proceedings of the 2012 IEEE International Conference on Electronics Design, Systems and Applications (ICEDSA), Kuala Lumpur, Malaysia, 5–6 November 2012. [CrossRef]
16. Rahman, A.; Guo, J.; Datta, S.; Lundstrom, M. Theory of ballistic nanotransistors. *IEEE Trans. Electron Devices* **2003**, *50*, 1853–1864. [CrossRef]
17. Lundstrom, M. Elementary scattering theory of the Si MOSFET. *IEEE Electron. Device Lett.* **1997**, *18*, 361–363. [CrossRef]

18. Zeng, L.; Liu, X.Y.; Du, G.; Kang, J.F.; Han, R.Q. On the effect of scattering in Schottky Barrier MOSFETs. In Proceedings of the IEEE International Conference on Electron Devices and Solid-State Circuits, Hong Kong, China, 8–10 December 2008; pp. 1–4. [CrossRef]
19. Khakifirooz, A.; Nayfeh, O.M.; Antoniadis, D. A Simple Semiempirical Short-Channel MOSFET Current–Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters. *IEEE Trans. Electron Devices* **2009**, *56*, 1674–1680. [CrossRef]
20. Lee, C.S.; Pop, E.; Franklin, A.D.; Haensch, W.; Wong, H.S.P. A Compact Virtual-Source Model for Carbon Nanotube FETs in the Sub-10-nm Regime—Part I: Intrinsic Elements. *IEEE Trans. Electron Devices* **2015**, *62*, 3061–3069. [CrossRef]
21. Lee, C.S.; Pop, E.; Franklin, A.D.; Haensch, W.; Wong, H.S.P. A Compact Virtual-Source Model for Carbon Nanotube FETs in the Sub-10-nm Regime—Part II: Extrinsic Elements, Performance Assessment, and Design Optimization. *IEEE Trans. Electron Devices* **2015**, *62*, 3070–3078. [CrossRef]
22. Xia, T.; Register, L.; Banerjee, S. Transmission through the band-gap states in Schottky-barrier carbon nanotube transistors. *IEEE Trans. Nanotechnol.* **2006**, *5*, 80–83. [CrossRef]
23. Rakheja, S.; Lundstrom, M.; Antoniadis, D. A physics-based compact model for FETs from diffusive to ballistic carrier transport regimes. In Proceedings of the IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014. [CrossRef]
24. Deng, J.; Wong, H.S.P. Modeling and Analysis of Planar-Gate Electrostatic Capacitance of 1-D FET With Multiple Cylindrical Conducting Channels. *IEEE Trans. Electron Devices* **2007**, *54*, 2377–2385. [CrossRef]
25. Lin, Y.; Cao, Y.; Ding, S.; Zhang, P.; Xu, L.; Liu, C.; Hu, Q.; Jin, C.; Peng, L.M.; Zhang, Z.; et al. Scaling aligned carbon nanotube transistors to a sub-10 nm node. *Nat. Electron.* **2023**, *6*, 506–515. [CrossRef]
26. Zeng, Q.; Wang, S.; Yang, L.; Wang, Z.; Pei, T.; Zhang, Z.; Peng, L.M.; Zhou, W.; Liu, J.; Zhou, W.; et al. Carbon nanotube arrays based high-performance infrared photodetector [Invited]. *Opt. Mater. Express* **2012**, *2*, 839. [CrossRef]