

## Article

# Horn Antenna on Chip Operating at 180 GHz Using the SiGe CMOS Process

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**Abstract:** This article proposes a chip antenna on millimeter-Waves. This antenna combined with TSMC 180 nm SiGe CMOS technology has the advantage of being small in size and is suitable for wireless communications. The multilayer architecture Horn antenna implemented on M4–M6 can meet both process reliability specifications and radiation performance. The results of the simulation show that the maximum gain is  $-4.2$  dBi. The return loss measurement results are almost consistent with the simulation results, and the bandwidth range is 177.4–183 GHz. This article first describes the antenna production process and measurement results, analyses the impact of the parameters on the antenna, and further compares it with other designs. The excellence of this article is that it proposes a design that solves the problem of large millimeter wave loss and successfully reduces the area. At the same time, this article can contribute to readers' future optimization and continued research directions, and at the same time contribute simulation and measurement trends to let readers understand the stability of CMOS chip antenna simulation and measurement.

**Keywords:** millimeter-Wave; antenna on chip; CMOS process



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## 1. Introduction

In the 5G era, the operating frequency is in the millimeter wave band. Because waves are generally short, antennas are mainly targeted at applications such as short-distance communications, 5G communications, wireless communications [1–3] and imaging radar [2,4,5]. Antennas are widely used in various communication systems, closely integrating people and things throughout the world, forming an interconnected world [4,6]. However, the structure of such a widely used antenna is not too complicated, which has led many people to invest in this research and develop various antennas [7]. Among them, antennas designed on wafers are popular because they are smaller in size, less susceptible to noise interference, and have excellent efficiency [8].

CMOS (Complementary Metal-Oxide-Semiconductor) technology plays a key role in chip antenna applications in modern communications [1,9] and radar systems [4,5,10]. One of its main advantages is its high degree of integration. The CMOS process allows the integration of multiple antenna elements and signal processing functions on a small chip. This highly integrated design not only saves space but also reduces the cost of the system [11].

In addition, CMOS chip antennas have excellent power consumption performance and do not require additional manufacturing processes to integrate the antenna [12], making them suitable for use in portable and low-power devices. These advantages make CMOS a promising choice in wireless communications, radar, and other antenna applications [11].

In the millimeter-Wave frequency band where atmospheric propagation and resistive losses are large [13,14], high-gain antenna types can be used to solve this phenomenon [5,7]. Horn antennas in wireless communication systems and radar systems [1,4] are widely used because of their large gain [5,13,15] and high efficiency [16]. Horn antennas are characterized by their simple structure [13], easy control [5,17], high efficiency, stable

radiation direction [15,18], moderate bandwidth [13,15,17–19], and powerful power processing capabilities [13], is widely used in the energy supply of tracking satellite, systems of phased array, devices of microwave heating, and as general standard components for calibrating and measuring high-gain antennas [17]. It is usually made up of metal and dielectric materials and performs consistently in various environments without requiring regular maintenance [5]. In general, the horn antenna is known for its wide-band performance [15,17], excellent directivity [15], simple structure [17] and wide application fields. It is used in radar [5], communications [17,20]. It plays an important role in many fields such as remote sensing and scientific research, providing reliable antenna solutions for many key applications.

In this article, the SiGe CMOS process is used and the Horn antenna is designed on the wafer. Through the horn antenna and the theory of electromagnetism and electromagnetic waves, the horn antenna is designed on CMOS M4–M6. At the same time, this experiment is expected to operate this chip horn antenna in a frequency band with a central frequency close to 180 GHz. In the feed part, the GSG feed method is used. This feed method not only increases signal integrity and improves high-frequency performance, but is also more convenient in connection. The composition of this article introduces the results and conclusions of the antenna design, simulation, and measurement in order. All simulation results are generated using electromagnetic simulation software.

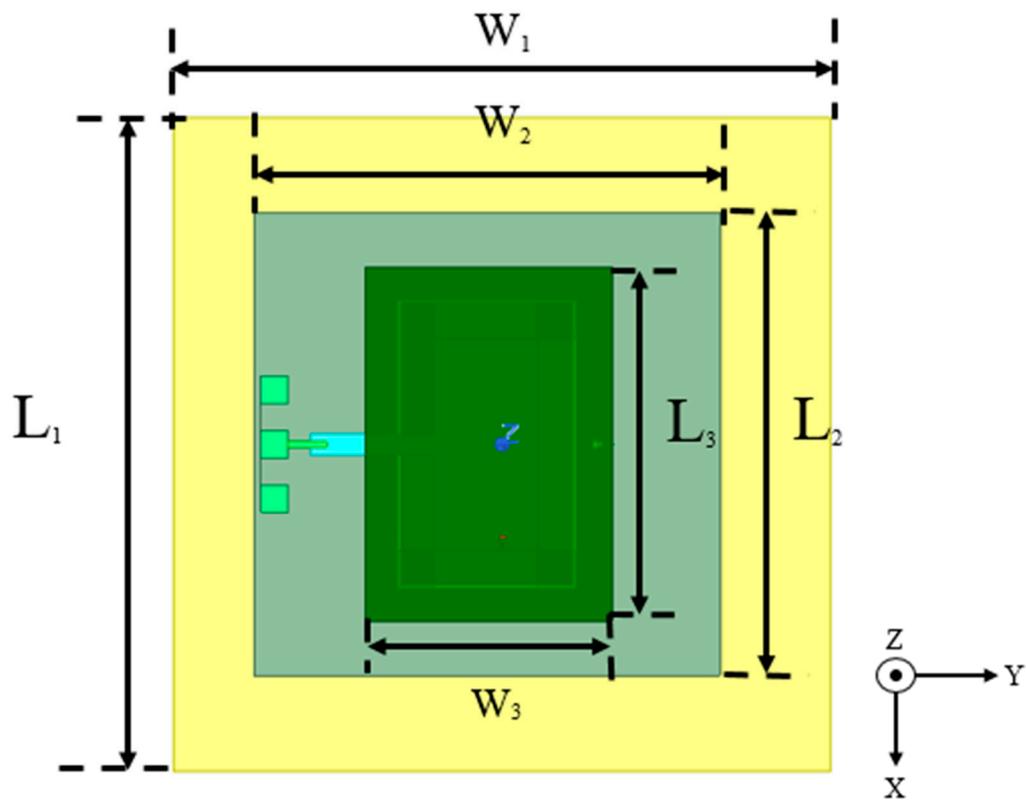
## 2. Antenna Design

### 2.1. Configuration

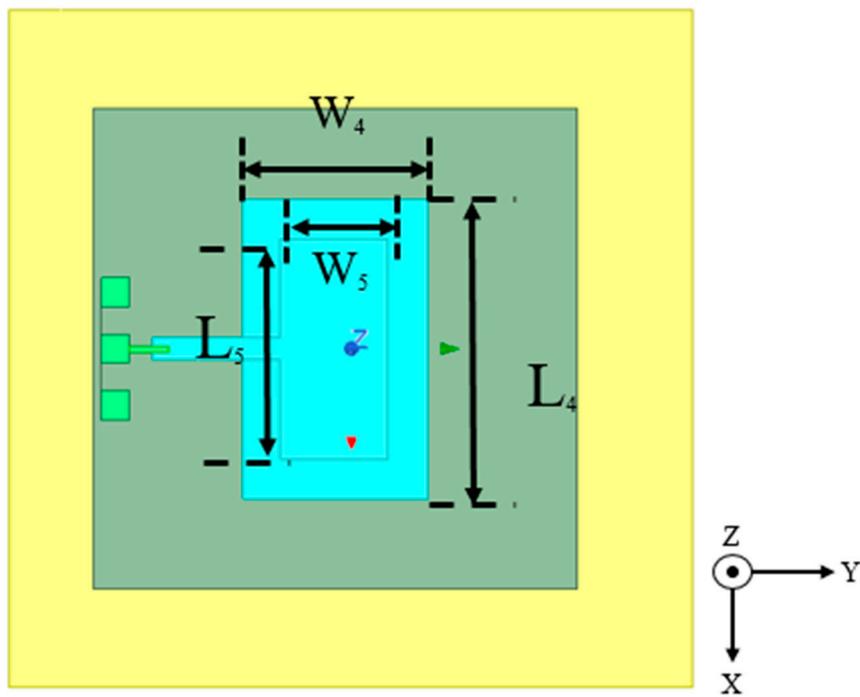
All antenna designs and GSG feeds are within this range in Figure 1a. The overall CMOS size is  $1200\ \mu\text{m} \times 1200\ \mu\text{m} \times 533.4\ \mu\text{m}$ , and the ground area is  $850\ \mu\text{m} \times 850\ \mu\text{m}$ . The upper layer and the transmission line that feeds into the antenna body are made of M6 material. Its dielectric coefficient  $\epsilon_r = 1$ , loss tangent = 0, and the conductivity (bulk conductivity) is 21,939,477.13 siemens/m. After parameter analysis, the width of the feed transmission line is  $10\ \mu\text{m}$ , which is optimal. The size of the upper cuboid is  $650\ \mu\text{m} \times 450\ \mu\text{m} \times 3.5\ \mu\text{m}$  in Figure 1a, while the size of the cuboid on the lower layer is  $530\ \mu\text{m} \times 325\ \mu\text{m} \times 2.91\ \mu\text{m}$  in Figure 1b, the material is M1 to M5, its dielectric coefficient  $\epsilon_r = 1$ , Loss tangent = 0, the conductivity (Bulk conductivity) is 24,189,646.83 siemens/m, and the middle aperture size is  $390\ \mu\text{m} \times 190\ \mu\text{m}$  in Figure 1b. Height is  $533.4\ \mu\text{m}$  in Figure 1c. All the parameters described above are presented in Table 1. All simulation results are obtained by electromagnetic simulation software, and the boundary conditions of the simulation process are all symmetrical. The chip horn antenna proposed comprises components M4–M6, as illustrated in Figure 1d.

**Table 1.** Detail Parameter (Unit:  $\mu\text{m}$ ).

Length	Value	Width/Height	Value
$L_1$	1200	$W_1$	1200
$L_2$	850	$W_2$	850
$L_3$	650	$W_3$	450
$L_4$	530	$W_4$	325
$L_5$	350	$W_5$	190
$L_6$	10	$h_1$	533.4

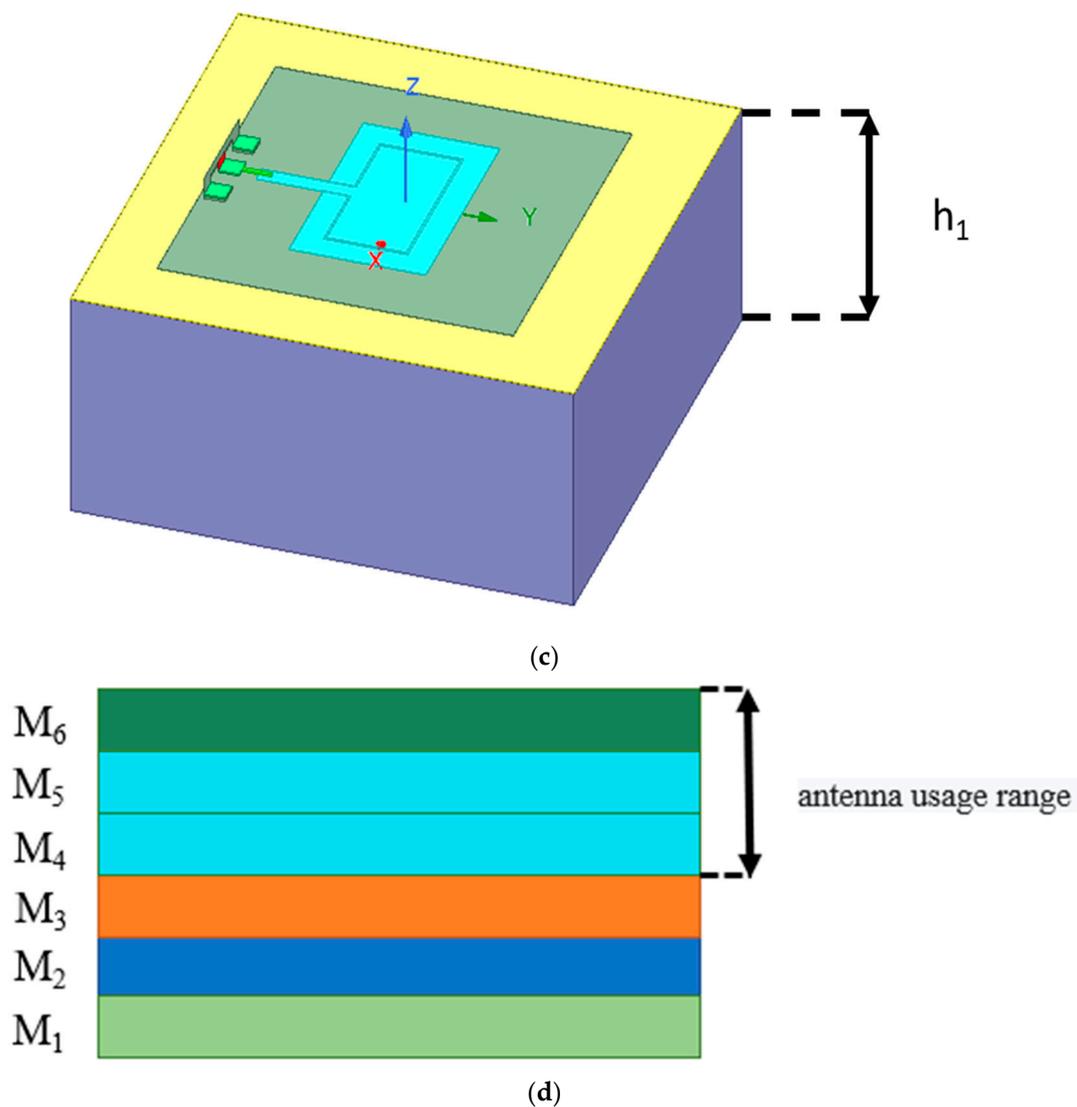


(a)



(b)

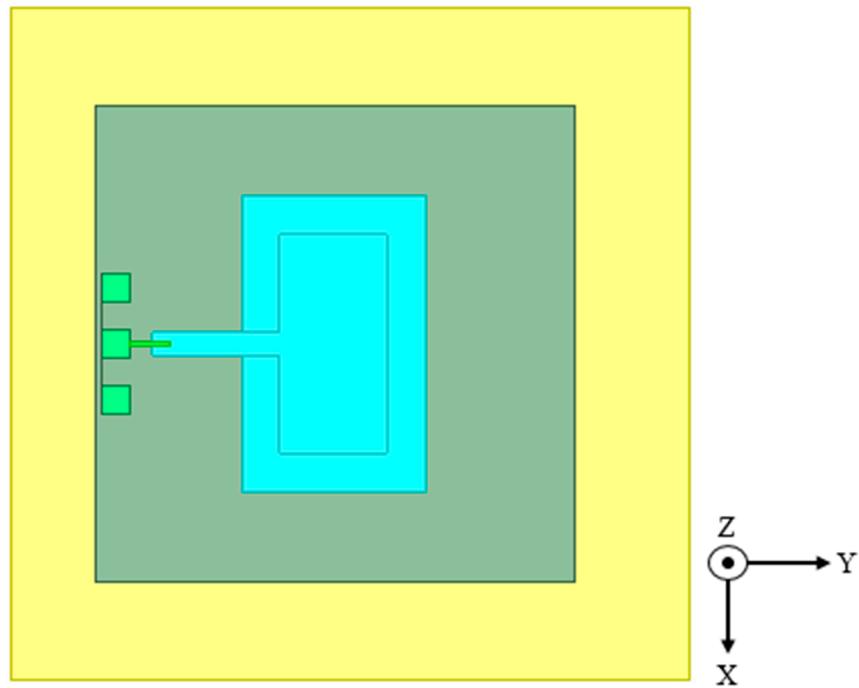
Figure 1. Cont.



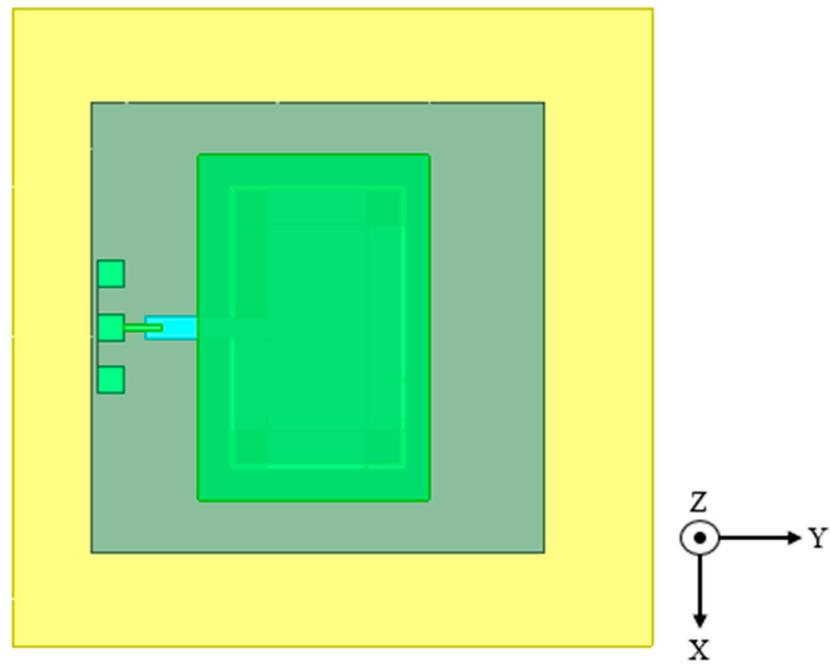
**Figure 1.** (a) Horn antenna (top view); (b) top view (without top layer); (c) height of the chip antenna height  $h_1$ ; (d) Antenna usage range.

## 2.2. Evolution of the Antenna

Type1: First, the rectangular horn antenna is designed in the fifth to sixth layers and the feed is connected from the sixth layer to the fifth layer so it can be connected to the GSG feed in Figure 2a. Type2: Add another layer to  $M_6$  in Figure 2b. It can be clearly seen that the return loss has dropped below  $-10$  dB, and the bandwidth is 5.05 GHz (183.03–188.08 GHz) in Figure 3. Type3: Enlarge the top layer to make its bandwidth wider, as shown in Figure 2c. The bandwidth is 7.67 GHz (177.16–184.83 GHz), in Figure 3.



(a)



(b)

Figure 2. Cont.

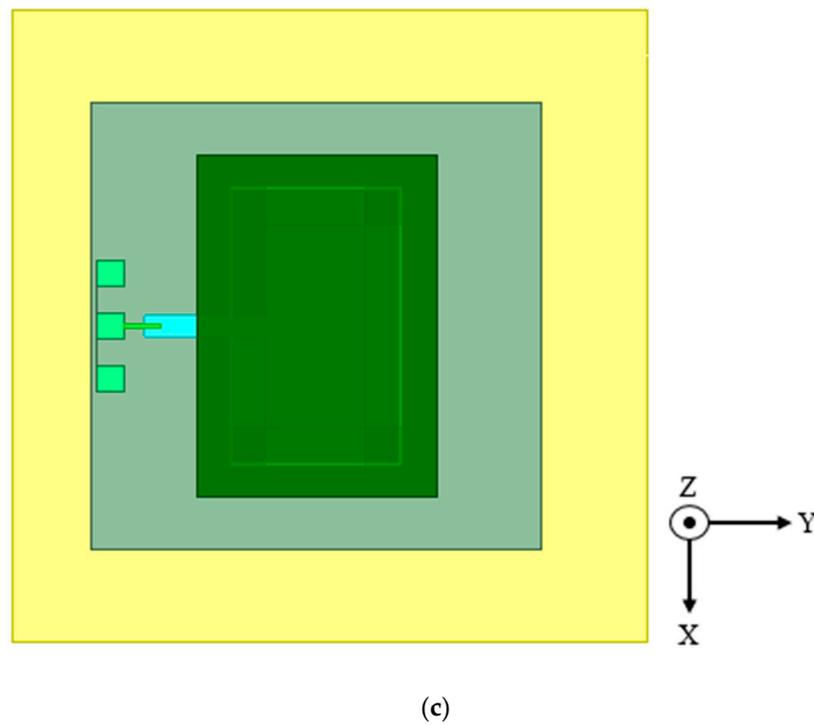


Figure 2. Evolution of Antenna Design. (a) Type1; (b) Type2; (c) Type3.

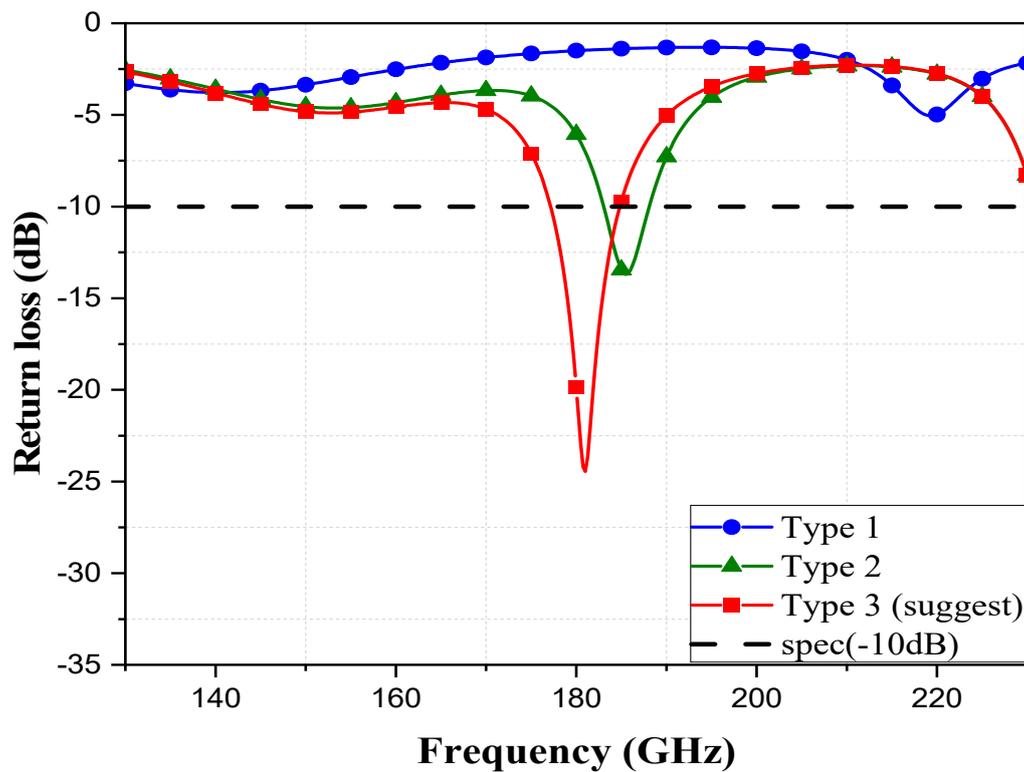
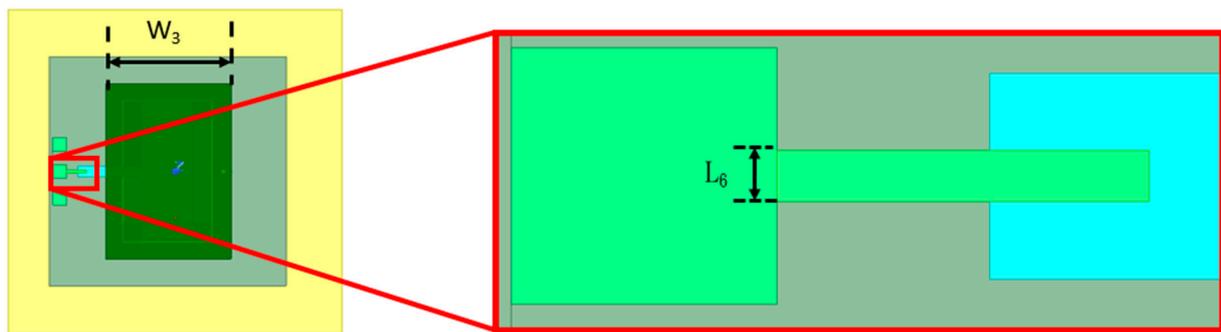


Figure 3. Comparison of three types of reflection coefficient.

### 2.3. Parameter Analysis

After the architecture is completed, some parameters are adjusted. This article will conduct parameter analysis on the feed width  $L_6$  and the top layer width  $W_3$ , as shown in Figure 4. First, the feed width  $L_6$  is analyzed for parameters.



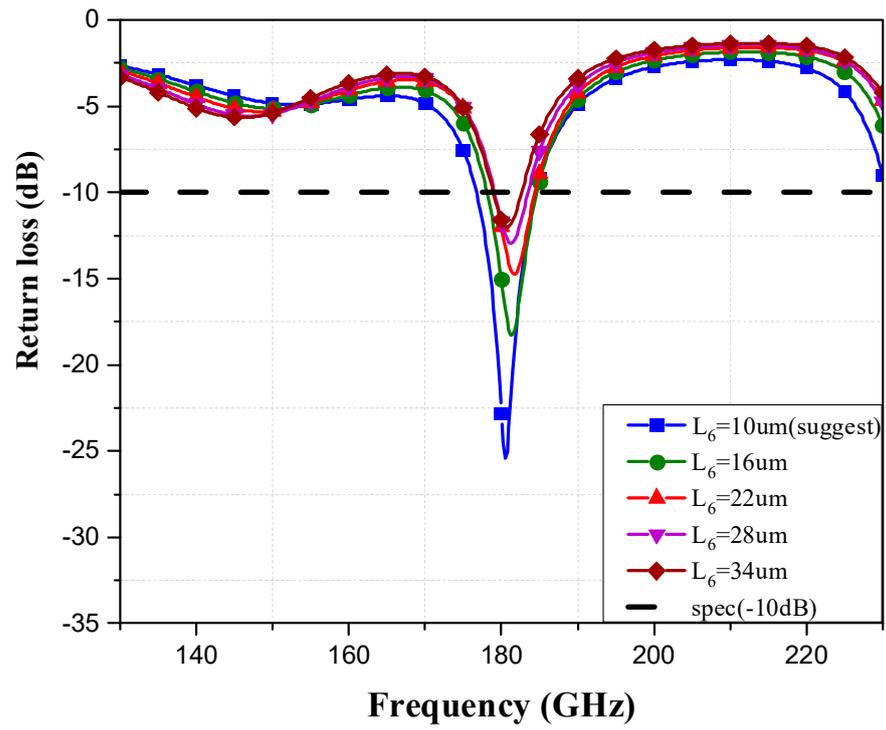
**Figure 4.** Parameter diagram of parameter analysis,  $W_3$  is the width of the top layer,  $L_6$  is the feed width.

The purpose of parameter analysis primarily focuses on optimizing the antenna's performance to meet specific application requirements. This involves measuring and adjusting key antenna design parameters, such as frequency range, gain, radiation pattern, bandwidth, impedance matching, and polarization characteristics. Through a precise analysis of these parameters, the antenna can achieve optimal performance in practical operations. The main advantages of parameter analysis including performance optimization, impedance matching, polarization adaptation, interference reduction. In addition, there are two very important reasons for parameter analysis. Frequency matching and Bandwidth improvement. Parameter analysis ensures that the antenna performs best within the targeted operating frequency range, which is particularly crucial for wireless communication systems, since different applications and services may require different frequency bands. Adjusting the antenna design can expand its effective operating frequency range, thereby supporting a wider range of applications and higher data transmission rates. This is also the reason why this article chooses two parameters for analysis. The first is to increase the bandwidth, and the second is to increase the bandwidth. Let the frequency operate at 180 GHz.

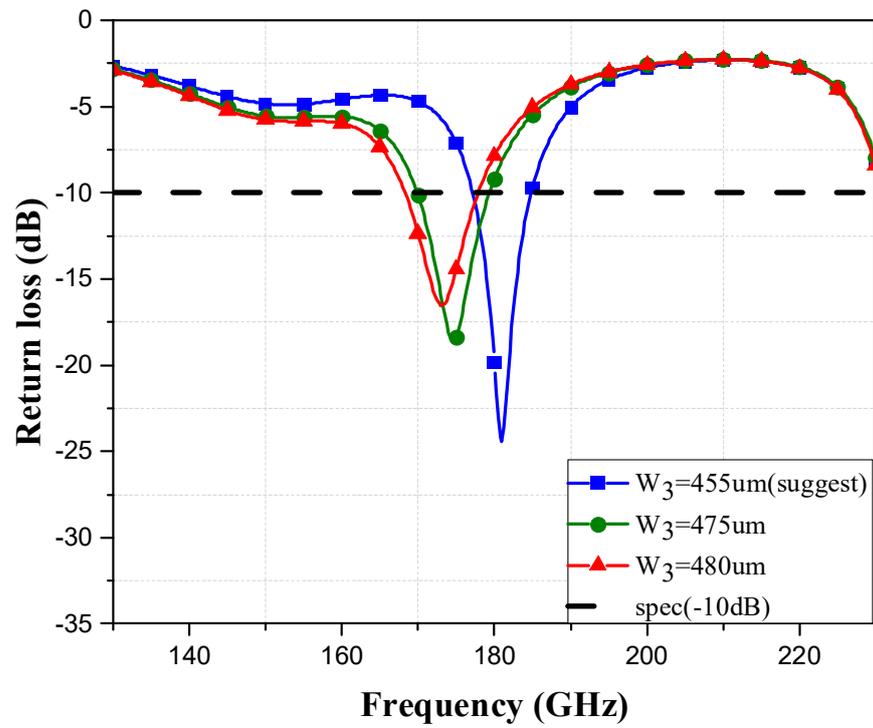
The reason for choosing  $L_6$  is because to carry out accurate measurement, using a GSG probe, a professional measurement tool. In this process, the parameter  $L_6$  was selected as the input point of the signal to adjust the matching parameters to ensure the best measurement results. Adjustment of  $W_3$  is to allow the bandwidth to operate at 180 GHz.

When the feed width  $L_6$  is 10  $\mu\text{m}$ . As shown by the blue line in Figure 5a, the return loss will be lower than  $-10$  dB at 176.73 GHz, the deepest point is  $-25.4172$  dB, and the bandwidth is 176.73–184.50 GHz. When the feed width  $L_6$  is 16  $\mu\text{m}$ . As shown by the green line in Figure 5a, the return loss will be lower than  $-10$  dB at 178.13 GHz, the deepest point is  $-18.2411$  dB, and the bandwidth is 178.13–184.65 GHz. When the feed width  $L_6$  is 22  $\mu\text{m}$ . As shown by the red line in Figure 5a, return loss will be lower than  $-10$  dB at 179.09 GHz, the deepest point is  $-14.7682$  dB, and the bandwidth is 179.09–184.40 GHz. When the feed width  $L_6$  is 28  $\mu\text{m}$ . As shown by the purple line in Figure 5a, the return loss will be lower than  $-10$  dB at 179.08 GHz, the deepest point is  $-12.9665$  dB, and the bandwidth is 179.08–183.47 GHz. When the feed width  $L_6$  is 34  $\mu\text{m}$ . As shown by the brown line in Figure 5a, return loss will be lower than  $-10$  dB at 178.94 GHz, the deepest point is  $-12.0275$  dB, and the bandwidth is 178.94–182.62 GHz.

After parameter analysis, when the feed width  $L_6$  is 10  $\mu\text{m}$ , the bandwidth is the widest and the reflection coefficient has the lowest value. Therefore, the results of the S parameter analysis when the feed width  $L_6$  is 10  $\mu\text{m}$  are used as the feed width of the antenna in this antenna in Figure 5a. Then the width of the  $W_3$  top layer is subjected to parameter analysis. When the width of the upper layer  $W_3$  is 455  $\mu\text{m}$ . As shown by the blue line in Figure 5b, return loss will be lower than  $-10$  dB at 177.16 GHz, the deepest point is  $-24.4551$  dB, and the bandwidth is 177.16–184.83 GHz.



(a)



(b)

Figure 5. (a)  $L_6$  parameter analysis return loss comparison; (b)  $W_3$  parameter analysis return loss comparison.

When the width of the upper layer  $W_3$  is 475  $\mu\text{m}$ . As shown by the green line in Figure 5b, return loss will be lower than  $-10$  dB at 169.88 GHz, the deepest point is  $-18.5647$  dB, and the bandwidth is 169.88–179.35 GHz. When the width of the upper layer  $W_3$  is 480  $\mu\text{m}$ . As shown by the red line in Figure 5b, return loss will be lower than  $-10$  dB at 179.09 GHz, the deepest point is  $-16.5554$  dB, and the bandwidth is 168.30–177.88 GHz.

After parameter analysis, when the width of the  $W_3$  top layer is 455  $\mu\text{m}$ , the reflection coefficient has the lowest value and the center frequency is closest to 180 GHz. Therefore, the results of the S parameter analysis when the top layer width  $W_3$  is 455  $\mu\text{m}$  are used as the antenna top layer width of the antenna in this article in Figure 5b.

From Tables 2 and 3, we can see that the wider the feed width, the narrower the bandwidth, and the larger the lowest point. The wider the width of the top layer, the frequency will move to a lower frequency, and the larger the lowest point will be. In summary, the analysis and optimization of antenna parameters is a complex but critical process that can significantly enhance the antenna's performance, ensuring the efficiency and reliability of wireless communication systems.

**Table 2.**  $L_6$  parameter analysis results (Bandwidth, Return loss lowest point).

Value (Unit: $\mu\text{m}$ )	Bandwidth (GHz)	Return Loss Lowest Point (dB)
10	7.77	$-25.4172$
16	6.52	$-18.2411$
22	5.31	$-14.7682$
28	4.35	$-12.9665$
34	3.68	$-12.0275$

**Table 3.**  $W_3$  parameter analysis results (center frequency, Return loss lowest point).

Value (Unit: $\mu\text{m}$ )	Center Frequency (GHz)	Return Loss Lowest Point (dB)
455	180.99	$-25.4172$
475	174.61	$-18.2411$
480	173.09	$-14.7682$

### 3. Simulation and Measurement

#### 3.1. Return Loss

Return loss (S11) is usually used to describe the reflection characteristics of components such as circuits or antennas. In microwave and radio frequency engineering, S11 is an important parameter that represents the reflection of the input signal by the component.

Figure 6 illustrates the comparison results of the Horn antenna on chip. Return loss ( $|S_{11}|$ ) between the measured and simulated. Return loss (1), where  $P_R$  and  $P_I$  are reflected power (W), and incident power (W) respectively. The results show that although the frequency changes toward low frequency, the simulation results and the measurement results have a very similar trend. The cause of the frequency shift may be due to minor manufacturing differences, such as differences in material properties, size, arrangement, etc. when manufacturing the chip antenna. When making chips, due to DRC (Design rule check) restrictions in the manufacturing process, the density will be filled with dummy, so there will be a slight error in the measurement. The measurement technology used in actual measurement may have certain limitations, such as limitations in measurement accuracy, measurement frequency range, etc. These factors can have an impact on the performance of the antenna, and these effects are difficult to fully account for in simulations.

$$\text{Reflection Coefficient}_{\text{dB}} = 10 \times \log_{10} \left( \frac{P_R}{P_I} \right) \quad (1)$$

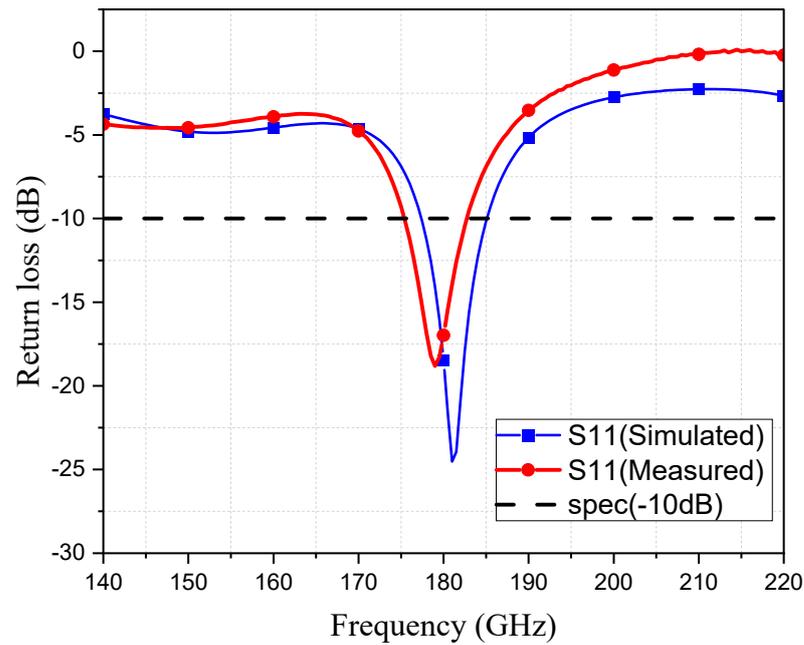


Figure 6. Simulation and measurement of the return loss.

3.2. 3D Radiation Pattern

The 3D radiation pattern is a theoretical model that is used to describe the radiation field of an antenna. The 3D radiation field pattern takes into account the radiation distribution in the three-dimensional space, including factors such as the intensity, direction, and frequency of the radiation. Radiation field patterns can accurately simulate radiation phenomena and optimize designs. Figure 7 shows the 3D field pattern radiation diagram of the electromagnetic simulation software. At a frequency of 180 GHz, this simulation result was obtained. It can be seen that the radiation direction is consistent with the expected result and radiates in the positive Z direction.

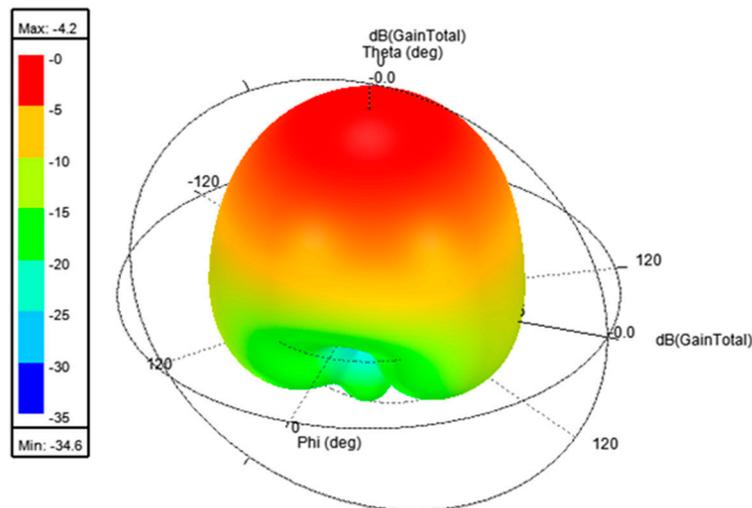
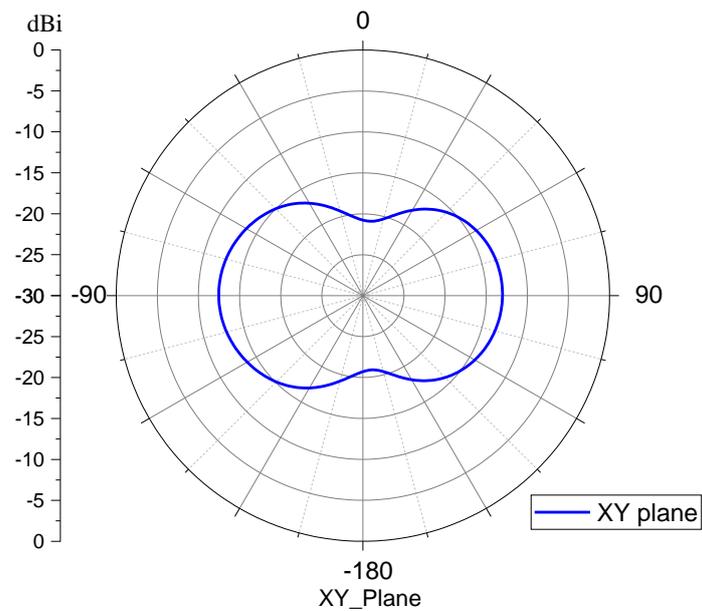


Figure 7. 3D radiation field simulation diagram.

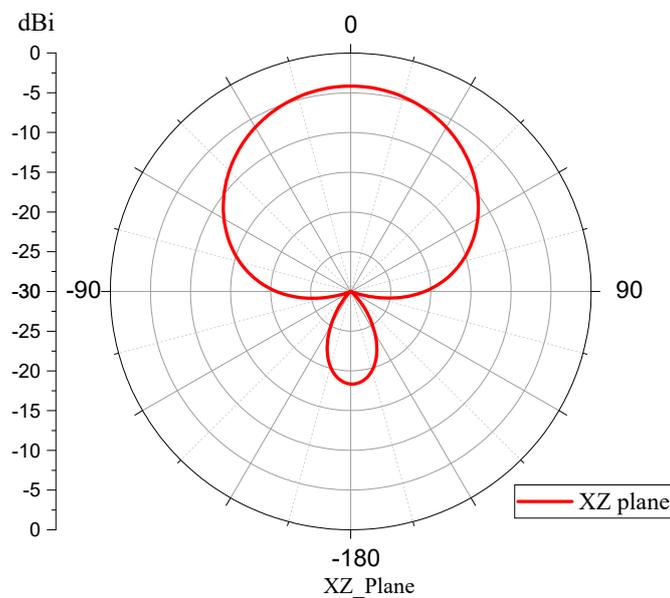
3.3. 2D Radiation Pattern Diagram

The 2D radiation pattern is a theoretical model used to describe the radiation distribution in two-dimensional space. In this model, space is divided into planes or surfaces, and the radiation field is confined to these planes or surfaces. Simplifying the problem by

restricting the radiation field to two dimensions makes analysis and calculations easier. The 2D radiation field pattern can be used to simulate and analyze radiation phenomena on various two-dimensional planes, including absorption, scattering and reflection processes. This helps to understand and optimize many technologies and applications related to surface radiation. Figure 8a–c respectively shows the 2D field pattern diagrams of XY, XZ and YZ planes at 180 GHz. It can be seen that the XY plane has a maximum value of  $-13.0297$  dB at 90 degrees. The maximum value of the XZ plane is  $-18.3562$  dB at 180 degrees. The maximum value of the YZ plane is  $-18.3561$  dB at 180 degrees.



(a)



(b)

**Figure 8.** *Cont.*

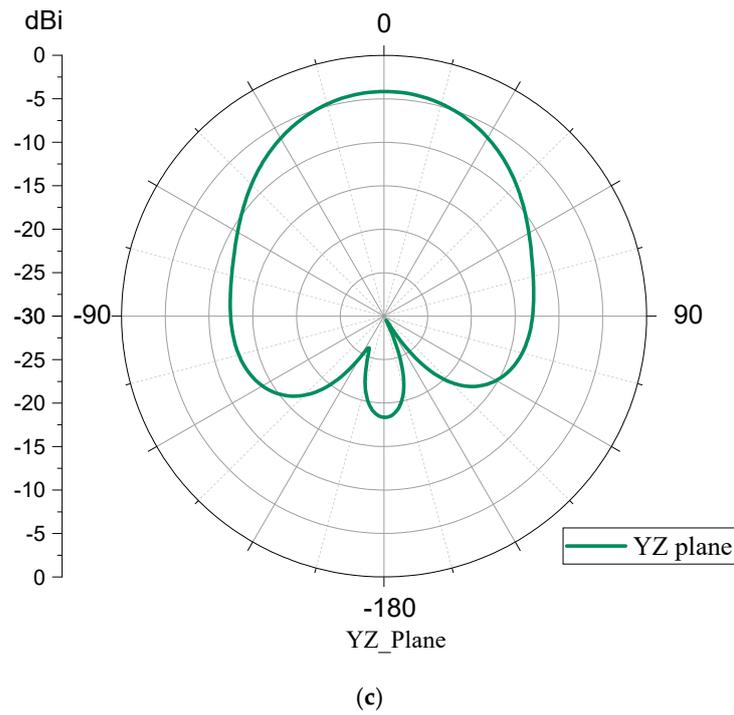


Figure 8. At 180 GHz, the 2D radiation pattern of the antenna. (a) XY Plane; (b) XZ Plane; (c) YZ Plane.

### 3.4. Gain

The gain of an antenna refers to the increase in the power of electromagnetic waves transmitted and received by the antenna in a specific direction relative to an ideal feed antenna. The gain of an antenna is usually expressed in dBi. If the gain increases, the antenna transmits and receives signals in that direction more effectively. Antenna gain can be calculated in Formula (2). Among them,  $G_{dB}$  is the gain of the antenna,  $\eta$  is efficiency, and  $A$  is the aperture area. Figure 9 shows the gain of this design. The gain is  $-4.21$  dBi at 180 GHz.

$$G_{dB} = 10\log_{10}\left(\frac{4\pi\eta A}{\lambda^2}\right) \tag{2}$$

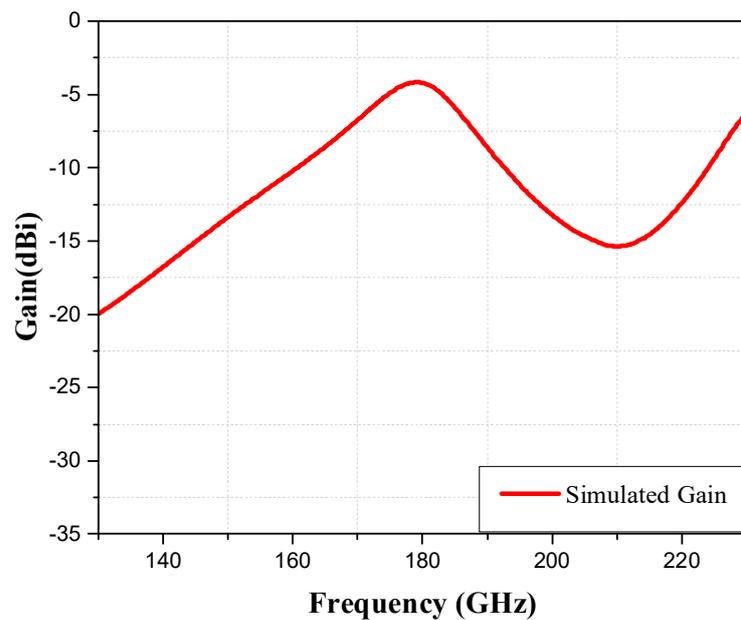
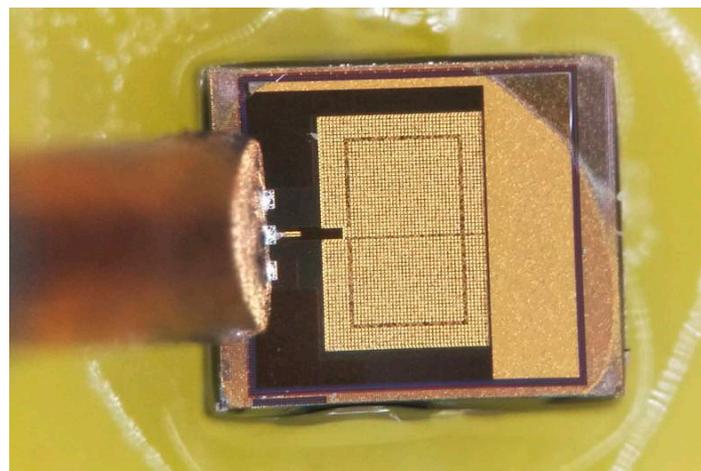


Figure 9. Antenna gain simulation.

### 3.5. Prototype and Measurement Environment

These three photos in Figure 10 were taken by myself during measurements at Taiwan Semiconductor Research Institute (TSRI). Figure 10a shows the chip Horn antenna designed in this article, taken at high magnification and measured from the front. Use the GSG probe when setting the needle. Figure 10b shows the measurement environment and Figure 10c shows the antenna measurement platform. Figure 10d shows the schematic measurement environment. The top is VNA (vector network analyzer). A vector network analyzer is an instrument that measures the network parameters of electrical networks. It is a type of radio frequency (RF) test equipment used to characterize components, circuits, and materials that affect radio and microwave frequencies. It has many functions, including S-Parameter measurement, Impedance measurement, Frequency response, Gain and phase measurement, and Time-Domain analysis. Then connect VDI (Variable Delay Insulator Frequency Upconverter) to both sides of the VNA. The VDI is commonly associated with frequency conversion equipment, particularly in radar and wireless communication systems. Such devices are typically used to convert signals from a lower frequency to a higher frequency. There is a DUT (Device Under Test Platform) under the VNA. This is a specialized platform designed for placing devices or objects under test, facilitating various measurements and tests. The platform ensures the stability and proper positioning of the test object during the measurement process, thus obtaining accurate test results.



(a)

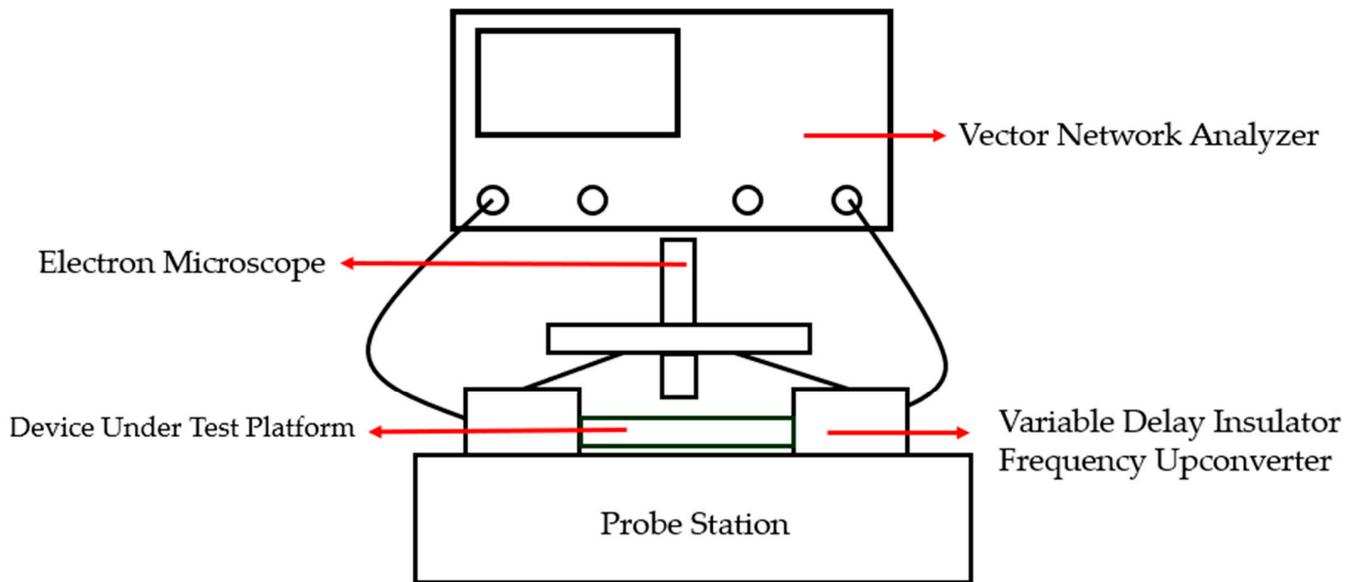


(b)

Figure 10. Cont.



(c)



(d)

**Figure 10.** Measurement environment (a) Antenna measurement front view; (b) Antenna measurement environment; (c) Antenna measurement platform; (d) Schematic measurement environment.

### 3.6. Discuss

In Table 4, the chip antenna proposed in this article is compared with chip antennas using different processes, and small dimension can be obtained. In addition, the bandwidth percentage of the antenna is also very competitive. Compared to [15,16,19], the proposed SiGe CMOS horn antenna has a benefit in bandwidth. Compared to the antennas of [15–18], the proposed antenna has a dimension advantage.

In SiGe CMOS technology, because its procedure enables the incorporation of RF front-end circuits, antennas and additional functionalities onto a single chip. Having this design feature saves space and reduces power consumption. As can be seen in Table 4, compared with other different processes, the process and design proposed in this article obviously have advantages in space and are also quite competitive in terms of bandwidth percentage. The spatial advantage of the SiGe CMOS Horn antenna in this article is evident from Table 4, thus affirming the superiority of this antenna.

**Table 4.** The proposed antenna is compared with chip antennas using different processes.

References	Process	Frequency (GHz)	* FBW (%)	Dimension (mm <sup>2</sup> )
[15]	Wire bonding	93.7	3.8%	2.1 × 2.1
[16]	IPD	94.5	2%	1.9 × 1.9
[17]	CMOS	94.5	10.5%	2.4 × 2.4
[18]	65 nm CMOS	280	*N/A	2.8 × 2.8
[19]	TSV	275	3.6%	*N/A
[20]	130 nm CMOS	165	5.2%	1.88 × 1.88
Proposed	SiGe CMOS	180	4.2%	0.85 × 0.85

\* FBW = Fractional Bandwidth. \*N/A = Not Available.

### 3.7. Future Outlook

Chip antennas, as highly integrated miniature antennas, have played a significant role in the field of wireless communication. They are widely used due to their small size, low cost, and ease of integration into various electronic devices, particularly mobile devices, Internet of Things (IoT) gadgets, and wearable technologies. With technological advancements and increasing demands for wireless communication, the future outlook included higher frequencies and wideband operation, with the evolution of 5G and future 6G technologies, chip antennas need to support higher frequencies and wider bandwidths. This will require the development of new materials and design techniques to achieve efficient antenna performance while maintaining their miniature size. And another future outlook is multifunctionality and Multiband, Chip antennas will need to support multiple wireless communication standards and bands simultaneously, including Wi-Fi, Bluetooth, LTE, and future technologies. This will make antenna designs more complex, but also enable a single device to support more wireless functionalities. The third is intelligent and adaptive antenna technologies, with the advancement of Artificial Intelligence (AI) and machine learning technologies, chip antennas can become smarter, capable of automatically adjusting their parameters based on the wireless environment and communication needs. This adaptive capability will further enhance the efficiency and reliability of wireless communication. The fourth is increased integration; Future chip antennas will be even more integrated, not just as standalone components but potentially integrated with other electronic components (such as microprocessors, sensors) on the same chip. This will help further reduce the device size and improve overall performance. The last one is Environmental Friendliness and Sustainability, With increasing awareness of environmental protection, future chip antenna designs will pay more attention to using recyclable or biodegradable materials to minimize environmental impact.

## 4. Conclusions

The operating frequency of the SiGe CMOS Horn antenna designed for the antenna is 180 GHz. Using SiGe CMOS can have low cost and reduce dimension. At the same time, the maximum bandwidth is found by analyzing the feed and the presence or absence of the uppermost layer and conducting measurement and verification. The return loss measurement results are in the range of 177.4–183 GHz, and the measurement bandwidth has a broadband advantage compared to other documents. The antenna used measures 0.85 mm × 0.85 mm, which is small and better than most designs. In addition, there are many areas worthy of development and research in this design in the future, including higher frequencies and wideband operation multifunctionality and multiband intelligent and adaptive technologies.

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**Data Availability Statement:** Data is contained within the article. The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding authors.

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**Conflicts of Interest:** The authors declare no conflicts of interest.

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