

Article

# High Performance CMOS Light Detector with Dark Current Suppression in Variable-Temperature Systems

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**Abstract:** This paper presents a dark current suppression technique for a light detector in a variable-temperature system. The light detector architecture comprises a photodiode for sensing the ambient light, a dark current diode for conducting dark current suppression, and a current subtractor that is embedded in the current amplifier with enhanced dark current cancellation. The measured dark current of the proposed light detector is lower than that of the epichlorohydrin photoresistor or cadmium sulphide photoresistor. This is advantageous in variable-temperature systems, especially for those with many infrared light-emitting diodes. Experimental results indicate that the maximum dark current of the proposed current amplifier is approximately 135 nA at 125 °C, a near zero dark current is achieved at temperatures lower than 50 °C, and dark current and temperature exhibit an exponential relation at temperatures higher than 50 °C. The dark current of the proposed light detector is lower than 9.23 nA and the linearity is approximately 1.15  $\mu\text{A}/\text{lux}$  at an external resistance  $R_{SS} = 10 \text{ k}\Omega$  and environmental temperatures from 25 °C to 85 °C.

**Keywords:** light detector; dark diode (DD); photodiode (PD); current amplifier (CA); dark current cancellation; variable-temperature system

## 1. Introduction

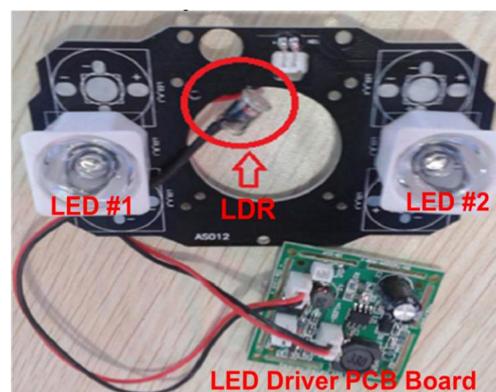
With the ever-increasing demand for eco-design, environmental legislation for electronics is focused on two major requirements. One is the internationalization of the restriction of hazardous substances and the waste of electrical and electronic equipment; the other is a new directive especially for energy using products and the registration, evaluation, authorization, and restriction of chemicals [1]. Lifetime extension is an important eco-design strategy for mitigating the environmental burden of developing new devices. Organic semiconductors increase the lifetime of large-area, low-cost image sensors by several thousand hours, and they monolithically integrate with photonic microsystems [2]. Miniaturized power supply units tend to have a smaller environmental impact at the production stage than traditional electronics do [1]; integrated circuitry can miniaturize power supplies. Colace reported on the first silicon-integrated, 2-D, light-sensitive array fabricated with CMOS technology and readout electronics. The proposed chip includes a light-sensitive array, analog-to-digital converters, dark current cancellation circuitry, and facilities for testing and calibration. It operates as a near-infrared camera [3].

Dark current cancellation is another important eco-design element for photosensors. In reference [4], a hybrid CMOS microfluidic microsystem was proposed for electrochemiluminescence-based biochemical sensing. In the CMOS imager, a two-transistor reset path technique is employed to attenuate the subthreshold leakage current and to reduce the dark current. The imager achieves a low photodiode

(PD) dark current of  $3.6 \text{ nA/cm}^2$ , but the reset voltage is as high as 2.3 V. However, sub-dark current measurement is completed by subtracting the dark signal frame from the captured frame, and the dark signal frame is stored off chip. Furthermore, a prototype integrated phototransistor-based CMOS active pixel sensor circuit with scintillating material was presented for X-ray imaging. Cancellation of the leakage current using a dummy phototransistor technique was tested and proved efficient [5]. In reference [6], an ultralow dark signal was presented for an embedded active-pixel CMOS image sensor. To achieve in-pixel dark current cancellation, a combined photogate and PD photon-sensing device was developed [6]. Specifically, the dark current was cancelled using a sensing device that was fabricated with a large area. In the current study, dark current cancellation was performed using a current amplifier (CA). A CA is a good photo-detection circuit, which is easily fabricated with CMOS technology. By cancelling the dark current, we can not only enhance the sensitivity of the CA but also reduce the power consumption. The proposed light detector provides a high performance and small chip area.

A high dynamic range light-to-frequency converter (LFC) chip is proposed with dark current suppression up to  $125 \text{ }^\circ\text{C}$ . By regulating the cathode voltage of the PD and using a replica amplifier, the dark current is reduced. Measurements show that the output frequency is more insensitive to the ambient temperature and process variation. Supply voltage variation is also minimized by implementing a constant delay module [7]. Figure 1 shows a demonstration board design which is implemented with the light-dependent resistor (LDR), the light-emitting diode (LED), and an LED driver printed circuit board (PCB). The typical LED driver with the LDR operates with a large dark current.

In this study, a CA with enhanced dark current cancellation was fabricated using  $0.18 \text{ }\mu\text{m}$  1P2M CMOS technology with a chip area of  $762 \text{ }\mu\text{m} \times 452 \text{ }\mu\text{m}$ , including pads. Simulated and measured results were obtained with white LED light and characterized using a lux meter at a supply voltage  $V_{CC}$  of 3.3 V, an external resistance  $R_{SS}$  of  $10 \text{ k}\Omega$ , and an environmental temperature varying from  $-40 \text{ }^\circ\text{C}$  to  $125 \text{ }^\circ\text{C}$ . The rest of this paper is organized as follows. Section 2 elucidates the proposed circuit topology of the light detector. Section 3 presents the simulated and measured results, and in Section 4, conclusions are drawn.



**Figure 1.** Demonstration board design implemented with the LDR, LED, and LED driver PCB.

## 2. Proposed Circuit Topology of the Light Detector

In this section, we propose a CA with dark current cancellation that is composed of a dark diode (DD) and a photodiode (PD). The DD senses the dark current in dark environment, while the PD senses the photodiode current in electric lighting. Figure 2 presents the schematic cross-section of an n+/p-substrate PD and its equivalent circuit. The PD is built with a p-n junction, which is sensitive to the environmental temperature. Figure 3 shows the simulated PD dark current as a function of environmental temperature ( $^\circ\text{C}$ ) and bias voltage (V) in dark conditions. According to the simulated results, the PD dark current (nA) is highly sensitive to the environmental temperature, but insensitive to the bias voltage.

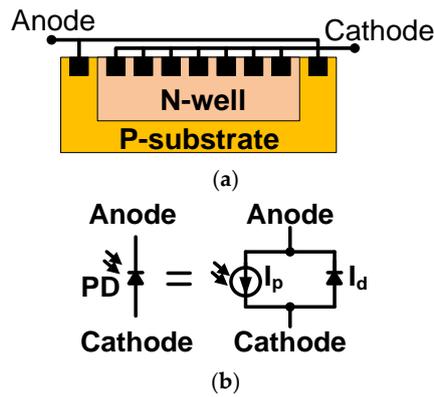


Figure 2. n+/p-substrate PD: (a) cross-section; and (b) the equivalent circuit.

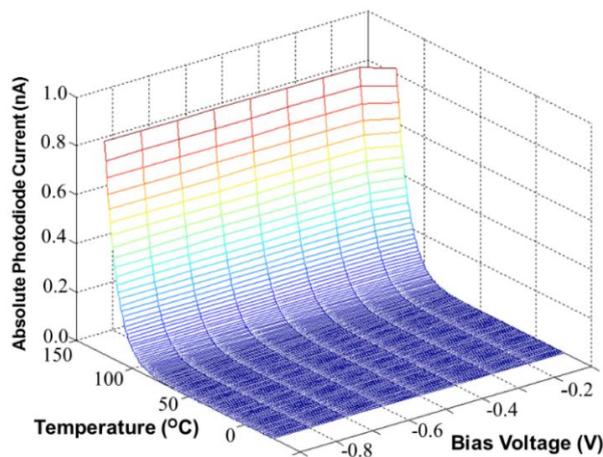


Figure 3. Simulated PD dark currents versus the environmental temperature (°C) and bias voltage (V) in dark conditions.

Furthermore, the sensing area of the PD is another important factor. The simulated dark current is approximately proportional to the area ratio, which is defined as the ratio of the PD area to  $300 \mu\text{m} \times 300 \mu\text{m}$ . Figure 4 shows the simulated dark current as a function of the environmental temperature (°C) in dark conditions. The smaller the area ratio is, the smaller the dark current is. All simulated dark current levels are settled to  $0.3 \text{ pA}$  due to imperfect diode model, which is provided from foundry. Figure 5 shows the CA of the PD, which operates without dark current cancellation. The resistance of the PD  $R_{PD}$  is equal to the voltage drop  $V_{PD}$  in the PD divided by its current  $I_{Light}$ . The light current of the PD  $I_{Light}$  is amplified with a current mirror, whose magnification is approximately equal to  $(W_2/W_1) \times (W_4/W_3) \times (W_6/W_5)$  with equal length ( $L$ ) for all MOSFETs. Thus, the output current  $I_O$  can be expressed with the total current gain  $A$ :

$$\begin{aligned}
 I_O &= \frac{(W_2/L_2)}{(W_1/L_1)} \times \frac{(W_4/L_4)}{(W_3/L_3)} \times \frac{(W_6/L_6)}{(W_5/L_5)} \times I_{Light} \\
 &= A \times I_{Light}
 \end{aligned} \tag{1}$$

where  $I_{Light}$ , also called the photodiode current, includes the illumination current  $I_{Lux}$  and the dark current  $I_{Dark}$ , which flow from  $V_{DD}$  to the ground in a dark environment. The photocurrent  $I_{Light}$  and dark current  $I_{Dark}$  are amplified  $A$  times. If the CA operates in a variable-temperature system without dark current cancellation, the dark current causes malfunction. This is the reverse of the characteristic of p-i-n PDs. For a reverse biased diode, the reverse bias current  $I_R$  can be defined by the following equation with reverse bias voltage  $V$  [8]:

$$I_R = I_S \times \exp(qV/nkT - 1) \tag{2}$$

where  $I_S$  is the saturation current,  $q$  is the electronic charge,  $kT$  is the Boltzman energy, and  $n$  is a parameter of which the value depends on contributions from both diffusion and surface-generation currents. For a 4H-SiC avalanche photodiode (APD), the dark current is close to the measurement limit at low bias levels. At high bias, the dark current is relatively insensitive to temperature, a characteristic that signifies tunneling. If we assume that the tunneling dark current undergoes avalanche multiplication similar to that of the photocurrent at high bias, the total dark current is expressed by reference [9]:

$$I_{dark} = Gain(V, T) \times I_{tunneling} \tag{3}$$

where  $Gain(V, T)$  is an additional correction factor obtained through photocurrent measurement. The tunneling current  $I_{tunneling}$  is proportional to  $A \times V^{3/2}$  with the device area  $A$  and the effective bias voltage  $V$  [9]. The objective of this study was to obtain a zero dark current in order to achieve higher photo resistance sensitivity.

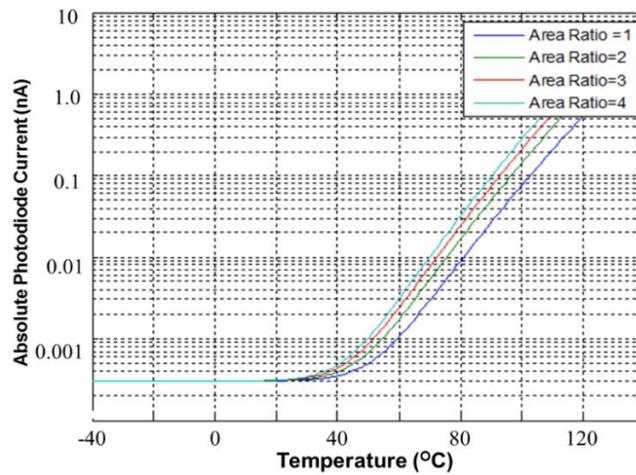


Figure 4. Simulated PD (dark) current versus standardized area ratio in dark conditions.

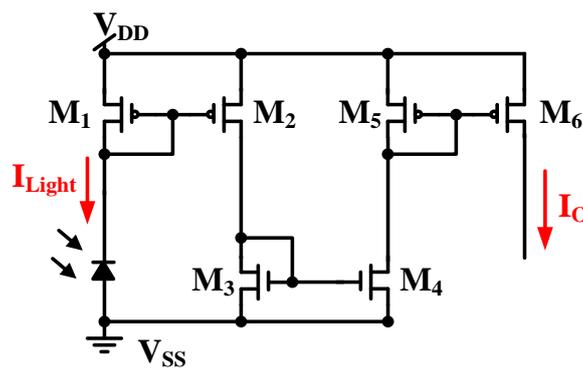


Figure 5. CA without dark current cancellation.

Figure 6 shows a CA with dark current cancellation that is composed of a dark diode (DD) and a PD [10]. The DD senses the dark current  $I_{Dark}$  in dark environments, while the PD senses the photodiode current  $I_{Light}$  in electric lighting. The photodiode size of PD ( $A_{PD}$ ) is two times of that of DD ( $A_{DD}$ ); and the MOSFET size of  $M_2$  is two times that of  $M_1$ , e.g.,  $A_{PD} = 2 \times A_{DD}$  and  $(W/L)_{M2} = 2 \times (W/L)_{M1}$ . Thus, the drain current  $I_{D3}$  of  $M_3$  is equal to the illumination current  $I_{Lux}$  and the output current  $I_O$  is expressed by:

$$I_{D3} = I_{Light} - I_{Dark} = I_{Dark} + I_{Lux} - I_{Dark} = I_{Lux} \quad (4)$$

$$I_O = \frac{(W/L)_6}{(W/L)_5} \times I_{Lux} = B \times I_{Lux} \quad (5)$$

where  $(W/L)_n$  is the metric ratio of transistor  $M_n$ , and  $B$  is the current gain. That is,  $(W/L)_{M3} = (W/L)_{M4}$  and  $(W/L)_{M6} = B \times (W/L)_{M5}$ . The output current  $I_O$  operates without the dark current  $I_{Dark}$ . That is, the dark current is cancelled in Figure 6. However, it is difficult to achieve a zero illumination current in light application because of the MOSFET mismatch in the CA. When both the DD and PD operate only with dark current, the two equivalent resistors of the DD and PD are expressed as  $R_{DD}$  and  $R_{PD}$ , respectively, and the current symbols,  $I_{Dark1}$ ,  $I_{Dark2}$ ,  $I_{Dark3}$ , and  $I_{Dark4}$ , denote the dark currents of  $M_1$ ,  $M_2$ ,  $M_3$ , and  $M_4$ , respectively, in dark conditions. As shown in Figure 7, the output current  $I_O$  is achieved:

$$I_O = B \times I_{Dark4} \quad (6)$$

where  $B$  is the current gain displayed in Equation (6) and is approximately 10,000 times. The output current  $I_O$  includes the amplified dark current of  $M_4$ . This circuit operates with a large dark current.

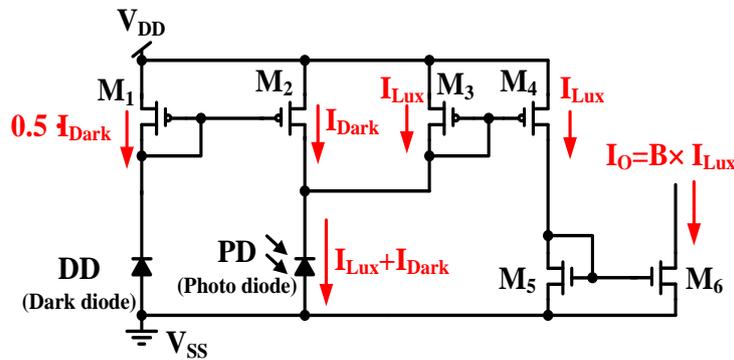


Figure 6. CA with dark current cancellation.

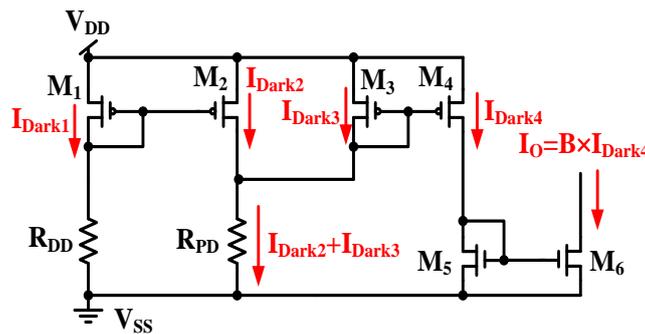


Figure 7. All dark currents of MOSFETs in Figure 6 in dark conditions.

The dark current in Figure 7 must be reduced. Figure 8 displays a CA with enhanced dark current cancellation. The MOSFET size of  $M_3$  is two times of that of  $M_4$ , e.g.,  $(W/L)_{M3} = 2 \times (W/L)_{M4}$ . As shown in Figure 8, current steering is implemented to draw a different current,  $I_{Light} - I_{Dark}$ , which is equal to the illumination current  $I_{Lux}$ . The output current  $I_O$  can then be expressed with the total current gain  $A_E$ , if  $(W/L)_{M1} = (W/L)_{M2}$ ,  $(W/L)_{M5} = (W/L)_{M6}$ , and  $(W/L)_{M8} = A_E \times (W/L)_{M7}$ . The output current  $I_O$  in Figure 8 operates without the dark current.

$$I_O = \frac{(W/L)_8}{(W/L)_7} \times (I_{Light} - I_{Dark}) = A_E \times I_{Lux} \quad (7)$$

When both the DD and PD operate only with dark currents, the two equivalent resistors of the DD and PD are expressed as  $R_{DD}$  and  $R_{PD}$ , and the current symbols,  $I_{Dark1}$ ,  $I_{Dark2}$ , and  $I_{Dark3}$ , denote the dark currents of  $M_1$ ,  $M_2$ , and  $M_3$ , respectively. As shown in Figure 9, the output current  $I_O$  is obtained.

$$I_O = A_E \times (I_{Dark2} - I_{Dark3}) = A_E \times I_{off} \tag{8}$$

where  $A_E$  is the current gain, as in Equation (7). The output current  $I_O$  can be reduced to approximately zero if the dark current of  $M_2$  is approximately equal to that of  $M_3$  ( $I_{Dark2} \approx I_{Dark3}$ ). The proposed circuit can also suppress the dark current induced by the environmental temperature, as described in Equation (3).

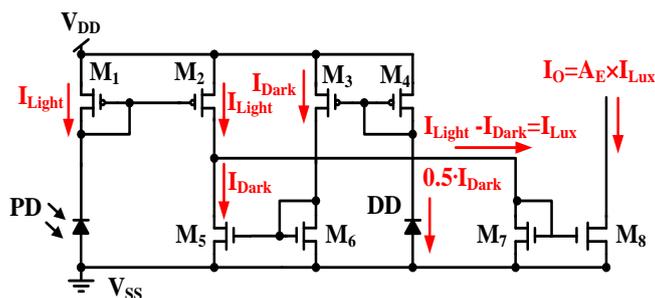


Figure 8. CA with enhanced dark current cancellation.

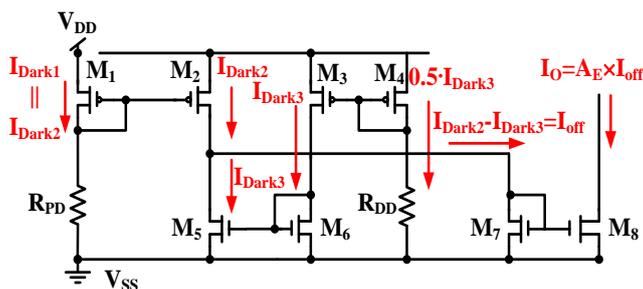
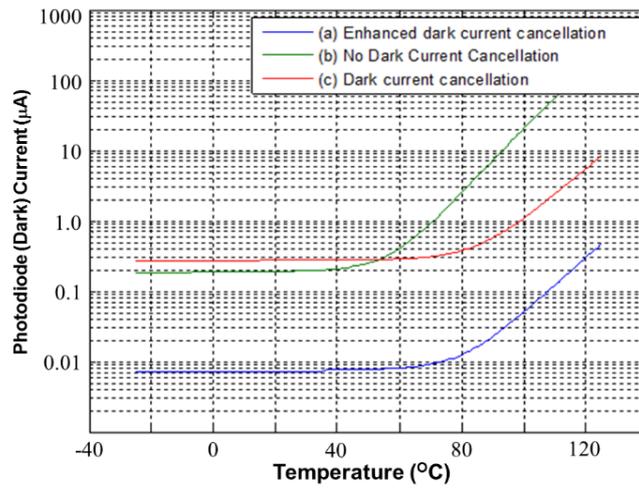


Figure 9. Dark currents of all MOSFETs in the proposed CA with enhanced dark current cancellation.

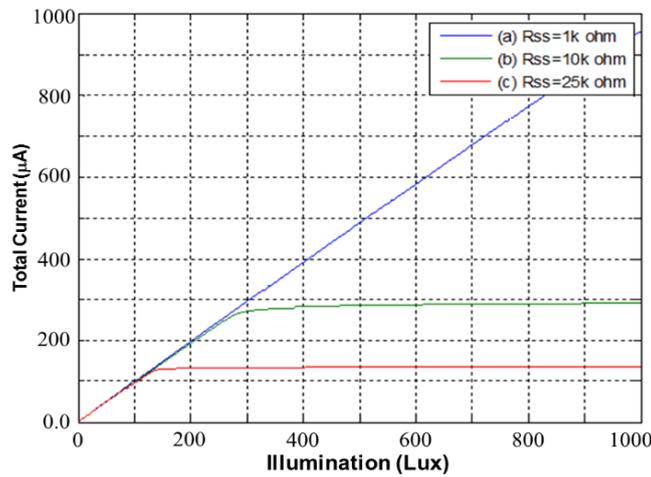
### 3. Simulated and Measured Results

Figure 10 presents the simulated PD dark current versus temperature for CAs. Three types of CA were compared. First, the proposed CA with enhanced dark current cancellation is indicated by Figure 10a. Next, a CA without dark current cancellation is denoted by Figure 10b. Finally, a CA with dark current cancellation is denoted by Figure 10c. According to the simulated results, the proposed CA with enhanced dark current cancellation operates with the lowest dark current. This means that the dark current can be cancelled perfectly with the proposed CA. The CA without dark current cancellation, which is denoted by Figure 10b, operates with a larger dark current. Note that the dark current level of curve Figure 10c is higher than that of Figure 10b below approximately 50 °C, because the magnification of curve Figure 10c is higher than that of curve Figure 10b.

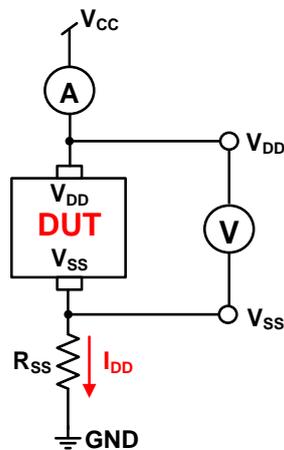
Figure 11 shows the simulated total current  $I_{DD}$  of the proposed CA as a function of illumination at three external resistances, namely  $R_{SS} = 1\text{ k}\Omega$ ,  $R_{SS} = 10\text{ k}\Omega$ , and  $R_{SS} = 25\text{ k}\Omega$ . As shown in Figure 11, a lower  $R_{SS}$  expands the illumination detection range. Two higher resistances,  $R_{SS} = 10\text{ k}\Omega$  and  $R_{SS} = 25\text{ k}\Omega$ , sharply force the proposed CA into saturation at 280 lux and 140 lux, respectively. Thus, for wide application, selecting a low  $R_{SS}$  is beneficial. Figure 12 shows the setup of the proposed CA that was used for measurement, with a current meter (A), voltage meter (V), and the design under test (DUT) chip. The external resistance  $R_{SS}$  was used to measure the total current  $I_{DD}$ , which was varied by applying illumination (lux) with white LED light.



**Figure 10.** Simulated PD dark currents versus temperatures for various CAs. (a) Proposed CA with enhanced dark current cancellation; (b) the CA without dark current cancellation; and (c) the CA with dark current cancellation.



**Figure 11.** Simulated total currents versus illumination (lux) for the proposed CMOS light detector.



**Figure 12.** Setup of the proposed CA for measurement.

Tables 1 and 2 summarize the simulated and measured dark current  $I_{Dark}$  and total current  $I_{DD}$  of the proposed CA with enhanced dark current cancellation at the PD area of  $300 \mu\text{m} \times 300 \mu\text{m}$

and a PD to DD area ratio of 2 times. Table 1 indicates that the measured dark currents are smaller than those of the simulations. This is because the PD model was always adopted in the simulations, but is not proven in the silicon process. However, the measured total currents are larger than those of the simulations. The total light current is approximately linear as a function of illumination in the simulation and the measurements in Table 2.

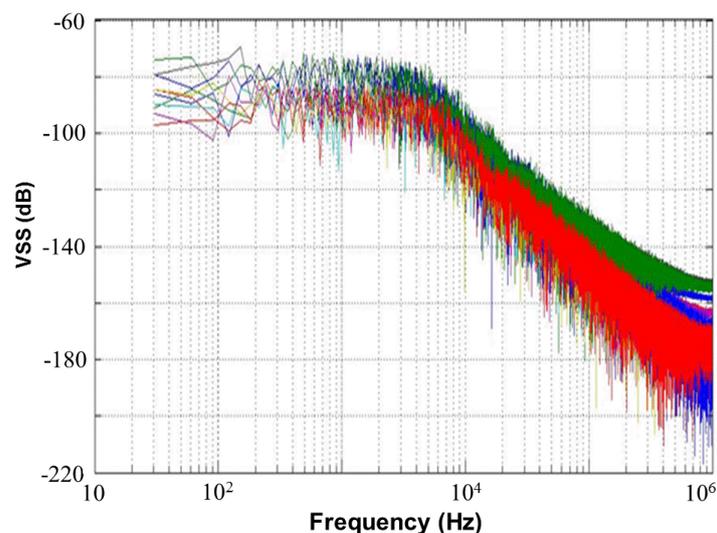
**Table 1.** Simulated and measured dark currents versus temperature for the proposed CA with enhanced dark current cancellation.

Temperatures (°C)	Simulations	Measurements
25	13.6 nA	1.24 nA
85	21.6 nA	9.23 nA
105	77.0 nA	36.4 nA

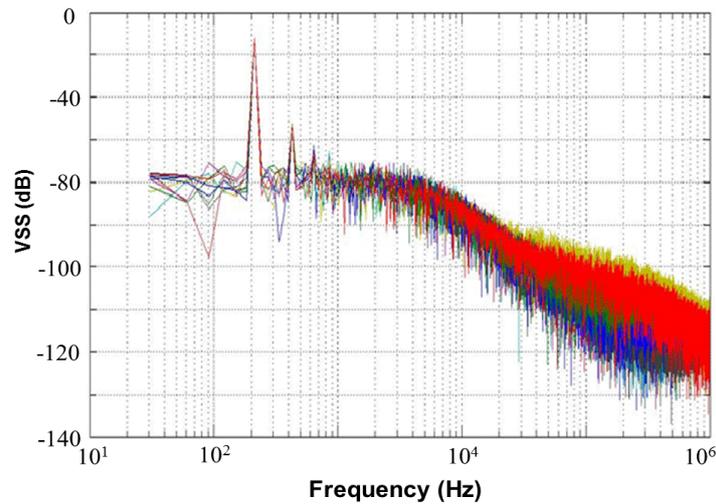
**Table 2.** Simulated and measured total currents versus illumination (lux) of the proposed CA with enhanced dark current cancellation.

Illuminations (lux)	Simulations	Measurements
10	8.78 $\mu$ A	18.2 $\mu$ A
100	99.3 $\mu$ A	145.0 $\mu$ A
200	194.0 $\mu$ A	236.0 $\mu$ A

Figure 13 shows a 65,536-point FFT simulation with a noise level of 80 dB and an external resistor  $R_{SS}$  of 1 k $\Omega$  for the proposed CMOS light detector. This figure presents a simulated frequency response of 10 Monte Carlo samples with random noises at node  $V_{SS}$ , which is shown in Figure 12. If a photodiode current signal, which is a superposition of a 250 lux (peak-to-peak) noiseless sine wave with a frequency of 210 Hz and a DC 500 lux, is fed to the proposed CMOS light detector, a plot of the frequency response of the simulated 10 Monte Carlo samples with random noises is made in Figure 14 at node  $V_{SS}$  for the proposed light detector. The current signal with frequency of 210 Hz performs without any random noises. Table 3 shows the simulated total harmonic distortions (THDs), signal-to-noise ratios (SNRs), and signal-to-noise+distortion ratios (SNDRs) of the 10 Monte Carlo samples with random noises at node  $V_{SS}$  of Figure 14 for the proposed light detector. As shown in Table 3, those simulated results of THD, SNR, and SNDR are roughly consistent. The Monte-Carlo approach can capture very nonlinear noise behaviors.



**Figure 13.** Frequency response of simulated 10 Monte Carlo samples with random noises at node  $V_{SS}$  of Figure 12 for proposed light detector, with  $R_{SS} = 1$  k $\Omega$ .

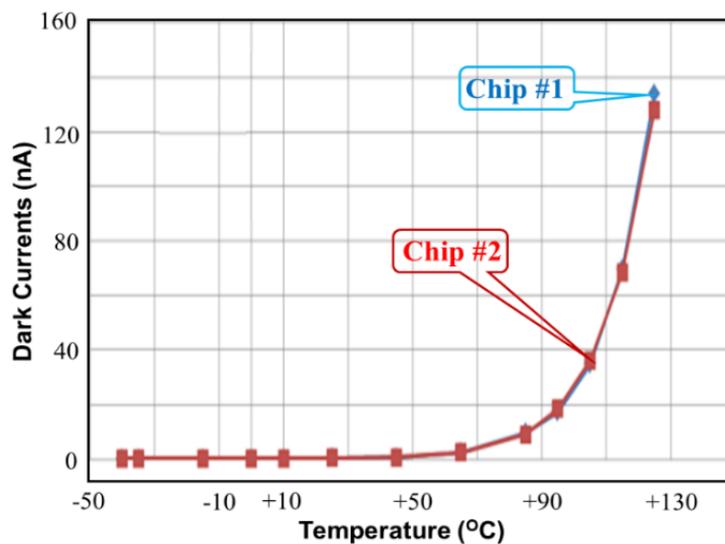


**Figure 14.** Frequency response of simulated 10 Monte Carlo samples with random noises and a 210 Hz sine wave at node  $V_{SS}$  of Figure 12 for the proposed light detector, with  $R_{SS} = 1 \text{ k}\Omega$ .

**Table 3.** Simulated THDs, SNRs, and SNDRs of the 10 Monte Carlo samples with random noises at node  $V_{SS}$  of Figure 14 for the proposed light detector.

Samples	1	2	3	4	5	6	7	8	9	10
THD (dB)	-39.84	-39.82	-39.84	-40.41	-39.85	-39.75	-40.27	-40.52	-40.06	-40.75
SNR(dB)	52.60	51.16	50.99	50.15	51.86	52.41	50.39	50.05	51.43	52.64
SNDR(dB)	39.61	39.51	39.52	39.97	39.58	39.52	39.87	40.07	39.76	40.48

Figure 15 shows the measured dark current versus temperature for the proposed CA with enhanced dark current cancellation. The maximum dark current is approximately 135 nA at 125 °C. This measurement proves that the proposed CA performs with low dark current as a function of the environmental temperature. According to the measurements in Figure 15, the device performs with zero dark current at temperatures lower than 50 °C and exhibits an exponential relation at temperatures higher than 50 °C. Notice that two measured dark currents are consistent in Figure 15, although chip #1 and chip #2 perform with different maximum dark currents at 125 °C.



**Figure 15.** Measured dark currents versus temperatures for the proposed CAs with enhanced dark current cancellation.

Table 4 summarizes the measured dark currents versus temperature of the proposed CAs, Chip #1 and Chip #2. Table 5 summarizes the measured output currents with respect to the illumination of the proposed CAs. According to the measured output currents in Table 5, the proposed CA performs with good linearity and wide illumination range.

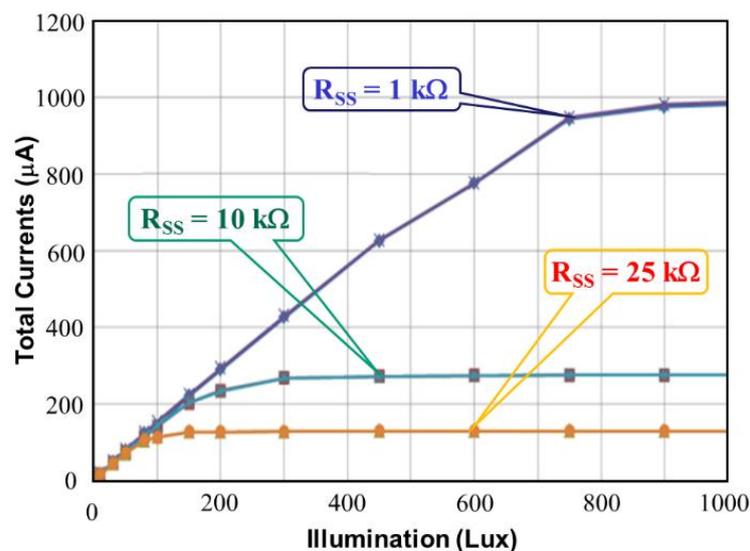
**Table 4.** Measured dark currents versus temperature of the proposed CAs, Chip #1 and Chip #2.

Temperatures (°C)	Chip #1	Chip #2
25	1.39 nA	1.24 nA
85	9.7 nA	9.23 nA
105	35 nA	36.4 nA

**Table 5.** Measured output currents with respect to illumination with  $R_{SS}$  of 1 k $\Omega$  for the proposed CAs.

Illumination (lux)	Chip #1	Chip #2
10	17.2 $\mu$ A	18.2 $\mu$ A
100	142 $\mu$ A	145 $\mu$ A
200	237 $\mu$ A	236 $\mu$ A
300	426 $\mu$ A	430 $\mu$ A
600	776 $\mu$ A	776 $\mu$ A
750	943 $\mu$ A	947 $\mu$ A
900	975 $\mu$ A	980 $\mu$ A

Figure 16 shows the total current as a function of illumination (lux) for the proposed CMOS light detector with dark current suppression at room temperature. The larger  $R_{SS}$  is, the lower the total current. As shown in Figure 16, two curves with  $R_{SS} = 10$  k $\Omega$  and  $R_{SS} = 25$  k $\Omega$  indicate saturation at low illumination, but the curve with  $R_{SS} = 1$  k $\Omega$  does not display saturation until 1000 lux. The measured total currents  $I_{DD}$  match those in Figure 11. Figure 17 shows the microphotograph of the proposed CMOS light detector with dark current suppression in a variable-temperature system. Note that the PD area  $A_{PD}$  is twice as large as the DD area  $A_{DD}$ . This arrangement not only lowers the dark current by contracting  $A_{DD}$  but also enhances the luminous efficiency by enlarging  $A_{PD}$ .



**Figure 16.** Measured total currents versus illumination (lux) for the proposed CMOS light detector.

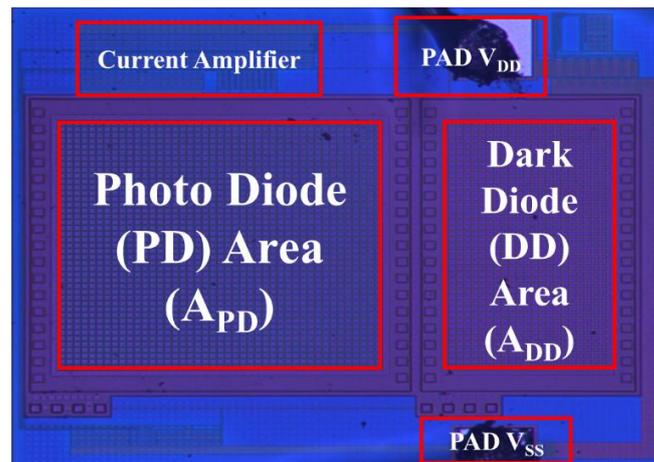


Figure 17. Microphotograph of the proposed CMOS light detector.

#### 4. Conclusions

This study presents a current steering method for drawing the current difference and lowering the dark current that is applied to the light detector in a variable-temperature system. The maximum dark current of the proposed CA is approximately 135 nA at 125 °C; and that the light detector proposed in this study performs with a low dark current as a function of the environmental temperature. Furthermore, the device obtains a zero dark current at temperatures lower than 50 °C and exhibits an exponential relation at temperatures higher than 50 °C. In addition, the larger  $R_{SS}$  is, the lower the total current is. Two curves with  $R_{SS} = 10 \text{ k}\Omega$  and  $R_{SS} = 25 \text{ k}\Omega$  indicate saturation at low illumination, but the curve with  $R_{SS} = 1 \text{ k}\Omega$  does not display saturation until 700 lux. Low external resistance  $R_{SS}$  results in a wide detected range of illumination (lux). The PD area  $A_{PD}$  is twice as large as the DD area  $A_{DD}$ . This design not only lowers the dark current by contracting  $A_{DD}$  but also enhances the luminous efficiency by enlarging  $A_{PD}$ . The chip area of the light detector is  $762 \mu\text{m} \times 452 \mu\text{m}$ , including pads. According to the measured results, the proposed CA successfully eliminates dark current from 50 °C to 125 °C.

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**Author Contributions:** This study is completed with three authors. W.-S.L. and J.-L.L. conceived and designed the experiments; W.-S.L. performed the experiments; G.-M.S. analyzed the data and wrote the paper.

**Conflicts of Interest:** The authors declare no conflict of interest.

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