

Article

1T Pixel Using Floating-Body MOSFET for CMOS Image Sensors

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Abstract: We present a single-transistor pixel for CMOS image sensors (CIS). It is a floating-body MOSFET structure, which is used as photo-sensing device and source-follower transistor, and can be controlled to store and evacuate charges. Our investigation into this 1T pixel structure includes modeling to obtain analytical description of conversion gain. Model validation has been done by comparing theoretical predictions and experimental results. On the other hand, the 1T pixel structure has been implemented in different configurations, including rectangular-gate and ring-gate designs, and variations of oxidation parameters for the fabrication process. The pixel characteristics are presented and discussed.

Keywords: 1T pixel, CMOS image sensors (CIS), floating-gate MOSFET, modeling, rectangular-gate pixel, ring-gate pixel.

1. Introduction

In recent R&D efforts on CMOS image sensors (CIS), there have been many attempts to reduce pixel size for higher image resolution and/or higher density of integration. One obvious way to do this

is to minimize the number of in-pixel transistors. This has led to architectural explorations instead of accepting 3 T and 4 T pixel structures as standard. Sharing pixel transistors has been proposed [1-3] and proved to be an effectively approach: it allows the number of transistors per pixel to be reduced to 2.5 T, 1.75 T, or 1.5 T. On the other hand, a more ambitious approach aims at ultimate achievement: single component for the pixel. There have been suggestions of specific transistor structures as single pixel component working on the charge-modulation principle [4-6]. However, to meet system integration requirements, the structure of the pixel transistor should be simple, compact, and integrable with minimum extra fabrication process steps.

This paper presents a 1T pixel using a floating-body MOSFET. Instead of employing a photodiode (PD), the transistor is also operated as photo-sensing device, with its floating body to collect and store charges during integration. For signal readout, the transistor is operated as source follower. Finally for reset operation, the stored charges can be evacuated by bias control. We describe this 1T pixel structure and its operating principle in the following section (Section 2). Our studies include device modeling and model validation (in Section 3), pixel implementation (in Section 4), as well as characterization. The evaluated performances are presented in Section 5.

2. Pixel Structure and Operating Principle

The proposed 1T pixel consists of an n-type MOSFET. Alternatively a p-type MOSFET may also be used. However, n-type transistor pixel operates with collection and storage of photo-generated holes rather than electrons, which is a better choice to reduce electrical crosstalk, because holes have much lower mobility than electrons.

The transistor structure differs from the conventional one mainly in that floating P-well with controlled doping profile is employed. It is also used as photo-sensing element of the pixel. At the same time, under different bias conditions, this same transistor can be operated to perform integration, readout and reset.

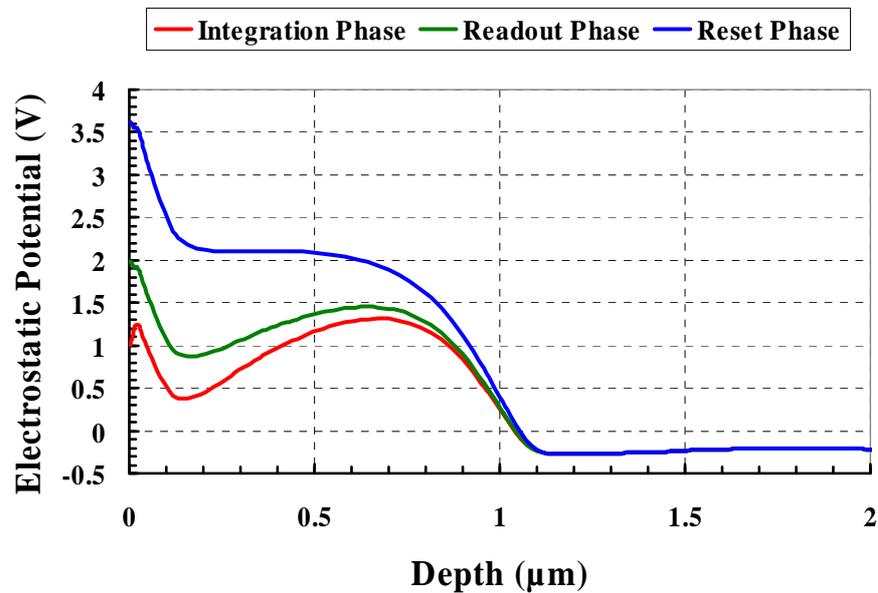
In the integration phase, a low voltage level is applied to the gate of the transistor to turn it off. The floating body of the transistor exhibits a potential valley for collecting and storing holes (red curve in Figure 1). The pixel being under illumination, light penetrates through the gate and is absorbed in the transistor body. There is separation of photo-generated electron-hole pairs due to built-in electrical field in the body. The electrons are swept away mainly to the V_{dd} -connected drain, while the holes are collected and accumulated in the potential valley. The stored holes raise the potential of the transistor body, which leads to a decrease of the transistor threshold voltage V_{th} [6].

In the readout phase, the transistor is switched on by applying a gate voltage higher than the maximum V_{th} corresponding to the dark conditions. The potential valley becomes shallower with shrink of charge-storage region under the transistor gate (green curve in Figure 1). The transistor in this phase is operated as a source follower with fixed gate and drain voltages. The decrease of V_{th} reflecting the amount of the stored charge is sensed as an increase of the transistor's effective gate-source voltage. Accordingly, the drain current and the output source voltage increase. The source voltage in this period can be readout by sampling.

For the reset of the pixel, a still higher voltage is applied to the transistor gate. At the same time, the source voltage is clamped to the drain voltage to minimize channel current. The potential valley

disappears and the stored holes are pushed away to the substrate because the transistor body potential near the silicon surface is so substantially increased that the potential becomes monotonic decreasing (blue curve in Figure 1).

Figure 1. Potential profile of the transistor body.



The operation of the 1T pixel can be verified by simulations using ISE TCAD tools, as is shown in Figure 2. The biasing conditions of the transistor are indicated in Table 1.

Figure 2. Simulations of the 1T pixel using ISE TCAD tools to verify its operation in different phases.

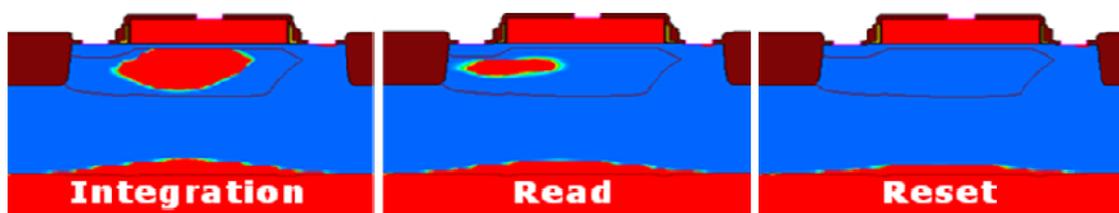


Table 1. Biasing conditions of the pixel transistor.

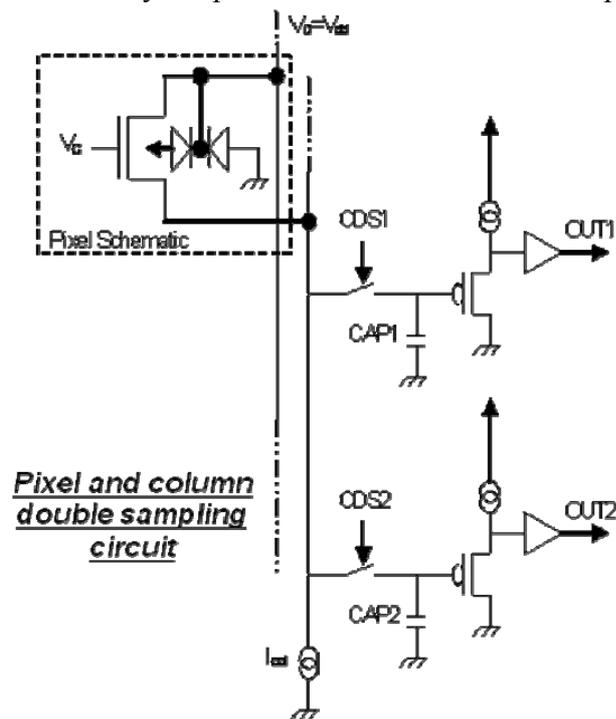
	V_D	V_G	V_S
Integration	3.3 V	~ 0 V	3.3 V
Readout	3.3 V	~ 2 V	Connection to load
Reset	3.3 V	3.3 V	3.3 V

One feature of this 1T pixel is its reset mode with depletion of the storage zone does not generate kTC noise. Thus there is no need to employ CDS (correlated double sampling). Instead, rapid simple

non-correlated double sampling is suggested (see Figure 3) to suppress V_{in} dispersion and thus to reduce FPN (fixed pattern noise). It is more efficient in reducing low-frequency noise.

One should notice that in readout mode, some stored holes are displaced under the source due to shrink of charge storage region under the gate and source potential lowering. This shift of the charge storage region to the source and toward the pixel edge should be stopped to avoid electrical crosstalk. One solution to the problem is to employ STI (shallow trench isolation), as shown in Figure 2. It was adopted in our first design configuration.

Figure 3. Readout by simple non-correlated double sampling.



3. Modeling and Model Validation

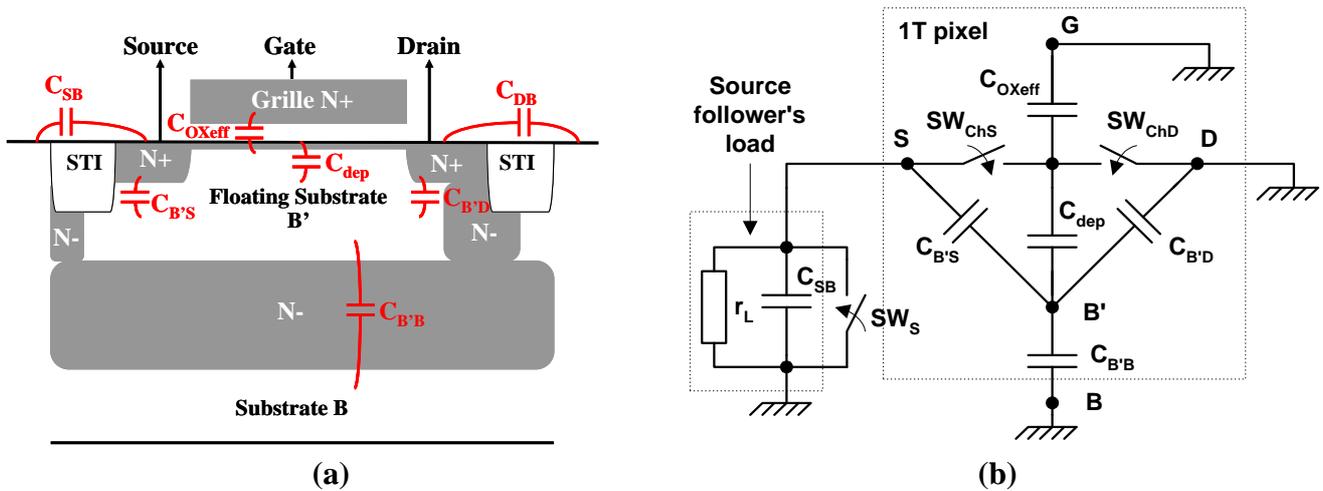
3.1. Model Description

For optimizing performances of the 1T pixel, we have built a model allowing determination of linear conversion characteristics such as conversion gain (CG). The modeling approach is described as follows.

The first step is to consider the capacitances of the pixel structure and to establish an ac equivalent circuit for estimating the total capacitance of the transistor's floating body. It is this capacitance that plays the role of charge storage and determines the relationship between stored holes and the potential of the floating body. Figure 4a shows the pixel structure with inherent capacitances. The pixel transistor has, beside its drain, gate, source and bulk having external connections, two internal nodes: its channel C and its floating body B' where holes can be stored in integration and readout modes. Figure 4b presents the corresponding ac equivalent circuit for both integration and readout operations. It does not include drain-ground and gate-ground capacitances because they are short-circuited by bias voltages. The switching positions of $S_{W_{ChS}}$, $S_{W_{ChD}}$ and S_{W_S} of the equivalent circuit depend on the operating modes. In integration mode, as the transistor is off, both $S_{W_{ChS}}$ and $S_{W_{ChD}}$ are thus open. In

readout mode, SW_{ChS} and SW_{ChD} are closed because the transistor is on (in saturation). It may look oversimplifying to assume the same potential for the source, the channel and the drain, but the situation is that the channel resistance of the on-state transistor is negligible ($\sim 10^6 \Omega$) compared to the impedances of the in-pixel capacitances ($\sim 10^{10} \Omega$) at operating frequencies, and that C_{Oxeff} is effectively “short-circuited” by at least half of the channel resistance in parallel with it. Another way to see it is that the channel resistance imposes the C node to much lower impedance, like a “shield” to prevent effect of C_{Oxeff} . For SW_S , it is open only in readout mode.

Figure 4. (a) 1T pixel structure with indication of capacitances. (b) Its ac equivalent circuit.



From the equivalent circuit of Figure 4b, the total capacitance of the floating body B' , denoted $C_{B'}$, can be written as:

$$C_{B'} = \begin{cases} \frac{C_{Oxeff} C_{dep}}{C_{Oxeff} + C_{dep}} + C_{B'S} + C_{B'D} + C_{B'B} & (Integration) \\ C_{dep} + C_{B'S} + C_{B'D} + C_{B'B} & (readout) \end{cases} \quad (1)$$

It should be noted that in reset mode, when the stored charges are (normally) completely evacuated, $C_{B'}$ can be considered to be short-circuited. What is more important is readout-mode $C_{B'}$, because it is related to the readout-determined conversion gain (CG) of the pixel, which will be expressed in (7).

The next step is to determine the pixel’s linear conversion characteristics. The following describes how the conversion gain is determined. It is defined as:

$$CG = \frac{\Delta V_{pix}}{\Delta N_{ch}} = \frac{1}{q} \frac{\Delta V_{pix}}{\Delta Q_{ph}} \quad (2)$$

where V_{pix} is the pixel output voltage, N_{ch} the number of the collected photo-generated charges being stored in the pixel’s integration capacitance, and Q_{ph} the quantity of the stored charges. For this 1T pixel, the integration capacitance is no other than $C_{B'}$. Thus the conversion gain can be expressed as:

$$CG = \frac{1}{q C_{B'}} \frac{\Delta V_{pix}}{\Delta V_{B'}} \quad (3)$$

On the other hand, a variation of floating body potential (due to stored charges) will induce a shift of the transistor’s threshold voltage V_{th} , which can be seen from the following relationship [7]:

$$V_{tn} = \Phi_{MS} - 2\Phi_F - \frac{\sqrt{2\varepsilon_0\varepsilon_{Si}qN_{B'}(2\Phi_F + V_{B'} - V_S)}}{C_{OXeff}/A_G} - \frac{Q_{ox} + Q_{shal}}{C_{OXeff}/A_G} \quad (4)$$

where Φ_{MS} is the work-function difference, $2\Phi_F$ is the surface inversion potential (which is 2 times the difference between the Fermi level of the substrate and intrinsic silicon), $N_{B'}$ the doping concentration of the transistor's (floating) body, $V_{B'}$ the floating-body potential, V_S the transistor's source potential, C_{OXeff} the effective gate-oxide capacitance, A_G the effective gate area, Q_{ox} the oxide charge density and Q_{shal} the shallow-implant charge density.

The derivative of V_{tn} with respect to $V_{B'}$ gives:

$$\Delta V_{tn} = -\frac{A_G}{2C_{ox}} \sqrt{\frac{2\varepsilon_0\varepsilon_{Si}qN_{B'}}{2\Phi_F + V_{B'} - V_S}} \Delta V_{B'} = -\frac{C_{dep}}{C_{ox}} \Delta V_{B'} \quad (5a)$$

with:

$$C_{dep} = \frac{A_G \varepsilon_0 \varepsilon_{Si}}{X_{dep}} \quad (5b)$$

and:

$$X_{dep} = \frac{\sqrt{2\varepsilon_0\varepsilon_{Si}(2\Phi_F + V_{B'} - V_S)}}{qN_{B'}} \quad (5c)$$

where X_{dep} is the depletion-layer thickness between the transistor's channel and its floating body. It can be seen from (5) that increasing the floating body potential causes a lowering of the threshold voltage.

As the transistor in readout mode is biased with a constant gate voltage, and the drain current is function of $(V_G - V_S - V_{tn})$, a decrease of V_{tn} amounts to an equivalent increase in V_G , i.e. $-\Delta V_{tn} = \Delta V_G$. Then, according to the source follower operation, we have:

$$\Delta V_{pix} = \Delta V_G A_v = -\Delta V_{tn} A_v \quad (6)$$

where A_v (~ 0.9) is the source follower's voltage gain.

From (3), (5) and (6), we can rewrite the conversion gain as:

$$CG = \frac{qA_v C_{dep}}{C_{OXeff} C_{B'}} \quad (7)$$

Finally this model may integrate models of involved parameters. For example, C_{dep} in the above expression is related to the silicon surface potential, which in turn depends on properties of gate oxide and Si/SiO₂ interface. We have modeled C_{dep} based on analytical descriptions in [8, 9]. This has enabled us to analyze effects of process parameters.

It should be mentioned that capacitances in the silicon are voltage-dependent, especially when they result from lightly-doped regions, such as $C_{SB'}$, $C_{B'D}$ and $C_{B'B}$. It implies that the total capacitance $C_{B'}$ may vary with the floating body potential. Consequently, the conversion linearity may degrade. However, as will be seen in the following subsection, $C_{SB'}$, $C_{B'D}$ and $C_{B'B}$ are much smaller than C_{dep} . This means that $C_{B'} \approx C_{dep}$. We obtain thus a simplified expression of CG:

$$CG \approx \frac{qA_v}{C_{OXeff}} \quad (8)$$

The above expression does not include capacitances in the silicon. Therefore, there are no significant effects of stored charges and induced potential variations on CG. The estimated linearity error of conversion is about 2%.

The expression (8) allows rough estimation of CG. It predicts (especially for process optimization) that CG may be improved by increasing the gate-oxide thickness t_{ox} .

3.2. Extraction of Parameters

Calculating CG needs prior determination of the involved parameters in its expression. Via simulations using ISE TCAD tools, we can extract geometrical parameters to evaluate the pixel structure's inherent capacitances. Figure 5 shows one simulation example of the pixel structure operated in readout phase. Table 2 gives expressions of parameters and extracted values for a 2.2 μm -pitch 1 T pixel.

Figure 5. Simulated 1T pixel structure in readout phase with indication of parameters.

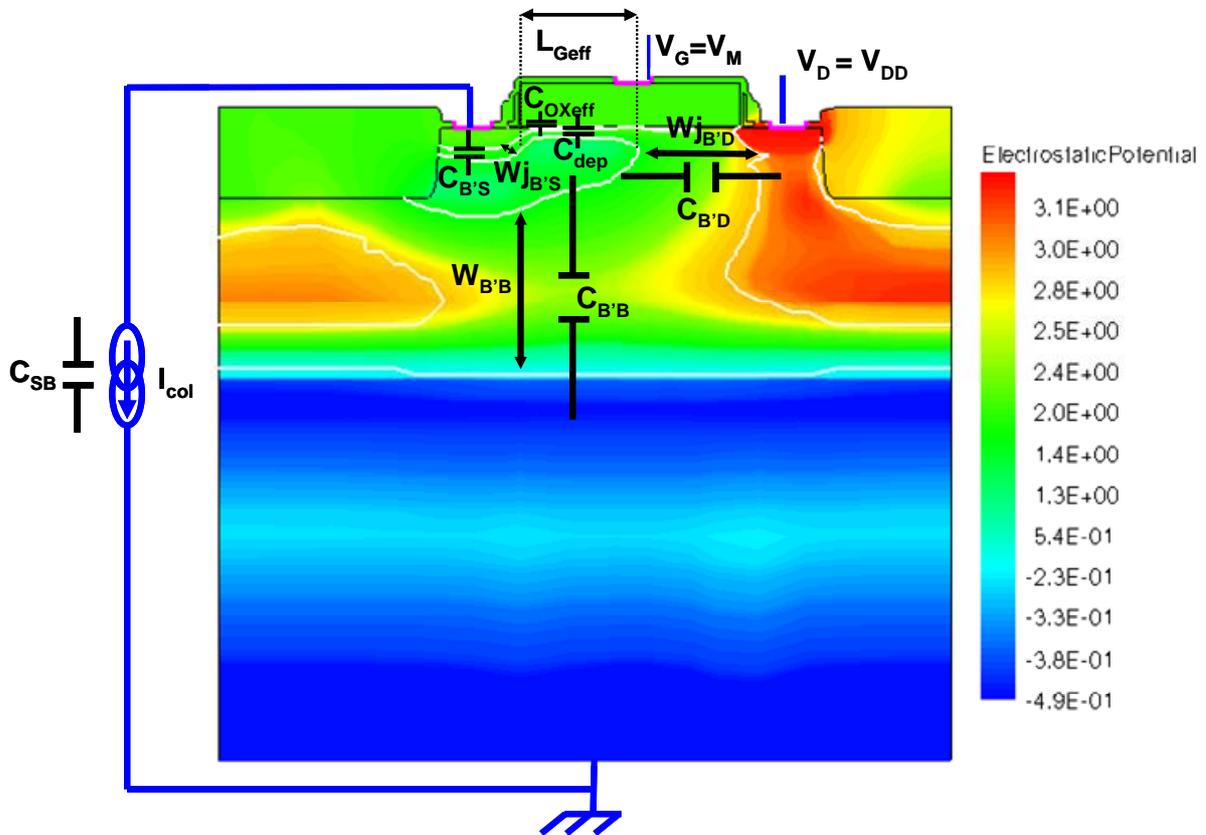


Table 2. Expressions of parameters and evaluated values for a 2.2 μm -pitch 1 T pixel.

Parameter	Expression	Value
A_G	$A_G = L_{Geff} \times W_{Geff}$	$0.62 \mu\text{m}^2$
C_{OXeff}	$C_{dep} = \frac{A_G \epsilon_0 \epsilon_{ox}}{t_{ox}}$	3.28 fF
C_{dep}	$C_{dep} = \frac{A_G \epsilon_0 \epsilon_{Si}}{X_{dep}}$	1.82 fF

Table 2. Cont.

$C_{B'D}$	$C_{B'D} = \frac{A_{j_{B'D}} \cdot \epsilon_0 \cdot \epsilon_{si}}{W_{j_{B'D}}}$	0.019 fF
$C_{B'S}$	$C_{B'S} = \frac{A_{j_{B'S}} \cdot \epsilon_0 \cdot \epsilon_{si}}{W_{j_{B'S}}}$	0.60 fF
$C_{B'B}$	$C_{B'B} = \frac{A_{G_{eff}} \cdot \epsilon_0 \cdot \epsilon_{si}}{W_{B'B}}$	0.081 fF
$C_{B'}$	$C_{B'} = C_{dep} + C_{B'S} + C_{B'D} + C_{B'B}$	2.52 fF

This example shows that the 1T pixel structure has $C_{oxeff} \gg C_{dep} \gg C_{SB'}, C_{B'D}, C_{B'B}$.

3.3. Model Validation

We have performed model validation by comparing model predictions with measured results in parametrical analysis. Figure 6a presents the layout of 3 pixel sizes: 2.2 μm pitch, 1.7 μm pitch and 1.4 μm pitch. Figure 6b shows the 3 simulated pixels (allowing extraction of geometrical parameters). The evaluated effective gate area $A_G (= L_{Geff} \times W_{Geff})$ for these pixel sizes is 1.15 μm^2 , 0.322 μm^2 and 0.161 μm^2 respectively. Figure 6c compares calculated and measured results on CG as a function of A_G . Both aspects of results show an increase of CG when scaling down the pixel. However, this increase is much slower than what predicts the scaling law, according to which CG would be inversely proportional to the pixel area. This comparison of results shows that the prediction from the model is fairly accurate. The fact of some involved capacitances that scale slowly may account for this CG evolution.

Figure 6. (a) Layout of three pixels in different sizes: 2.2 μm pitch, 1.7 μm pitch and 1.4 μm pitch. (b) Simulated structures of the three pixels. (c) Conversion gain against effective gate area.

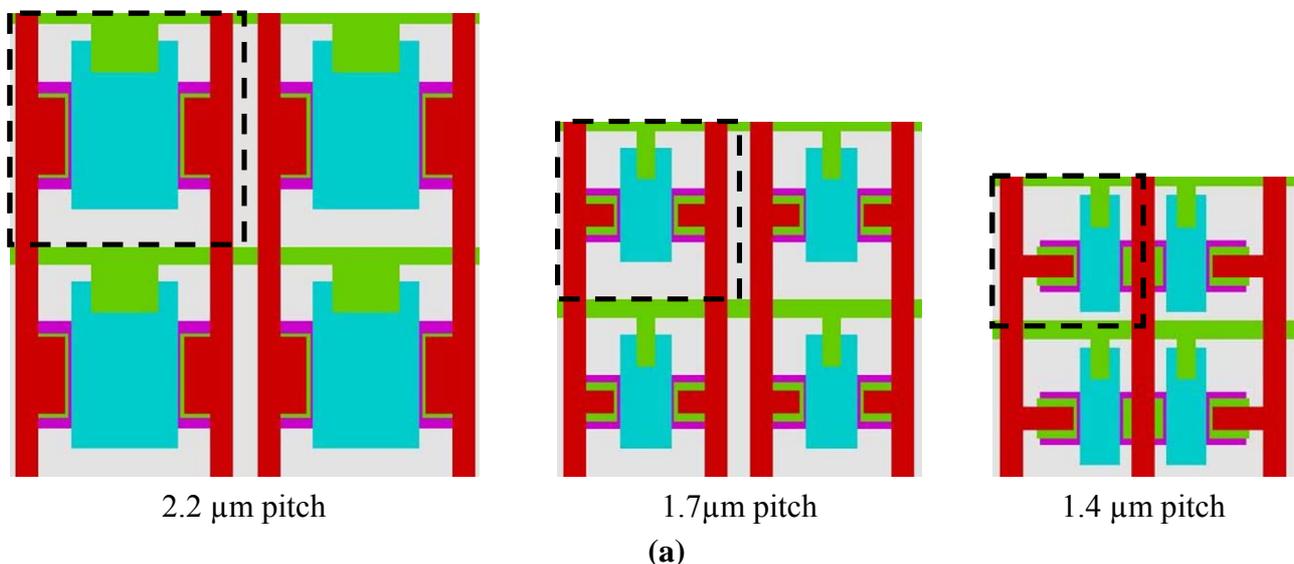


Figure 6. Cont.

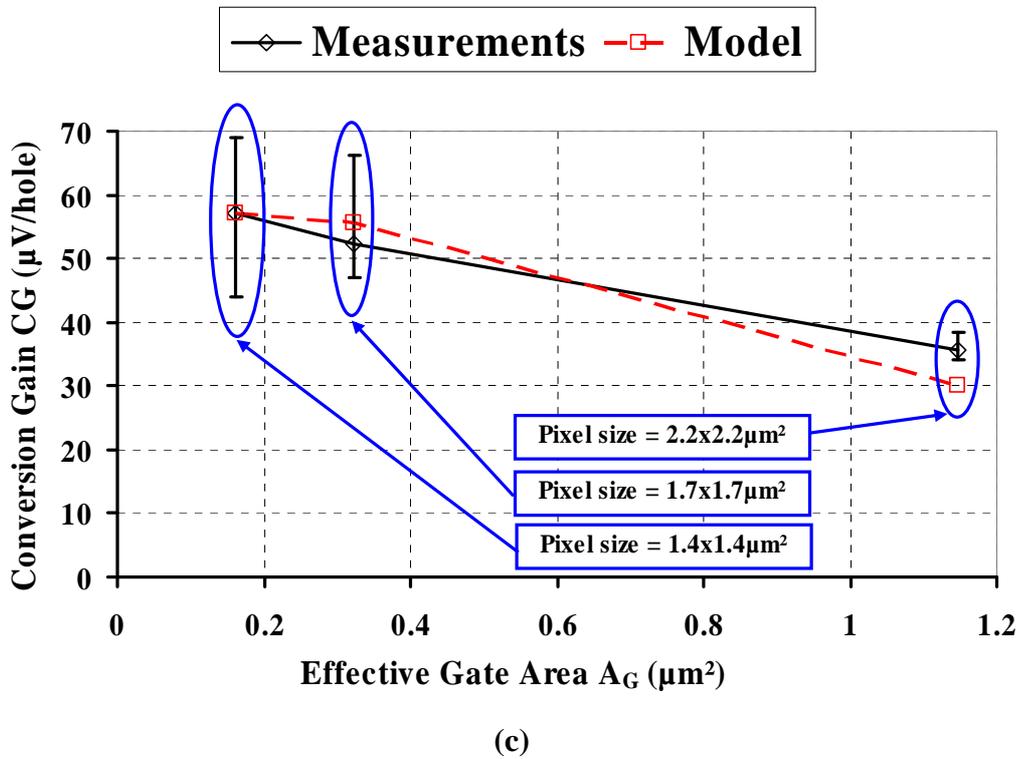
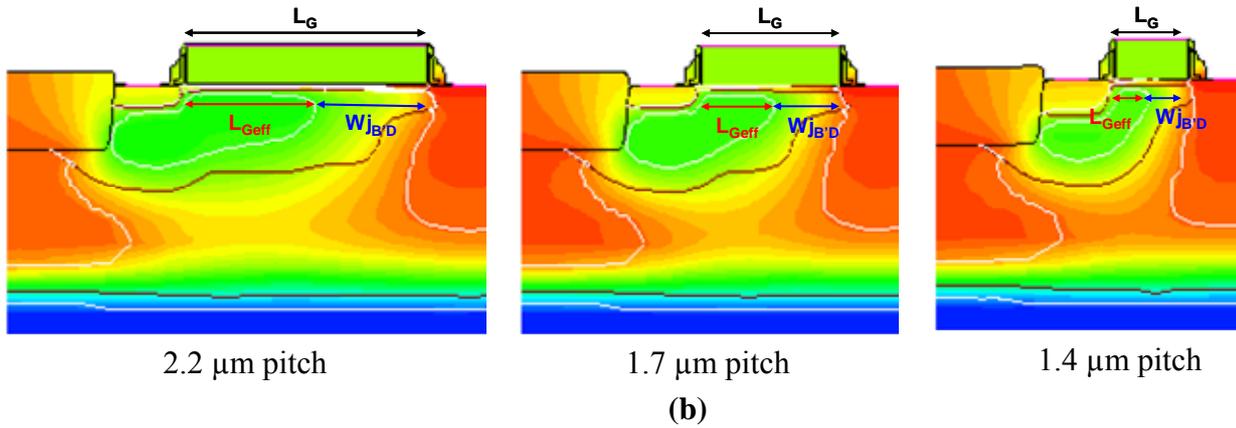
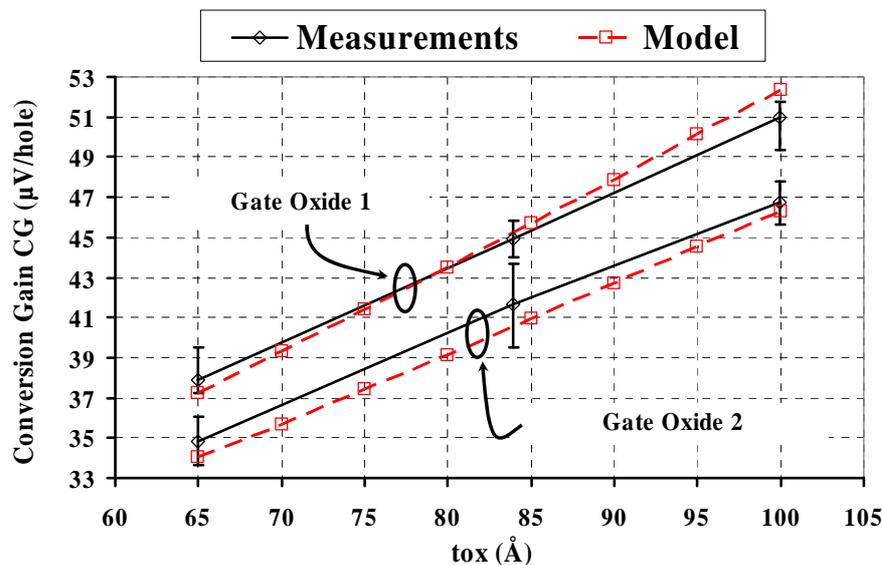


Figure 7 plots calculated and measured results on CG versus gate-oxide thickness: $t_{ox} = 65 \text{ \AA}$, 84 \AA and 100 \AA respectively. Two configurations of oxidation process are compared: one is oxidation plus nitridation (gate oxide 1), and the other is oxidation only (gate oxide 2). It has been reported [10, 11] that gate-oxide nitridation leads to a much higher density of Si/SiO₂ interface traps. The charged interface states induces a shift of surface potential, which causes C_{dep} to change. Accordingly CG may alter. The observed agreement between model prediction and experimental measurements confirms the validity of the model.

Figure 7. Conversion gain versus gate oxide thickness for two configurations of oxidation process: oxidation with nitridation (gate oxide 1) and oxidation only (gate oxide 2).



4. Implementation Configurations

Conventional design of the 1T pixel is the rectangular-gate configuration, as shown in Figure 6a. Implementing the 1T pixel in rectangular-gate configuration has minimized transistor size. However as already mentioned, to avoid electrical crosstalk we should employ STI. This solution unavoidably increases pixel size. Moreover, it also increase significantly the pixel dark current, because of increased silicon surface depletion areas, where dark-current generation is a major contribution [12].

Another way of designing 1T pixel is a ring-gate configuration, with source at the center and peripheral drain (shown in Figure 8a). This time the readout-induced shift of the charge-storage region goes to the pixel center, which does not raise crosstalk problems. Thus there is no need to employ STI. The floating body of the transistor is shielded by a deep buried N-type layer and N peripheral region below the drain (see Figure 8b). The surrounding drain and the non-depleted N-peripheral region underneath in the peripheral pixel area also play the role of pixel isolation. This STI suppression allows not only smaller pixel size and/or fill-factor improvement, but also substantial reduction of surface dark current component.

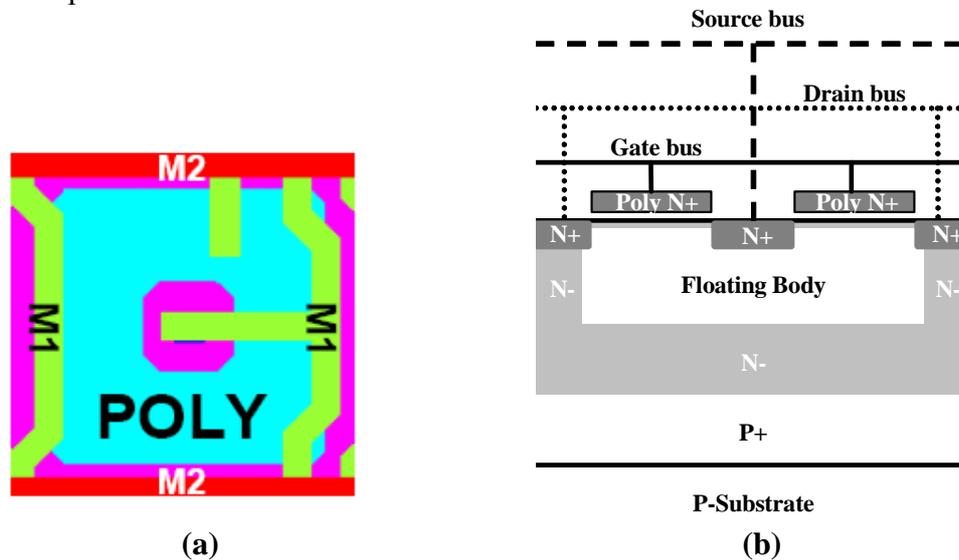
At the fabrication process level, we have implemented several configurations on test chips with variations of parameters, with the aim of both model validation (subsection 3.3.) and optimization of pixel characteristics. This includes:

- increasing gate-oxide thickness to enhance CG;
- gate oxidation with and without nitridation (gate oxide 1 and gate oxide 2) to choose one with better noise performance.

As gate-oxide nitridation may induce much more interface traps, a higher level of low-frequency noise in the MOS transistor is predicted. The interface-trap-related noise includes RTS (Random Telegraph Signal) noise and 1/f noise due to both carrier-trap (ΔN) and charge-scattering ($\Delta\mu$) effects [13-15]. The low-frequency noise is becoming an important issue for CMOS image sensors (CIS) as

the size of transistor components continues to shrink [16]. It may have dominant contribution to pixel read noise, and thus should be taken into account in the choice of oxidation parameters.

Figure 8. Ring-gate design of the 1 T pixel structure in a 0.13 μm CMOS process & 90 nm copper-based process. (a) 1.4 μm -pitch pixel layout. (b) Cross-section view of the implemented pixel structure.



It should be mentioned that stored holes in the pixel transistor's floating body will not communicate with interface traps, and that the main noise effect of these traps is resulting fluctuations of the transistor drain current when it is in readout mode.

5. Pixel Characteristics

Measurements of test chips have been made to estimate impacts of oxidation process parameters on CG (shown in Figure 7) and on temporal noise. Temporal noise of the pixel structure has been evaluated by measuring its output fluctuations in dark conditions with short integration duration, so as to neglect dark-current-contributed shot noise. The measured results shown in Table 3 confirm noise lowering with the increase of t_{ox} , because increasing t_{ox} will enhance CG, and thus lead to lower equivalent noise. On the other hand, the observed difference of noise levels between oxidation with and without nitridation indicates that interface-trap-induced noise is a main temporal noise source.

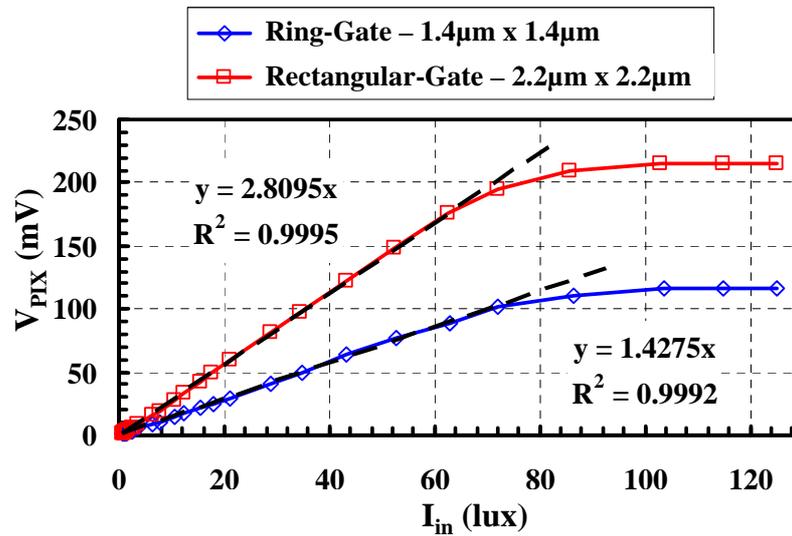
Table 3. Temporal noise (in equivalent holes) corresponding to different oxidation process parameters.

t_{ox}	65 Å	84 Å	100 Å
Ox + Ni (gate oxide 1)	5.1 h^+	4.9 h^+	4.8 h^+
Ox only (gate oxide 2)	4.5 h^+	4.1 h^+	4.0 h^+

Figure 9 shows two photo-conversion transfer characteristic curves, corresponding to a 2.2 μm -pitch rectangular-gate pixel and a 1.4 μm -pitch ring-gate pixel respectively. From the photoelectric

conversion characteristic curve $V_{pix}(I_{in})$, several performance aspects can be evaluated: the first portion of the curve before saturation determines the sensitivity and the linearity, while the saturation level indicates the full-well capacity (FWC).

Figure 9. Photo-conversion transfer characteristic curves of two design configurations: 2.2 μm -pitch rectangular-gate pixel and 1.4 μm -pitch ring-gate pixel respectively.



The sensitivity corresponds to the slope of the curve divided by the integration time t_{int} :

$$S = \frac{1}{t_{int}} \frac{\Delta V_{pix}}{\Delta I_{in}} \quad (9)$$

It can be shown to be geometry-dependent, and proportional to the pixel's sensing surface area as well as its conversion gain. Table 4 presents measured sensitivity of different design configurations. The obtained results show that:

- pixel shrink will lead to rapid degradation of sensitivity;
- for a given pixel size the ring-gate configuration has better sensitivity than the rectangular-gate one.

Table 4. Different design configurations and their sensitivity evaluated by measuring test chips.

	Pixel size (μm^2)	Fill factor	Sensitivity ($\text{h}^+/\text{lux.s}$)
Rectangular-gate	$2.2 \times 2.2 = 4.84$	46%	1840
Rectangular-gate	$1.7 \times 1.7 = 2.89$	40%	550
Rectangular-gate	$1.4 \times 1.4 = 1.96$	34%	290
Ring-gate	$1.4 \times 1.4 = 1.96$	50%	590

Table 5 compares characteristics of two fabricated CIS test chips, one integrating an array of 2.2 μm -pitch rectangular-gate pixels [17], and the other an array of 1.4 μm -pitch ring-gate pixels [18]. The pixel fabrication process requires only three extra masks for specific implants and is fully compatible with the CMOS digital process.

Table 5. Comparison of measured characteristics between the 2.2 μm -pitch rectangular-gate pixel and the 1.4 μm -pitch ring-gate pixel.

Parameter	2.2 μm -pitch rectangular-gate	1.4 μm -pitch ring-gate	Testing conditions
Process	0.13 μm 1 P 4 M CMOS	0.13 μm FE + 90 nm BE 1P 3M CMOS	
Test chip size	3.2 mm \times 3.2 mm	3.0 mm \times 3.2 mm	
Pixel size	2.2 μm \times 2.2 μm	1.4 μm \times 1.4 μm	
Number of Pixels	CIF (352 \times 288)	VGA (672 \times 512)	
Fill factor	46 %	50 %	Without microlens
Supply voltage	1.2 V / 3.3V	1.2 V / 3.3 V	
Conversion gain	35 $\mu\text{V}/\text{h}^+$	58 $\mu\text{V}/\text{h}^+$	
Full well capacity	6200 h^+	2000 h^+	
Dark current	500 h^+/s	39.7 h^+/s	Mean value @ RT
Pixel temporal Noise	6 h^+	2.4 h^+	In darkness
Pixel Dark FPN	39.5 h^+	4.3 h^+	Without additional correction circuit
Noise floor	40 h^+	4.9 h^+	Temporal noise, FPN & DSNU in darkness
Dynamic range	44 dB	52 dB	Usable Well over Noise floor
Sensitivity	1840 $\text{h}^+/\text{lux}\cdot\text{s}$	590 $\text{h}^+/\text{lux}\cdot\text{s}$	B/W sensitivity without microlens Halogen 3200 K IR cut off 650 nm

The 1.4 μm -pitch ring-gate pixel has improved characteristics compared to its 2.2 μm -pitch rectangular-gate counterpart:

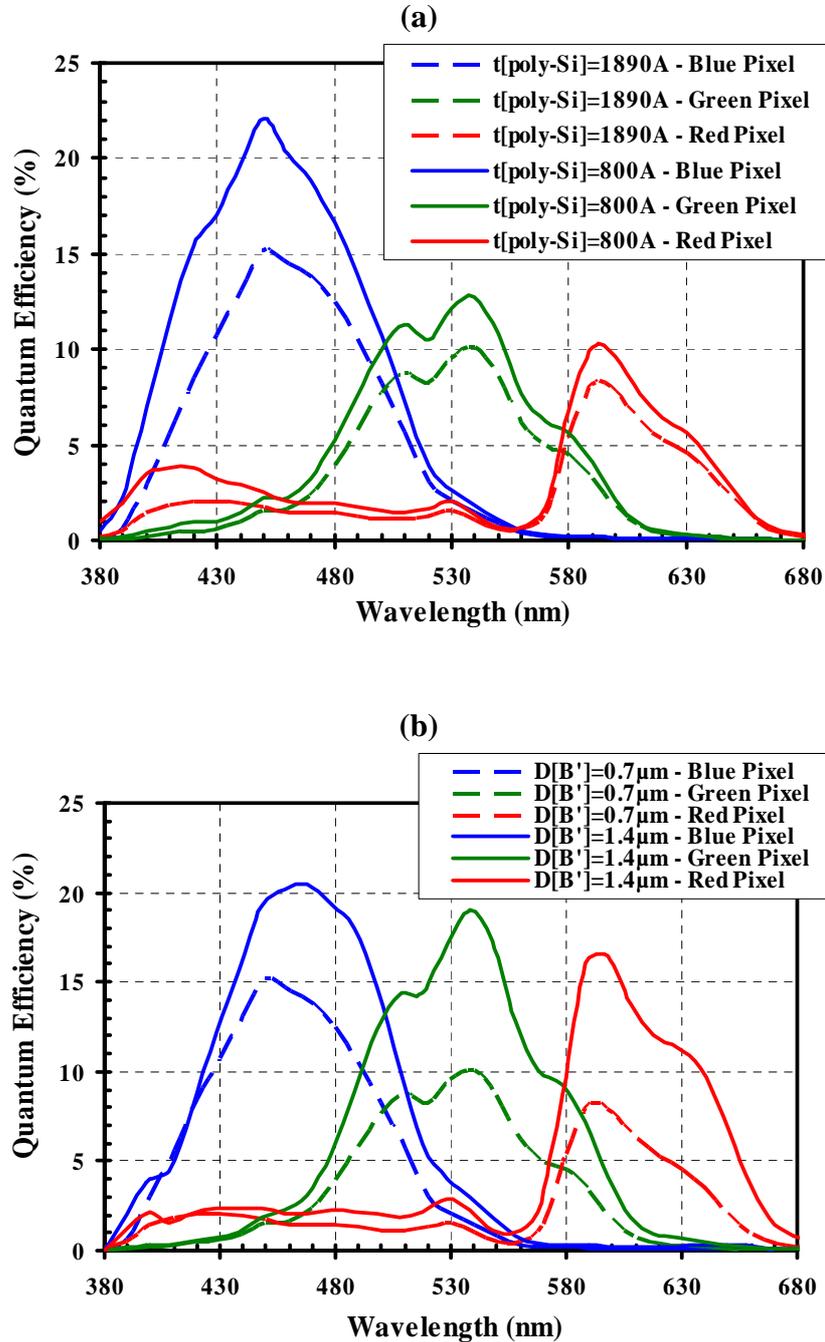
- smaller size for a comparable fill factor, mainly because STI is not employed;
- larger CG, because of smaller size;
- much lower dark current thanks to STI suppression, smooth-shape layout and smaller size;
- lower temporal noise, partly because of CG improvement;
- much lower Dark FPN (Fixed Pattern Noise, which may in large part be due to dark current), thanks to dark current reduction;
- larger dynamic range, because improved signal-to-noise ratio outweighs FWC degradation.

The 1.4 μm -pitch pixel has also degraded performances:

- lower FWC, because of smaller size and ring shape of the charge-storage region [19];
- poorer sensitivity, due to size reduction.

The above comparison between the two design configurations shows that some performance aspects can substantially be enhanced by the use of appropriate design techniques. It is, however, a challenging task to preserve and/or improve FWC and sensitivity when reducing pixel size. Methods of improvements include optimization of process and bias parameters. Figure 10 presents two examples of quantum-efficiency (QE) improvement: employing thinner Poly-Si gate to reduce short-wavelength absorption loss (Figure 10a), and enlarging charge-collecting region by implant optimization (Figure 10b).

Figure 10. Simulated results on the pixel quantum efficiency (with color filters) for: (a) a poly-gate $t_{poly-si} = 800 \text{ \AA}$ (solid curves) compared to $t_{poly-si} = 1890 \text{ \AA}$ (dash curves); (b) charge-collecting region centered at depth $D_B = 1.4 \mu\text{m}$ (solid curves) instead of $D_B = 0.7 \mu\text{m}$ (dash curves).



FWC of the 1T pixel may be improved by lowering V_m of the transistor via shallow channel implant, so as to widen the gate-bias-voltage difference between reset and readout modes (i.e. $V_G^{Rst} - V_G^{Rd}$). As can be seen from Figure 1, V_G^{Rd} should be low enough for obtaining a potential valley with a certain depth, and V_G^{Rst} should be high enough to sweep away completely stored holes. Decreasing V_m leads to the decrease of V_G^{Rd} , which means an increase of the term $(V_G^{Rst} - V_G^{Rd})$. Another way of increasing the term $(V_G^{Rst} - V_G^{Rd})$ is to consider possible higher supply voltages (for the thick-gate-oxide pixel). It should be noted that rectangular-gate configuration cannot benefit from this

supply-voltage relaxation because of early appearance of band-to-band tunneling effect [17]. Ring-gate configuration, on the other hand, seems to withstand a higher supply voltage without sharp increase of dark current.

Via implant control, the potential profile of the pixel transistor can be optimized to increase the depth of the potential valley in readout mode, but this will also increase difficulties to ensure complete evacuation of stored holes in reset phase. It should be mentioned that V_G is not the only controlling voltage: the perimeter of the charge-storage region depends on the transistor bias voltages V_S , V_G and V_D . Especially V_S has a more efficient control than V_G , with:

$$\frac{\partial W_{jB'S}}{\partial V_S^{Rst}} \gg \frac{\partial X_{dep}}{\partial V_G^{Rst}} \quad (10)$$

Thus, combining optimization of bias and implant parameters may be an effective approach for FWC improvement.

6. Conclusions

We have proposed a floating-body MOSFET as a single pixel component. It can be operated as photo-sensing device and source-follower transistor, with charge storage and charge evacuation via bias control. Our investigation into this 1T pixel structure includes modeling and model validation, implementation and characterization.

The pixel structure has been modeled by establishing an equivalent circuit, which allows analytical description of the pixel's linear conversion characteristics. The relationship of the conversion gain with key parameters has thus been determined. The involved parameters have also been modeled and integrated in the device model to allow parametrical analysis. Model validation has been done by comparing theoretical predictions and experimental results.

The proposed pixel structure has been designed in rectangular-gate and ring-gate configurations. Due to stored charges moving toward the transistor's source, the former requires the use of STI to avoid electrical crosstalk, while the latter with the transistor's source at the pixel center suppresses this need. The implemented configurations on test chips include variations of oxidation process parameters for model validation and performance optimization.

The obtained results confirm that reducing pixel size improves conversion gain, but degrades full well capacity. Ring-gate pixel design has much lower dark current than the rectangular-gate counterpart, mainly thanks to STI suppression and smooth-shape layout. Moreover, the ring-gate pixel has lower noise and much lower dark FPN. Dark FPN may largely be contributed by dark current. The dynamic range for the ring-gate pixel is larger, meaning that signal-to-noise ratio outweighs FWC degradation. However, the sensitivity, like FWC, is also degraded in the same proportion. Possible improvements of performances include optimization of process and bias parameters.

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