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A Flexible Experimental Laboratory for Distributed Generation Networks Based on Power Inverters

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Abstract: In the recently deregulated electricity market, distributed generation based on renewable sources is becoming more and more relevant. In this area, two main distributed scenarios are focusing the attention of recent research: grid-connected mode, where the generation sources are connected to a grid mainly supplied by big power plants, and islanded mode, where the distributed sources, energy storage devices, and loads compose an autonomous entity that in its general form can be named a microgrid. To conduct a successful research in these two scenarios, it is essential to have a flexible experimental setup. This work deals with the description of a real laboratory setup composed of four nodes that can emulate both scenarios of a distributed generation network. A comprehensive description of the hardware and software setup will be done, focusing especially in the dual-core DSP used for control purposes, which is next to the industry standards and able to emulate real complexities. A complete experimental section will show the main features of the system.

Keywords: distributed generation; power inverter; microgrid; voltage sag; reactive current injection; laboratory setup

1. Introduction

In the deregulated electricity market a huge quantity of small renewable power sources, mainly photovoltaic and wind systems, but also conventional cogeneration, microturbines and advanced storage systems such as fuel cells, are being connected to the main grid [1]. The conventional architecture of an inverter-based distributed generation network is shown in Figure 1. As it can be seen, loads are also distributed and can be purely power consumers or consumers/generators (i.e., a private residence/facility with photovoltaic panels that presents a positive net consumption during certain periods of the day and negative consumption during other periods). In addition, the loads can present some degree of intelligence used to adapt its power demand depending on local measures or remote commands. In this sense, a challenging and attractive load form is the plug-in electric vehicle charged from residential distribution feeders, which can be used also to store energy and other ancillary purposes [2,3]. Thanks to the advances in power electronics, high performance power converters are commonly used as interface between the generation sources and the grid. Thus, the set formed by a power source and its power converter can be called distributed generation source (DGS), and it can be connected or disconnected to the whole network. These converters are locally governed in order to manage the power sources generation to its optimum and to fulfill the increasingly stringent rules of the applicable grid codes and standards [4–6]. In addition, they must be managed

by a dedicated central controller or by a distributed control system to optimize the overall power generation. Thus, a communication channel, dedicated or public, will be normally present.

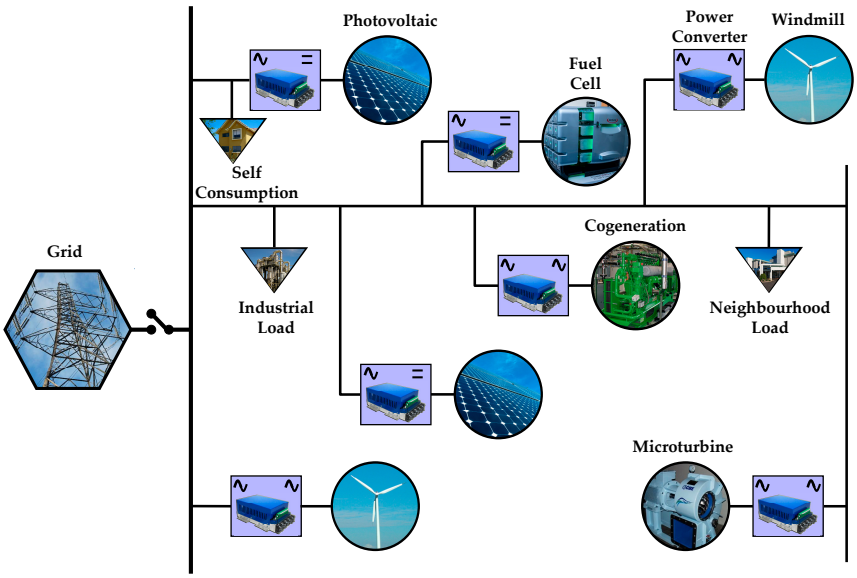

Figure 1. Distributed generation network connected to the main grid through a power switch.

The distributed network is connected to/disconnected from the main grid through a main power switch [7]. In the first (connected) case the power flow can be from or to the grid depending on the power generation/consumption on the distributed network. This is the simplest scenario because the main grid is considered ideal and infinite in terms of power generation/consumption. In this case the grid is responsible for regulating the voltage, following power quality standards [4]. The main grid management system will decide the amount of power that needs to be generated and where it must be generated. The communication channel between the management system and the network nodes provides the control commands to the nodes and receives the local generation data from the nodes. When the power sources can adjust its power output to a desired value (dispatchable sources, e.g., a gas microturbine) they will generate the amount of active/reactive power decided by the central controller taking into account different weight factors such as power costs, system efficiency, pricing schedules, etc. Related to renewable sources like windmills and photovoltaic panels (i.e., non-dispatchable sources) the central controller can only adjust its active and reactive power generation set-point up to a certain limit. Normally, in the grid connected mode the nodes act as voltage followers (voltage fixed by the main grid), thus working as controlled current sources or network-feeding converters [8]. For a correct operation of the network-feeding sources it is required that the grid presents a well-regulated voltage. In this way, when the grid voltage suffers disturbances, the DGS must be controlled accordingly [4]. The highly distributed nature of the DGS must be seen as an opportunity to collaboratively alleviate power quality disturbances. Thus, grid codes and standards propose different protocols for DGS during disturbances, mainly related to low-voltage ride-through (LVRT) and reactive current injection (RCI) [5,6]. In grid codes, the stringent requirements on LVRT and RCI during voltage sags [9] are a promising and profitable research field that must be taken into account [10–14].

On the other case, when the distributed network is isolated, and depending on the number of generation and consumption nodes, this scenario can be generally named a microgrid (μG) [15–17]. Due to the absence of external energy interchanges, in an isolated system the net power must be zero, i.e., power generation must be the as consumption. Thus, an efficient μG power control and power-quality control (centralized or distributed) must be present to manage and equalize the

distributed generation and, no less importantly, to ensure meeting quality standards. In this way, at least one DG must act as voltage source with the aim of maintain the voltage and power quality as the main grid does in a grid connected network. Thanks to its power-generation controllable nature, the dispatchable DGS can be programmed to work as voltage sources, or network-forming converters [8]. Of course, the non-dispatchable sources can be also present in this configuration but working as network-feeding nodes, which are seen as negative loads (providing power instead of consuming it). The remaining power required by the network loads must be provided cooperatively by the dispatchable sources. The droop method is one of the most promising control schemes for connecting multiple voltage sources that share the load and maintain the voltage quality of an islanded μG [18,19]. This control is based in three hierarchical levels: local primary control to ensure load sharing between inverters through the deviation of the voltage amplitude and frequency; communication based secondary control to restore the voltage and frequency to nominal values; and agent based tertiary controller for overall energy optimization issues. The two main drawbacks of the droop method are, first, the reduction of the power quality due to the voltage amplitude and frequency deviation, and second, the requirement of a communication channel to restore the perturbed power quality. An interesting recent work based on the well-known consensus technique proposes the μG control without using droop method [20]. Secondary control has also been a hot research issue in recent years, focused mainly on avoiding the use of the common one-to-all communication centralized controller [21–26]. In this way different works deal with avoiding the use of communications between nodes [24–26]. All these works try to guarantee perfect power quality restoration, while providing robustness, reliability and redundancy to the power network. These ambitious objectives will surely attract great attention in future research.

In a highly competitive research world, the above mentioned scenarios require a flexible experimental setup in order to obtain the experimental results that validate the theoretical proposals. Different works describe examples of experimental setups that can be used in these research fields [27–32]. Each of these laboratory setups presents its own particularities, but the main common objective in all of them is to dispose of sufficient nodes to emulate a distributed generation network. Although these works describe different approaches for the control implementation, recent development of powerful digital controllers points to the use of almost industrial-standard devices able to emulate real complexities [33]. Following these guidelines a power network laboratory (PNL) has been established in the Department of Electronic Engineering in the Technical University of Catalonia at Vilanova i la Geltrú, Barcelona, Spain.

The paper is organized as follows: Section 2 in this work describes comprehensively how PNL is implemented. Section 3 describes in detail one state-of-the-art control for each scenario: a grid-connected system based on network-feeding nodes, and an isolated microgrid system based on network-forming nodes. Section 4 regards the communication issues inside the laboratory setup. Section 5 deals with the distributed digital controllers debugging and launching environment. Section 6 provides selected experimental results using the previously described controls, illustrating the laboratory setup characteristics. Section 7 provides some concluding remarks.

2. Experimental Network Implementation

A distributed generation three-phase network composed of four generation nodes (#1 to #4 in Figure 2) and a Pacific Power AC source [34] that emulates the grid is implemented in the laboratory setup; see photograph shown in Figure 3 and also Table 1 for detailed information about the hardware equipment. The four nodes are feed by a common Amrel DC source [35]. Three-phase inductances in series with power resistors (Z_{12}, Z_{23}, Z_{34} and Z_g) emulate the wires that connect different nodes geographically dispersed and the grid. Each node can feed its own local load $R_{Local\ i}$ and collaboratively a common load R_{Common} located near the AC source. The resistive loads are implemented using low-cost single-phase heaters connected in wye configuration with a floating neutral node. The basic control functionalities of each node are implemented in dedicated digital signal processors (DSP).

An Ethernet link between nodes provides a communication channel which is used to implement higher level controllers in the DSPs. These controllers can be implemented distributedly between nodes or centralized in one of them, which can be viewed as a central controller. A computer is also linked to the Ethernet network in order to supervise and visualize the system behavior in real time. The same computer is used to program and debug the control algorithms that will run in the DSPs. Table 2 summarizes the main component and parameter values. Each node consists of a power inverter fed by the DC source which can be programmed to maintain an ideal constant voltage at its output or to emulate a photovoltaic panel (i.e., voltage drooping as the supplied current grows). The inverter is composed by three main building blocks: the power stack; a damped LCL filter formed by a discrete power inductor and capacitor and the parasitic elements of an isolation transformer (see Figure 2); and the control platform. The next subsections will describe the main parts of the nodes.

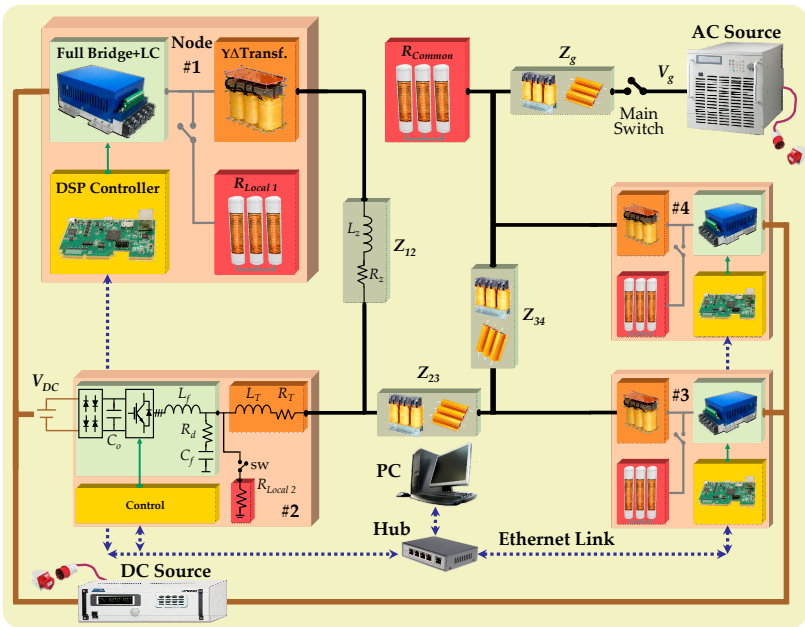

Figure 2. Scheme of the laboratory setup.

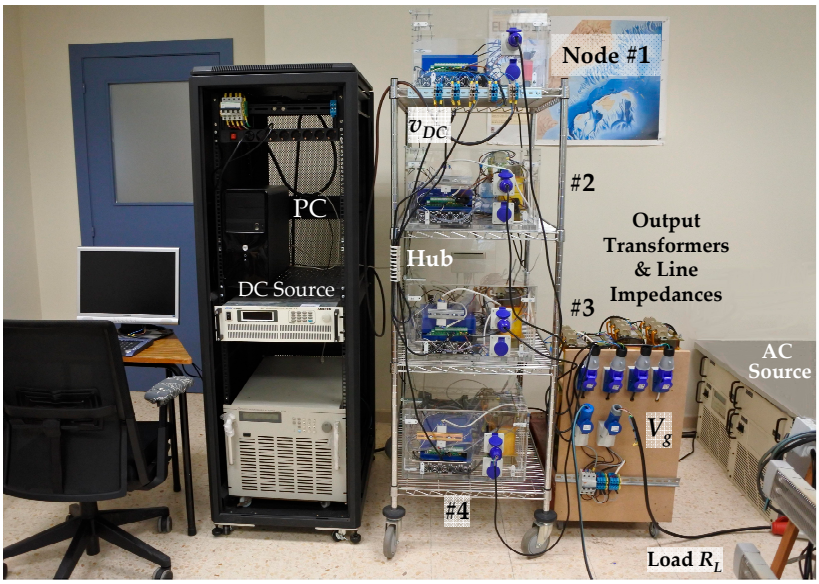

Figure 3. Photo of the power network laboratory setup.

Table 1. Hardware equipment.

Component	Model	Ratings
AC source	Pacific Power, 360AMX(T)-UPC32	Input: 208/240 Vac, 50–60 Hz, 3 phase Output: 0–341 Vac l–n, 16 A, 3 phase
DC source	Amrel, SPS800-19	Input: 208/240 Vac, 50–60 Hz, 3 phase Output: 0–800 Vdc, 19 A
IGBT bridge	Guasch, MTL-CBI0060F12IXHF	V_{dc_max} = 750 V, $I_{max_per_phase}$ = 30 Arms, f_{switch} = 10 kHz
Isolation transformer	Eremu, 21-10309WW	Dyn11, 3 × 400/3 × 400 Vac, 5 kVAr
DSP controller	Texas Instruments, Concerto F28M36P63C	
Current sensors	Talema, AC1025	0–25 Adc/ac
Voltage sensors	Lem, LV25-P	0–400 Vdc/ac

Table 2. Electric parameters.

Parameter Name	Acronym	Value	Units
Grid voltage (line to neutral, l–n)	V_g	110	Vrms
Grid frequency	f_g	60	Hz
DC-link voltage	V_{DC}	350	V
DC-link capacitance	C_o	1.5	mF
LC filter inductances	L_f	5	mH
LC filter capacitances	C_f	1.5	µF
LC filter damping resistors	R_d	68	Ω
Transformer equivalent inductance #1, #2	$L_{T1,2}$	1	mH
Transformer equivalent resistance #1, #2	$R_{T1,2}$	0.5	Ω
Transformer equivalent inductance #3, #4	$L_{T3,4}$	0.6	mH
Transformer equivalent resistance #3, #4	$R_{T3,4}$	1.13	Ω
Line impedances	Z_g, Z_{12}, Z_{23}, Z_{34}	configurable	
Common resistive load	R_{Common}	24/48	Ω
Local resistive loads	$R_{Local\ 1\ldots4}$	48/96	Ω

2.1. Control Platform

Digital controllers are commonly employed in modern high-performance three-phase power converters, and between them, the most used are digital signal processors (DSPs) and field programmable gate arrays [33,36]. Although the controller's main requirement is to manage efficiently the input/output energy, it must provide also flexibility, improved communication capabilities and reliability, intrinsic attributes of DSPs. In this way, the conventional commercial implementation of real-time control and communications in power electronics applications is based on state-of-the-art floating point DSP, relaying in a single-core processor that develops all the power control tasks thanks to its fast dedicated hardware peripherals (analog to digital converters, pulse width modulators, and communication modules among others). On the other hand, mainstream laboratory approaches use complex and effective control solutions to manage a distributed system, such as the embedded software development platform dSPACE [32]. This approach is very interesting due to its flexibility and complete control toolboxes which ensure low prototyping time delays. These systems rely in high-performance PowerPCs that usually manage more than one node at a time [37]. This characteristic makes difficult to emulate the complex interactions of different DSPs working distributely with inherent transmission delays and also, and more important, with different physical clock generators. In this way, recent works deal with clock synchronization issues in digitally controlled distributed generation networks [38–42]. To the best of the authors' knowledge, most of these works provide only simulation results due to the inherent difficulty in obtaining experimental results. Thus, to emulate adequately a real network each node must be controlled by its own digital controller, and then synchronization

problems can be experimentally validated [41,42]. This was the scenario chosen when designing the PNL facility.

In a network with dispersed nodes, an efficient and reliable communication link is fundamental to establish a hierarchical control and supervision functionalities. Commonly DSPs are provided with build-in communication services, as controller area network (CAN). However, CAN systems are used habitually in the automotive industry but not for power system communications [43]. In terms of communication performance, these schemes commonly bring the communications link to secondary priority respect to the main control loops, thus limiting the bandwidth. To improve the communication behavior, two separate devices can be used, one for the control tasks and the second for managing the communication and supervisory tasks, with the disadvantage of both increasing cost and size and decreasing reliability. To overcome these drawbacks, DSPs with two cores have become an interesting option to perform real time control and communications independently in each core. A two processor core configuration avoids harmful interactions between them and complex board connections. The laboratory setup described in this work is based on a dual core DSP: the Concerto dual-core F28M36P63C [44]. This device is implemented in the industry-standard 188-pin DIMM form factor board supplied by a single 5V power rail: Concerto control card H63C2 Experimenter Kit [45]. Thanks to the DIMM docking station all the control card signals are accessible. Programming/debugging is done through a JTAG connector. An Ethernet communication interface is also implemented in the control card. Code Composer Studio™ (CCS), the Texas Instruments integrated development environment (IDE), is used to debug and program both the control routines in the C28 core and the communication protocols in the M3 core.

Figure 4 shows a simplified schematic of a Texas Instruments Concerto microcontroller with dual hybrid architecture comprised of a C28 core and an ARM® Cortex™-M3 core. Each processor is completely independent, with its own memory, peripherals, interruptions controller and ROM/RAM memory. Each core executes its own code separately to maximize their performance: one responsible for the real-time control processes and the other accounting for the communication protocols.

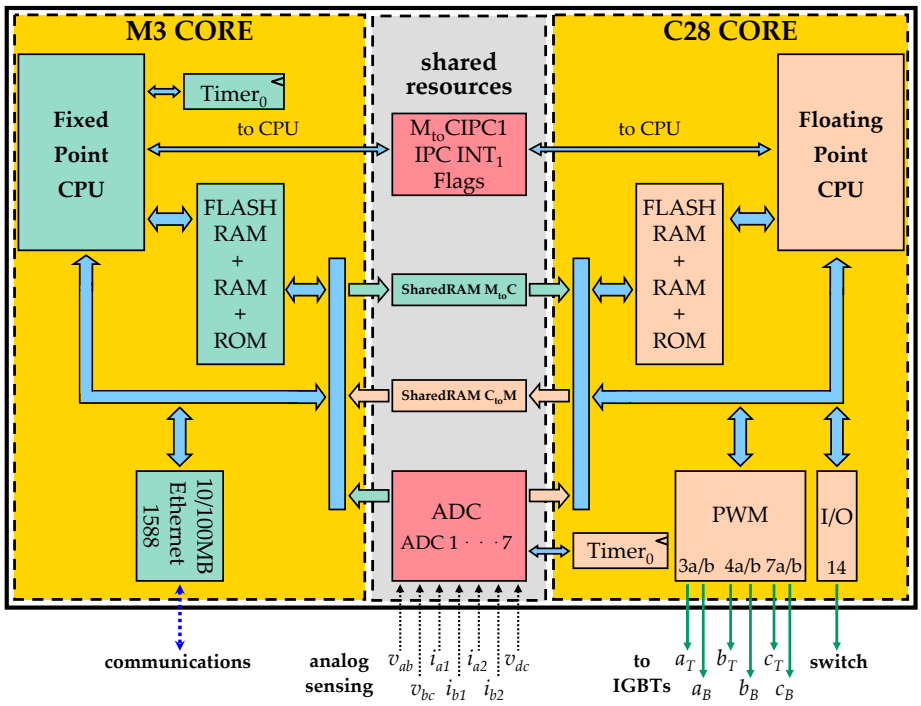

Figure 4. Simplified schematic of the Concerto microcontroller with the peripherals used for control and communications.

The main feature of the C28 core is its integrated floating-point central processing unit with a 32 × 32-bit multiply-accumulate processing capability. As a single core, it is being used in industrial control applications due to its powerful power processing and control peripherals availability (such as PWMs and ADCs). The ARM Cortex-M3 core is used widely for host communications thanks to its wide variety of peripherals, including Ethernet 1588, USB, CAN, some universal asynchronous receiver-transmitters, several serial ports, etc. As a prominent characteristic it implements an Ethernet media access controller that conforms to IEEE 802.3 specifications and fully supports 10BASE-T and 100BASE-TX standards, which enables high performance network connectivity. This core handles perfectly TCP/IP protocols at full scale thanks to its amount of available memory.

Several shared resources simplify and provide high performance connectivity between the two independent cores. Some of these resources are programmed to be read or written by only one or the other core, to avoid conflicts. The shared resources are: (1) the 25 ADC channels with a resolution of 12 bits running at 2.9 mega samples per second. The result registers can be accessed indistinctly by the two processors, in order to be used for control, communication, and system supervision purposes; (2) shared RAM (SRAM) memory mapped in different blocks that can be owned by C28 or M3 processors and used for its specific applications or for transferring data between them by a direct memory access bus. When processor M3 manages (writes, reads or executes) some of these blocks the C28 core is limited to read, which is referred as master to control (MtoC) message. In the opposite case, the ownership is assigned to the C28 core and it can send messages to the M3, which is referred as a control to master (CtoM) message.

2.2. Power Stack

The chosen power stack is an IGBT bridge (MTL-CBI0060F12IXHF from Rectificadores Guasch [46]) with three main parts: rectifier input, capacitor bank and three-phase full bridge IGBT switches. The input is through a three-phase full bridge diode rectifier. This diode-based input is useful to detect control malfunctions which could cause DC-link voltage increments. Also it avoids return currents to the DC source that emulates the distributed generator. A capacitor bank (C_o = 1.5 mF) forms the DC-link. A three-phase full bridge plus a brake IGBT module configures the main core of the power stack.

2.3. Output Filter

The output filter is a damped LCL filter [47–49] composed by a three-phase inductance L_f, a capacitor bank C_f with damping resistors R_d to attenuate the filter resonance, and a wye-delta transformer (wye connection at the inverter side). This transformer introduces the output inductance L_T of the filter and ensures isolation between the input and the output of the inverter. Also it introduces some parasitic resistance useful to emulate R/L lines (R_T). The RC branch of the LCL filter is wye-connected, with a floating neutral node, as the usual implementation described in the literature.

3. Control

Regardless of the state of the main switch, i.e., being the network grid-connected or isolated, each network node can be controlled as network-feeding or network-forming depending on the possibility of dispatching its generated energy [8]. When the prime mover of the DGS is a renewable source, for instance a photovoltaic or wind generator, its inherent intermittence makes its energy generation non-dispatchable and it will act as a network-feeding node. In this case, the utility grid or other/others DGS working as voltage source must regulate the amplitude and frequency of the network voltage required to drive the non-dispatchable DGS as an active/reactive power controlled current source. The active power injected to the network will be determined by the local DC-link voltage controller, responsible of extracting the maximum available power from the prime mover [47]. The reactive power set point will be determined by a higher hierarchical level controller, i.e., grid code accomplishment or power quality requirements. When the prime mover is a conventional power source, e.g., a gas

turbine, its energy generation is dispatchable, and can be modulated following different criteria: economical and environmental costs, losses minimization, etc. In this case the DGS can act indistinctly as a network-feeding or as a network-forming converter. The most challenging scenario is when the network is disconnected from the main grid, and one or more DGS are responsible for maintaining the network voltage independently of the load consumption. When disconnected from the main grid, network-forming converters must feed the local loads cooperatively, and also maintain a well regulated voltage amplitude and frequency to be followed by network-feeding converts. The other scenario is when the network is grid connected and the voltage quality is maintained usually by distant high-power plants. Figure 5 shows the simplified schematic of each network node and the control block diagram in case of network-feeding and network-forming converters. In both cases, the controller located in the C28 core senses the local voltage **v** vector and currents $\mathbf{i_1}$ (in the inverter output) and $\mathbf{i_2}$ (in the LC filter output) using an analog isolated sensing board. Also the DC-link voltage v_{DC} is sensed. For each three-phase current vector only two phase currents are sensed, i_a and i_b, being i_c reconstructed taking into account that in a three-phase three-wire system:

$$i_a + i_b + i_c = 0 \tag{1}$$

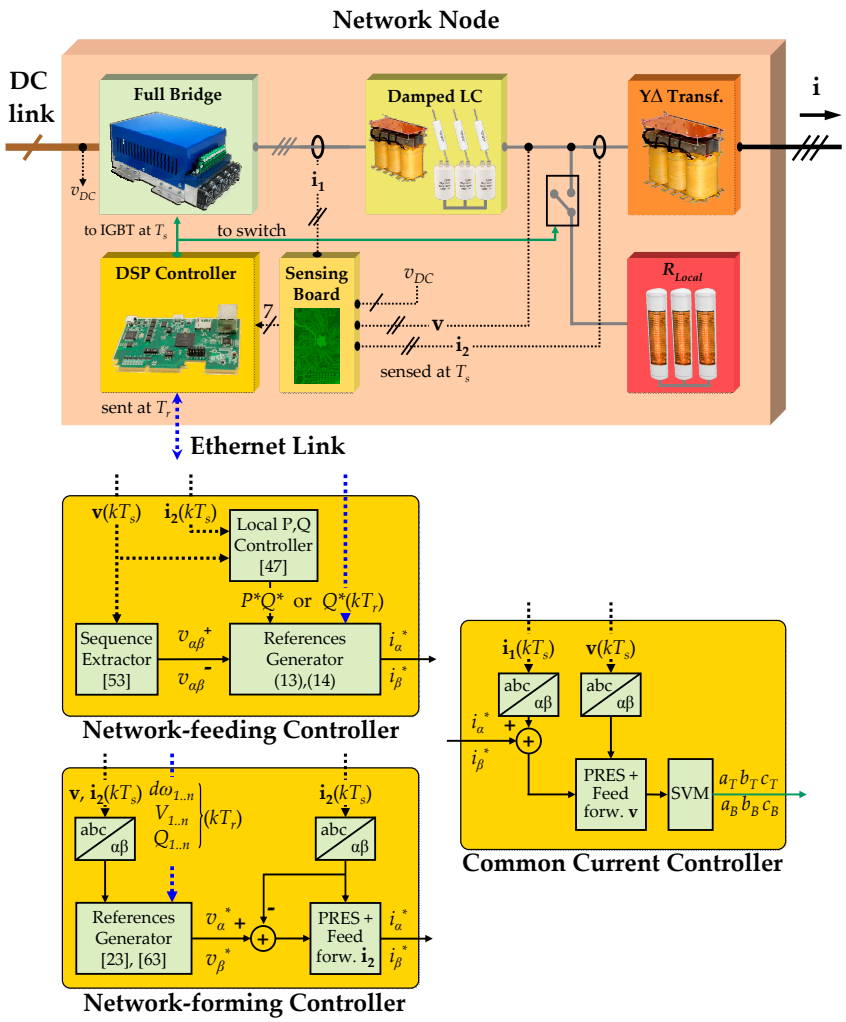

Figure 5. Basic scheme of each network node and its control.

The currents are sensed using Talema AC1025 current transformers. The same idea applies for the voltage vector **v**, only two phase to phase voltages are sensed v_{ab} and v_{bc}. The voltages (including

DC-link voltage) are sensed using Lem LV25-P hall effect voltage transducers. The sampling rate of these variables is T_s = 100 µs, i.e., the maximum switching rate of the IGBT switches [46]. Besides local variables, the conventional controls require also data (at a time rate T_r) from other network nodes or from higher hierarchical level controllers. The next subsection deals with the description of the controllers.

3.1. Network-Feeding Controller

Independently of being in grid connected or islanded mode, when a node acts as a power controlled current source, the reference for the current that must be injected can be expressed in a general form as:

$$\mathbf{i}^* = f\,(P^*, Q^*, \mathbf{v}) \tag{2}$$

being f a function of the active and reactive power references P^* and Q^* shaped by the converter output voltage **v** (i.e., following this voltage reference). Figure 6a shows the simplified diagram of a network-feeding node represented by a power controlled current source wired to the network through the bus $\mathbf{v_n}$. The impedance L_o, R_o, models the output impedance of the source. Impedance L_n, R_n models the isolation transformer impedances and the line connections between nodes. In this case the converter will inject to the network with active and reactive power by ensuring that **i** = **i***. This objective will be accomplished by the conventional inner current control loop: a PRES controller over the $\mathbf{i_1}$ current error with a feed-forwarding term **v** driving a space vector modulator that provides the control signals for the IGBT bridge $a_T - a_B$ (leg a, top and bottom switch respectively), $b_T - b_B$ and $c_T - c_B$ [50,51]. The network-feeding main control scheme can be seen in Figure 5.

Taking into account that the phase voltage vector **v** can be unbalanced it can be expressed in stationary reference frame (SRF) as:

$$v_\alpha = v_\alpha^+ + v_\alpha^- = V^+\cos(\omega t) + V^-\cos(\omega t + \delta) \tag{3}$$

$$v_\beta = v_\beta^+ + v_\beta^- = V^+\sin(\omega t) - V^-\sin(\omega t + \delta) \tag{4}$$

where $v_\alpha{}^+$, $v_\beta{}^+$ and $v_\alpha{}^-$, $v_\beta{}^-$ are the positive and negative sequence voltages respectively, V^+ and V^- are their amplitudes, ω is the grid angular frequency, and δ is the phase angle between positive and negative sequences.

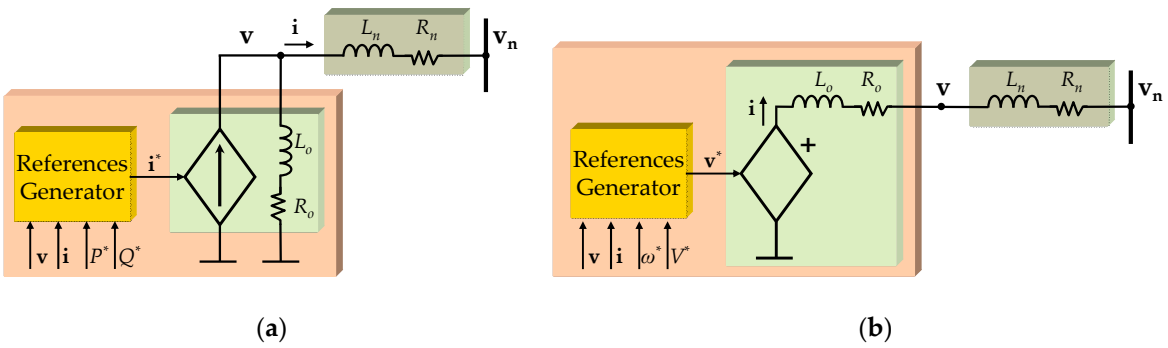

Figure 6. Simplified schematic of (**a**) network-feeding node, (**b**) network-forming node.

As stated before, the injected current **i** must be shaped by the output voltage **v**, thus in a general form it must be a function of both the positive and the negative sequence voltages. To accomplish this objective a sequence extractor should be used to estimate the sequence voltages from the SRF voltage vector [52,53]. Afterwards, when the sequence voltages are known, the amplitudes of the positive and negative sequences can be calculated on-line using:

$$V^{+} = \sqrt{(v_{\alpha}^{+})^{2} + (v_{\beta}^{+})^{2}} \tag{5}$$

$$V^{-} = \sqrt{(v_{\alpha}^{-})^{2} + (v_{\beta}^{-})^{2}} \tag{6}$$

The reference currents are expressed as a function of active and reactive powers:

$$i_{a}^{*} = i_{a}^{*}(p) + i_{a}^{*}(q) \tag{7}$$

$$i_{\beta}^{*} = i_{\beta}^{*}(p) + i_{\beta}^{*}(q) \tag{8}$$

where the active and reactive components can be expressed in a general form using [54]:

$$i_{\alpha}^{*} = \frac{2}{3}\frac{k_{p}^{+}v_{\alpha}^{+} + k_{p}^{-}v_{\alpha}^{-}}{k_{p}^{+}(V^{+})^{2} + k_{p}^{-}(V^{-})^{2}}P^{*} + \frac{2}{3}\frac{k_{q}^{+}v_{\beta}^{+} + k_{q}^{-}v_{\beta}^{-}}{k_{q}^{+}(V^{+})^{2} + k_{q}^{-}(V^{-})^{2}}Q^{*} \tag{9}$$

$$i_{\beta}^{*} = \frac{2}{3}\frac{k_{p}^{+}v_{\beta}^{+} + k_{p}^{-}v_{\beta}^{-}}{k_{p}^{+}(V^{+})^{2} + k_{p}^{-}(V^{-})^{2}}P^{*} - \frac{2}{3}\frac{k_{q}^{+}v_{\alpha}^{+} + k_{q}^{-}v_{\alpha}^{-}}{k_{q}^{+}(V^{+})^{2} + k_{q}^{-}(V^{-})^{2}}Q^{*} \tag{10}$$

In Equations (9) and (10) k_{p}^{+}, k_{p}^{-}, k_{q}^{+}, and k_{q}^{-} are the active and reactive balancing factors used to flexibly inject power through positive and negative sequences. In a non-dispatchable DGS, the active power reference P^{*} is usually calculated by a local controller using local variables. Its aim is to extract the maximum allowable energy from the source [47,55]. Active power curtailment can also be required to protect the inverter from over currents when a voltage sag occurs [10,11]. When the source is dispatchable the reference active power can be set by a higher level controller. The reactive power reference Q^{*} can be calculated locally or can be set by a higher level controller. When calculated locally, Q^{*} is determined to fulfil the stringent reactive current injection (RCI) requirements set by grid codes during voltage disturbances [12]. RCI can also be used with the aim of supporting the grid voltage when the grid impedance is mainly inductive [13,14]. The reactive power reference for each node can also be determined by a centralized controller when a general voltage control is required [56,57]. In addition, the balancing factors in Equations (9) and (10) can be used to provide ancillary functions to the DGS specially during voltage disturbances [10,58,59]: avoid DC-link voltage oscillation during network voltage unbalancing, provide some voltage support during unbalanced voltage droops, among others. Some degrees of freedom exist in the selection of the balancing parameters. For instance, in this work, two additional ancillary objectives will be defined for the network-feeding nodes working with the control scheme based on Equations (9) and (10). First objective (reduction of DC-link oscillations) will be fulfilled choosing the following relationships between the sequence balancing parameters:

$$k_{p}^{+} = k_{p}; \quad k_{p}^{-} = (1 - k_{p}) \tag{11}$$

$$k_{q}^{+} = k_{q}; \quad k_{q}^{-} = (1 - k_{q}) \tag{12}$$

with k_{p} and k_{q} taking values between 0 and 1. Then the DC-link oscillations are avoided when injecting active and reactive powers during unbalanced network voltages [54] and, in this case, the injected currents are expressed as:

$$i_{\alpha}^{*} = \frac{2}{3}\frac{k_{p}v_{\alpha}^{+} + (1 - k_{p})v_{\alpha}^{-}}{k_{p}(V^{+})^{2} + (1 - k_{p})(V^{-})^{2}}P^{*} + \frac{2}{3}\frac{k_{q}v_{\beta}^{+} + (1 - k_{q})v_{\beta}^{-}}{k_{q}(V^{+})^{2} + (1 - k_{q})(V^{-})^{2}}Q^{*} \tag{13}$$

$$i_{\beta}^{*} = \frac{2}{3}\frac{k_{p}v_{\beta}^{+} + (1 - k_{p})v_{\beta}^{-}}{k_{p}(V^{+})^{2} + (1 - k_{p})(V^{-})^{2}}P^{*} - \frac{2}{3}\frac{k_{q}v_{\alpha}^{+} + (1 - k_{q})v_{\alpha}^{-}}{k_{q}(V^{+})^{2} + (1 - k_{q})(V^{-})^{2}}Q^{*} \tag{14}$$

As a drawback, although not as harmful as DC-link voltage oscillations, the instantaneous reactive power will suffer oscillations with maximum amplitude [60].

The second objective to be accomplished using Equations (13) and (14) will be to provide voltage support to the network during voltage sags. Then the changes in voltage **v** due to the injected current **i** must be estimated. Independently of the amount of P^* and the origin of Q^*, when currents (13) and (14) are injected into the network they will produce some effects over the DGS output voltage **v** due to the equivalent impedance seen by the converter [58,59]:

$$V^+ \approx V_n^+ + \frac{2}{3}R_n \frac{k_p V^+}{k_p (V^+)^2 + (1-k_p)(V^-)^2} P^* + \frac{2}{3}\omega L_n \frac{k_q V^+}{k_q (V^+)^2 + (1-k_q)(V^-)^2} Q^* \quad (15)$$

$$V^- \approx V_n^- + \frac{2}{3}R_n \frac{(1-k_p) V^-}{k_p (V^+)^2 + (1-k_p)(V^-)^2} P^* - \frac{2}{3}\omega L_n \frac{(1-k_q) V^-}{k_q (V^+)^2 + (1-k_q)(V^-)^2} Q^* \quad (16)$$

The voltage support objective during a voltage sag is to increase the amplitude of the positive sequence voltage V^+ (to restore voltage amplitude) and to reduce the amplitude of the negative sequence voltage V^- (to balance phase voltages) [61]. As Equation (15) clearly shows, the positive sequence of active and reactive currents increases the positive sequence voltage, accomplishing the objective of voltage supporting. On the other hand, as seen in Equation (16), the negative sequence of the reactive current reduces the negative sequence voltage. In this case the negative sequence of the active current increases the negative sequence (increasing phase voltages unbalance). This last effect is a drawback of the proposal described by Equations (13) and (14) with the main objective of avoid DC-link voltage oscillations. Being P^* determined by the active power generated in the source, Q^* needs to be determined accurately to control the voltage support capabilities. In other words, the practical scenario in which Equations (13) and (14) provide good voltage support is limited to networks with inductive dominant behavior.

3.2. Network-Forming Controller

When the network is disconnected from the main grid (i.e., in islanded mode) one or more converters must regulate the network voltage. In this case some of the network nodes will work as voltage sources or network-forming converters. Figure 6b shows the simplified diagram of a network-forming node, represented by a voltage controlled voltage source with an output impedance L_o, R_o connected to the network at the bus $\mathbf{v_n}$ through an equivalent impedance L_n, R_n. The usual two nested control loops are programmed in the local controllers: a fast inner current loop with $\mathbf{i_1}$ (as in network-following converters described before) and a slow outer voltage loop used to fix the converter output voltage **v** [19] (see Figure 5). The transient response of both loops are accelerated against step changes due to external perturbations with feed-forwarding the output voltage **v** in the current loop and the output current $\mathbf{i_2}$ in the voltage loop [19]. The main task (i.e., to regulate the voltage) can be accomplished using different approaches: master-slave scheme and multi-master scheme. The first approach is used when only one node acts as voltage source setting its own reference voltage to the network, the others act as network-following converters. This is the simplest way but lacks of flexibility and reliability: if master crashes the complete network collapses, thus requiring a complex protocol to change from slave to master in replacing the failed voltage node. The state-of-the-art multi-master scheme is based in the high reliable voltage droop control to manage different nodes acting as voltage sources [15]. This control is based in three levels of hierarchy: primary, secondary and tertiary control layers [62,63].

In hierarchical control, the primary layer is based on a local controller that ensures active and reactive power sharing between network-forming nodes. This controller depends only on local sensed variables and is based on dropping the output-voltage frequency and amplitude magnitudes regarding the active and reactive power supplied by the source respectively, emulating a conventional synchronous generator [64]:

$$v_\alpha^* = V^* \sin(\omega^* t) \tag{17}$$

$$v_\beta^* = -V^* \cos(\omega^* t) \tag{18}$$

$$\omega^* = \omega_o - m_p P \tag{19}$$

$$V^* = V_o - n_q Q \tag{20}$$

where ω_o and V_o are the nominal network angular frequency and voltage amplitude, respectively. The slopes m_p and n_q are the gain parameters to drop proportionally ω_o and V_o regarding the averaged values (low pas filtered) of the instantaneous active and reactive powers:

$$p = \frac{3}{2}(v_\alpha i_{2\alpha} + v_\beta i_{2\beta}) \tag{21}$$

$$q = \frac{3}{2}(-v_\alpha i_{2\beta} + v_\beta i_{2\alpha}) \tag{22}$$

$$P(s) = p(s)\frac{\omega_c}{s + \omega_c} \tag{23}$$

$$Q(s) = q(s)\frac{\omega_c}{s + \omega_c} \tag{24}$$

In Equations (23) and (24) ω_c is the cut-off frequency of the low pass filter, and s is the Laplace operator. The filter provides noise and harmonic attenuation and besides gives usually a slow response of some seconds, as desired in this application.

To ensure the system controllability by using the droop method expressed in Equations (19) and (20) the equivalent impedance seen by the converter must be dominantly inductive [65]. In this sense a supplementary loop is necessary to add a virtual inductance that summed to the line impedance seen by the inverter guarantees a mainly inductive impedance [66]:

$$v_\alpha^* = V^* \sin(\omega^* t) + Z_v i_{2\beta} \tag{25}$$

$$v_\beta^* = -V^* \cos(\omega^* t) - Z_v i_{2\alpha} \tag{26}$$

being Z_v a pure inductance (i.e., R_v = 0 Ω).

Active power sharing between network-forming nodes is accomplished perfectly due to the fact that the network frequency is a global variable and, thus, all the network nodes have the same frequency in steady state:

$$\omega = \omega_1^* = \ldots. = \omega_i^* \tag{27}$$

It is worth mentioning that the perfect active power sharing:

$$m_p P_1 = m_p P_2 = \ldots = m_p P_i \tag{28}$$

is accomplished if the droop slopes m_p are equal in all the network nodes.

On the other hand, a perfect reactive power sharing is not achieved with the droop on the voltage amplitude (20) due that the amplitude is not a global variable, and thus is different in each node:

$$V_1 \neq V_2 \neq \ldots. \neq V_i \tag{29}$$

Thus, this controller only provides slight reactive-power equalization.

With Equations (19), (20), (25) and (26) any number of network-forming converters can share the network active and reactive powers without knowing any other variables than its local sensed output voltage and current. Thus no communication between nodes is required, which provides high robustness and reliability to this primary control.

When a new converter is going to be connected to the network its output voltage must be synchronized with the network voltage before the connection [67]. Thus, some seconds before the connection, a phase locked loop (PLL) is used to synchronize the reference voltage of the still inactive converter with the network voltage in the point of connection. Once the reference voltage of the inactive node has been delayed θ rad/s in order to be synchronized with the network voltage, the node is turned on to participate in the power sharing. Due that its initial mean values of active and reactive powers will be zero, the node will begin to operate with the following references:

$$v_\alpha^* = V_o \sin(\omega_o t + \theta) \tag{30}$$

$$v_\beta^* = -V_o \cos(\omega_o t + \theta) \tag{31}$$

Thanks to the slow dynamics provided by the low pass filters (23) and (24), the new connected converter will experience a soft start in the active and reactive power injection.

In a hierarchical droop controller, the secondary level is responsible for overcoming the drawbacks of the primary layer, i.e., frequency deviation and unequal reactive power sharing. Normally a communication channel is used to interchange local data between nodes and a centralized controller that calculates the correction terms and send them using a one-to-all protocol [63]. With this approach, the frequency can be completely restored an also the voltage amplitude in the centralized controller node can be set to any desired value. This centralized approach has been used extensively but lacks of robustness due its master-slave topology. Secondary level distributed or decentralized approaches are very interesting because they overcome the master-slave weakness. These approaches rely on a distributed control fed by local data interchanged between neighboring nodes [21,22]. The neighboring nodes use a dedicated communication channel to interchange its local data at a slow transmission rate T_r, several orders of magnitude over the sensing/switching period T_s. In the case of consensus based secondary control scheme, one particular node i only receives data from n neighbors and calculates its own correction terms [23]. A global objective is reached with only partial data through "gossiping" between adjacent nodes. In this work, the correction term for the frequency is $d\omega_i$ and modifies the primary control as:

$$\omega_i^* = \omega_o - m_p P_i + d\omega_i \tag{32}$$

The aim of this term is to accomplish a double objective: restore the local angular frequency ω_i to its nominal value ω_o and to equalize the values of the correction terms $d\omega$:

$$\omega_o = \omega_1 = \ldots. = \omega_{n-1} = \omega_n \tag{33}$$

$$d\omega_i = d\omega_1 = \ldots. = d\omega_{n-1} = d\omega_n \tag{34}$$

The correction term is calculated using a two integral controller as:

$$d\omega_i = k_\omega \int (\omega_o - \omega_i^*) dt + k_{d\omega} \int \sum_{j=1}^{n} \left(d\omega_j - d\omega_i\right) dt \tag{35}$$

From Equation (35), it can be noted that only the locally calculated correction term $d\omega_j$ will be transmitted between the n neighbor nodes.

Similarly, two control objectives are accomplished by adding a correction term dV in the voltage expression of the primary layer:

$$V_i^* = V_o - n_q Q_i + dV_i \tag{36}$$

where the voltage correction term is calculated using n pairs of transmitted data from the adjacent nodes, the local node output voltage V_j and the reactive power supplied to the network Q_j.

$$dV_i = k_V \int \sum_{j=1}^{n} (V_o - V_j) dt + k_Q \int \sum_{j=1}^{n} (Q_j - Q_i) dt \tag{37}$$

where the local node output voltage is calculated as follows:

$$V = \sqrt{v_\alpha^2 + v_\beta^2} \tag{38}$$

This usually noisy magnitude requires to be processed by a low-pass filter as in Equations (23) and (24). It must be noted that in Equation (37) the double integral secondary controller is responsible for equalizing the reactive power sharing:

$$Q_i = Q_1 = \ldots = Q_{n-1} = Q_n \tag{39}$$

and also controlling the mean voltage amplitude (between the n nodes) to the nominal value V_o:

$$V_o = \frac{\sum_{j=1}^{n} V_j}{n} \tag{40}$$

The complete controller schematic for network-forming converters is shown in Figure 7.

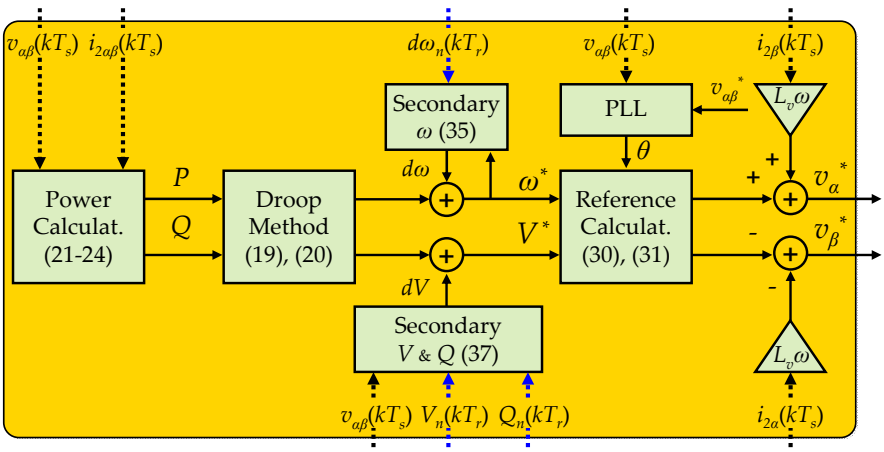

Figure 7. Primary and secondary control layers for the network-forming converters.

The tertiary control manages the energy flow inside the network and between the network and the grid during grid-connected mode. There are different approaches for tertiary control implementation, based on centralized or decentralized schemes [15–17]. When the main goals are to optimize market and economic profits, the centralized approach is the most commonly used. A single controller centralizes all the information of the network parameters in an all-to-one communication infrastructure. Then, the tertiary controller computes the energy set-points and sends the government data to the local controllers. The main goal of the decentralized tertiary controllers is to improve the overall performance of the system. The most promising decentralized scheme is based on multi-agent intelligent systems (MAS), where each agent has local intelligence and can take some decisions independently [68]. Then, the centralized controller is divided into simple software agents located dispersedly in the local controllers, which provides high robustness to the whole system. As can be seen, tertiary control relies on the power distribution optimization and will not be discussed deeply here.

4. Communications

As previously stated, basic operation of a power network relies on different control elements with a communication link between them: local controllers managing each distributed source/load and a distributed/centralized controller to ensure optimal energy management and power quality. In addition, when the network is connected to other networks or to the main grid, other communication channels must be established with higher hierarchical levels in order to provide a distributed supervisory control and data acquisition (SCADA) of the whole system. As a consequence, this application requires an advanced communication system to deliver real time information and commands. Until present days, DSPs used as industrial controllers in these environments had different, but limited, possibilities to implement communication links. Conventional DSPs carry built-in communication interfaces as for example CANopen, ControlNet, DeviceNet, Fieldbus, Modbus, Optomux, Profibus and Profinet. These applications provide custom communication protocols which makes difficult to implement new functionalities and improvements, and as a major drawback: are considered very limited in terms of throughput compared with recent non-real time technologies [43]. Thus, connecting the power network through the World Wide Web or local area networks (LAN) using common protocols and standards is the most desirable scenario in an increasingly connected world. The almost ubiquitous, fast and cheap, local area network is Ethernet, running over the Transmission Control Protocol and Internet Protocol (TCP/IP) protocol suite. The weakness (in a distributed control scenario) of a communication network based on Ethernet is its non-deterministic and asynchronous nature, in which the main objective is a reliable delivery, being secondary when the data is received. Thus in the proposed experimental setup the use of Ethernet for communications is an interesting and powerful choice.

On the one hand, data sent using TCP/IP protocol is packed in bulky and long messages, with intrinsically long latencies that can reach hundreds of milliseconds. TCP/IP guarantees that all the information packets will reach its destination through powerful (but slow) re-transmission mechanisms. When distributed real-time control is required, re-transmitting old data is, generally, not very useful [69] and can lead to instabilities. On the other hand, User Datagram Protocol (UDP/IP) is a non-reliable protocol preferable for real-time control because it is based in short messages with low latency (some milliseconds). UDP/IP does not guarantee that the data reach its destination (there is not re-transmission) thus a packet can be lost "forever" due to congestion or channel noise. This last drawback is not significant in the present application, since, as explained above, the data exchanged between the network nodes (i.e., frequency, voltage amplitude, mean reactive power, etc.) are sent at a slow time rating (usually from 100 ms to 1 s) and in this way, when a packet is lost, previously received old data can be maintained in the control calculation without bringing the system to a crash. In addition, the amount of data exchanged at this level (secondary and tertiary control) is small and the low payload protocol UDP/IP can be used.

In the described PNL setup, both TCP/IP and UDP/IP protocols are used simultaneously. TCP is used to implement the SCADA system to supervise the entire network with a PC and also to launch the DSPs, and UDP for secondary control implementation. These protocols are running in the communications dedicated core M3. The code that implements the protocols are directly adapted from the Lightweight (lwIP) IP stack, which is available as an open source resource [70]. Thanks to this light stack, the use of full scale TCP-UDP/IP protocols only requires a typical code size from 25 to 40 kilobytes and from 10 to a few tens of kilobytes of RAM [71], that are available in the M3 core.

Figure 8 shows a diagram including control and communication functions performed by the dual-core DSP. The diagram presents, as an example, the specific functions for operating the node #1 as UDP server. A timer interrupt at T_s launches the main control calculation function in node #1 C28 core. After sensing the input variables, the control core generates the droop primary level signals. Secondary control (35) and (37) is implemented using its own data [ω_1*$((k-1)T_s)$; $d\omega_1((k-1)T_s)$; $V_1(kT_s)$, $Q_1(kT_s)$] and data transmitted from nodes #2 and #3 [$d\omega_2(kT_r)$, $d\omega_3(kT_r)$; $V_2(kT_r)$, $V_3(kT_r)$, $Q_2(kT_r)$, $Q_3(kT_r)$] that is available in the C28 core SRAM memory. After obtaining the secondary control

values, core C28 calculates the reference values of $\omega_1{}^*$ and $V_1{}^*$ using (32) and (36). Finally, C28 stores the local variables: $d\omega_1(kT_s)$, $V_1(kT_s)$ and $Q_1(kT_s)$ in the shared RAM. A timer interruption at a rating T_r is configured in the M3 core to launch a periodical interruption. When serving this interruption, M3 core reads $d\omega_1$, V_1 and Q_1 from the SRAM, packs these data into an UDP datagram adding also the number of the inverter as the first data [1, $d\omega_1$, V_1, Q_1] and sends it to nodes #2 and #3 through UDP.

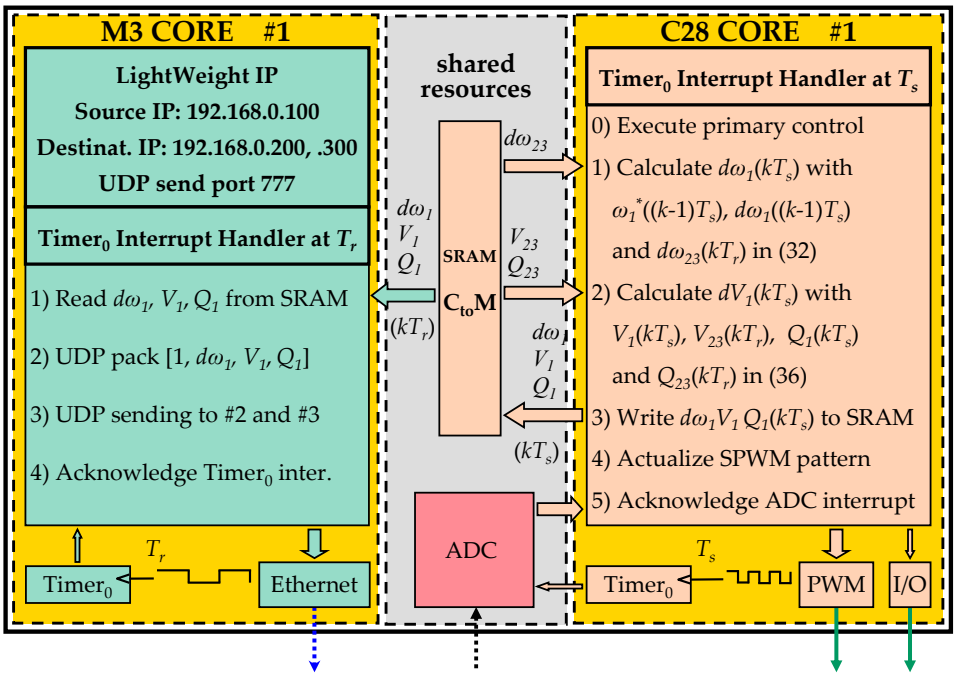

Figure 8. Dual-core DSP functions for operating the node #1 as UDP server.

Although not shown in this work, the communication functions when node #1 receives an UDP datagram (acting as a client) is as follows: when M3 core receives an UDP datagram through Ethernet connection (for example from node #2) it unpacks $d\omega_2(kT_r)$, $V_2(kT_r)$ and $Q_2(kT_r)$ data and writes them into the shared RAM. Then M3 raises an inter-processor communication interruption to C28 core that will be served by an interrupt handler in the C28 core. When attaining the software interruption, C28 core reads $d\omega_2(kT_r)$, $V_2(kT_r)$ and $Q_2(kT_r)$ from the SRAM, reads also that the data comes from node #2 and updates node #2 data values in the C28 local controller. When executing the next main control calculation function, C28 core will use the updated variables for calculating the secondary control. A complete description of the protocols implementation can be found in [72] (pp. 397–400).

The TCP/IP protocol is used for debugging/initialization and SCADA tasks in order to communicate the M3 core with the PC through Debug Server Scripting (DSS) platform implemented in Matlab [73]. The next section will describe this implementation.

5. Debugging

As stated before, the programming and debugging environment for Concerto dual-core used in the PNL is Code Composer Studio, the integrated development environment (IDE) from Texas Instruments that supports the Microcontroller and Embedded Processors portfolio [74]. CCS is an Eclipse-based environment that provides a complete and powerful suite of tools used to develop and debug embedded applications: C/C++ compiler, source code editor, project build environment, debugger, profiler, among others. The IDE provides an easy of use interface for each step of the application development flow, with a fully segregation between the code development for C28 and M3 cores. When programming and debugging more than one DSP at a time (four in our system) the Debug Server Scripting (DSS) tool provides a complete control over programming, debugging

and running multiple microcontrollers. DSS is the base debug engine of CCS and its Application Programming Interface (API) can be easily accessed in Java. The debugging library provides services to connect, program, start, stop, debug data, etc. that are accessed using Matlab scripts. Matlab is used to call libraries in Java allowing an easy integration of the DSS into the power network setup for programming and debugging the DSPs. Matlab is used to automatically download the binary files into the microcontroller. Also, and most important in the present application, Matlab provides Ethernet sockets to communicate with the DSPs during the tests. In this case, TCP/IP is used to synchronize the procedure to run and launch an experiment. It is worth mentioning that Matlab implements neither soft-nor hard real-time tasks, because the microcontrollers run at its own and all the tasks are running in isolation from the host PC, including the data communication via UDP/IP connections for the secondary control tasks. Figure 9 illustrates these functionalities.

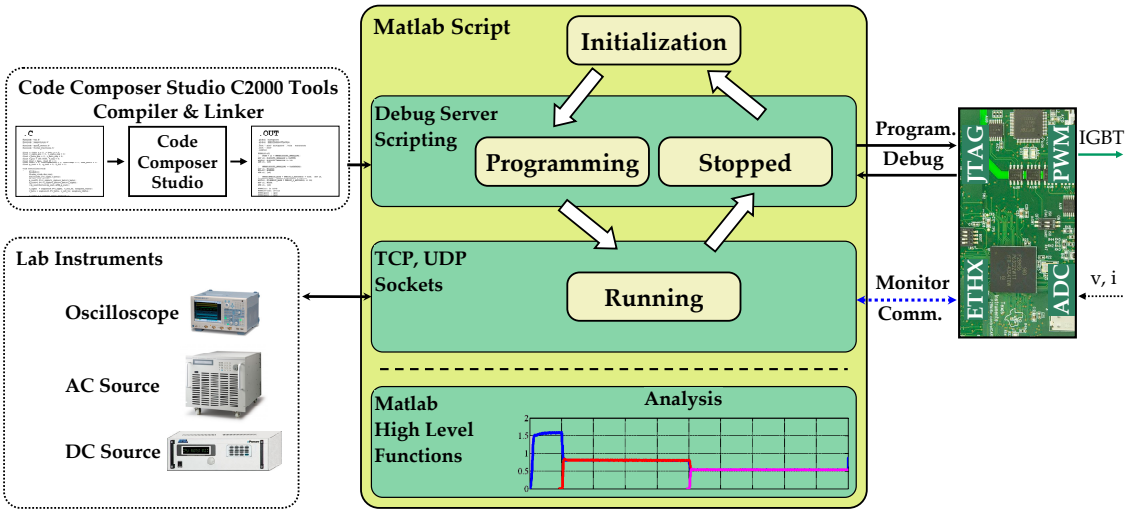

Figure 9. Programming, debugging and launching DSS over Matlab.

6. Experimental Results

Using the high flexibility of the laboratory network described in previous sections, two experimental setups have been implemented to clearly show the powerfulness of the PNL implementation. First, a grid connected network consisting on four nodes working as network-feeding converters will be implemented and tested. The behavior of the network when a voltage sag appears will be investigated. In this case each converter will take its own control decisions and no communications will be used.

Second, an islanded μG will be implemented, with three network-forming nodes and with the fourth node acting as a programmable load (network-feeding node injecting active power). This setup will be driven by a two level scheme, with a droop based primary and a consensus based secondary controller that uses the communication channel. In this last setup two different cases will be tested: (a) ideal clock conditions, and (b) when some clock drift desynchronizes controllers. Table 3 lists the additional system hardware and control parameters (see Table 2 for the rest of parameters).

Table 3. Additional system and control parameters.

Parameter Name	Acronym	Value	Units
Node nominal rated power (base power)	S_b	1.5	kVAr
Node nominal rated current	I_{rated}	5	A rms
Global load rated power	P_L	1.5	kW
Local loads rated power	$P_{L1,2,3}$	0.25	kW
Droop method virtual inductance	L_v	10	mH
Droop method virtual resistance	R_v	0	Ω
Line inductance $_{12}$	L_{12}	2	mH
Line resistance $_{12}$	R_{12}	65	mΩ
Line inductance $_{23}$	L_{23}	0.8	mH
Line resistance $_{23}$	R_{23}	110	mΩ
Line inductance $_{34}$	L_{34}	0.8	mH
Line resistance $_{34}$	R_{34}	110	mΩ
Active power reference	P_i*	0.5	kW
Reactive power reference nominal conditions	Q_i*	0	kVAr
Reactive power reference when sag occurs	Q_i*	0.9	kVAr
Sequences balancing parameters	k_p, k_q	0.5	
Frequency droop parameter	m_p	1	mrad/(Ws)
Voltage droop parameter	n_q	10	mV/(V Ar)
Proportional gain PRES voltage compensator	k_{pv}	1	mA/V
Integral gain PRES voltage compensator	k_{iv}	3	A/(Vs)
Proportional gain PRES current compensator	k_{pi}	30	A^{-1}
Integral gain PRES current compensator	k_{ii}	800	$(As)^{-1}$
Sampling and switching rate	T_s	100	µs
Transmission rate	T_r	100	ms

6.1. Test 1, Grid Connected Network under Voltage Sags

Figure 10 shows a simplified diagram of the grid connected network. The grid is emulated by the AC source that provides a regulated three-phase voltage $\mathbf{v_g}$. The four converters are programmed as power controlled current sources, emulating, for example, four photovoltaic-generation modules. Buses $\mathbf{v_1}$ to $\mathbf{v_4}$ are colored differently to easily identify the measured voltages and powers in the following figures. Each converter is governed by its own active and reactive power references P_i* and Q_i* (for i = 1 to 4). The global resistive load R_L is located in parallel with the AC-source to avoid injecting all the generated active power ($P_1 + P_2 + P_3 + P_4$) to this source. Following the operating rules of this two quadrant AC-source, and in order to avoid damaging it, only 25% of the rated active power can be absorbed by the source.

A type II voltage sag was programmed in the AC-source to evaluate the behavior of the system under a static sag. Figure 11 shows the phase-to-neutral voltages in per unit values (p.u.) at the output of node #1. Before t = 0 s the grid phase voltages $\mathbf{v_g}$ are perfectly balanced at 1 p.u. The four nodes are injecting to the network the same reference powers P_i* = 500 W and Q_i* = 0 VAr using the reference current calculation scheme (13) and (14), see Figure 12. It must be noted that, being 1.5 kW the load rated power, only 500 W are being absorbed by the grid/AC-source. As can be appreciated in Figure 11, the phase voltages at node #1 ($\mathbf{v_1}$) present a slightly higher value than at node $\mathbf{v_g}$ (0.03 p.u. higher). This effect is due to the fact that the impedance seen at the output of the converters has some resistive part (see the transformers data in Table 2), and active currents produce voltage increments (as stated in (15) and (16)). At t = 0 s the sag begins and after a computation delay of 0.01 s due to the sequences extractor [53] the sag is detected. Until t = 0.125 s the sag control is deliberately inactive to clearly show its behavior without any control action. At t = 0.125 s the reference reactive powers are set to Q_i* = 0.9 kVAr in (13) and (14), thus providing RCI as grid codes require (black dashed line in Figure 12). When the fault is cleared (t = 0.25 s) the RCI is still working during the detection delay of 0.01 s. At t = 0.26 s the voltage restoration is detected and the reactive power reference is reset to 0 VAr. As can be seen in Figure 12 top subfigure, active power references P_i* are set to 0 at t = 0.375 s to

clearly show the output voltage without any injection. As can be noted in Figure 11 between t = 0.375 s and t = 0.5 s the voltage vector $\mathbf{v_1}$ is perfectly balanced at 1 p.u. because the nodes are inactive.

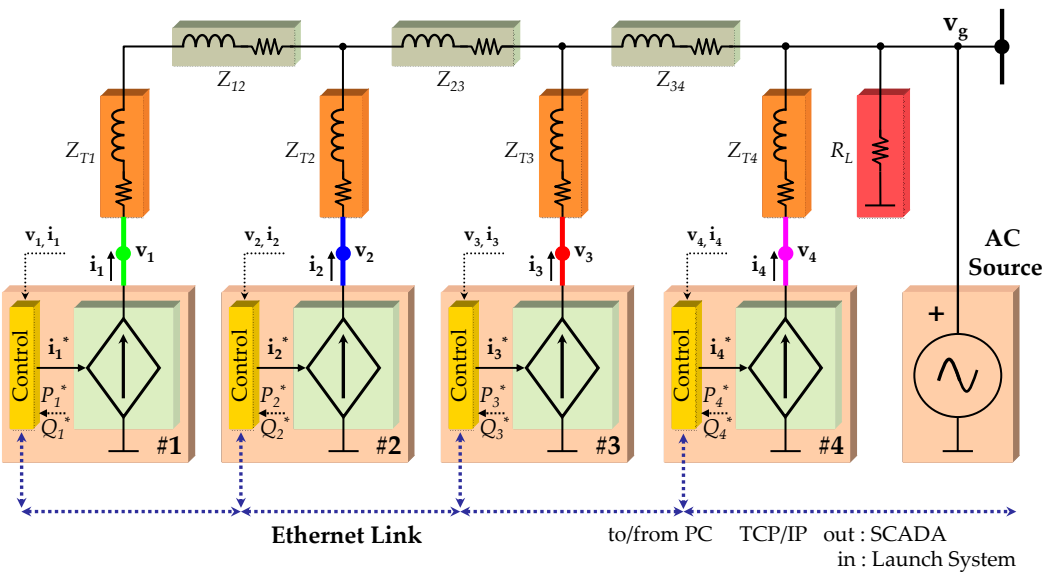

Figure 10. Test 1, grid connected network setup.

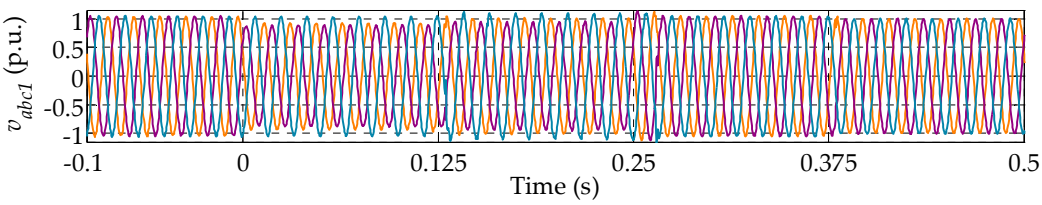

Figure 11. Test 1, sensed phase voltages at the output of converter $\mathbf{v_1}$ during the voltage sag.

The second objective of the RCI scheme (13) and (14) is to avoid oscillations in the instantaneous active power and thus also in the DC-link voltage. Figure 12, top, clearly shows the fulfillment of this objective. In addition, it can be clearly noted that the instantaneous reactive powers present an oscillation of 200 VAr, without adverse effects in the system. With the proposed scheme, minimum oscillation in active power is related to maximum oscillation in reactive power.

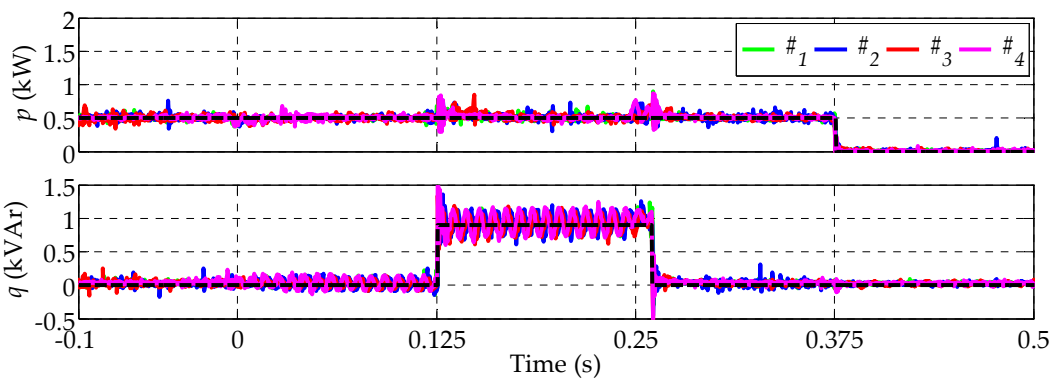

Figure 12. Test 1, measured instantaneous active and reactive powers of DGS #1, #2, #3 and #4. Active and reactive power references in black dashed lines.

Figure 13 presents the generated currents in the four network nodes. Before the sag the currents are both in phase with the voltage (only active power is generated) and perfectly balanced with an amplitude of 2.1 A. At t = 0.01 s some current unbalance appears, due to the negative sequence voltage. To continue injecting the generated active powers P_i* = 0.5 kW the current amplitudes must be increased due to the voltage amplitudes have been reduced. The maximum current amplitude appears in the phase with lowest voltage amplitude (purple trace in Figure 11). This last effect is very interesting for voltage support purposes, it maximizes the support in the most perturbed phase [14]. As stated before, at t = 0.125 s RCI starts. In this test the strategy of injecting the maximum allowable current I_{rated} is chosen [54], and the maximum amplitude current reaches 5 A, also in the most perturbed phase (in purple). After t = 0.375 s the currents are set to 0 A in order to clearly show the node voltages without any injection.

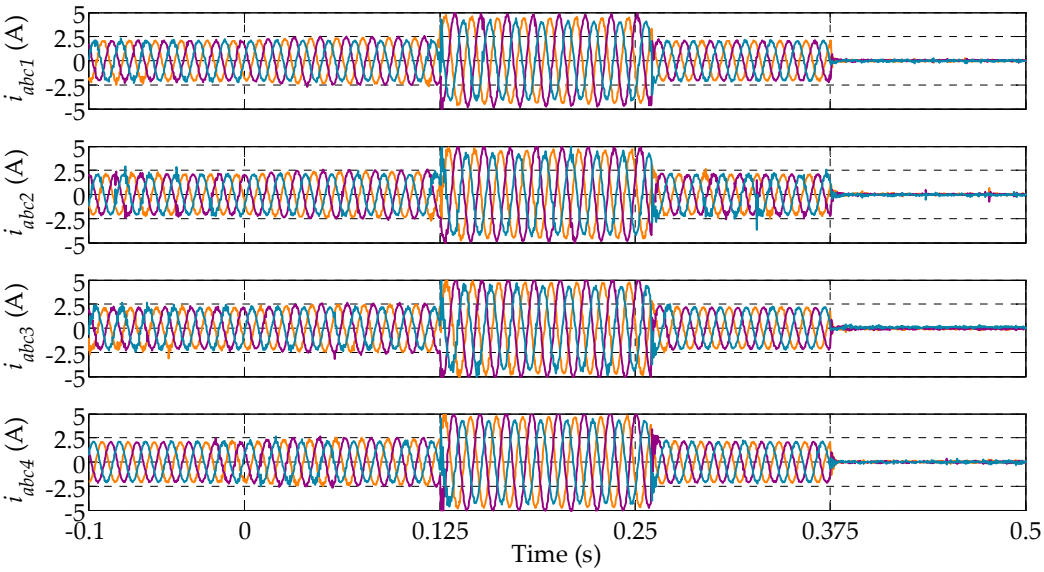

Figure 13. Test 1, sensed phase currents during the voltage sag.

Figure 14 shows the positive and negative sequence voltages during the test. Before the sag, the negative sequences V_{ni} (being the sub index i = 1, 2, 3 and 4) in the four nodes are zero. When the sag starts the positive sequences V_{pi} are reduced to roughly 0.95 p.u. and some negative sequence appears V_{ni} = 0.09 p.u. due to the voltage imbalance. When RCI starts, positive sequences are increased and negative sequences are decreased as stated in (15) and (16). As can be noted in Figure 10, node #1 presents maximum equivalent inductance (4.6 mH) seen from its terminals, thus maximum voltage support is done at this point, i.e., maximum increase in positive sequence voltage V_{p1}. Also it must be noted that the reactive current flowing through line $R_{23}L_{23}$ comes from nodes #1 and #2, which increases the voltage increment at this line. The same applies to $R_{34}L_{34}$ with a high total current coming from nodes #1, #2 and #3. Node #4 presents a minimum equivalent inductance of 0.6 mH, thus voltage support is minimum at this point. In addition, only a slight decrease in the negative sequence V_{ni} can be noted in Figure 14 bottom. This minor effect is because of the negative sequence voltage presents a small magnitude and its effect over the reference currents (13) and (14) is also low.

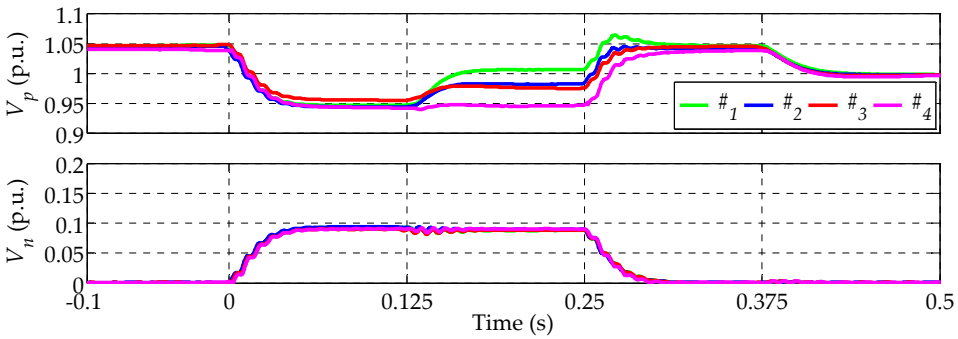

Figure 14. Test 1, positive and negative sequence voltages.

6.2. Test 2a, Islanded Microgrid with Ideal Synchronization

Figure 15 shows a simplified diagram of an islanded μG. Three converters (#1, #2 and #3) are programmed as network-forming voltage sources, emulating dispatchable generation units. Each network-forming node feeds its own local load R_{Li}. Also the global resistive load R_L must be fed. The last converter (#4) is programmed as a power controlled current source used to emulate different load profiles with dynamically changing references P_4* and Q_4*. The main objective of the three nodes that form the μG will be to share cooperatively the total active and reactive powers. The system is driven by a droop controller (32) and (36) plus a consensus secondary controller over UDP/IP communication protocol. It must be noted that a pure-inductive virtual output-impedance has been programmed in the droop controller (R_v = 0 Ω, L_v = 10 mH, see Table 3).

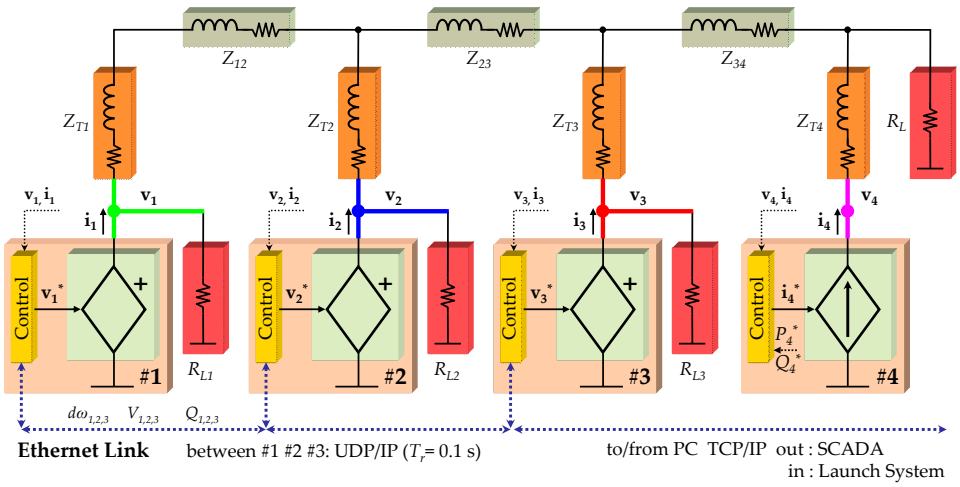

Figure 15. Test 2, diagram of the islanded μG laboratory setup.

Figure 16 shows a black start of the μG and its response for a variable generation profile of node #4. The sequence of events is the following: first at t = 0 there is the black soft-start of node #1 (during 1 s, see Figure 16 middle traces). Initially the fixed load is composed by the global load R_L and the local loads R_{L1}, R_{L2} and R_{L3}. Node #4 begins to inject P_4* = 0.3 kW and Q_4* = −0.27 kVAr (inductive load) at t = 1 s. Between 1 s and 10 s only node #1 feeds the μG. The apparent power fed by node #1 is 2.5 kVAr. At t = 9 s node #2 begins the phase synchronization obtaining θ from the PLL and using it in (30) and (31). At t = 10 s the reference voltage $\mathbf{v_2}$* is synchronized with $\mathbf{v_1}$ and node #2 begins to energize the μG cooperatively with node #1. At t = 20 s node #3 is connected to the grid after its own synchronization period. At t = 25 s node #4 begins a parabolic shape active power generation (emulating a photovoltaic panel), see Figure 16 top.

Figure 16, middle, shows the perfect active power sharing obtained with the two level consensus controller. Figure 16, bottom, shows the node frequencies that present a under/over shot when there is an active power step change. These step changes are produced by the consecutive connection of the three grid-forming nodes. High over/under shots are produced by the quick response of the primary droop controller (proportional controller). Also it can be appreciated that after a small settling time (0.8 s) the secondary controller restores the frequency to its nominal value 60 Hz.

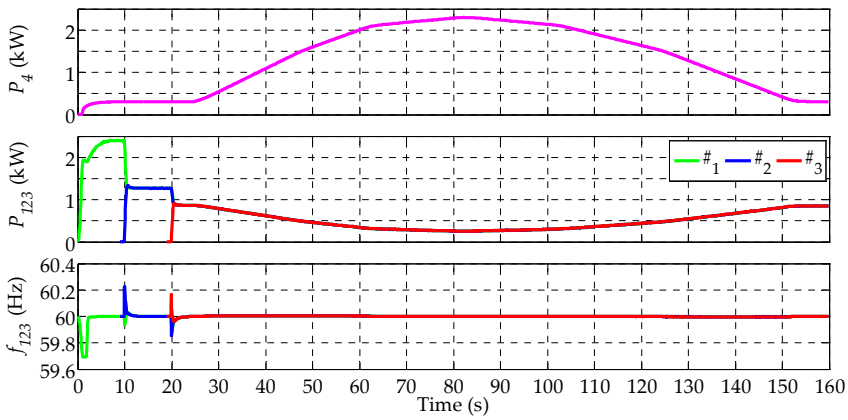

Figure 16. Test 2a, nodes active powers and frequencies, islanded μG.

Figure 17, top, shows the instantaneous reactive power absorbed by node #4. Middle subfigure shows the perfect reactive power sharing obtained thanks to the droop plus consensus controllers. As can be appreciated between t = 1 s and t = 10 s node #1 supplies a reactive power of roughly 0.5 kVAr and the grid-feeding node #4 only demands −0.27 kVAr. The divergence between these two values is due to the inductive power demanded by the grid connections (transformers and wiring lines). Figure 17, bottom, shows the amplitudes at the output of each grid-forming node and also its mean value V_m (black trace), correctly placed at 1 p.u. due to the voltage restoration secondary controller.

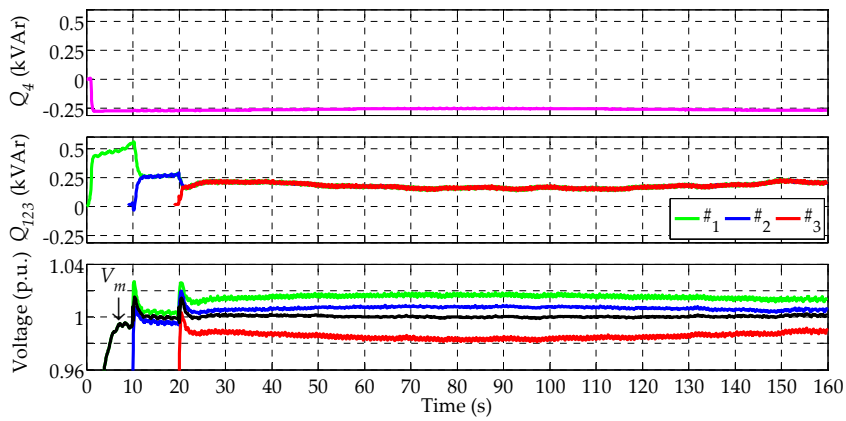

Figure 17. Test 2a, nodes reactive powers and voltage amplitudes, islanded μG.

6.3. Test 2b, Islanded Microgrid with Clock Drift in the DSP Controllers

As described above, each node in the experimental network is driven by its own processor, and thus with their own internal clocks. Therefore, the time signals of each processor will differ from the others due to clock drifts. Then, when testing a system that will work in a real world environment, it is very interesting to analyze the impact of clock drifts on frequency regulation and active power sharing. The drift rate of the Concerto clocks is bounded by 0.99998 and 1.00002 (it uses a crystal oscillating

at 20 MHz with a frequency deviation of 20 parts per million [75]). In order to clearly demonstrate the influence of this parameter, the clock drift rate of the DSPs has been magnified by a factor of 5. In addition, DSP 1 is considered as the global time of the system (to which the other two clock drifts are referenced). Table 4 shows the clock drifts rates of the DSPs for this test.

Table 4. Clock drift rates.

Parameter Name	Acronym	Value
Clock drift rate of digital processor 1	d_1	1.0000
Clock drift rate of digital processor 2	d_2	1.0001
Clock drift rate of digital processor 3	d_3	0.9999

Figure 18 shows the same scenario described in test 2, but with the magnified clock drifts detailed in Table 3. Compared to Figure 16, it is evident that clock drifts introduce a noticeable error in power sharing.

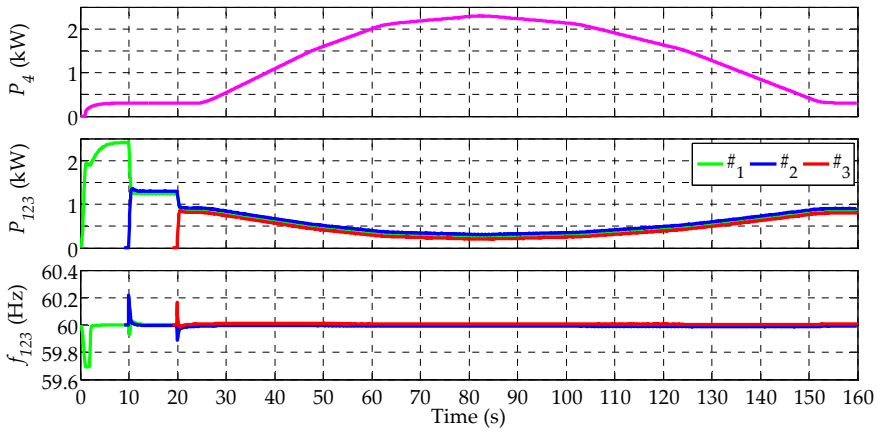

Figure 18. Test 2b, active powers and frequencies, islanded µG with control DSPs desynchronized due to clock drifts.

Figure 19 repeats the experiment but deactivating all the secondary controllers and driving the µG with only the droop-based primary controllers. Obviously, without secondary control, the frequencies of the inverters do not reach the nominal frequency (60 Hz). What it is even more interesting is to note that the error in power sharing is the same that in previous test. Therefore, the clock drift impacts seriously in the droop-based primary control and the effect is nearly negligible in consensus-based secondary control.

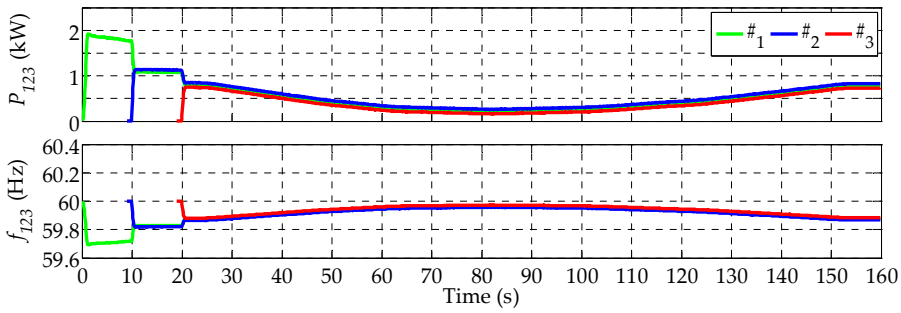

Figure 19. Test 2b, active powers and frequencies, islanded microgrid with control DSPs desynchronized due to clock drifts. Only primary controller activated.

7. Conclusions

This work has comprehensively described a testbed that emulates a distributed generation network based on three-phase power inverters. A detailed explanation about the hardware implementation has been provided. The control platform, the software basics and the communication requirements have also been described in detail. The main objective of the setup is to obtain experimental results which can confirm the validity of different control proposals. The testbed presents high flexibility because it can be configured to emulate different distributed power-network scenarios. In this work two scenarios have been considered, an islanded network and a grid connected network. For each scenario one state-of-the-art controller has been presented. A complete experimental section has demonstrated the interesting and flexible behavior of the described testbed.

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References

1. Adefarati, T.; Bansal, R.C. Integration of renewable distributed generators into the distribution system: A review. *IET Renew. Power Gener.* **2016**, *10*, 873–884. [CrossRef]
2. Ma, Z.; Callaway, D.; Hiskens, I.A. Decentralized charging control of large populations of plug-in electric vehicles. *IEEE Trans. Control Syst. Technol.* **2013**, *21*, 67–78. [CrossRef]
3. Kundu, S.; Hiskens, I.A. Overvoltages due to synchronous tripping of plug-in electric-vehicle chargers following voltage dips. *IEEE Trans. Power Del.* **2014**, *29*, 1147–1156. [CrossRef]
4. IEEE Standards Association. *IEEE Application Guide for IEEE Std 1547, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems*; IEEE Std. 1547.2-2008; IEEE Standards Association: Piscataway, NJ, USA, 2009.
5. Altin, M.; Goksu, O.; Teodorescu, R.; Rodriguez, P.; Jensen, B.-B.; Helle, L. Overview of recent grid codes for wind power integration. In Proceedings of the 12th International Conference on Optimization of Electrical and Electronic Equipment, Brasov, Romania, 20–22 May 2010; pp. 1152–1160.
6. Troester, E. New German grid codes for connecting PV systems to the medium voltage power grid. In Proceedings of the 2nd International Workshop Concentrating Photovoltaic Power Plants, Darmstadt, Germany, 9–10 March 2009; pp. 1–4.
7. Rocabert, J.; Azevedo, G.M.S.; Luna, A.; Guerrero, J.M.; Candela, J.I.; Rodríguez, P. Intelligent connection agent for three-phase grid-connected microgrids. *IEEE Trans. Power Electron.* **2011**, *26*, 2993–3005. [CrossRef]
8. Rocabert, J.; Luna, A.; Blaabjerg, F.; Rodríguez, P. Control of power converters in AC microgrids. *IEEE Trans. Power Electron.* **2012**, *27*, 4734–4749. [CrossRef]
9. Bollen, M.H.J. *Understanding Power Quality Problems: Voltage Sags and Interruptions*, 1st ed.; IEEE Press: New York, NY, USA, 2000.
10. Milicua, A.; Abad, G.; Rodriguez Vidal, M.A. Online reference limitation method of shunt-connected converters to the grid to avoid exceeding voltage and current limits under unbalanced operation—Part I: Theory. *IEEE Trans. Energy Convers.* **2015**, *30*, 852–863. [CrossRef]
11. Guo, X.; Zhang, X.; Wang, B.; Wu, W.; Guerrero, J.M. Asymmetrical grid fault ride-through strategy of three-phase grid-connected inverter considering network impedance impact in low-voltage grid. *IEEE Trans. Power Electron.* **2014**, *29*, 1064–1068. [CrossRef]
12. Tsili, M.; Papathanassiou, S. A review of grid code technical requirements for wind farms. *IET Renew. Power Gen.* **2009**, *3*, 308–332. [CrossRef]
13. Camacho, A.; Castilla, M.; Miret, J.; Borrell, A.; Garcia de Vicuña, L. Active and reactive power strategies with peak current limitation for distributed generation inverters during unbalanced grid faults. *IEEE Trans. Ind. Electron.* **2015**, *62*, 1515–1525. [CrossRef]

14. Miret, J.; Camacho, A.; Castilla, M.; García de Vicuña, J.L.; de la Hoz, J. Reactive current injection protocol for low-power rating distributed generation sources under voltage sags. *IET Power Electron.* **2015**, *8*, 879–886. [CrossRef]
15. Guerrero, J.M.; Chandorkar, M.; Lee, T.-L.; Loh, P.C. Advanced control architectures for intelligent microgrids—Part I: Decentralized and hierarchical control. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1254–1262. [CrossRef]
16. Guerrero, J.M.; Loh, P.C.; Lee, T.-L.; Chandorkar, M. Advanced control architectures for intelligent microgrids—Part II: Power quality, energy storage, and AC/DC microgrids. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1263–1270. [CrossRef]
17. Lasseter, R.; Piagi, P. MicroGrids: A conceptual solution. In Proceedings of the IEEE 35th Power Electronics Specialists Conference, Aachen, Germany, 20–25 June 2004; pp. 4285–4290.
18. Tuladhar, A.; Jin, H.; Unger, T.; Mauch, K. Control of parallel inverters in distributed AC power systems with consideration offline impedance. *IEEE Trans. Ind. Appl.* **2000**, *36*, 321–328. [CrossRef]
19. Lopes, J.A.P.; Moreira, C.L.; Madureira, A.G. Defining control strategies for microgrids islanded operation. *IEEE Trans. Power Systems.* **2006**, *21*, 916–924. [CrossRef]
20. Nasirian, V.; Shafiee, Q.; Guerrero, J.M.; Lewis, F.L.; Davoudi, A. Droop-free distributed control for AC microgrids. *IEEE Trans. Power Electron.* **2016**, *31*, 1600–1617. [CrossRef]
21. Liu, W.; Gu, W.; Sheng, W.; Meng, X.; Wu, Z.; Chen, W. Decentralized multi-agent system-based cooperative frequency control for autonomous microgrids with communication constraints. *IEEE Trans. Sustain. Energy* **2014**, *5*, 446–456. [CrossRef]
22. Guo, F.; Wen, C.; Mao, J.; Song, Y.-D. Distributed secondary voltage and frequency restoration control of droop-controlled inverter-based microgrids. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4355–4364. [CrossRef]
23. Lu, L.Y.; Chu, C.C. Consensus-based droop control synthesis for multiple DICs in isolated micro-grids. *IEEE Trans. Power Syst.* **2015**, *30*, 2243–2256. [CrossRef]
24. Xin, H.; Zhao, R.; Zhang, L.; Wang, Z.; Wong, K.P.; Wei, W. A decentralized hierarchical control structure and self-optimizing control strategy for F-P type DGs in islanded microgrids. *IEEE Trans. Smart Grid.* **2016**, *7*, 3–5. [CrossRef]
25. Hua, M.; Hu, H.; Xing, Y.; Guerrero, J.M. Multilayer control for inverters in parallel operation without intercommunications. *IEEE Trans. Power Electron.* **2012**, *27*, 3651–3663. [CrossRef]
26. Rey, J.M.; Marti, P.; Velasco, M.; Miret, J.; Castilla, M. Secondary Switched Control with no Communications for Islanded Microgrids. *IEEE Trans. Ind. Electron.* **2017**, in press. [CrossRef]
27. Lidula, N.; Rajapakse, A. Microgrids research: A review of experimental microgrids and test systems. *Renew. Sustain. Energy Rev.* **2011**, *15*, 186–202. [CrossRef]
28. Lasseter, R.H.; Eto, J.H.; Schenkman, B.; Stevens, J.; Vollkommer, H.; Klapp, D.; Linton, E.; Hurtado, H.; Roy, J. CERTS microgrid laboratorytest bed. *IEEE Trans. Power Del.* **2011**, *26*, 325–332. [CrossRef]
29. Salehi, V.; Mohamed, A.; Mazloomzadeh, A.; Mohammed, O.A. Laboratory-based smart power system, Part I: Design and system development. *IEEE Trans. Smart Grid.* **2012**, *3*, 1394–1404. [CrossRef]
30. Salehi, V.; Mohamed, A.; Mazloomzadeh, A.; Mohammed, O.A. Laboratory-based smart power system, Part II: Control, monitoring, and protection. *IEEE Trans. Smart Grid.* **2012**, *3*, 1405–1417. [CrossRef]
31. Rasheduzzaman, M.; Chowdhury, B.H.; Bhaskara, S. Converting an old machines lab into a functioning power network with a microgrid for education. *IEEE Trans. Power Syst.* **2014**, *29*, 1952–1962. [CrossRef]
32. Meng, L.; Luna, A.; Rodríguez Díaz, E.; Sun, B.; Dragicevic, T.; Savaghebi, M.; Vasquez, J.C.; Guerrero, J.M.; Graells, M.; Andrade, F. Flexible system integration and advanced hierarchical control architectures in the microgrid research laboratory of Aalborg University. *IEEE Trans. Ind. Appl.* **2016**, *52*, 1736–1749. [CrossRef]
33. Buccella, C.; Cecati, C.; Latafat, H. Digital control of power converters—A survey. *IEEE Trans. Industr. Inform.* **2012**, *8*, 437–447. [CrossRef]
34. Pacific Power Source. Available online: https://pacificpower.com/Resources/Documents/360AMX_Datasheet.pdf (accessed on 10 July 2017).
35. American Reliance. Available online: http://www.programmablepower.com/products (accessed on 10 July 2017).
36. Bueno, E.J.; Hernandez, A.; Rodriguez, F.J.; Giron, C.; Mateos, R.; Cobreces, S. A DSP- and FPGA-based industrial control with high-speed communication interfaces for grid converters applied to distributed power generation systems. *IEEE Trans. Ind. Electron.* **2009**, *56*, 654–669. [CrossRef]

37. Lu, X.; Guerrero, J.M.; Sun, K.; Vasquez, J.C.; Teodorescu, R.; Huang, L. Hierarchical Control of Parallel AC-DC Converter Interfaces for Hybrid Microgrids. *IEEE Trans. Smart Grid.* **2014**, *5*, 683–692. [CrossRef]
38. Mandal, K.; Banerjee, S. Synchronization phenomena in microgrids with capacitive coupling. *IEEE Trans. Emerg. Sel. Top. Circuits Syst.* **2015**, *5*, 364–371. [CrossRef]
39. Velasco, M.; Marti, P.; Camacho, A.; Miret, J.; Castilla, M. Synchronization of local integral controllers for frequency restoration in islanded microgrids. In Proceedings of the 42nd Annual Conference of the IEEE Industrial Electronics Society, Firenze, Italy, 24–27 October 2016.
40. Schiffer, J.; Ortega, R.; Hans, C.A.; Raisch, J. Droop-controlled inverter-based microgrids are robust to clock drifts. In Proceedings of the 2015 American Control Conference, Chicago, IL, USA, 1–3 July 2015; pp. 2341–2346.
41. Schiffer, J.; Hans, C.A.; Kral, T.; Ortega, R.; Raisch, J. Modelling, analysis and experimental validation of clock drift effects in low-inertia power systems. *IEEE Trans. Ind. Electron.* **2016**, *64*, 5942–5951. [CrossRef]
42. Torres-Martínez, J.; Castilla, M.; Miret, J.; Rey, J.M.; Moradi-Ghahderijani, M. Experimental study of clock drift impact over droop-free distributed control for industrial microgrids. In Proceedings of the 42nd Annual Conference of the IEEE Industrial Electronics Society, Beijing, China, 29 October–1 November 2017.
43. Decotignie, J.D. Ethernet-based real-time and industrial communications. *Proc. IEEE* **2005**, *93*, 1102–1117. [CrossRef]
44. Texas Instruments, F28M36x Concerto Microcontrollers Report SPRS825C. Available online: http://www.ti.com/product/F28M36P63C2 (accessed on 10 July 2017).
45. Texas Instruments, H63C2 Concerto Experimenter Kit. Available online: http://www.ti.com/tool/tmdsdock28m36 (accessed on 10 July 2017).
46. MTL-CBI0060F12IXHF Data Sheet. Available online: http://www.e-guasch.com (accessed on 10 July 2017).
47. Figueres, E.; Garcera, G.; Sandia, J.; Gonzalez-Espin, F.; Rubio, J.C. Sensitivity study of the dynamics of three-phase photovoltaic inverters with an LCL grid filter. *IEEE Trans. Ind. Electron.* **2009**, *56*, 706–717. [CrossRef]
48. Liserre, M.; Teodorescu, R.; Blaabjerg, F. Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values. *IEEE Trans. Power Electron.* **2006**, *21*, 263–272. [CrossRef]
49. Liu, J.; Zhou, L.; Yu, X.; Li, B.; Zheng, C. Design and analysis of an LCL circuit-based three-phase grid-connected inverter. *IET Power Electron.* **2017**, *10*, 232–239. [CrossRef]
50. Blaabjerg, F.; Teodorescu, R.; Liserre, M.; Timbus, A.V. Overview of control and grid synchronization for distributed power generation systems. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1398–1409. [CrossRef]
51. Zmood, D.N.; Holmes, D.G.; Bode, G.H. Frequency-domain analysis of three-phase linear current regulators. *IEEE Trans. Ind. Appl.* **2001**, *37*, 601–610. [CrossRef]
52. Bollen, M.H.J. Algorithms for characterizing measured three phase unbalanced voltage dips. *IEEE Trans. Power Del.* **2003**, *18*, 937–944. [CrossRef]
53. Matas, J.; Castilla, M.; Miret, J.; Garcia de Vicuña, L.; Guzman, R. An adaptive pre-filtering method to improve the speed/accuracy trade-off of voltage sequence detection methods under adverse grid conditions. *IEEE Trans. Ind. Electron.* **2014**, *61*, 2139–2151. [CrossRef]
54. Sosa, J.L.; Castilla, M.; Miret, J.; Matas, J.; Al-Turki, Y.A. Control strategy to maximize the power capability of PV three-phase inverters during voltage sags. *IEEE Trans. Power Electron.* **2016**, *31*, 3314–3323. [CrossRef]
55. Trujillo Rodriguez, C.; Velasco de la Fuente, D.; Garcera, G.; Figueres, E.; Guacaneme Moreno, J.A. Reconfigurable control scheme for a PV microinverter working in both grid-connected and island modes. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1582–1595. [CrossRef]
56. Baran, M.E.; El-Markabi, I.M. A multiagent-based dispatching scheme for distributed generators for voltage support on distribution feeders. *IEEE Trans. Power Syst.* **2007**, *22*, 52–59. [CrossRef]
57. Bottura, R.; Borghetti, A. Simulation of the Volt/Var control in distribution feeders by means of a networked multiagent system. *IEEE Trans. Ind. Inform.* **2014**, *10*, 2340–2353. [CrossRef]
58. Camacho, A.; Castilla, M.; Miret, J.; Matas, J.; Guzman, R.; de Sousa-Pérez, O.; Martí, P.; García de Vicuña, L. Control strategies based on effective power factor for distributed generation power plants during unbalanced grid voltage. In Proceedings of the 39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, Austria, 10–13 November 2013; pp. 7134–7139.

59. Miret, J.; Camacho, A.; Castilla, M.; Garcia de Vicuña, L.; Matas, J. Control scheme with voltage support capability for distributed generation inverters under voltage sags. *IEEE Trans. Power Electron.* **2013**, *28*, 5252–5262. [CrossRef]
60. Rodriguez, P.; Timbus, A.V.; Teodorescu, R.; Liserre, M.; Blaabjerg, F. Flexible active power control of distributed power generation systems during grid faults. *IEEE Trans. Ind. Electron.* **2007**, *54*, 2583–2592. [CrossRef]
61. Camacho, A.; Castilla, M.; Miret, J.; Vasquez, J.C.; Alarcon-Gallo, E. Flexible voltage support control for three-phase distributed generation inverters under grid fault. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1429–1441. [CrossRef]
62. Vasquez, J.C.; Guerrero, J.M.; Miret, J.; Castilla, M.; Garcia de Vicuña, L. Hierarchical control of intelligent microgrids. *IEEE Ind. Electron. Mag.* **2010**, *4*, 23–29. [CrossRef]
63. Guerrero, J.M.; Vasquez, J.C.; Matas, J.; Garcia de Vicuña, L.; Castilla, M. Hierarchical control of droop-controlled AC and DC microgrids—A general approach towards standardization. *IEEE Trans. Ind. Electron.* **2011**, *58*, 158–172. [CrossRef]
64. Li, B.; Zhou, L.; Yu, X.; Zheng, C.; Liu, J. Improved power decoupling control strategy based on virtual synchronous generator. *IET Power Electronics.* **2017**, *10*, 462–470. [CrossRef]
65. Guerrero, J.M.; Garcia de Vicuna, L.; Matas, J.; Castilla, M.; Miret, J. Output impedance design of parallel-connected UPS inverters with wireless load-sharing control. *IEEE Trans. Ind. Electron.* **2005**, *52*, 1126–1135. [CrossRef]
66. He, J.; Li, Y.W. Analysis, design, and implementation of virtual impedance for power electronics interfaced distributed generation. *IEEE Trans. Ind. Appl.* **2011**, *47*, 2525–2538. [CrossRef]
67. Vasquez, J.C.; Guerrero, J.M.; Savaghebi, M.; Eloy-Garcia, J.; Teodorescu, R. Modeling, analysis, and design of stationary-reference-frame droop-controlled parallel three-phase voltage source inverters. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1271–1280. [CrossRef]
68. Katiraei, F.; Iravani, R.; Hatziargyriou, N.; Dimeas, A. Microgrids management. *IEEE Power Energy Mag.* **2008**, *6*, 54–65. [CrossRef]
69. Walsh, G.C.; Ye, H. Scheduling of networked control systems. *IEEE Control Systems Mag.* **2001**, *21*, 57–65. [CrossRef]
70. Lightweight IP. Available online: http://savannah.nongnu.org/projects/lwip (accessed on 10 July 2017).
71. Using the Stellaris® Ethernet Controller with Lightweight IP (lwIP). Texas Instruments Application Report SPMA025C. Available online: http://www.ti.com/lit/an/spma025c/spma025c.pdf (accessed on 10 July 2017).
72. Castilla, M. (Ed.) *Control Circuits in Power Electronics: Practical Issues in Design and Implementation*; IET Press: London, UK, 2016.
73. Debug Server Scripting. Available online: http://processors.wiki.ti.com/index.php (accessed on 10 July 2017).
74. Code Composer Studio (CCS) Integrated Development Environment (IDE). Available online: http://www.ti.com/tool/ccstudio (accessed on 10 July 2017).
75. Texas Instruments, Schematics F28M36x Control CARD. Available online: http://www.ti.com/tool/tmdscncd28m36 (accessed on 10 July 2017).

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