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A Method for the Realization of an Interruption Generator Based on Voltage Source Converters

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Abstract: In this paper we described the structure and working principle of an interruption generator based on voltage source converters (VSCs). The main circuit parameters of the VSCs are determined according to the target of power transfer capability, harmonic suppression, and dynamic response capability. A state feedback linearization method in nonlinear differential geometry theory was used for dq axis current decoupling, based on the mathematical model used in the dq coordinate system of VSCs. The direct current control strategy was adopted to achieve the independent regulation of active power and reactive power. The proportional integral (PI) link was used to optimize the dynamic performance of the controller, and PI parameters were adjusted. Disturbance voltage waves were generated by the regular sampling method. PSCAD/EMTDC simulation results and physical prototype experiments showed that the device could generate various disturbance voltage waveforms steadily, and had good dynamic and steady-state performance.

Keywords: power quality; interruption; voltage source converter; power control

1. Introduction

With the rapid development of technology, the load structure of the power system has changed a lot in recent years. A large number of non-linear loads have resulted in power quality problems such as voltage fluctuations, distortions, and unbalanced connections to the power system [1–4]. With the improvement of China's industrial automation, the precise automatic equipment used is very sensitive to power quality, and power quality problems might cause equipment stoppages. Problems of power quality monitoring, analysis, and management have thus become important issues in electric power supply and utilization [5]. In view of this, a power interruption generator can be used to provide disturbance signal sources to test the correctness of the power quality analysis theory, or examine power quality control devices. In addition, a power interruption generator can also be used to test the operation characteristics of electric power equipment under disturbance conditions. Research on these interruption generators has been focused on trying to achieve flexibility, regulation, and high precision [6].

At present, most power quality interruption generators are designed based on power electronics [7]. The Shanxi Electric Power Research Institute has come up with a power quality interruption device that can simulate the voltage output and current disturbance of a power system. The device has the characteristics of good output waveform, large power, and high voltage grade, and can output the waveforms of voltage sag, voltage fluctuation and flicker, voltage harmonic, current harmonic, and the unbalanced 3-phase voltage and current [8]. A series hybrid power quality interruption generator was developed by the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources of North China Electrical University, and it was based on carrier phase –shifting sinusoidal pulse width modulation [9]. In [10], a back to back 2 H bridge

is used in the main circuit structure and a multi-level cascade is used in voltage source inverter. Both these devices have the advantages of flexibility and diversity. However, their structures are complex [11]. In [12], it proposed a new design of power electronic voltage interruption generator. It adopts uncontrollable rectifier and booster circuit. It can only simulate voltage swell and sag, but its duration, depth, start-stop phase and type can all be adjusted smoothly.

The method of using the phase shift circuit to regulate transformer taps to produce disturbances has been used in many other devices. These devices are less expensive and stable in operation, but have potential problems such as inconvenient settings, a single disturbance wave, and so on. A device developed by the University of Arizona provides the disturbance signal source by means of a circuit switch and transformer tap controlled by a simulated phase-shift circuit [13]; however, the device can only realize the voltage sag waveform and is unable to adjust continuously. In [14], a scheme based on interleaved paralleled H-bridges topology was proposed. It presented a control method composed of DC voltage feed forward control and a phase shifting PWM method. The scheme reduces the load regulation of the large capacity voltage interruption generator; however, the design of the output impedance parameters is inconvenient for the small capacity one. The synchronous compensator is convenient in realizing power disturbances, but its scope of application is limited by its weight and volume.

In this paper, we presented the idea of applying voltage source converters (VSCs) to the interruption generator to deal with their shortcomings. Compared with the current devices, the interruption generator based on VSCs has a simpler main circuit, but it still has good dynamic and steady-state performance and it can generate various disturbance voltage waveforms compared with the devices that use the phase shift circuit to regulate transformer taps. The rest of this paper is organized as follows: Section 2 gives a mathematical model of the interruption generator based on VSCs in an abc coordinate system. The influence on the system and the selection principle of the main circuit parameters are also analyzed. Section 3 discusses the control objectives; the grid side converter provides a stable DC voltage while the load side converter provides the disturbance waveform according to the specified modulation wave. The power decoupling controller is designed based on the nonlinear feedback linearization theory, and the dynamic performance of the controller is optimized based on the classical control theory. In Section 4, the dynamic and steady-state performance of the controller is verified by PSCAD/EMTDC (Version 4.2.0, Manitoba HVDC Research Centre, Winnipeg, MB, Canada) simulation results. Then, in Section 5, a physical prototype is designed to prove the simulation results in Section 4. Finally, Section 6 presents our conclusions.

2. Structure of the Main Circuit in VSCs

The structure diagram of an interruption generator based on the VSC is given in Figure 1. The controlled rectifier transforms the AC voltage into a high precision DC voltage. The inverter is used to generate a specified disturbance voltage for the load.

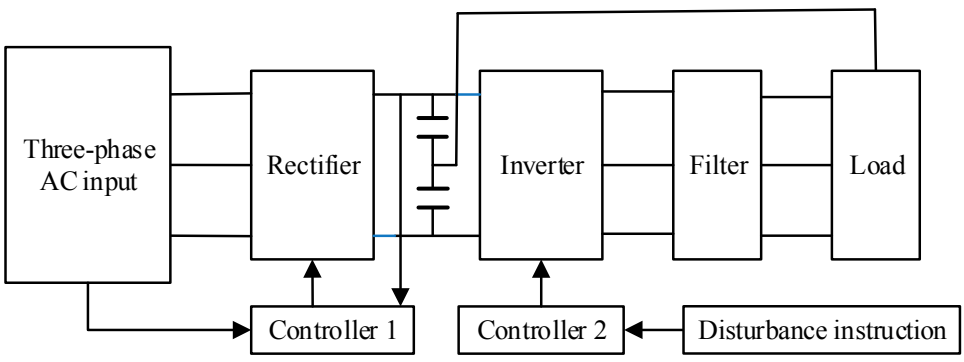

Figure 1. Structure diagram of the proposed system.

2.1. Mathematical Models in an abc Coordinate System

To simplify the study, we made two assumptions:

(1) A 3-phase infinite power supply is ideal and symmetrical.
(2) The switch is ideal, and its switching-delay is ignored.

The single side topology of the VSC is shown in Figure 2. E_{sa}, E_{sb}, and E_{sc} are AC voltages; i_a, i_b, and i_c are AC input currents; U_a, U_b, and U_c are AC side output voltages of the converter; i_L is the load current; R is the equivalent resistance; L is AC filter reactance; and C is the DC side capacitor.

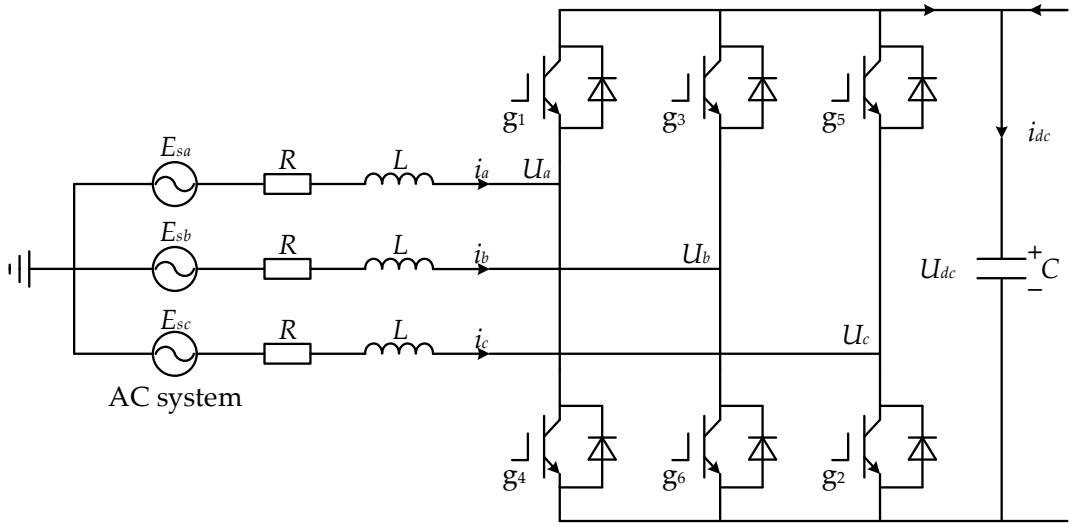

Figure 2. Structure diagram of the topology.

The mathematical model of the converter can be expressed as follows:

$$\begin{cases} L\frac{di_a}{dt} = E_{sa} - Ri_a - U_a \\ L\frac{di_b}{dt} = E_{sb} - Ri_b - U_b \\ L\frac{di_c}{dt} = E_{sc} - Ri_c - U_c \\ C\frac{dU_{dc}}{dt} = i_s - i_L \end{cases} \quad (1)$$

2.2. The Design of AC Side Inductance

According to Equation (1), the equivalent circuit of the AC side is shown in Figure 3. Since the filter inductance has a restraining effect on the high frequency current component, the fundamental component frequency current is the only component that should be considered. In addition, the filter inductance also stores reactive power, which flows in 3-phase circuits. When the capacity of the device is fixed, a large reactive power will reduce the transmission capability of the active power, thus reducing the efficiency of the device. As a result, there is an upper limit on the selection of the inductance. Meanwhile, the filter inductor also plays a role in restraining the sudden change in current. Therefore, there is also a lower limit on the selection of the inductance [15,16].

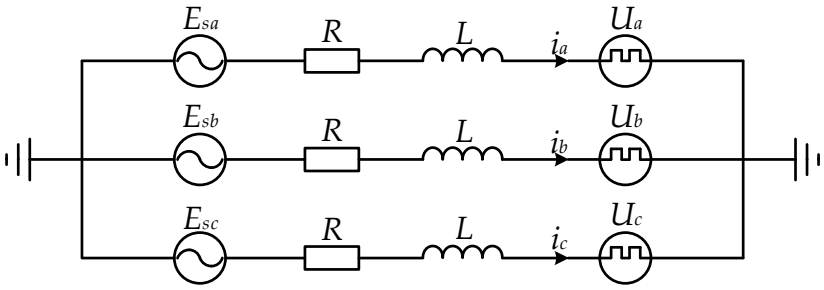

Figure 3. Structure diagram of the AC side equivalent circuit.

Three indices are defined as follows for the limits of the inductance:

(1) The steady-state active transmission capacity index: the inductance voltage should not be greater than 20% of the AC rated voltage.
(2) Transient operation performance: the current variation in a control cycle should be less than 10% of the AC rated current. It reflects the transient condition constraints.
(3) Filtering performance: the total harmonic distortion of current should be less than or equal to 5%.

According to the above indices, which are related to device capacity, AC voltage, DC capacitor voltage, control cycle, and other parameters [17,18], the expression of the inductance selection is shown in Equation (2):

$$\frac{(2u_{dc} + 3E_{sa})E_{sa}T_s \cos\varphi}{0.4P_L} \leq L \leq \frac{3E_{sa}^2 \cos\varphi}{10\omega P_L} \tag{2}$$

2.3. The Design of DC Side Capacitor

As shown in Equation (1), the increase of the DC side capacitor C can reduce the voltage fluctuation. Meanwhile, the capacitor cannot be too large considering the size and cost of the device. The main reason for causing the DC voltage fluctuation is the difference of instantaneous power between the rectifier and the inverter [19]. During device testing, the maximum power change occurs at the moment of loading, when the power of the DC side capacitor suddenly changes from 0 to P. However, when the device is applied to power quality problems in a lab, there may be backward power flow, that is to say, the operation performance of the inverter changes from the absorbed power P to the feedback power P, and the fluctuation of the DC side voltage is the most severe at this time [20,21]. The DC side voltage fluctuation rate is defined as 10% in a control cycle. Considering the characteristic of the capacitor element, the expression of the capacitance C is as follows:

$$C \geq \frac{20P_{\max}T_s}{u_{dc}\Delta u_{dc\max}} \tag{3}$$

2.4. Constraint of Disturbance Load

The choice of the disturbance load is limited when the DC side voltage is stable [22]. If the load is very small, it will inevitably lead to a larger load current and the power for the load demand will be greater. When the power of the load exceeds the capacity of the device, the DC side voltage will no longer be stable, and voltage drop will occur. In addition, the current should be less than the maximum allowable current of the power device, otherwise the device will be burned out [23–25]. Therefore, the minimum load is subject to the two constraints above, as shown in Equation (4). $S_{\max}$ is the capacity of AC power, and $I_{\max}$ is the maximum current through the switching device.

$$Z > \max\left(\frac{u_{dcref}^2}{S_{\max}}, \frac{u_{dcref}}{I_{\max}}\right) \tag{4}$$

3. Design of the Controller Device

3.1. Dynamic Mathematical Model in dq Coordinate System

For a 3-phase power supply, the d axis is coincided with the space vector, and the d axis is $\pi/2$ ahead of the q axis. $E_{sd} = U_m$, and $E_{sq} = 0$. The Kirchhoff equations and power equations of the rectifier in the rotating dq coordinate system are shown in Equations (5) and (6):

$$\begin{pmatrix} L\frac{di_d}{dt} \\ L\frac{di_q}{dt} \\ C\frac{du_{dc}}{dt} \end{pmatrix} = \begin{pmatrix} E_{sd} \\ E_{sq} \\ 0 \end{pmatrix} - \begin{pmatrix} R & -\omega L & m_d \\ \omega L & R & m_q \\ -m_d & -m_q & 0 \end{pmatrix} \begin{pmatrix} i_d \\ i_q \\ u_{dc} \end{pmatrix} - \begin{pmatrix} 0 \\ 0 \\ i_L \end{pmatrix} \tag{5}$$

$$\begin{cases} P = E_{sd} i_d \\ Q = E_{sd} i_q \end{cases} \tag{6}$$

The function of the rectifier is to stabilize the DC side voltage, that is to say, the essence of the rectifier is to control the power supply to inject the active power into the DC side capacitor. The design of the power controller is based on Equation (6). The active and reactive power of the AC side power supply are respectively proportional to the current of the d axis and q axis. Based on the above analysis, the direct current control strategy is determined [26].

3.2. Decoupling Method Based on State Feedback Linearization

Based on Equation (5), there is a coupling between i_d and i_q. That is to say, there is a coupling between P and Q, which brings great inconvenience to the design of the controller. The nonlinear state feedback linearization theory is a powerful tool for solving this kind of problem. This theory makes the non-linear systems linearized by non-linear coordinate transformation over a wide range. This enables the multiple input and output system to be linearized and decoupled at the same time [27,28].

The state equations and output equations of the decoupled controllable linear system by coordinate transformation and state feedback are shown in Equation (7):

$$\begin{cases} \begin{bmatrix} \frac{dz_1}{dt} \\ \frac{dz_2}{dt} \end{bmatrix} = -k \begin{bmatrix} z_1 \\ z_2 \end{bmatrix} + k \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \\ \begin{bmatrix} Y_1 \\ Y_2 \end{bmatrix} = \begin{bmatrix} z_1 \\ z_2 \end{bmatrix} \end{cases} \tag{7}$$

The state variables z_1 and z_2 are equal to i_d and i_q, respectively. According to the optimal control theory, the relations between the new input variables, v_1 and v_2, and state variables can be represented as:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \begin{bmatrix} z_1 \\ z_2 \end{bmatrix} \tag{8}$$

Based on Equations (7) and (8), a set of output variables i_d and i_q corresponds to a set of reference values i_{dref} and i_{qref} of the dq axis currents. Thus, direct current control is achieved. The power switch function, which is applied in the power switch by sinusoidal pulse width modulation (SPWM) is deduced as in Equation (9):

$$\begin{pmatrix} m_d \\ m_q \end{pmatrix} = \frac{1}{u_{dc}} \begin{pmatrix} -Rx_1 + \omega x_2 L - \dot{z}_1 L + E_{sd} \\ -\omega x_1 L - Rx_2 - \dot{z}_1 L \end{pmatrix} \tag{9}$$

3.3. Optimization of Controller Dynamic Performance

The closed-loop transfer function of current shown in Equation (10) is derived from the Laplace transform of the Equation (7):

$$\begin{cases} \Phi_{id}(s) = \frac{i_d(s)}{i_{dref}(s)} = \frac{k}{s+k} \\ \Phi_{iq}(s) = \frac{i_q(s)}{i_{qref}(s)} = \frac{k}{s+k} \end{cases} \tag{10}$$

According to Equations (7) and (10), the closed-loop transfer function of current is a first-order inertial element. The classical control theory shows that the first-order inertial element provides good dynamic properties and there is no overshoot, static error or oscillation in the system. The stability of the system is determined by the proportionality coefficient k. According to the Routh criterion, if $k > 0$, the system is stable, that is to say, the closed-loop poles should be in the left half plane of the s domain. And the response speed can be regulated by adjusting k.

The device is controlled by digital signal processors. In digital control systems, the sampling delay and the switching delay are related to the control cycle T_c. The sampling delay time is equal to the control cycle. And the switch has two states: turn-on and turn-off in one control cycle, so the switching delay cycle is half of the control cycle. The dynamic block diagram of the current loop is shown in Figure 4.

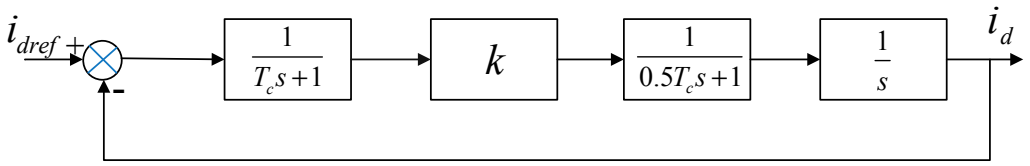

Figure 4. Dynamic block diagram of the current loop.

The frequency of the electronic power switch is high. The s^2 term coefficient is much smaller than the s term coefficient after the combination of the delay link. Therefore, the s^2 term can be neglected, and the open-loop transfer function is expressed as:

$$G_i(s) = \frac{k}{s(1.5T_c s + 1)} \tag{11}$$

where k is the proportionality coefficient and T_c is the control cycle. Equation (12) is the closed-loop characteristic equation of the current loop system:

$$s^2 + \frac{1}{1.5T_c}s + \frac{k}{1.5T_c} = 0 \tag{12}$$

The angular frequency and damping ratio of the system is expressed as:

$$\begin{cases} \omega_n = \sqrt{\frac{k}{1.5T_c}} \\ \xi = \frac{1}{2}\sqrt{\frac{1}{1.5kT_c}} \end{cases} \tag{13}$$

The overshoot and adjusting time of the system are shown in Equation (14). In this paper, we defined the current tracking index as the overshoot $\sigma\% < 10\%$ and the adjusting time $t_s < 5$ ms. The proportionality coefficient k can be calculated according to Equations (12) and (13):

$$\begin{cases} \sigma\% = e^{-\pi\xi/\sqrt{1-\xi^2}} \times 100\% \\ t_s = \frac{4.5}{\xi\omega_n} \end{cases} \tag{14}$$

Equations (10)–(14) express the rapidity and stability of current tracking. However, there is a condition that the inductance L and the equivalent resistance R be completely determined. In actual engineering, reactors are usually installed on the grid side, and the inductance on the transmission line is very small compared with the reactors. Therefore, the transmission line inductance can be neglected and the inductance L of the system can be considered as accurate. The equivalent resistance R is the grid side equivalent loss resistance of the device and is not easy to determine. It is related to the line loss, the switching loss, and temperature [29]. Based on Equation (9), the power switch function considering the disturbance resistance ΔR is expressed as:

$$\begin{pmatrix} m_d \\ m_q \end{pmatrix} = \frac{1}{u_{dc}} \begin{pmatrix} -(R+\Delta R)x_1 + \omega x_2 L - \dot{z}_1 L + E_{sd} \\ -\omega x_1 L - (R+\Delta R)x_2 - \dot{z}_1 L \end{pmatrix} \tag{15}$$

Based on Equations (5) and (15), the open loop transfer function of the current-loop considering the disturbance resistance ΔR is shown in Equation (16). The d axis current has the same open-loop transfer function as the q axis current, therefore, we take the d axis current as an example:

$$G_{id}(s) = \frac{kL}{sL + \Delta R}, \tag{16}$$

The switching delay and sampling delay make the order of the system transfer function higher. The PI link is used to reduce the order and improve its stability. In order to simplify the design, k is set to 1, and the dynamic block diagram of the current loop considering resistance disturbance and system delay is shown in Figure 5.

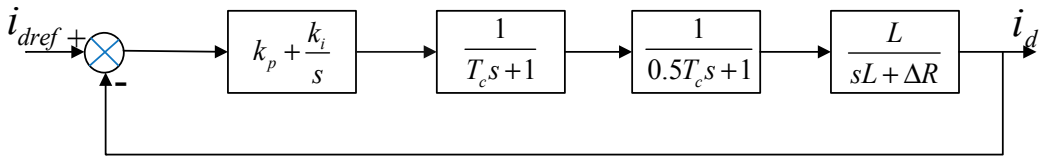

Figure 5. Dynamic block diagram of the current loop considering resistance disturbance and system delay.

The open-loop transfer function is expressed as:

$$G_{id}(s) = \frac{k_p(s + T_i)}{s} \frac{1}{1.5T_c s + 1} \frac{1}{s + \frac{\Delta R}{L}}, \tag{17}$$

$$T_i = \frac{k_i}{k_p}, \tag{18}$$

Equation (17) is a three order oscillation link. The pole-zero cancellation is used to reduce the order. According to the automatic control theory, in the s domain, the poles far from the imaginary axis have little influence on the system. In general, the poles caused by the resistance disturbance are closer to the imaginary axis than those caused by the delay link.

Let $T_i = \frac{\Delta R}{L}$. Based on the pole-zero cancellation, the pole caused by the resistance disturbance is eliminated by the zero point of PI correction. This will offset the influence of the pole. The corrected open-loop transfer function is expressed as:

$$G_{id}(s) = \frac{k_p}{s(1.5T_c s + 1)} \tag{19}$$

In this study, the optimal damping ratio ξ was set to 0.707. Equations (20) and (21) show the PI correction of the current loop:

$$k_p = \frac{1}{3T_c}, \tag{20}$$

$$k_i = \frac{\Delta R}{3T_c L} \tag{21}$$

Substituting Equations (20) into Equation (19) and neglecting the higher order terms, the open-loop transfer function is expressed as:

$$G_{id}(s) = \frac{1}{3T_c s}, \tag{22}$$

The closed-loop transfer function is expressed as:

$$G_{id}(s) = \frac{1}{3T_c s + 1} \tag{23}$$

According to Equations (22) and (23), the current loop is approximately equivalent to a first order inertial link, and the inertial time constant is $3T_c$. Based on the step response property of the first order inertial link, 98.2% reference value can be reached after $12T_c$–$15T_c$. When the switching frequency is high, that is to say, the control cycle is short, the current tracking has good rapidity.

DC side capacitor voltage relates to the active power injected into the VSC from the AC power supply. Based on Equation (6), the DC side voltage loop with PI correction is added onto the d axis current loop. It forms a double closed loop system. The dynamic structure is shown in Figure 6.

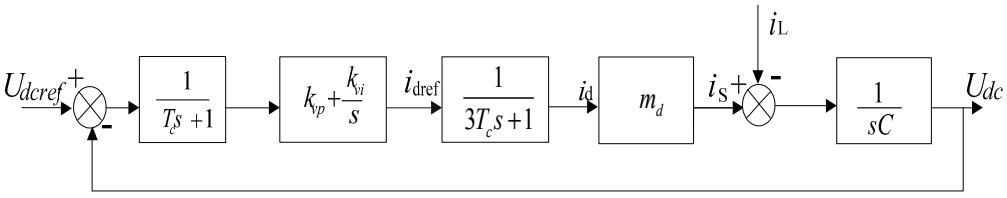

Figure 6. Dynamic block diagram of voltage loop.

According to the characteristics of the switching function, m_d is a nonlinear link, and it is inconvenient for the system design. When using SPWM modulation, the maximum value of m_d is 1. Therefore, when m_d = 1, it has the greatest impact on the system. Combining the delay terms and neglecting the higher order terms, the simplified dynamic structure is shown in Figure 7.

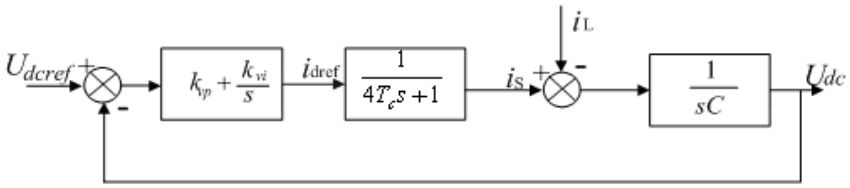

Figure 7. Simplified dynamic block diagram of voltage loop.

According to Mason Gain Formula, the system transfer function is expressed as:

$$u_{dc}(s) = \frac{k_{vp}s + k_{vi}}{4CT_c s^3 + Cs^2 + k_{vp}s + k_{vi}} \cdot u_{dcref}(s) - \frac{4T_c s^2 + s}{4CT_c s^3 + Cs^2 + k_{vp}s + k_{vi}} \cdot i_L(s) \tag{24}$$

The system consists of two responses: the DC voltage, and the disturbance current of the load. The system error $E(s)$ is expressed as:

$$E(s) = u_{dcref}(s) - u_{dc}(s), \tag{25}$$

The input is a unit step signal, and the disturbance current is also a step signal, but its amplitude is a:

$$u_{dcref}(s) = \frac{1}{s}, \tag{26}$$

$$i_L(s) = \frac{a}{s}, \tag{27}$$

According to the final theorem, the steady-state error can be represented as:

$$e_{ss} = \lim_{s \to 0} sE(s) = 0, \tag{28}$$

The steady-state error is not influenced by the disturbance current. There is no static error during the steady state. The characteristic equation of closed loop voltage is as follows:

$$s^3 + \frac{1}{4T_c}s^2 + \frac{k_{vp}}{4CT_c}s + \frac{k_{vi}}{4CT_c} = 0, \tag{29}$$

To achieve the required dynamic performance and steady-state performance in higher order systems, the usual treatment in engineering is to arrange two of the poles as a pair of conjugate poles, and configure the other two poles far away from the imaginary axis. The characteristic equation is expressed as:

$$(s^2 + 2\xi\omega_n s + \omega_n^2)(s + n\xi\omega_n) = 0, \tag{30}$$

Comparing Equations (29) and (30), the parameters after the PI correction of the voltage loop are as follows:

$$\begin{cases} k_{vp} = 4CT_c(2n\xi^2 + 1)\omega_n^2 \\ k_{vi} = 4CT_c n\xi\omega_n^3 \end{cases}, \tag{31}$$

$$\omega_n = \frac{1}{4\xi T_c(n+2)}, \tag{32}$$

In summary, the control structure of the interruption generator based on VSCs is shown in Figure 8.

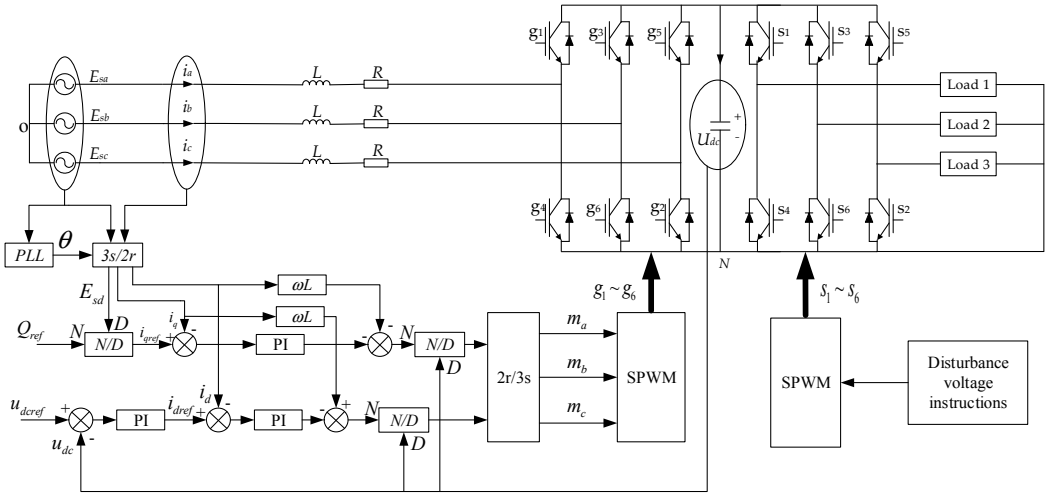

Figure 8. Structure diagram of the control system.

4. Analysis of Simulation Case

4.1. Parameters of Simulation Case

The simulation parameters of the main circuit and the controller are respectively shown in Tables 1 and 2. The simulation platform based on PSCAD/EMTDC is shown in Figure 9.

Table 1. Parameters of the main circuit.

Parameters of Main Circuit	Values
AC phase voltage/V	220
Grid-side reactor/mH	2.3
Equivalent loss resistance/Ω	0.05
Equivalent capacitance of DC side/μF	7050
Operating voltage of DC side capacitor/V	700
Control cycle/ms	0.25
Equivalent disturbance load/Ω	50

Table 2. Parameters of the controller.

PI Parameters of Current Loop		PI Parameters of Voltage Loop	
k_p	Ti	k_{vp}	T_{vi}
1400	0.00089 s	0.6	0.02 s

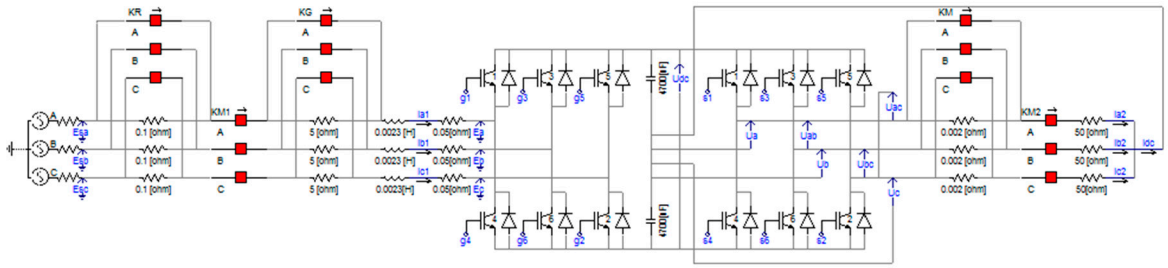

Figure 9. Simulation platform based on PSCAD/EMTDC.

4.2. Verification of Controller Performance

According to Figures 5 and 7, a dynamic structure based on double closed loop control was constructed in MATLAB/Simulink (R2014b, MathWorks, Natick, MA, USA), which is shown in Figure 10a,b; its unit step response is shown in Figure 11a,b.

The current tracking can be completed in 4 ms, which is basically consistent with the theoretical value. The overshoot is very small, and there is no static error in steady state. The DC side voltage reaches the steady-state value of 700 V in 100 ms with no static error in steady state, and the overshoot is 7%. The simulation results thus verified the correctness of the controller design.

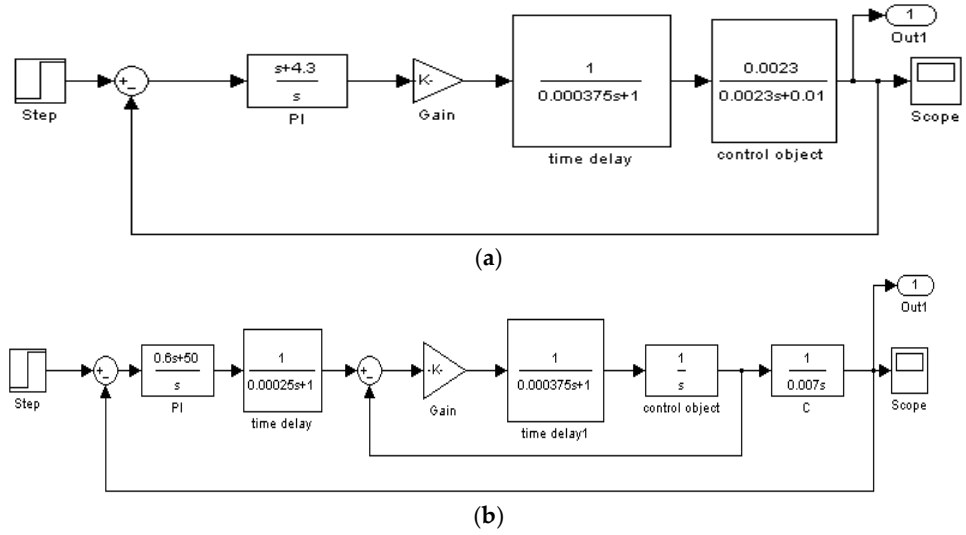

Figure 10. (**a**) Dynamic simulation model of current loop; (**b**) dynamic simulation model of voltage loop.

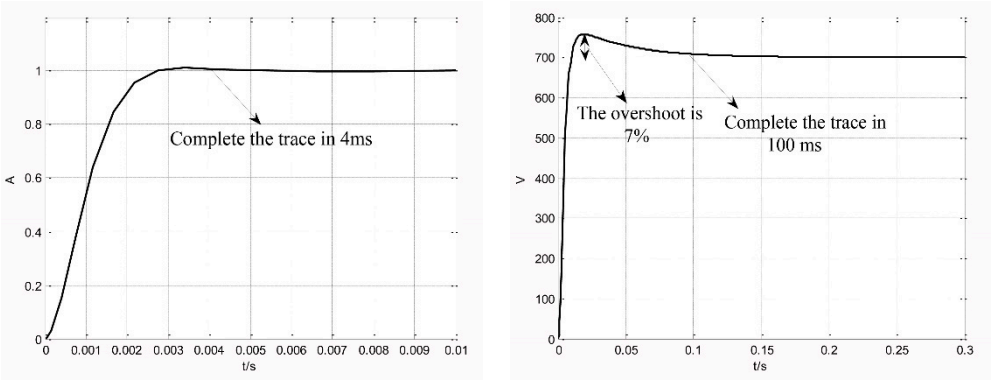

Figure 11. (**a**) Unit step response of current loop; (**b**) unit step response of voltage loop.

4.3. Simulation Research

The performance of the rectifier is verified in Figure 12. At 0.2 s, the reactive power of the AC side flowing into the rectifier increased from 0 to 20 kVar, that is to say, Q_{ref} = 20 kVar, under the no-load operating condition. The power tracking was done in about 5 ms, as shown in Figure 12a. In Figure 12b, the reactive power jump did not affect the voltage stability of the DC side. Figure 12c shows waveforms of the AC side voltage and current, whose phase difference was 90°. Figure 12d is the current spectrum of the AC side, and shows that there was no low-order harmonic which will cause pollution to the grid. Figure 12e is the voltage waveform of the DC side sudden increase load. The DC voltage recovered after one cycle, and the maximum change rate was 2%. Furthermore, the performance of the controller against external disturbances was good. In Figure 12f, when the equivalent resistance of the AC side increased by 0.1 Ω, the DC side voltage was almost unchanged, which shows that the controller had good performance against internal disturbances.

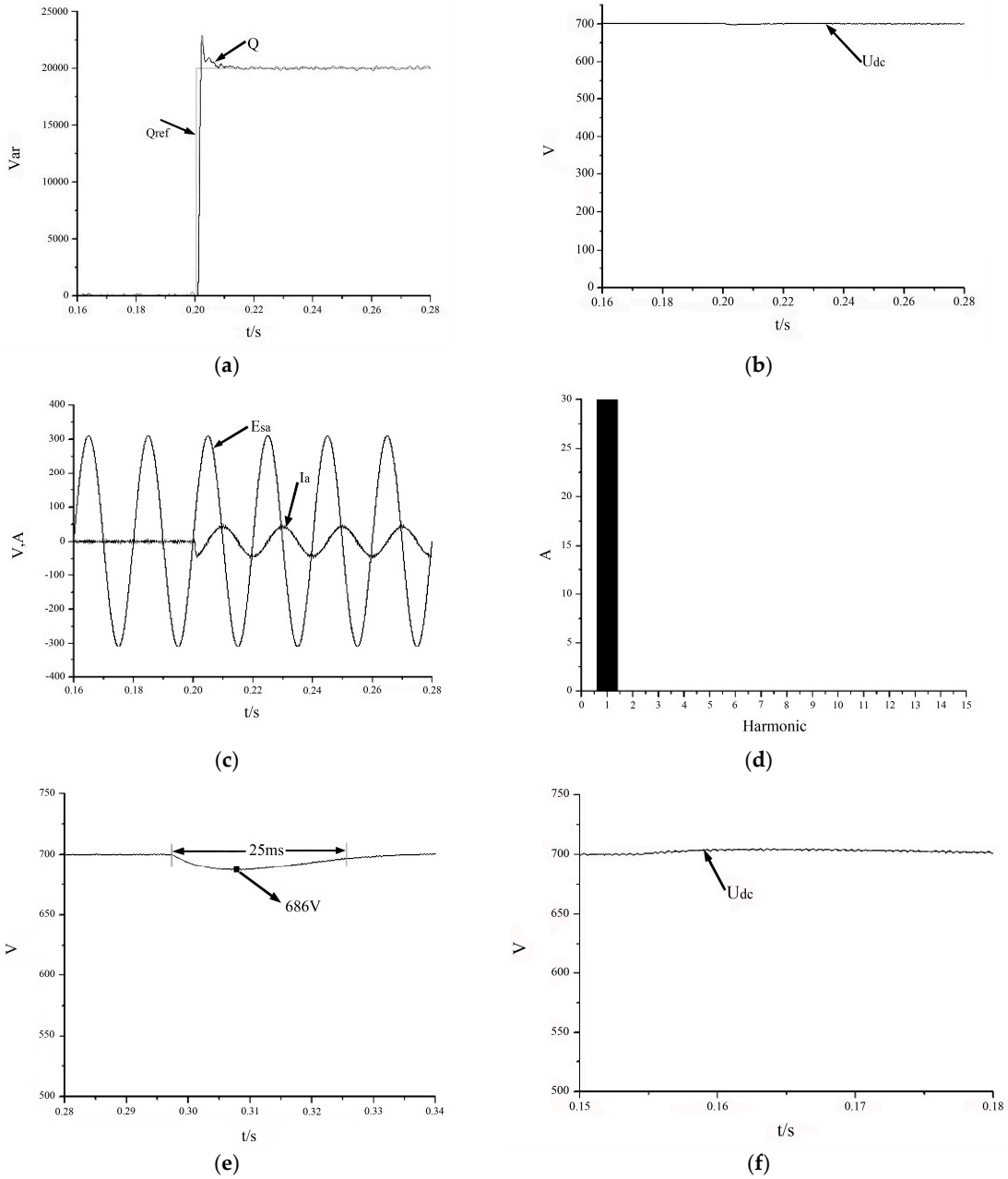

Figure 12. (**a**) Jump of the reactive power; (**b**) voltage of DC side; (**c**) voltage and current of AC side; (**d**) current spectrum; (**e**) voltage of DC side with external disturbances; (**f**) voltage of DC side with internal disturbances.

In Figure 13, the feasibility of the method of the interruption generator was verified by several typical disturbance waveforms produced by SPWM waves based on the regular sampling method. Figure 13a is the voltage sag waveform. The voltage dropped by 10%, and the voltage sag lasted for four cycles. Figure 13b is the voltage swell waveform. The voltage increased by 12.5%, and the voltage swell lasted for four cycles. Figure 13c is the voltage interruption waveform, which lasted four cycles. Figure 13d,e are frequency offset waveforms. The frequencies of the modulation wave were 49 Hz and 51 Hz. Figure 13f is the fundamental waveform with 0.5 times third harmonic injection. Figure 13g is the 3-phase unbalanced waveform with a degree of unbalance of 32.5%. Figure 13h is the voltage flick waveform. The modulation wave was obtained by superposition of the fundamental waveform and the wave whose amplitude was 10% of the fundamental waveform and frequency was 15 Hz.

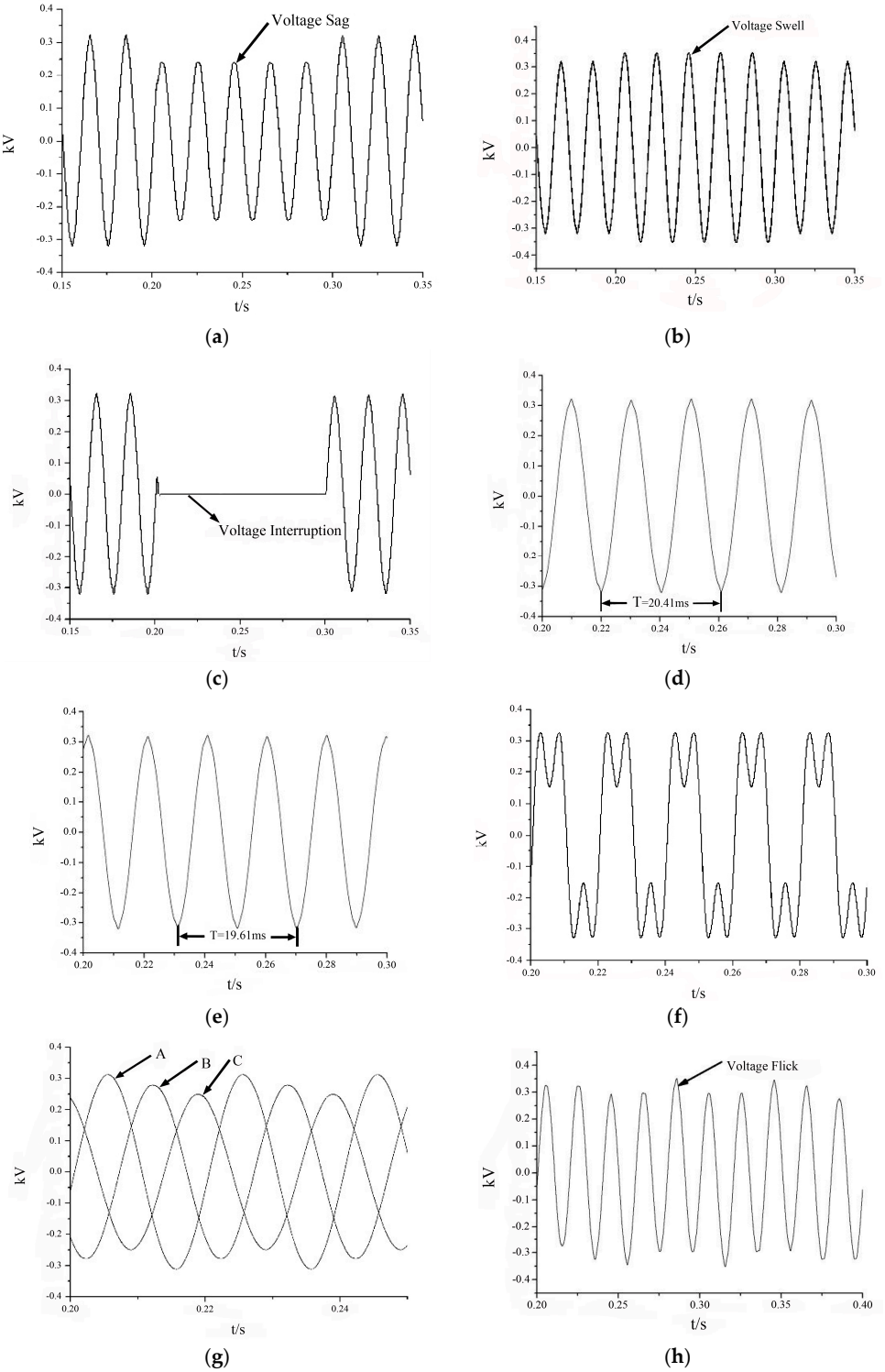

Figure 13. (**a**) Voltage sag; (**b**) voltage swell; (**c**) voltage interruption; (**d**) waveform of 49 Hz; (**e**) waveform of 51 Hz; (**f**) harmonic injection; (**g**) 3-phase unbalanced waveform; (**h**) voltage flick.

5. Experimental Results and Analyses

A 30 kVA VSC physical prototype shown in Figure 14 was designed to prove the method above. The control chip is TMS320LF2812 (Texas Instruments, Dallas, TX, USA). Figure 15 gives the structure diagram of the physical prototype, which consists of a grid-side converter, an isolation transformer, a DC unit, a load side converter, and a line switch. Technical indices of the device are shown in Table 3.

Figure 14. Physical prototype.

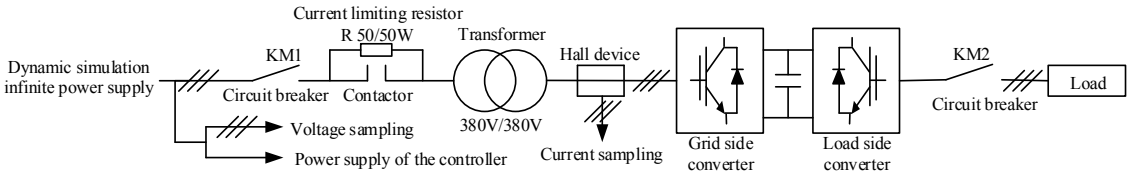

Figure 15. Structure diagram of the physical prototype.

Table 3. Technical indices of device.

Electrical Parameters	Technical Indexes
Capacity of device	30 kVA
Capacity of load	100 A
Error of DC voltage	±1%
Range of disturbance voltage	0–112%
Maximum harmonic number of voltage	17

The device provides the following disturbance waveforms.

Figure 16 shows the waveform of voltage sag: the voltage dropped by 21.4% from 220 V to 173 V for 100 ms.

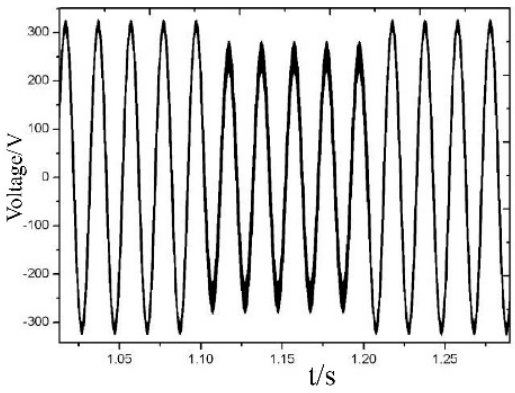

Figure 16. Waveform of voltage sag.

Figure 17 shows the waveform of voltage swell: voltage increased by 12.5% from 220 V to 248 V for 100 ms.

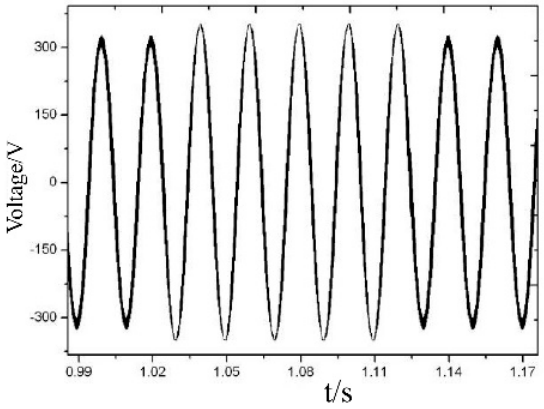

Figure 17. Waveform of voltage swell.

Voltage interruption is the most serious problem for power quality. Figure 18 is the waveform of voltage interruption, showing an interruption for 120 ms.

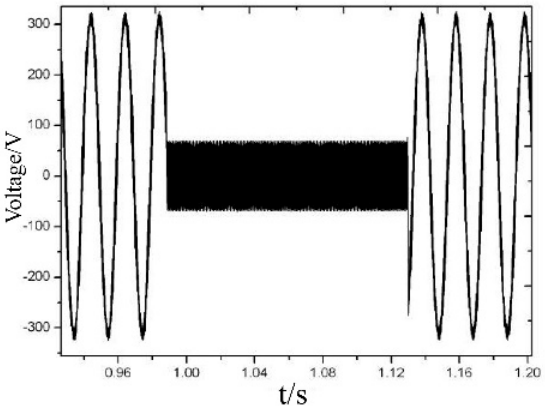

Figure 18. Waveform of voltage interruption.

A 0.5 times third harmonic voltage was injected into the fundamental voltage, as shown in Figure 19.

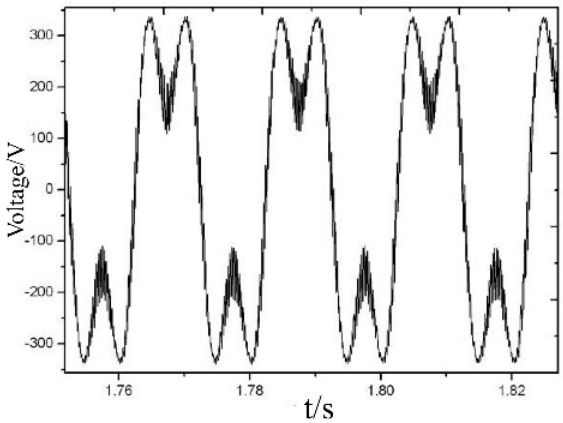

Figure 19. Waveform with third harmonic injection.

The output of the 3-phase unbalanced waveform was realized by differing the amplitudes of the 3-phase modulation wave. The 3-phase voltage waveform with a degree of unbalance of 32.5% is shown in Figure 20.

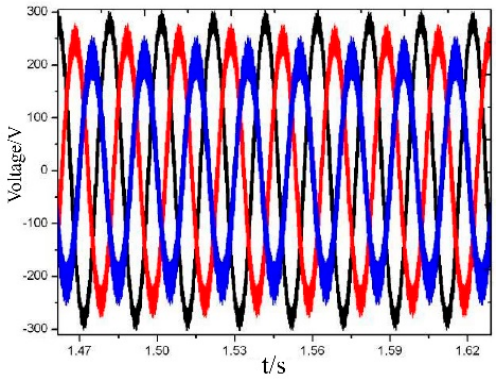

Figure 20. Waveform of 3-phase unbalanced voltage.

The stability of the DC voltage guarantees the output waveform. Figure 21 shows the error of the DC side voltage under the condition of the voltage sag shown in Figure 16. The error was between −0.2% and 0.6%, and the maximum fluctuation was 6 V. These results met the device indices.

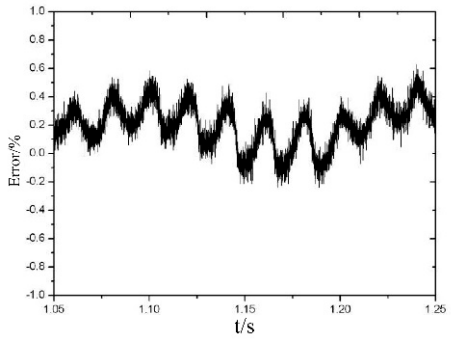

Figure 21. DC voltage error of voltage sag.

When the load side was connected to the grid for the grid connected experiment, and the device is working in the state of uncontrolled rectifier, the phases of the grid voltage and output voltage shown in Figure 22 coincided.

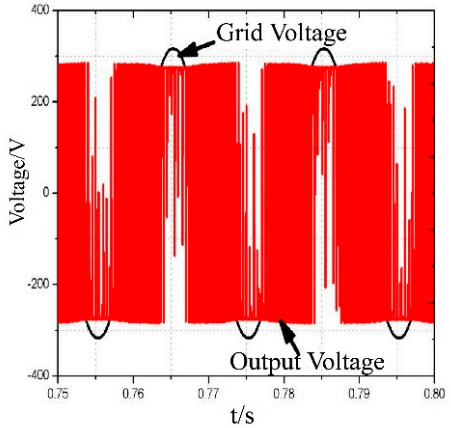

Figure 22. Voltage relation before grid connection.

The load side was connected to the grid through 50 Ω resistance. Figure 23 provides the relationships between the grid-side voltage, load side output voltage, and system voltage. The fluctuation of the current was small, thus proving that the load side was connected to the grid. The voltage sag experiment after grid connection is shown in Figure 24. Phases of the output voltage and the grid voltage were the same. The output voltage dropped by 5.4% from 280 V to 265 V for 100 ms, while the device remained stable.

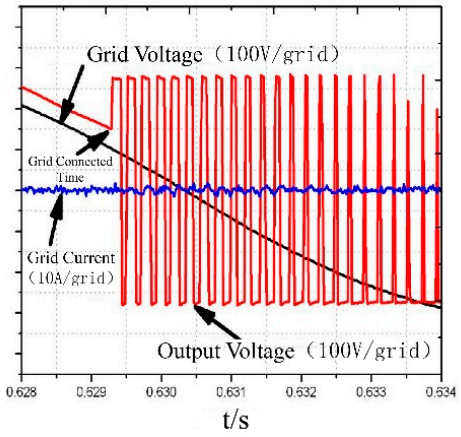

Figure 23. Parameters in grid connection.

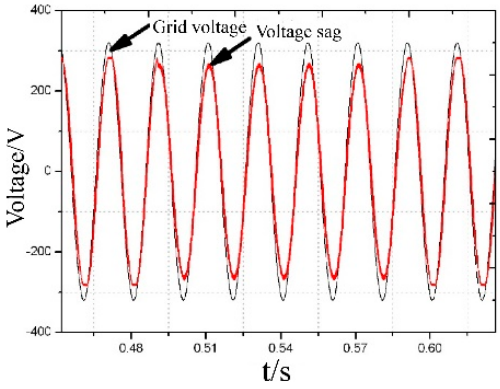

Figure 24. Voltage sag experiment after grid connection.

6. Conclusions

In this paper, we presented a universal design method for the main circuit and controller based on the operation condition and power control theory. A PSCAD/EMTDC simulation platform for an interruption generator was created, and then a 30 kVA physical prototype was established in a dynamic simulation lab based on the simulation. The simulation and experimental results showed that the interruption generator based on the VSC has the advantages of high voltage accuracy, and various disturbance waves. We provided an experimental platform for addressing power quality problems and measuring operating characteristics of compensation equipment under disturbance conditions.

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Author Contributions: Junhui Li designed the experiments and wrote the paper; Tianyang Zhang performed the experiments; Gangui Yan provided important guidance; Lei Qi contributed reagents/materials/analysis tools.

Conflicts of Interest: The authors declare no conflict of interest.

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