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Comprehensive Analysis of LCL Filter Interfaced Cascaded H-Bridge Multilevel Inverter-Based DSTATCOM

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Abstract: Three-phase two-level voltage source converters are used for distribution static compensator (DSTATCOM) applications and can be replaced by a multilevel inverter. In this paper, an LCL filter interfaced cascaded H-bridge multilevel inverter-based (CHBMLI) DSTATCOM is simulated and its performance is analyzed considering the system parameters. The analysis considers factors including the switching frequency, modulation index, and filter parameters of a DSTATCOM system. The LCL filter design and analysis for the low switching frequency operation of CHBMLI is proposed in this paper. Phase shift pulse-width modulation is used for the generation of switching signals. The reference current is generated using synchronous reference frame theory (SRFT) for reactive power and harmonic compensations. The simulation model of the CHBMLI-based DSTATCOM system is developed in MATLAB Simulink. The results are demonstrated for a linear/non-linear load under unbalanced conditions, considering the voltage sag and swell in the system due to a disturbance in the load.

Keywords: cascaded H-bridge multilevel inverter-based (CHBMLI); LCL filter; phase shift pulse width modulation (PSPWM); distribution static compensator (DSTATCOM)

1. Introduction

It is essential to recognize power quality issues in power systems. Power quality refers to a system's ability to maintain a sinusoidal power distribution voltage and current at a rated magnitude and frequency. Therefore, any disturbance in a distribution system is referred to as a power quality issue. Power transmission may have an effect on power quality, but it only has a minor effect because modern transmission systems have lower resistance-to-reactance ratios, and consequently, have lower damping ratios [1–3]. Also, the generating system is not usually the primary cause of any existing non-ideal behavior, and thus, it is not often a major concern in terms of power quality. The roots of power quality issues are categorized in two ways: natural causes and manmade causes, which may be due to the load or a feeder. The second category plays a major role in contributing to the rise in power quality issues. Some of the manmade causes that affect power quality include transformers, the charging and discharging of capacitors, nonlinear loads such as power electronic loads (e.g., an uninterrupted power supply), speed drive converters, and the time-variant switching of large loads.

Power grids that are connected to various types of loads suffer from dynamic and transient changes due to power quality issues; to monitor the functioning of the grid, online real-time monitoring systems are therefore required. Real-time power quality monitoring requires a system set-up that enables corrective actions to be taken. A real-time power quality monitoring system is thus necessary to provide the required information, both locally and more widely throughout the system [4,5]. Therefore,

the monitoring system must be aware of the effects of poor power quality on the safety, reliability, and efficiency of the many types of equipment connected to the grid. The various aspects of power quality to be considered include voltage fluctuations, voltage sag-swell, voltage imbalance, and higher-order harmonics in the grid current [6].

The cumulative use of power electronic loads by both industry and local consumers results in a considerable amount of harmonic injection, and a poor power factor. Conventionally, passive filters have been used to eliminate the current harmonics and improve the power factor. However, the use of passive filters has many disadvantages, including a high value inductance, damping effects, and the large size of the capacitor bus. Recently, with the rapid progress being made in modern power electronics technology, filter applications are oriented towards the use of active filters, rather than passive filters. The basic difference between passive and active filters is that the active filters have the ability to compensate for randomly varying currents [7].

Recent developments in power systems and emerging power device technologies include the flexible AC transmission system (FACTS) and custom power devices, where deregulated power systems with flexible new control capabilities fall under the category of custom power devices. Custom power devices are classified into network configuration-type and compensation-type devices; the former type actually alters the properties of the power system network, enhancing the power quality [8].

In any distribution system, the presence of an unbalanced load or nonlinear loads can inject higher order harmonics or cause an imbalance in the system. The custom power devices are used to prevent such unbalanced and distorted currents from being drawn into the grid of the distribution line, either connected in series or shunt configurations. One such shunt-connected custom power device is the distribution static compensator (DSTATCOM) that can dynamically inject a compensating current with the desired amplitude, frequency, and phase. For reactive power compensation and harmonic elimination applications, the DSTATCOM is one of the fastest and most reliable modular custom power devices. DSTATCOM can be used to ensure that the current drawn from the grid is nearly sinusoidal and distortion-free. A voltage source converter (VSC) is commonly used to realize a DSTATCOM. The VSC structure determines the level or extent of compensation that the device can provide in the grid. If a three-phase four-wire system is connected to a balanced load, then a balanced compensating current is required to maintain the smooth operation of the system. However, in the above scenario, if the source current or load is unbalanced or distorted, the required compensation current must be unbalanced and distorted to mitigate the lack of balance or distortion in the system [9,10]. DSTATCOM behaves like a controlled voltage or current source in the grid. DSTATCOM can supply the required reactive power to the problem load from the circulating energy that is present between the phases of the AC system.

DSTATCOM requires a VSC for its functionality and one of the preferred converter topologies is the multilevel VSC. An alternating voltage source in phase with the grid voltage can be generated through the application of a suitable control scheme to a multilevel inverter-based DSTATCOM [11,12]. Multilevel inverters (MLIs) are capable of producing a synthesized output voltage from several input DC voltage levels. As per the MLI topology, a voltage waveform with a near-sinusoidal shape can be obtained by using a sufficient number of DC sources. Therefore, MLIs have been gaining attention in recent years, for their application in medium and high voltage systems [13].

Cascaded H-bridge MLI (CHBMLI) have the advantages of lower operating switching frequencies, a reduced electromagnetic interference, and a modular structure. However, it requires separate DC sources/capacitors for each bridge. The modularity of topology and the ease of lower to higher level expansion are some of the application-based advantages of the CHBMLI-based DSTATCOM [14]. Several applications of cascaded MLIs have been attempted, including the STATCOM, motor drive applications, and the integration of renewable energy sources. CHBMLI has certain advantages over the diode-clamped MLI and the capacitor-clamped MLI, as they require additional clamping diodes

and clamping capacitors [15,16]. In such inverter topologies, the switching of power electronic devices injects higher level harmonics into the grid.

A proper current control is required for the generation of pulse width modulation (PWM) signals, to mitigate the harmonics. The different PWM techniques can be adopted to optimize the switching frequency of each of the power electronic devices. There are two main types of carrier-based modulation techniques that have been developed by extending conventional PWM: phase shift PWM (PSPWM) and level shift PWM. However, other modulation techniques have been proposed in the literature [17]. Sinusoidal PWM (SPWM) offers a nearly constant switching frequency and reduced complexity for MLIs when compared to other modulation techniques, including hysteresis current control and space vector modulation (SVM), which have contrasting disadvantages. The modulation techniques that are used for MLIs can be classified into three types, comprising SVM, SPWM, and selective harmonics elimination PWM. In recent years, several authors have attempted to generalize the available PWM techniques for various multilevel inverter topologies [18,19]. Based on previous efforts, it was observed that the generation of PWM signals for CHBMLI, using phase shift and level shift PWM, have been found to be reliable, supported by a reduced complexity [20].

The computation of reference quantity using a proper control algorithm is responsible for the generation of PWM signals to improve the power quality. In general, these control algorithms can be classified, based upon the reference generation in the stationary/rotating axis frame. Synchronous reference frame theory (SRFT) is based on a set of instantaneous power equations defined in the time domain. In an SRFT-based system, it has been acknowledged that the d-component and q component of the load current are responsible for the active power and reactive power, respectively [21–24].

In this paper, a five-level CHBMLI-based DSTATCOM is implemented and a phase-shift PWM technique is adopted for the generation of switching signals, because of the uniform distribution of power stress on each switching device. An LCL filter interfaced MLI system is proposed, due to its inherent advantage over L and LC filter-based systems. An LCL filter is designed with a reduced inductor size to avoid resonance issues, using an appropriate damping technique [25–27]. This paper involves the operation in a switching frequency range of 1–5 kHz, and the LCL filter design is thus performed with passive damping for a better attenuation bandwidth. The reference signal is generated using SRFT for the indirect current control of the LCL filter interfaced DSTATCOM system. The performance of the MLI inverter system is validated under different load conditions, such as balanced and unbalanced linear/non-linear loads, considering power quality issues. The proposed system is also investigated considering the effect of change in the dc voltage capacitance and switching frequency on the dc bus voltage under transient conditions.

2. System Description and Design

2.1. Basic Structure

The CHBMLI topology utilized for DSTATCOM offers both modularity and flexibility, corresponding to a change in the voltage level and switching frequency. The basic circuit of the three-phase CHBMLI is shown in Figure 1, considering generalized m-levels. The circuit consists of $(m-1)/2$ cascaded cells in each phase. Each CHBMLI cell requires an isolated DC source/capacitor for the generation of a synthesized output ac voltage. The generalized system equations, as in Equations (1)–(4), are for the DC voltage and output ac voltage of CHBMLI. For the DSTATCOM application, the CHBMLI bandwidth must be decided upon, based on the highest level of harmonics which need to be compensated. In the case of CHBMLI, the increased level of inverters has a linear relation with the number of H-bridge cells and dc sources/capacitors required for the implementation of the system. However, the improvement in the output voltage performance does not follow the linear relation and there will not be a considerable improvement in the performance corresponding to increased levels. Therefore, five and seven level inverters are predominantly used for system

implementation at a medium voltage (415–1100 V). Each of the H-bridges that are connected in cascade can generate three output levels: $+V_{dc}$, 0, and $-V_{dc}$.

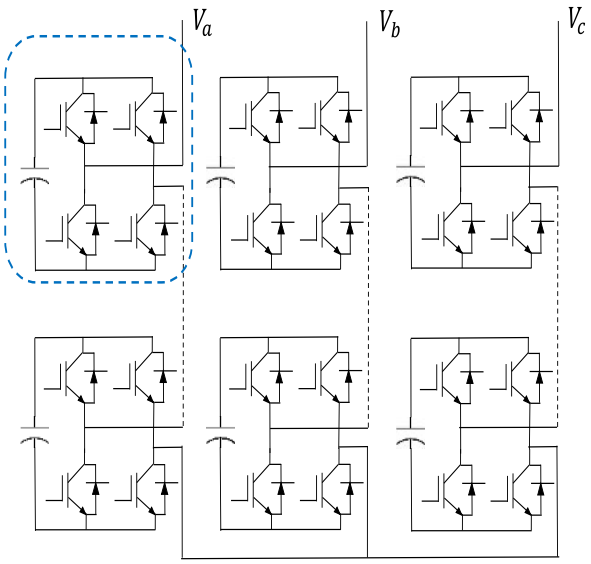


Figure 1. Three-phase cascaded H-bridge multilevel inverter (CHBMLI) structure.

The peak value of the output voltage per phase can be written as:

$$V_a = V_{aH1} + V_{aH2} + \ldots + V_{aH[(m-1)/2-1]} + V_{a[(m-1)/2]} \quad (1)$$

by assuming that each of the H-bridges has an equal DC bus voltage, i.e., $V_{aH1} = V_{aH2} = \ldots = V_{aH[(m-1)/2-1]} = V_{a[(m-1)/2]} = V_{dc}$.

The output voltage of the CHBMLI is also written as:

$$V_A(\omega t) = \sum_{n=1}^{n=\infty} f(x,n)(\sin\ n\omega t) \quad (2)$$

where:

$$f(x,n) = \frac{4V_{dc}}{n\pi} \sum_{k=1}^{(m-1)/2} (a_n \cos n\alpha_k) \quad (3)$$

It is necessary for the switching angles to be restricted such that:

$$\frac{\pi}{2} > \alpha_m > \ldots\ldots \alpha_2 > \alpha_1 \quad (4)$$

2.2. Implemented System

A five-level CHBMLI-based DSTATCOM is analyzed and investigated, and connected to the grid via an LCL filter. The CHBMLI (acting as the VSC) for the DSTATCOM application offers control capabilities similar to those of the traditional three-leg inverter. The only difference between these inverters is that more gate signals are required by the earlier invertor, but one of the advantages of the proposed system is that a reduced total harmonics distortion (THD) can be achieved in the converter voltage. The application of an appropriate control scheme with an optimum inverter level produces a voltage source inverter that can generate an alternating voltage in phase with the source voltage. The analysis of the DSTATCOM is also conducted, based on the filter that is applied between the system and the STATCOM. Similarly, the five inverter voltage levels are $-2V_{dc}$, $-V_{dc}$, 0, V_{dc}, and $2V_{dc}$; these voltage levels are added to provide the synthesized output of the MLI. The voltage waveform

in each phase of the five-level cascaded inverter consists of five leveled outputs, with two H-bridges connected in the cascade. Each phase of this voltage is fed to the distribution line through a coupling inductance, to form a shunt-connected DSTATCOM, as shown in Figure 2, where V_{sa}, V_{sb}, and V_{sc} are the source phase voltages that are connected to a nonlinear load or reactive load. L_s is the per phase line inductance, and I_{La}, I_{Lb}, and I_{Lc} represent the per phase load currents. As shown in Figure 2, the CHBMLI is connected in shunt configuration to the load, and thus, at the point of common coupling (PCC), Kirchhoff's law can very easily be applied. Generalized phasor diagrams of the leading and lagging power factor (PF) load compensation are shown in Figure 3, where cos θ is a PF.

The focus of this paper is on the analysis and effects of different parameters on the design of a DSTATCOM for reactive power and harmonics compensation. As shown in Figure 2, the system configuration used is the CHBMLI-based DSTATCOM. Linear, nonlinear, and unbalanced loads are connected to the system, and draw lagging or leading, distorted and unbalanced load currents from the source, respectively. The shunt-connected device allows for the compensation of the reactive power and harmonics to be performed, and the avoidable component of the current is supplied by the DSTATCOM.

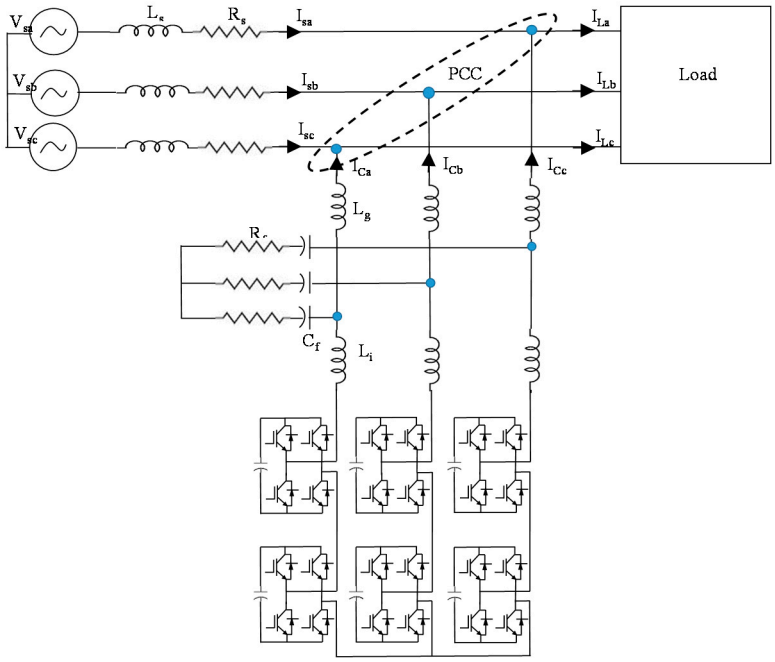


Figure 2. Shunt-connected distribution static compensator (DSTATCOM) system.

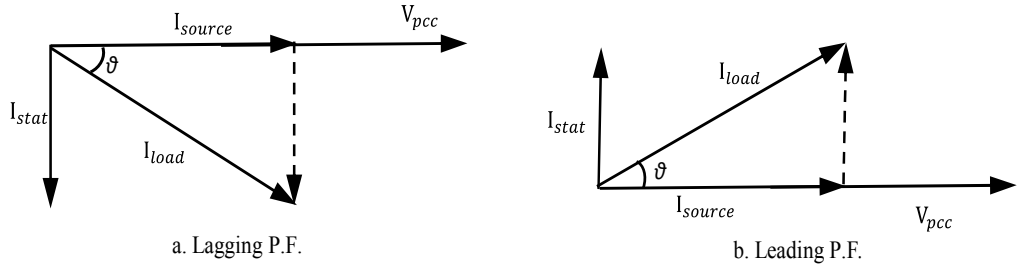


Figure 3. Phasor diagrams of DSTATCOM with (**a**) leading and (**b**) lagging power factor (PF) loads.

After the connection of the shunt device, the current equation will be as expressed in Equation (5). The nature of the compensation current generated by the shunt device is entirely dependent on the purpose of the required power quality improvement. At the PCC, the resulting source current should be sinusoidal.

$$\begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} = \begin{bmatrix} I_{Ca} \\ I_{Cb} \\ I_{Cc} \end{bmatrix} + \begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} \quad (5)$$

2.3. DC Link System

Here, the selection of the topology used for the DSTATCOM application is based on the symmetrical structure of the CHBMLI. If all the parameters and all the switching pulses for all of the H-bridge units are symmetrical, then the actual power of each unit will be identical. However, because of the dispersion of the capacitors and the switching losses of the IGBTs, the active power of each of the H-bridge units is different. A five-level MLI topology has been adopted for the analytical study, meaning that there are two H-bridges in each phase, and therefore, there are two capacitors per phase and a total of six capacitors in the five-level cascaded H-bridge inverter-based DSTATCOM. The voltages across each of the capacitors should be balanced throughout the operation. Many techniques are available to balance the voltages across the DC link capacitors. Many advanced and intelligent techniques have also been proposed for the balancing of the capacitor voltage, because it is a prominent part of the overall system design and operation.

In reference [28], a mathematical formulation for the cascaded H-bridge capacitance is derived as:

$$C_{\text{dc-cascaded}} = \frac{I_{\text{rms}} \times 100}{\sqrt{2}\pi f_{\text{g}} \% V_{\text{r}} V_{\text{dc}}} \left[1 - \sin\left(\arccos\left(\frac{M\pi}{4}\right)\right)\right] \quad (6)$$

where I_{rms} is the root mean square (*RMS*) load current (rated), f_{g} is the frequency of the system's supply, V_{r} is the peak-to-peak ripple voltage, V_{dc} is the DC bus voltage, and M is a modulation index. The voltage balancing can be performed in a phase-wise manner, i.e., the voltages across each of the phases should be equal, and if not, this can be achieved by using an individual voltage balancing technique. In this paper, an individual voltage balancing technique is used for voltage balancing of each capacitor. To distribute the total active power between all of the H-bridges and to make the capacitor voltage equal to the reference voltage, one extra loop must be added to the control system. The proportional integral (PI) controller is one of the most commonly applied linear feedback controllers, and has been used here because of its simplicity, applicability, and ease of control. The current responsible for power loss due to charging and discharging of capacitors (i_{dloss}) is calculated and function of this controller can be elaborated simply, using the following mathematical equation:

$$i_{\text{dloss}} = K_{\text{p}}(V_{\text{dcref}} - V_{\text{dc}}) + K_{\text{i}} \int (V_{\text{dcref}} - V_{\text{dc}}) \quad (7)$$

This equation shows only one PI controller, which drives the system to make the capacitor voltage equal to the reference value of the DC link voltage (V_{dcref}) however there are six PI controllers in the proposed feedback control loop across each bridge. All of the controllers have the same proportional gain (K_{p}) and Integral gain (K_{i}) values. The trial-and-error method is used to determine values of the proportional and integral gains.

2.4. Reference Current Generation for CHBMLI

Various voltage and current control techniques are available for the control of the STATCOM, and because of its reduced complexity and ease of implementation, an indirect current control technique is used for reactive power and harmonics compensation. A basic block diagram that depicts the reference current generation for indirect current control, is shown in Figure 4, and is responsible for reactive power and harmonic compensation.

According to the current control technique implemented using the d-q component, the direct and quadrature axis current is responsible for the active power and reactive power, respectively. The load current passes through the low pass filter (LPF) to obtain the fundamental components of the current.

Therefore, only the active component of the power should be required from the source, or only the average DC component (I_d^*) is required to be fed from the grid. A certain amount of the active power is also consumed by the DSTATCOM, due of the charging and discharging of the capacitors, and this component of the current is responsible for some losses in the grid. The current that is responsible for maintaining the capacitor voltage is added to the active power component of the current, to regulate the capacitor dc voltage by compensating for inverter losses. The mathematical equation involved in the transformation of cuurent from abc to dq0 axis, and in the dq0 to abc axis transformation, is as follows:

$$\begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin \omega t & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \tag{8}$$

The inverse transformation from the dq0 to abc phases can then be written as:

$$\begin{bmatrix} I_a^* \\ I_b^* \\ I_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \omega t & -\sin \omega t & \frac{1}{\sqrt{2}} \\ \cos(\omega t - \frac{2\pi}{3}) & -\sin(\omega t - \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \\ \cos(\omega t + \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_d^* \\ I_q^* \\ I_0^* \end{bmatrix} \tag{9}$$

The generalized reference current for indirect control is calculated using the following equations:

$$V_t = \sqrt{\frac{2}{3}(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)} \tag{10}$$

$$I_{qt} = K_p(V_{tref} - V_t) + K_i \int (V_{tref} - V_t) \tag{11}$$

$$I_d^* = I_{df} + I_{d,loss} \tag{12}$$

$$I_q^* = I_{qf} + I_{q,t} \tag{13}$$

V_t is termed as the terminal voltage of the PCC that is regulated through the PI controller to maintain the power quality of the system, considering the voltage sag and swell caused by disturbance.

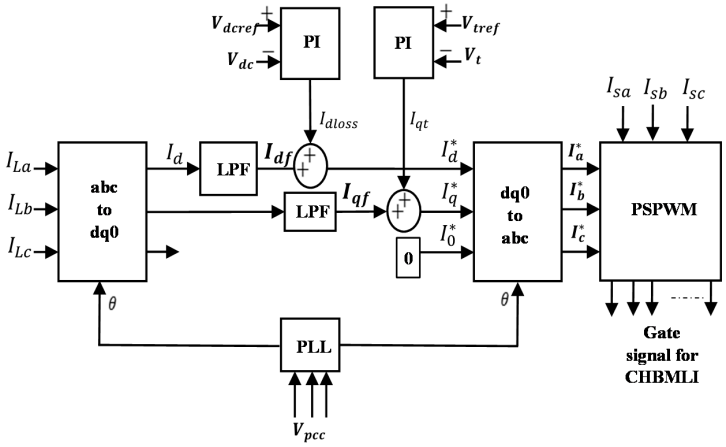


Figure 4. Block diagram of control algorithm used for reactive power compensation. PI: proportional-integral; LPF: low pass filter; PLL: phase locked loop; and PSPWM: phase shift pulse width modulation.

3. SPWM for CHBMLI

Many modulation techniques have been developed by researchers for MLIs; however, for the DSTATCOM application, SPWM techniques are modular and avoid any complexity in the system.

Other commonly used modulation techniques for MLIs include SVM and the selective harmonics elimination technique, and some nonlinear modulation techniques have also been developed for the CHBMLI. Two types of SPWM techniques have been utilized for CHBMLISs: level shift SPWM and phase shift SPWM. Both modulation techniques have advantages, such as the ease of implementation, a constant switching frequency, and the linear nature of control. For m-level CHBMLI, $(m-1)$ carrier signals (triangular) are compared to the one modulating signal (sinusoidal) in order to generate the PWM signals.

3.1. Level Shift Modulation-Based System

A level shift modulation technique requires that all carrier signals have the same frequency and phase, but their amplitudes are reduced by the average value and shifted along the vertical axis as shown in Figure 5. An implemented five-level inverter that required four triangular signals is compared to the sinusoidal signal, in order to generate the PWM signal for the switches. The modulation index can be varied by changing the magnitude of the sinusoidal wave. Further classifications of the level shift modulation have been conducted, but for simplicity, all of the carrier waves can be taken in the same phase.

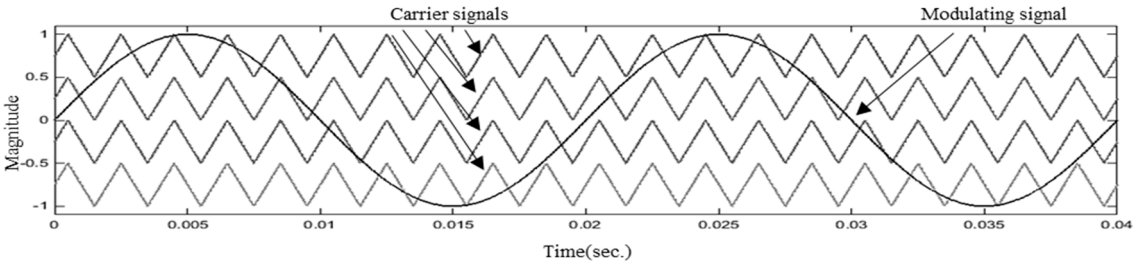


Figure 5. Level shift modulation

3.2. Phase Shift Modulation-Based System

Similar to level shift PWM, phase shift PWM uses $(m-1)$ carrier signals; however, the carrier signals are phase shifted, while their amplitudes and frequencies are identical as shown in Figure 6. The phase shifts of $360/(m-1)$ degrees between each sequential carrier signal are required. In this paper, a five-level inverter is used, and thus four carrier signals with 90° phase shifts are compared with the reference signal, in order to generate the PWM signal for CHBMLI. Phase shift modulation also has one important advantage in that it eases the modulation index change process. Phase shift modulation produces an equal power stress on each switching device, and thus, the modularity and switching losses are distributed across the entire MLI structure. In this paper, the phase shift modulation technique is implemented on a five-level CHBMLI and the satisfactory results demonstrate its applicability and modularity for MLI applications.

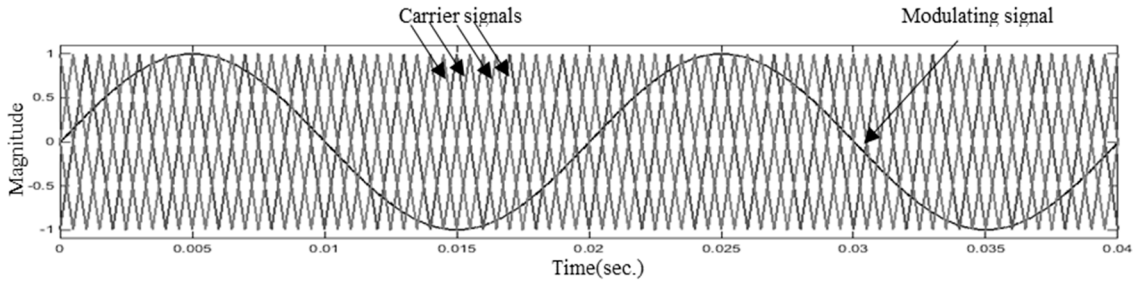


Figure 6. Phase shift modulation.

4. LCL Filter Design

Another function of the proposed distribution system is to suppress the additional higher order harmonics that are present in the output voltage generated by power electronic converters, because these harmonics affect the PCC voltage and current. To suppress the harmonics generated by the power electronic devices, the LCL filter is used because it offers advantages such as a small inductor size and cost effectiveness. The minimum filter inductor required to limit the current ripple, considering the single inductor filter system, is given by:

$$L_{\text{fmin}} = \frac{V_{\text{m}}}{v_{\text{s}} f_{\text{s}}} \tag{14}$$

where f_{s} is the switching frequency, V_{m} is the amplitude of the source voltage, and v_{s} is the peak amplitude of the triangular carrier signal.

Several researchers [28–31] have used an LCL filter for two-level VSC and a better performance is obtained when compared to L/LC filters, as an LCL filter is capable of providing an attenuation of 40 dB/decade beyond the switching frequency, for a large frequency range. The main objective of using the CHBMLI is to provide low switching losses because the output voltage contains fewer switching ripples compared to the conventional two-level VSC . However, a CHBMLI operates at a low switching frequency compared to the conventional two-level inverter. So, the parameter design of an LCL filter is needs to be modified, according to the operating condition of the MLI system, by following fundamental design constraints. In this study, an LCL filter is designed for an MLI system operating at a lower switching frequency, to avoid the use of a large-sized bulky inductor.

The LCL filter design is required to follow the constraint of the resonance frequency of the filter, switching frequency of the inverter, and fundamental frequency of the grid system, given the inequality (15). The grid impedance may vary substantially, along with its stiffness, so the filter resonance frequency may also vary, and thus specific care must be taken when designing the filter. Current filter design practices dictate that the inductor should be small in size, while the capacitor size may vary or can be large. However, the capacitor design deals with the power factor constraint. The filter design constraint in Equation (16) limits the size of the capacitor.

$$10 f_{\text{g}} << f_{\text{res}} << 0.5 f_{\text{s}} \tag{15}$$

$$C_{\text{f}} < 0.05 C_{\text{b}} \tag{16}$$

$$C_{\text{b}} = \frac{1}{\omega_{\text{g}} Z_{\text{b}}} \tag{17}$$

$$Z_{\text{b}} = \frac{V^2_{\text{source}-\text{LL}}}{P_{\text{inv}}} \tag{18}$$

The filter design includes two inductors that are termed as grid side and inverter side inductances, and both inductors should have an optimum value so that they work correctly for the given operation.

$$L_{\text{g}} = \frac{V_{\text{s}-\text{phase}}}{2\sqrt{6} f_{\text{s}} i_{\text{ripple.peak}}} \tag{19}$$

where a = 1 and L_{i} can be defined as:

$$L_{\text{g}} = a L_{\text{i}} \tag{20}$$

where C_{b} is the base capacitance, Z_{b} is the base impedance, ω_{g} is the angular frequency of the grid, $V_{\text{source-LL}}$ is the source voltage, P_{inv} is the inverter's rated power, $V_{\text{s-phase}}$ is the RMS value of the source phase voltage, and $I_{\text{ripple.peak}}$ is taken to be 20% of the rated current. f_{g}, f_{res}, and f_{s} are the grid, resonance, and switching frequencies, respectively. The Bode diagram shown in Figure 7 illustrates the performance of the LCL filter with and without damping resistances of various values (passive

damping). Passive damping of the LCL filter allows the resonance to be avoided. The attenuation capability of the LCL filter is reduced over the high frequency range for high values of damping resistance, and thus, an optimum resistance value of 0.5 Ω is selected. The filter capacitance value is determined, based on the assumption that $C_f = 0.015\ C_b$. The value of the capacitor in the LCL filter can be chosen very easily and should satisfy the above relationship for the lower order harmonics.

The LCL filter design procedure in the proposed work has been performed, based on the consideration that the operating switching frequency ranges from 1 kHz to 5 kHz, while the resonance frequency of the designed LCL is 629 Hz, to satisfy the consideration of Equation (15); the converter side inductance of the filter should be selected with particular care, because the current ripples vary substantially within a single switching period. L_g is designed first, and the values of L_i are subsequently chosen, accordingly. Therefore, the LCL filter offers an outstanding option for the proposed system considering various constraints. The passive/active damping methods can be used to avoid resonance issues. The passively damped system is adopted by using a damping resistance for ease of system control implementation. In this paper, the two inductors are taken to have equal values.

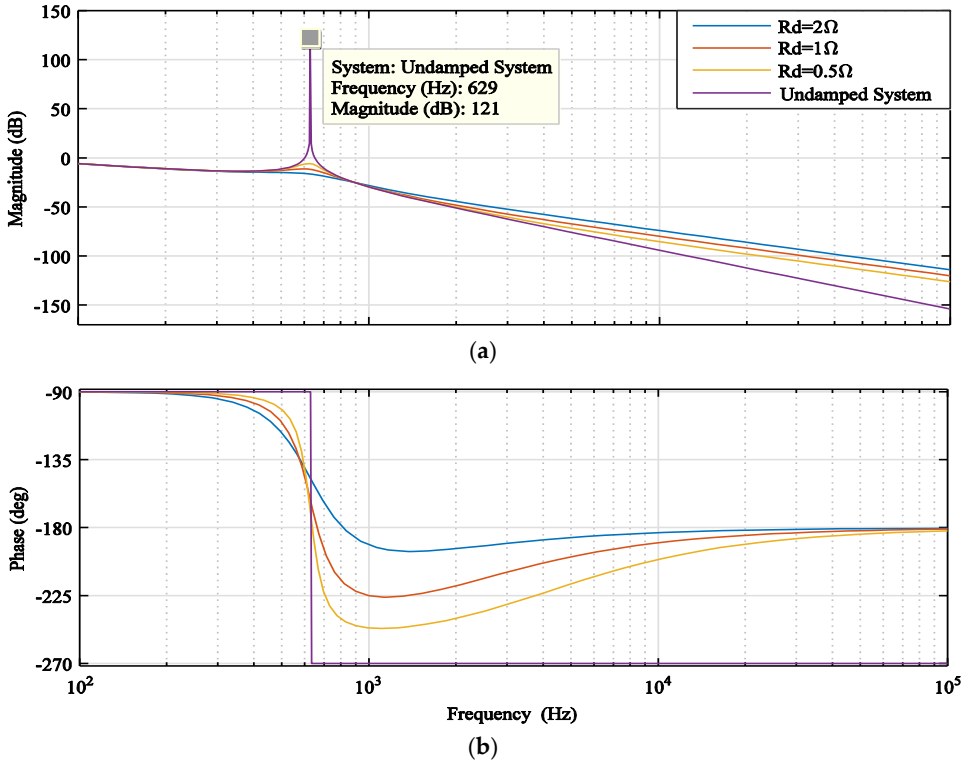


Figure 7. Bode diagram of the LCL filter. (**a**) Magnitude vs. Frequency; and (**b**) Phase vs. Frequency.

5. Results and Discussion

The DSTATCOM system shown in Figure 2 is implemented and simulated under the unity power factor (UPF) mode, to force the grid to supply the fundamental active components of the power through the proper generation of the reference current. The CHBMLI-based DSTATCOM developed in MATLAB Simulink (2014b, MathWorks, Natick, MA, USA) was analyzed for linear and non-linear loads under UPF operation. Table 1 shows the values of all parameters of the proposed system. Each of these values is taken for a 1100 V line-to-line voltage system, under the condition that there are two bridges in each phase that produce the same voltage level, where a value of 450 V should be maintained across each bridge. The point of this analysis is to assess the performance of this system when using phase shift SPWM.

Table 1. Simulation data used illustrating the STATCOM performance.

S. No.	Simulation Parameter	Values
1.	Source voltage	1100 V
2.	Frequency	60 Hz.
3.	Sources reactance	0.01 Ω and 1.6 mH
4.	LCL Filter Parameter	L_g = 1.6 mH, L_s = 1.6 mH, C_f = 80 µF, R_d = 0.5 Ω
5.	DC link voltage per cell	450 V
6.	K_p, K_i	1.2×10^{-3}, 7×10^{-4}
7.	Capacitor	800 µF
8.	Switching Frequency	1000–5000 Hz
9.	Linear Load	65 KVA 0.8 PF lagging
10.	Non Linear Load	Rectifier load R = 50 Ω, L = 500 mH
11.	Unbalanced load	In phase C 10 KVA

5.1. System Performance

5.1.1. Linear Load Condition

The performance of the DSTATCOM system is analyzed considering the linear type R-L load connected to the system. The generated reference current forces the DSTATCOM to compensate for the reactive power required by the load. Therefore, the grid can operate under UPF up to the capacity of the DSTATCOM system, compensating for the reactive power. The PCC voltage corresponding to the DSTATCOM output is demonstrated in Figures 8–11. For the DSTATCOM performance evaluation load, the source and DSTATCOM current is shown in Figures 12–14 for a linear, unbalanced, and non-linear load, for a time duration of 0–15 s, 0.15–0.30 s, and 0.30–0.45 s, respectively. The load source current and DSTATCOM current under a balanced load condition from time t = 0–0.15 s, are demonstrated in Figure 12a–c, respectively. The linear load connected to the system switched to the unbalanced condition at time t = 0.15–0.30 s, by disturbing phase "c" of the load. The source current was maintained in the balanced condition during unbalance in the system as the unbalanced compensating current provided by the DSTATCOM. The compensating current enables the source current to supply balanced active power to the load, as shown in Figure 13a–c, during an unbalanced condition.

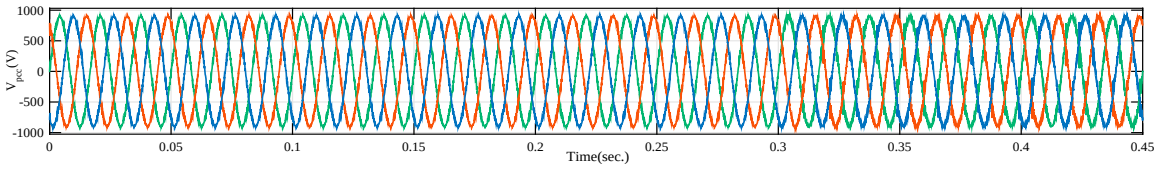


Figure 8. Point of common coupling (PCC) voltage under a balanced load (0.8 PF), unbalanced load, and nonlinear load at a time of 0–0.15, 0.15–0.3, and 0.3–0.45 s, respectively.

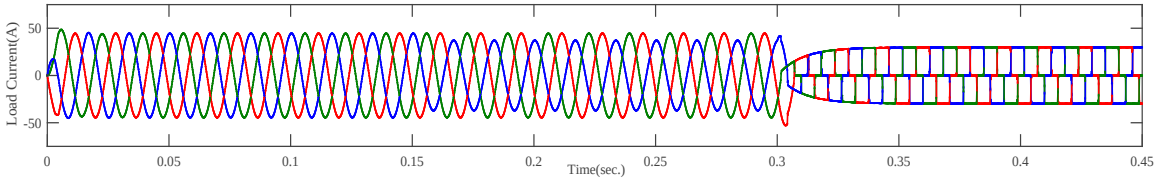


Figure 9. Load current under a balanced load (0.8 PF), unbalanced load, and nonlinear load at a time of 0–0.15, 0.15–0.3, and 0.3–0.45 s, respectively.

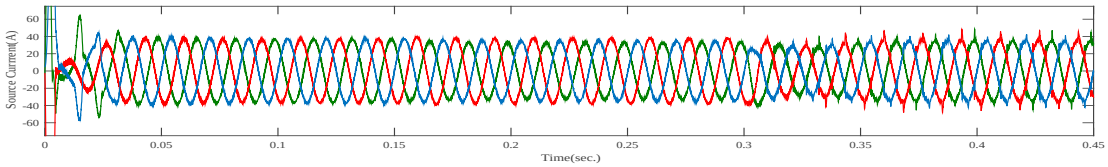


Figure 10. Source current under a balanced load (0.8 PF), unbalanced load, and nonlinear load at a time of 0–0.15, 0.15–0.3, and 0.3–0.45 s, respectively.

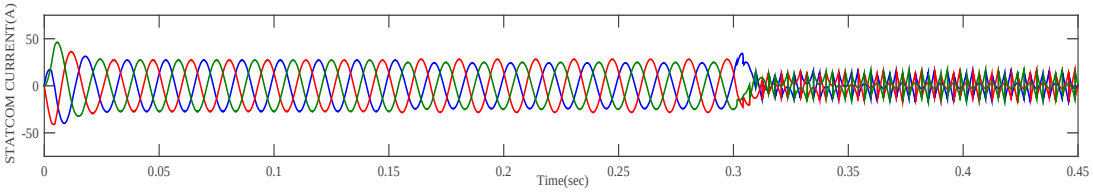


Figure 11. DSTATCOM current under balanced (0.8 PF), unbalanced, and non-linear loads at times of 0–0.15, 0.15–0.3, and 0.3–0.45 s, respectively.

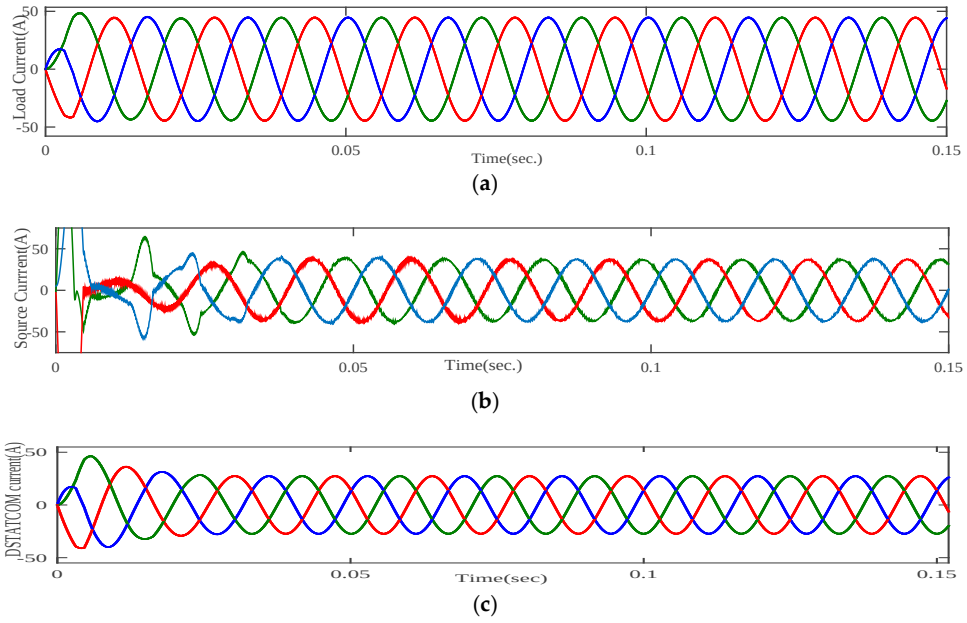


Figure 12. Currents under linear load conditions. (**a**) Load current; (**b**) source current; and (**c**) DSTATCOM current.

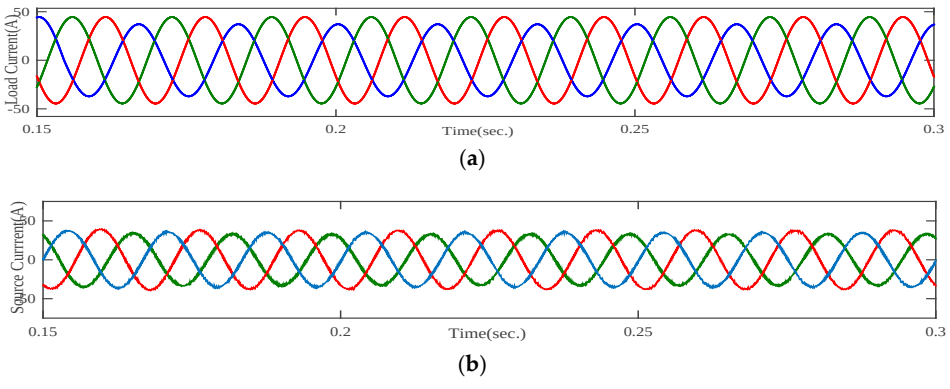
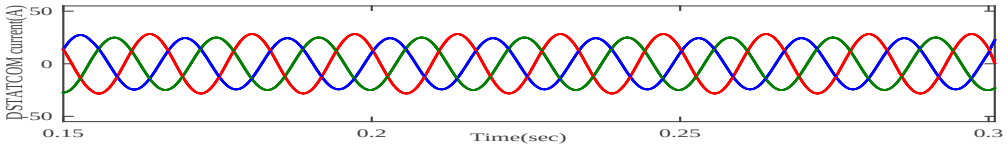


Figure 13. *Cont.*

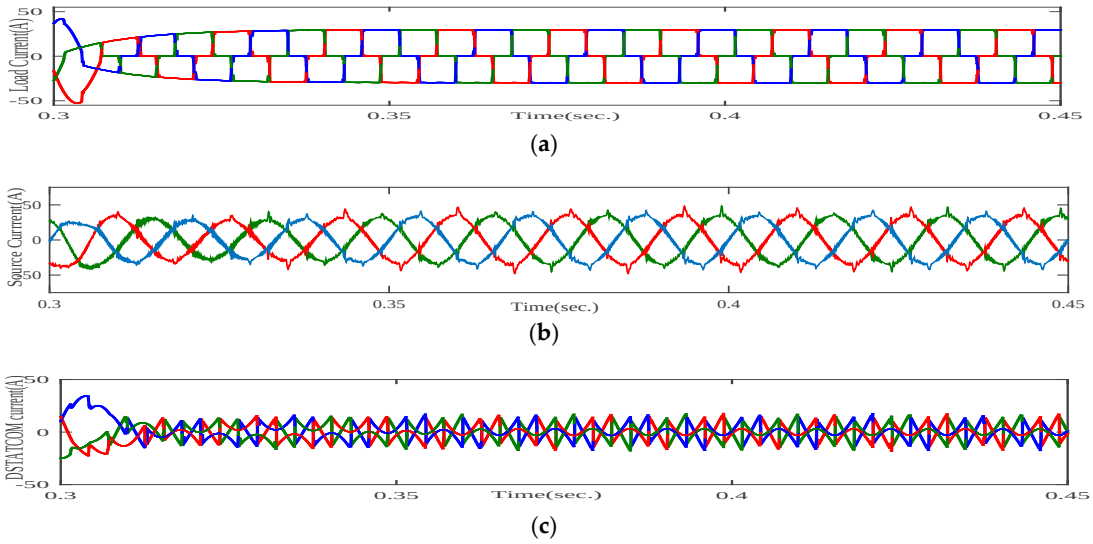


(**c**)

Figure 13. Currents under unbalanced load conditions. (**a**) Load current; (**b**) source current; and (**c**) DSTATCOM current.

5.1.2. Non-Linear Load Condition

The DSTATCOM system was investigated considering the non-linear load condition needed to validate the system performance. The diode bridge rectifier with a R-L load was considered to be a non-linear type load, and was connected to the system at t = 0.3 s. The PCC voltage of the system, as shown in Figure 8, is maintained under a non-linear load condition. The harmonic compensating current provided by the DSTATCOM, as shown in Figure 14a–c, forced the source current, supplying the active power component. The power supplied by the source, the DSTATCOM, and the power required by the load, are demonstrated in Figures 15–17 for linear and non-linear load conditions. The grid is only supplying active power, as the reactive power required by the load is compensated for by the DSTATCOM.



(**a**)

(**b**)

(**c**)

Figure 14. Currents under nonlinear load conditions. (**a**) Load current; (**b**) source current; and (**c**) DSTATCOM current.

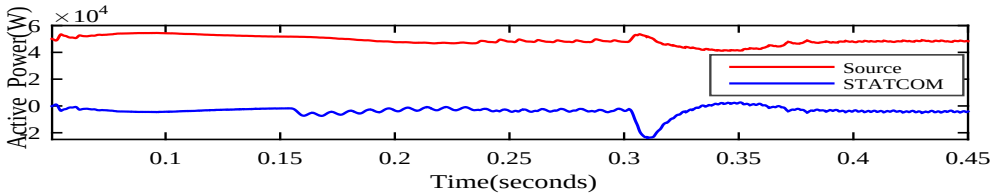


Figure 15. Active power supplied by source and DSTATCOM under different load conditions.

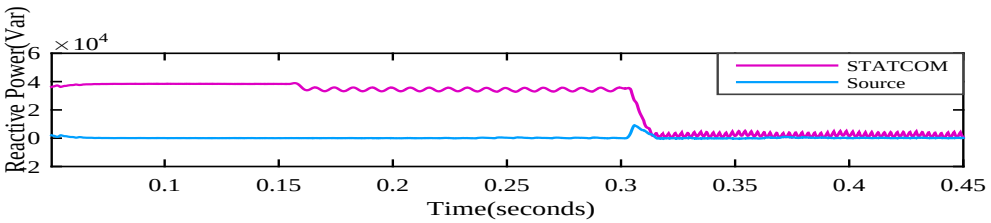


Figure 16. Reactive power supplied by source and DSTATCOM under different load conditions.

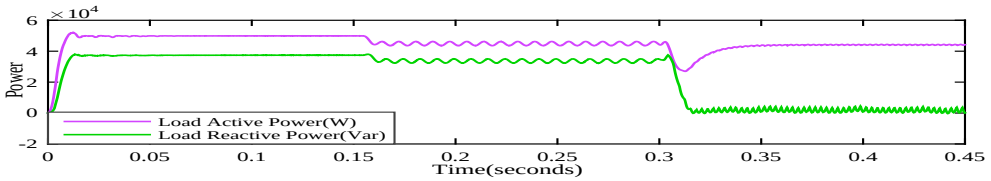


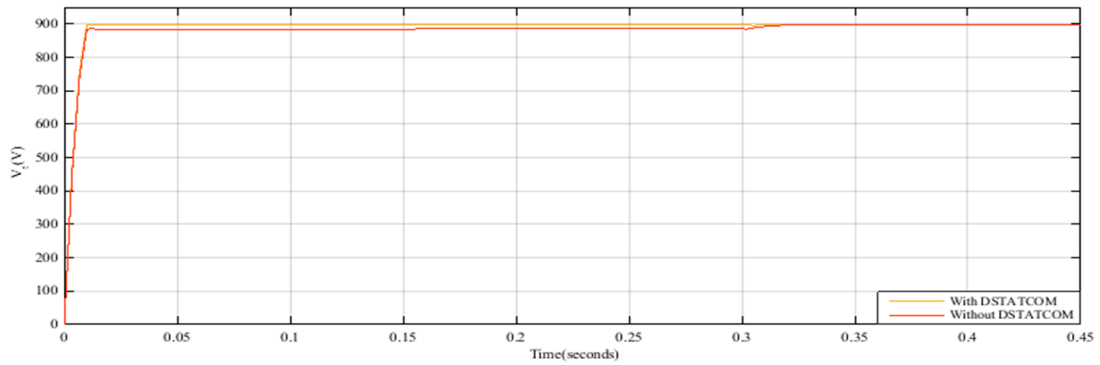
Figure 17. Load power required under different load conditions.

5.2. Power Quality Analysis

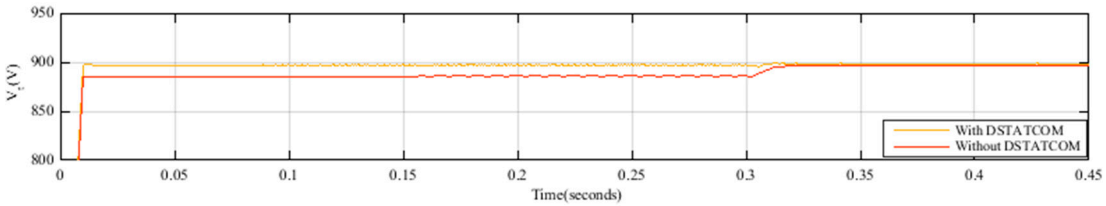
5.2.1. Voltage Disturbance

The change in load creates a disturbance in the PCC voltage of the system, resulting in voltage sag/swell. The DSATCOM system is capable of maintaining the PCC voltage under the normal condition, by supplying a compensating current. The PCC voltage shown in Figure 18a is balanced under the disturbance, caused by the unbalanced load condition and change in load. The terminal voltage at the PCC (V_t), computed using Equation (10), is examined to investigate the performance of the DSTATCOM and is used as a validation of its effectiveness. The reference V_t can be computed as in Equation (21):

$$V_t = \sqrt{\frac{2}{3}\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)} = \sqrt{\frac{2}{3}\left(3\left(\frac{1100}{\sqrt{3}}\right)^2\right)} = 898 \text{ V} \quad (21)$$



(**a**)



(**b**)

Figure 18. (**a**) Peak amplitude of PCC voltage during load change; and (**b**) zoomed view.

The PCC voltage of the system shown in the figure demonstrates the condition of the DSTATCOM when it is connected and unconnected to the system. The system without DSTATCOM is unable to maintain the V_t under a linear load condition and changes when there is perturbation, due to the connection of a non-linear load in the system. Thereore, the effectiveness of the CHBMLI-based DSTATCOM is investigated for V_t, considering the voltage disturbance due to perturbation in the load.

5.2.2. Fast Fourier Transform Analysis of Source Current under Various Load Conditions

As the switching frequency changes (i.e., increases in this case), the other important system parameter that is affected is the source current, and the THD in the source current decreases under linear load conditions, as shown in Table 2. Therefore, for a better application of the proposed system, the frequency should be high, while for a multilevel operation, the frequency should be kept within optimal limits to ensure that the switching losses do not exceed acceptable limits, as shown in Figures 19–21.

Table 2. Source current *THD* (total harmonics distortion) under different switching frequencies.

S. No.	Switching Frequency (Hz)	Source Current (*THD* %)
1.	1000	0.62
2.	2000	0.58
3.	3000	0.53
4.	4000	0.48
5.	5000	0.43

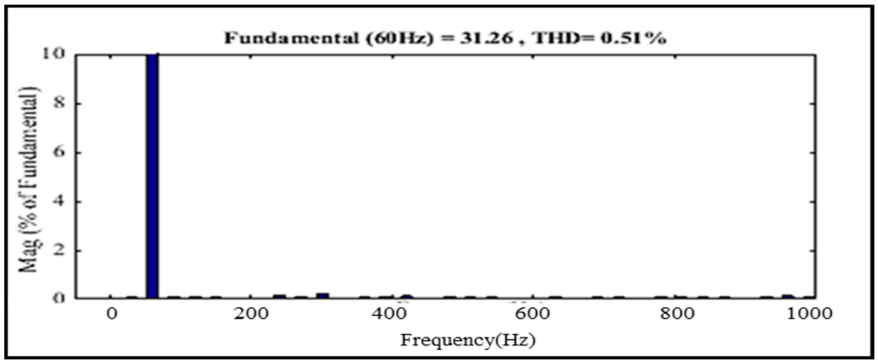


Figure 19. THD of source current under linear load conditions.

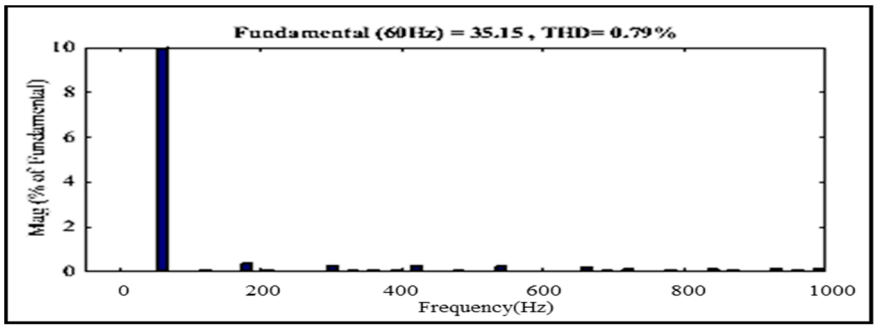


Figure 20. THD of source current under unbalanced load conditions.

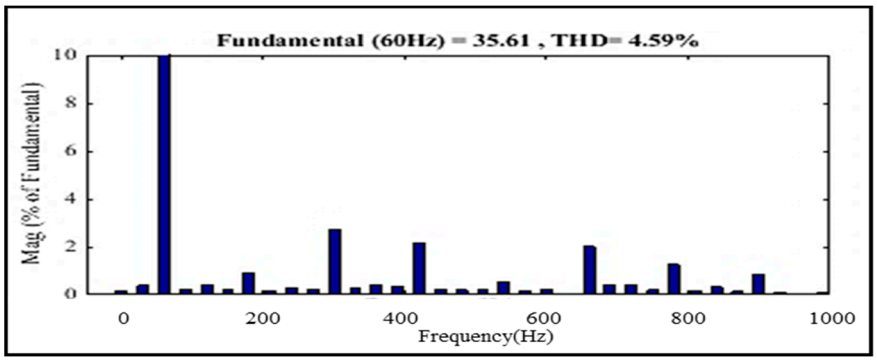


Figure 21. THD of source current under nonlinear load conditions.

A current THD of less than 5% is acceptable, as per IEEE Standard 519-1992 (IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems). The reduction in the source current distortion illustrates the effectiveness of components such as the MLI, the LCL filter, and the DC link capacitor, and that of the switching technique at different frequencies. To provide a complete DSTATCOM design with an appropriate control algorithm to prevent losses, avoid system complexity, and maintain operational stability, the control algorithm and all of the parameters must be selected correctly.

5.3. Effect of System Parameters

5.3.1. DC Link Capacitor

In this analysis of the DSTATCOM, the two important components that have been analyzed are the DC link capacitor and the coupling filter. The DC link capacitor is a prominent part of the proposed DSTATCOM system, in that each H-bridge cell contains an isolated DC link capacitor. In custom power device applications, it is desirable for the DC link capacitor to be small in size when compared with the AC capacitor bank, to compensate for the same amount of reactive power. The modulation index is kept constant by the insertion of a proportional controller into the system. The proportional controller maintains the amplitude of the error signal that is obtained by comparing the reference current with the source current. These parameters affect the capacitor value and vice versa, as depicted in Equation (6); this is verified by various results that were obtained by correct modelling of the system. The DC link capacitance affects the ripple in the DC bus voltage, irrespective of the applied filter.

While the system operation is quite complex, it is often found that the value of the DC link capacitor is also a very important factor in the current system, so further analysis is conducted based on different capacitor values and the performance is illustrated in the results. As the results show, different capacitor values produce different overshoot values, which can be easily understood using the results presented here. The voltage ripple in the DC link is inversely proportional to the capacitance value. This means that to produce a lower ripple in the DC link, it is necessary to choose the optimum capacitor value. The relationship between the voltage ripple and the capacitance is illustrated by the results shown in Figure 22a–c, which were obtained using capacitor values of 650, 950, and 1200 μF during linear load operation of the DSTATCOM. The simulation results obtained verify the relationship expressed in Equation (9) and we see that as the capacitor value increases, the ripples in the DC voltage decrease. Similarly, the transient response of the DC link voltage can be obtained for different capacitor values of 650, 800, and 950 μF, as shown in Figure 23. In this case, the switching frequency is kept constant at 1000 Hz and the load is changed at 0.5 s.

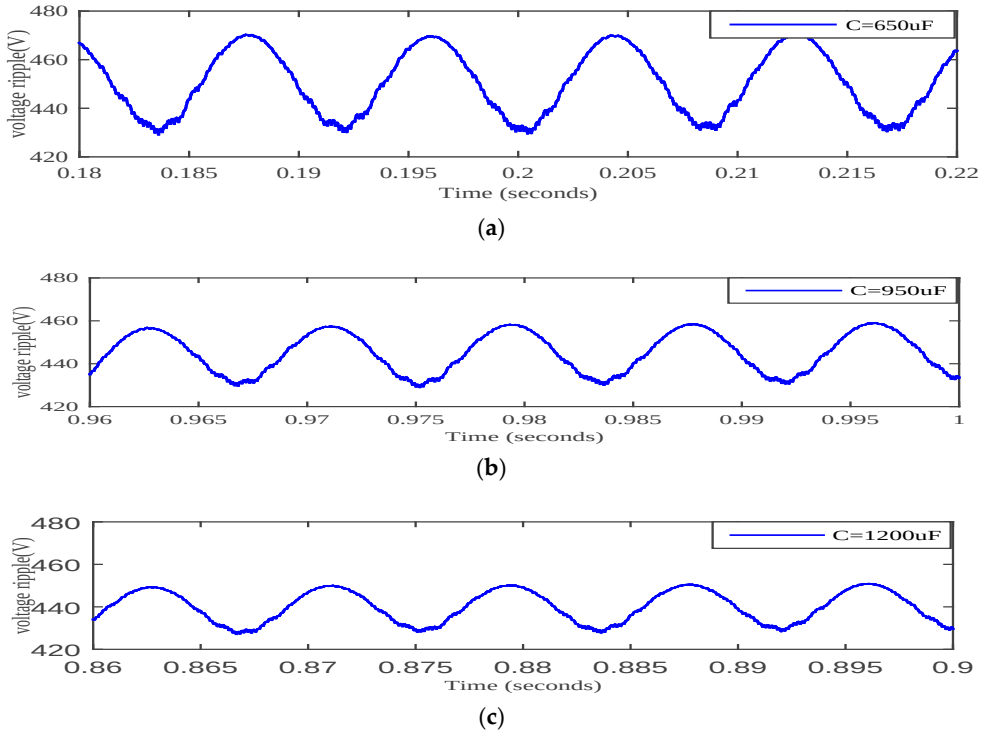


Figure 22. DC bus voltage ripples for different capacitor values. (**a**) C = 650 µF; (**b**) C = 950 µF; and (**c**) C = 1200 µF.

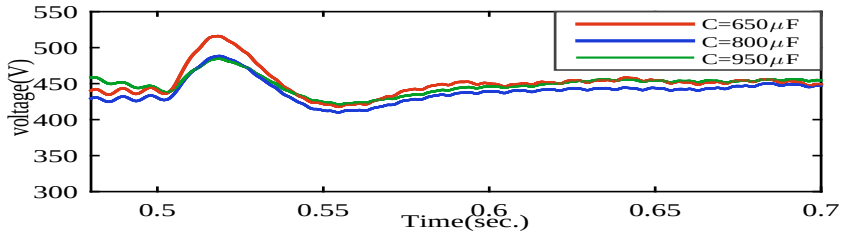


Figure 23. Transient overshoot waveforms of DC voltage for different capacitance values.

5.3.2. Switching Frequency

In this paper, the LCL filter is proposed for a lower switching frequency range and the differences in the system performance under these conditions are also analyzed. The analysis is also conducted on the basis of the switching frequency, as it varies from 1 kHz to 5 kHz. As we see, the switching frequency does not affect the DC voltage ripples in this case, and subsequent results confirmed that a variation of the switching frequency does not affect the DC voltage ripples, as shown in Figure 24. The magnitude of the ripples is almost identical for the three different switching frequencies.

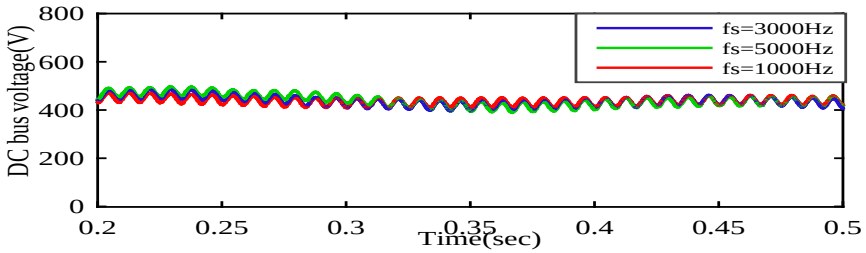


Figure 24. DC bus voltage of 450 V and voltage ripples at different switching frequencies.

6. Conclusions

An LCL filter interfaced cascaded H-bridge multilevel inverter-based (five-level) DSTATCOM is comprehensively analyzed and investigated considering load conditions, the power quality performance, and the effect of system parameters. The DC-link voltage is maintained using a PI controller for each H-bridge. The LCL filter is designed considering the constraints for a lower operating switching frequency (1–5 kHz) of CHBMLI. The performance of the CHBMLI-based DSTATCOM is evaluated for reactive power compensation, harmonic compensation, and load balancing under a linear load, Non-linear load, and unbalanced load condition. The power quality issues are investigated for a disturbance in the PCC voltage (voltage sag and swell) under an unbalanced load and load change condition. The source current THD under different load conditions (0.51% linear load, 0.79% unbalanced load, 4.59% nonlinear load) is achieved and is well within the IEEE-519 standards of 5%. The effect of switching frequency and the DC link capacitor on the DC link voltage ripples is investigated, to provide the optimum selection of system parameters.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Ghosh, A.; Ledwich, G. *Power Quality Enhancement Using Custom Power Devices*; Springer Science & Business Media LLC: Berlin, Germany, 2002.
2. Zeng, Z.; Li, H.; Tang, S.; Yang, H.; Zhao, R. Multi-objective control of multi-functional grid-connected inverter for renewable energy integration and power quality service. *IET Power Electron.* **2016**, *9*, 761–770. [CrossRef]
3. Dai, N.Y.; Lao, K.W.; Wong, M.C.; Wong, C.K. Hybrid Power quality conditioner for co-phase power supply system in electrified railway. *IET Power Electron.* **2012**, *5*, 1084–1094. [CrossRef]
4. Ise, T.; Hayashi, Y.; Tsuji, K. Definition of power quality levels and simplest approach for unbalanced power quality. In Proceedings of the Ninth International Conference on Harmonics and Quality of Power, Orlando, FL, USA, 1–10 October 2000; Volume 2, pp. 385–390.
5. Kushare, G.A.A.; Kala, S. Development of web based power quality monitoring system for handling user custom power quality query and auto power quality monitoring report notification via email. In Proceedings of the IET-UK International Conference on Information and Communication Technology in Electrical Sciences (ICTES 2007), Chennai, Indian, 20–22 December 2007; pp. 1–7.
6. Qader, M.R. A novel strategic-control-based distribution static synchronous series compensator (DSSSC) for power quality improvement. *Int. J. Electr. Power Energy Syst.* **2015**, *64*, 1106–1118. [CrossRef]
7. Zhou, G.; Wu, B.; Xu, D. Direct power control of multilevel inverter based active power filter. *Electr. Power Syst. Res.* **2007**, *77*, 284–294. [CrossRef]
8. Iyer, S.; Ghosh, A.; Joshi, A. Inverter topologies for DSTATCOM application-asimulation study. *Electr. Power Syst. Res.* **2005**, *75*, 161–170. [CrossRef]
9. Grady, W.M.; Samotyj, M.J.; Noyola, A.H. Survey of active power line conditioning methodologies. *IEEE Trans. Power Delivery* **1990**, *5*, 1536–1542. [CrossRef]
10. Balikci, A.; Akpinar, E. A multilevel converter with reduced number of switches in STATCOM for load balancing. *Electr. Power Syst. Res.* **2015**, *123*, 164–173. [CrossRef]
11. Li, S.; Xu, L.; Haskew, T.A. Control of VSC-based STATCOM using conventional and direct-current vector control strategies. *Electr. Power Energy Syst.* **2013**, *45*, 175–186. [CrossRef]
12. Dike, D.O.; Mahajan, S.M. Voltage stability index-based reactive power compensation scheme. *Int. J. Electr. Power Energy Syst.* **2015**, *73*, 734–742. [CrossRef]

13. Gupta, V.K.; Mahanty, R. Optimized switching scheme of cascaded H-bridge multilevel inverter using PSO. *Int. J. Electr. Power Energy Syst.* **2015**, *64*, 699–707. [CrossRef]
14. Rao, G.N.; Raju, P.S.; Sekhar, K.C. Harmonic elimination of Cascaded H-bridge multilevel inverter based active power filter controlled by intelligent techniques. *Int. J. Electr. Power Energy Syst.* **2013**, *61*, 56–63.
15. Gupta, R.; Ghosh, A.; Joshi, A. Control of cascaded transformer multilevel inverter based DSTATCOM. *Electr. Power Syst. Res.* **2007**, *77*, 989–999. [CrossRef]
16. Panda, A.K.; Patnaik, S.S. Analysis of cascaded multilevel inverters for active harmonic filtering in distribution networks. *Int. J. Electr. Power Energy Syst.* **2015**, *66*, 216–226. [CrossRef]
17. Bradaschia, F.; Limongi, L.R.; Cavalcanti, M.C.; Neves, F.A.S. A generalized scaler pulse-width modulation for nine-switch inverters: An approach for non-sinusoidal modulating waveform. *Electr. Power Syst. Res.* **2015**, *212*, 302–312. [CrossRef]
18. Akagi, H.; Watanabe, E.H.; Aredes, M. *Instantaneous Power Theory and Applications to Power Conditioning*; John Wiley & Sons, Inc.: Hoboken, NJ, USA, 2007.
19. Tripathi, R.N.; Singh, A. Design and control of grid interconnected solar photovoltaic (SPV) System with improvement in power quality. In Proceedings of the IEEE 5th International Conference on Power and Energy Systems (Advances in Power System), Kathmandu, Nepal, 28–30 October 2013.
20. Zafari, A.; Jazaeri, M. STATCOM systems in distribution and transmission systems: A review of power-stage topoloies and control methods. *Int. Trans. Electr. Energy Syst.* **2016**, *26*, 323–346. [CrossRef]
21. Lee, T.L.; Taiwan, K.; Hu, S.-H.; Chan, Y.H. D-STATCOM with positive-sequence admittance and negative-sequence conductance to mitigate voltage fluctuations in high-level penetration of distributed-generation systems. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1417–1428. [CrossRef]
22. Chellammal, N.; Dash, S.S.; Premalatha, S.; Rayaguru, N.K. Three phase Multicurrier PWM Switched Cascaded Multilevel Inverter as Voltage Sag Compensator. *AASRI Procedia* **2012**, *2*, 282–287. [CrossRef]
23. Young, C.M.; Wu, S.F. Selective harmonic elilmination in multi-level inverter with zig-zag connection transformers. *IET Power Electron.* **2014**, *7*, 876–885. [CrossRef]
24. Pandey, R.; Tripathi, R.N.; Hanamoto, T. Multiband HCC for cascaded H-bridge multilevel inverter based DSTATCOM. In Proceedings of the 2016 IEEE 11th Conference on Industrial Electronics and Applications (ICIEA), Hefei, China, 5–7 June 2016.
25. Zhao, G.; Liu, J.; Han, M. Design of input filters considering the stability of STATCOM system. *J. Power Electron.* **2011**, *11*, 904–913. [CrossRef]
26. Vodyakho, O.; Chris, C.M. Three level inverter based shunt active power filter in phase three-wire and four wire systems. *IEEE Trans. Power Electron.* **2009**, *24*, 1350–1363. [CrossRef]
27. Shin, D.; Kim, H.; Lee, J.; Kim, T. Design of LCL filter for improving robustness of grid-connected voltage source inverter. In Proceedings of the 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, USA, 14–18 September 2014; pp. 2940–2946.
28. Sirisukprasert, S. The Modelling and Control of a Cascaded-Multilevel Converter—Based STATCOM. Ph.D. Thesis, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, 13 February 2004.
29. Tripathi, R.N.; Singh, A.; Hanamoto, T. Design and control of LCL filter interfaced grid connected solar photovoltaic (SPV) System using power balance theory. *Int. J. Electr. Power Energy Syst.* **2015**, *69*, 264–274. [CrossRef]
30. Zue, A.O.; Chandra, A. Simulation and staibility analysis of a 100 KW grid connected LCL photovoltaic inverter for industry. In Proceedings of the 2006 IEEE Power Engineering Society General Meeting, Montreal, QC, Canada, 18–22 June 2006.
31. Teodorescu, R.; Blaabjerg, F.; Borup, U.; Liserre, M. New control structure for grid-connected LCL PV inverters with zero steady-state error and selective harmonic compensation. In Proceedings of the Nineteenth annual Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 22–26 February 2004; Volume 1, pp. 580–586.