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Performance Improvement for Two-Stage Single-Phase Grid-Connected Converters Using a Fast DC Bus Control Scheme and a Novel Synchronous Frame Current Controller

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Abstract: Two-stage single-phase grid-connected converters are widely used in renewable energy applications. Due to the presence of a second harmonic ripple across the DC bus voltage, it is very challenging to design the DC bus voltage control scheme in single-phase grid-connected inverters. The DC bus voltage controller must filter the ripple and balance a tradeoff between low harmonic distortion and high bandwidth. This paper presents a fast DC bus voltage controller, which uses a second order digital finite impulse response (FIR) notch filter in conjunction with input power feedforward scheme to ensure the steady-state and dynamic performance. To gain the input power without extra hardware, a Kalman filter is incorporated to estimate the DC bus input current. At the same time, a modulation compensation strategy is implemented to eliminate the nonlinearity of the grid current control loop, which is caused by the DC bus voltage ripple. Moreover, a novel synchronous frame current controller for single-phase systems is also introduced, and its equivalent model in stationary frame has been derived. Simulation and experimental results are provided to verify the effective of the proposed control scheme.

Keywords: grid-connected converter; DC bus voltage controller; finite impulse response (FIR) notch filter; Kalman filter; synchronous frame current controller

1. Introduction

Renewable energy is the key to future global sustainability. Two-stage converters are widely used for interfacing renewable energy resources with the utility grid. The first stage is typically a DC-DC converter for photovoltaics (PVs) or an AC-DC rectifier for wind turbines (WTs) [1]. Normally, the first stage performs maximum power point tracking (MPPT) and boosts the input voltage into an appropriate level for the second stage. The main task of the second stage (a DC-AC inverter for most systems) is to ensure that all of the power extracted by the first stage is transferred to the grid stably and smoothly [2,3]. Figure 1 shows the configuration of a two-stage single-phase grid-connected converter.

For a two-stage single-phase grid-connected converter, the instantaneous output power pulsates at twice line frequency (2-f). As a strong and robust MPPT control strategy is implemented for the first stage, the input power is controlled to a maximum and constant level at steady state [4]. Thus, the DC bus is used to decouple the power pulsation of grid side from the source side. The DC bus capacitor functions as an internal energy storage device to supply the oscillatory output power demand. As a result, there is a 2-f ripple across the DC bus voltage. Regulating the DC bus voltage, which is

conducted by the second stage, is vitally important in order to guarantee the reliable operation of the power systems [5].

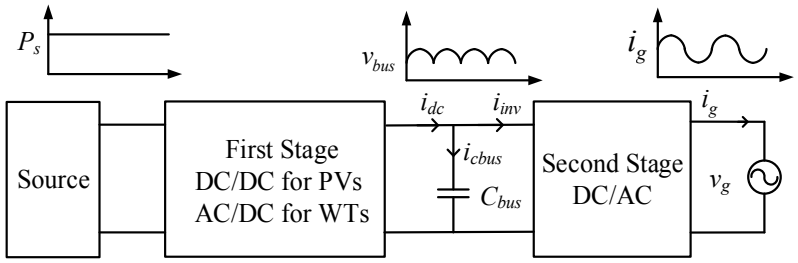

Figure 1. Configuration of a two-stage single-phase grid-connected converter.

The DC-AC inverter is controlled by a dual-loop control strategy. The outer loop controls the DC bus voltage by generating the reference current for the inner current loop. The inner controller is aimed to achieve adaptive and accurate current tracking. Conventionally, a proportional-integral (PI) controller is utilized to regulate the bus voltage, but it is hard to address the problem caused by the 2-f ripple. As a consequence, the reference for the output current is distorted, and there is a third harmonic component and a phase shift (which causes reactive current injection) at the grid current [6]. According to IEEE standard 929-2000 [7], the current total harmonic distortion (THD) must be limited to less than 5%. In order to ensure the quality of the grid current, the bandwidth of the bus voltage control loop is significantly reduced, which makes the transient response poor. The designer has to use large capacitor or high-voltage power switching devices in case of triggering over the voltage protection or malfunction of the inverter during transients. A solution to reduce the 2-f voltage ripple is to connect the energy storage elements to the bus through an active low-frequency ripple control device (ALFRCD), which injects harmonic current into the DC bus [8,9]. This approach solves the problem by essentially eliminating the ripple at the bus voltage, while using a minimal bus capacitor. Nevertheless, it exhibits low efficient, and needs complex hardware and control systems for power applications, which makes the overall system expensive or inefficient.

To suppress the distortion in the output current, a second order infinite impulse response (IIR) notch filter [10] or a high order FIR filter [11] can be introduced into the bus control loop to filter the second harmonic ripple. These methods successfully eliminate the distortion. However, since the notch filter brings about a large negative phase shift at the frequencies lower than the notch frequency, the increase of the bus voltage control loop crossover frequency is limited, and dynamic performance can't be good enough. In [12], a power feedforward control scheme, which is one of direct power control (DPC) schemes, is proposed to reduce the DC bus capacitance requirements and to improve the dynamic response for pulse width modulation (PWM) rectifiers. In order to implement the power feedforward control scheme in two-stage single-phase grid-connected converters, the DC bus input current is required and can be provided by the MPPT controller or extra current sensors. However, various topologies are used for the first stage, such as PV module-integrated DC-DC converters [13], interleaved parallel DC-DC converters [14], multi-string topologies [15] or multiple renewable energy sources [16]. At the same time, the DC-AC inverters in distributed generation systems often provide multi-functions such as, energy management for energy storage devices, power sharing for local loads, communication devices, protection units, and the control center [17]. Thus, controlling the two stages by separate processors is required to spread the computational load and enhance the flexible of the system, which makes the power feedforward control hard to implement.

The other main task of the inverter is to rapidly follow the reference current signals. Therefore, a fast and robust grid current control scheme is required. However, the 2-f voltage ripple also affects the grid side current control loop. Reference [18] illustrates that the current control loop turns to be a nonlinear system when considering the bus voltage ripple. The nonlinear section becomes a

harmonics source for the output current. Besides, the current regulator should be selected reasonably. Synchronous frame controllers are originally introduced for three-phase systems, and then extended to single-phase applications. In single-phase systems, the traditional approach is to create a set of imaginary quantities orthogonal to those of the single-phase system so as to obtain DC quantities by means of a $\alpha\beta/dq$ transformation. The orthogonal component is provided by an orthogonal signal generation (OSG) block [19,20]. This control method is described as virtual vector control. Although the steady-state performance of the virtual vector control is acceptable, the OSG block makes the controller complicated and hard to analyze the stability. As a result, the implementation of this method for a single-phase grid-connected inverter with an inductor-capacitor-inductor (LCL) filter is difficult.

In this paper, an accurate math model is proposed to analyze the ripple-caused harmonic for PI-based DC bus voltage control loop. A novel DC bus voltage controller is introduced, which is able to improve the transient response of the DC bus voltage control loop significantly. In this method, a second order digital FIR notch filter is implemented to eliminate the distortion in the reference current. At the same time, the input power feedforward control scheme is used to improve the dynamic performance. A DC bus input current estimator using a Kalman filter is established to identify the input current magnitude and to suppress noises without extra hardware. To eliminate the nonlinear section of grid current control system, which is caused by the DC bus voltage ripple, a modulation compensation strategy is also introduced.

Moreover, a novel synchronous frame current controller is proposed for a single-phase grid-connected inverter with an LCL filter. A theoretical analysis method is provided to illustrate its equivalent model in stationary frame. Thanks to the phase-locked loop (PLL), unlike the conventional proportional-resonant (PR) controller in stationary frame, the proposed synchronous frame controller is not sensitive to the grid fundamental frequency variation, while remaining the advantage of zero steady-state error and fast transient response.

This paper is organized as follows: Section 2 provides the analysis of the harmonic distortion caused by DC bus voltage ripple for a conventional control system, Section 3 presents the proposed DC bus voltage controller, the modulation compensation strategy and the novel synchronous frame current control scheme for single phase systems. Section 4 covers the system design and simulation. Section 5 presents experimental results of the proposed control scheme, and Section 6 draws a conclusion.

2. Model of an Inverter with a Conventional Control System

2.1. Bus Voltage Control System

Figure 2a shows the schematic of a single-phase grid-connected inverter with an LCL filter. C_{bus}, L_1, L_2, C and R_d are the bus capacitor, inverter side inductor, grid side inductor, the capacitor of LCL filter and damping resistor, respectively. i_{dc} and i_{inv} denote the input current and output current of the DC bus. i_{cbus}, i_c, i_{L1} and i_g denote the current of C_{bus}, C, L_1 and L_2, respectively. v_{inv} is the inverter output voltage.

Figure 2b presents a typical control system for the inverter. $G_{c\text{-}bus}(s)$ denotes the transfer function of the bus voltage controller, $G_{c\text{-}current}(s)$ denotes the transfer function of the inner current controller. The bus voltage controller ensures the bus voltage v_{bus} equal to its reference value V_{ref}. The output of bus voltage controller acts as the reference value for the amplitude of the output current and is called I_{ref}. The signal after multiplication with the PLL signal, which is synchronous and in-phase with the grid voltage v_g, generates a reference for the grid current and is denoted by i_{ref}. The current control loop regulates the grid current (i_g) according to the reference (i_{ref}). Passive or active damping techniques are required to smooth the resonance peak of the LCL filter.

Conventionally, a PI controller is used to regulate the DC bus voltage. A simplified model of the bus voltage control system is presented in Figure 2c, where K_{pv} and K_{iv} are the proportional gain and the integral gain of the bus voltage controller, respectively. The block diagram shows that the bus voltage control loop is not in the form of a linear time invariant (LTI) loop, due to the two multiplications

before and after the current control system. The two multiplications introduce time-varying terms into the equations, which lead to the intrinsic nonlinearity of single-phase systems. Generally, the current control loop is designed much faster than the bus voltage controller. Thus, the interaction between the two control loops can be neglected, and the designs of the two loops are done independently. During the analysis of bus voltage control system, we assume that the current control loop is fast and its transients are neglected as compared to the relative slow bus voltage control loop. Based on the assumption, the current control loop is substituted with unity gain.

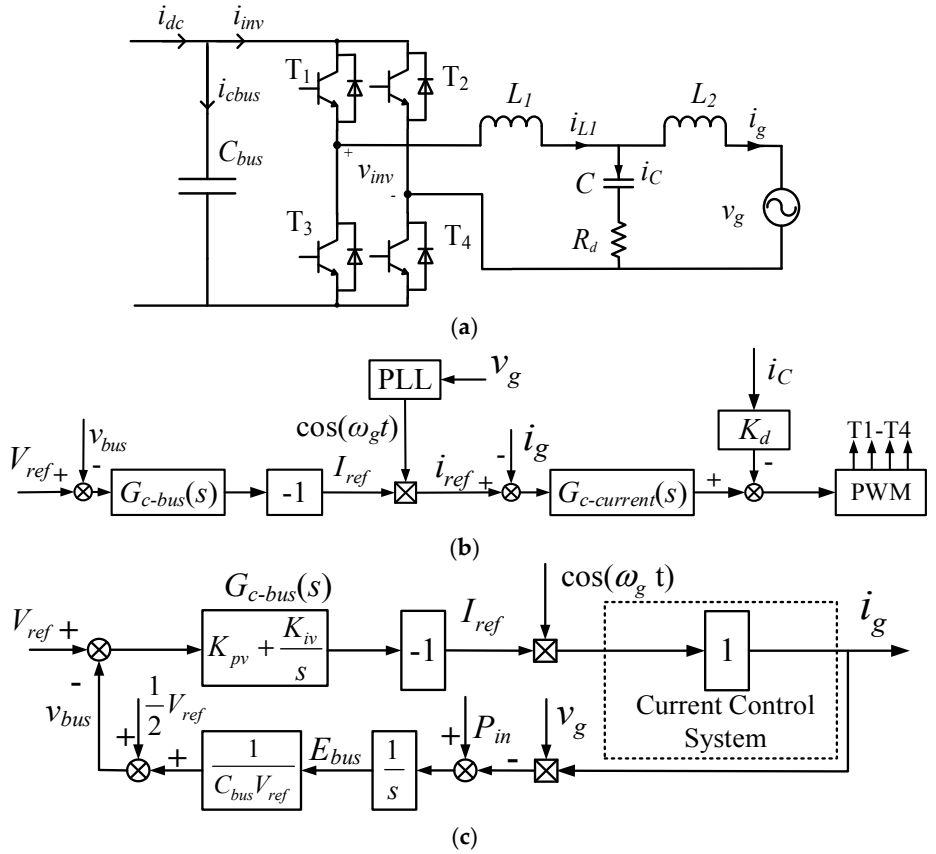

Figure 2. (**a**) Circuit diagram of a single-phase grid-connected inverter with an LCL filter; (**b**) control system of the inverter; and (**c**) simplified model of the bus voltage control system.

The instantaneous output power of an inverter P_g is calculated as $P_g = v_g \times i_g = V_g \cos(\omega_g t) \times I_{ref} \cos(\omega_g t) = 0.5 \times V_g I_{ref} + 0.5 \times V_g I_{ref} \cos(2\omega_g t)$. Where V_g is the amplitude of the grid voltage, ω_g is the fundamental frequency of grid voltage. Ideally, I_{ref} only contains DC component. Neglecting the possible power losses, the balance of the power relationship is expressed as $P_{in} = P_{bus} + P_f + P_g$. The input power to the bus (P_{in}) is extracted from the primary source. As a MPPT controller is implemented for the first stage, P_{in} is controlled to a maximum and constant level at steady state. P_f is the instantaneous power of the inverter output filter. P_{bus} denotes the instantaneous power of the bus capacitor. The DC bus capacitor is used to decouple the power ripple by providing low-frequency current. As a result, there is a 2-f ripple across the DC bus voltage.

A similar situation exists when three phase grid-connected voltage source converters mean to operate under voltage unbalanced sags produced by grid faults [21]. A large power ripple is produced by the existence of negative sequence components in the grid voltage. The injection of negative-sequence currents can be used to suppress the oscillation on the DC bus voltage due to the oscillation of the power injected to the grid. However, when considering the power ripple produced

by a large grid connection inductance, the designers face a dilemma whether to compensate the ripple in the power injected to the grid or the ripple in the converter output power.

P_f is neglected in this paper as it is a more general situation. The bus voltage is denoted by v_{bus}. The energy of the bus capacitor is expressed as $E_{bus} = 0.5 \times C_{bus}{v_{bus}}^2$. Since the bus voltage ripple Δv_{bus} is much smaller than v_{bus} in most situation, this nonlinear term is linearized as follows:

$$\begin{aligned} E_{bus} &= \tfrac{1}{2}C_{bus}v_{bus}^2 = \tfrac{1}{2}C_{bus}(V_{ref} + \Delta v_{bus})^2 \\ &\approx \tfrac{1}{2}C_{bus}V_{ref}^2 + C_{bus}V_{ref}\Delta v_{bus} \end{aligned} \tag{1}$$

$$v_{bus} \approx \frac{E_{bus}}{C_{bus}V_{ref}} + \frac{1}{2}V_{ref} \tag{2}$$

Figure 3 describes the formation process of the harmonic distortion. The 2-f ripple in bus voltage causes a same frequency ripple in the amplitude of reference current. After the regulation of the current control loop, the output current is distorted. In order to analyze the distortion, I_{ref} is assumed to include a DC component (a_0) and a second harmonic component (a_2). θ is the phase angle of the second harmonic. 4th and higher order harmonics are neglected in the analysis. I_{ref} is given by:

$$I_{ref} = a_0 + a_2\cos(2\omega_g t + \theta) \tag{3}$$

Considering the gain of the bus voltage controller $G_{c\text{-}bus}(s)$ at $2\omega_g$, an equation is given as follows:

$$\begin{aligned} \int_0^t [P_{in} - V_g\cos^2(\omega_g t)I_{ref}]\mathrm{d}t * \frac{|G_{c\text{-}bus}(j2\omega_g)|}{C_{bus}V_{ref}} \\ = a_2\cos(2\omega_g t + \theta) \end{aligned} \tag{4}$$

As derived in the Appendix A, Equations (5) and (6) are given as follows:

$$P_{in} = \frac{V_g}{2}a_0 + \frac{V_g}{4}a_2\cos(\theta) \tag{5}$$

$$\begin{cases} a_2 \approx \frac{a_0|G_{c\text{-}bus}(j2\omega_g)|V_g}{4\omega_g C_{bus}V_{ref}\sin(\theta) - |G_{c\text{-}bus}(j2\omega_g)|V_g\cos(\theta)} \\ \theta = \arctan\left(-\frac{4\omega C_{bus}V_{ref}}{|G_{c\text{-}bus}(j2\omega_g)|V_g}\right) \\ |\Delta v_{bus}|_{\mathrm{pp}} \approx \frac{2a_2}{|G_{c\text{-}bus}(j2\omega_g)|} \end{cases} \tag{6}$$

where $|\Delta v_{bus}|_{\mathrm{pp}}$ is the peak to peak value of the bus voltage ripple at steady state. The grid current i_g is therefore given by (7) and (8):

$$\begin{aligned} i_g &= I_{ref}\cos(\omega_g t)\Big) \\ &= I_{g1}\cos(\omega_g t + \varphi) + I_{g3}\cos(3\omega_g t + \theta) \end{aligned} \tag{7}$$

$$\begin{cases} I_{g1} = \sqrt{a_0^2 + \frac{1}{4}a_2^2 + a_0 a_2\cos(\theta)} \\ I_{g3} = \frac{a_2}{2} \\ \varphi = \arctan(\frac{a_2\sin(\theta)}{2a_0 + a_2\cos(\theta)}) \end{cases} \tag{8}$$

where I_{g1} and I_{g3} are the amplitudes of fundamental component and third harmonic, respectively. φ stands for phase angle of the fundamental current. The THD of the gird current is approximately given by:

$$\mathrm{THD} \approx \frac{a_2}{2\sqrt{a_0^2 + 0.25a_2^2 + a_0 a_2\cos(\theta)}} \tag{9}$$

If $a_0 >> a_2$, Equation (5) can be simplified as:

$$P_{in} \approx \frac{V_g}{2} a_0 \tag{10}$$

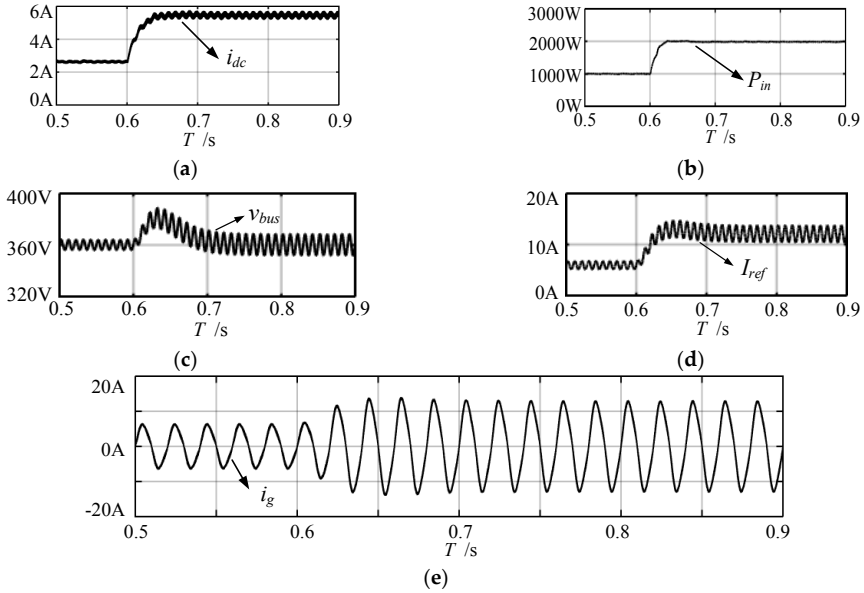

Figure 3. Waveforms of a two-stage single-phase gird-connected inverter using a small DC bus capacitor and a PI-based DC bus voltage controller. (**a**) Input current; (**b**) Input power; (**c**) Bus voltage; (**d**) The amplitude of the reference current; and (**e**) Grid current.

To verify the proposed math model, a two-stage single-phase PV system is simulated by using MathWorks MATLAB/Simulink software R2014b. The simulation parameters are described in Section 4. Figure 4 shows the amplitudes of the third harmonic current, which are obtained by using theoretical calculation and simulation.

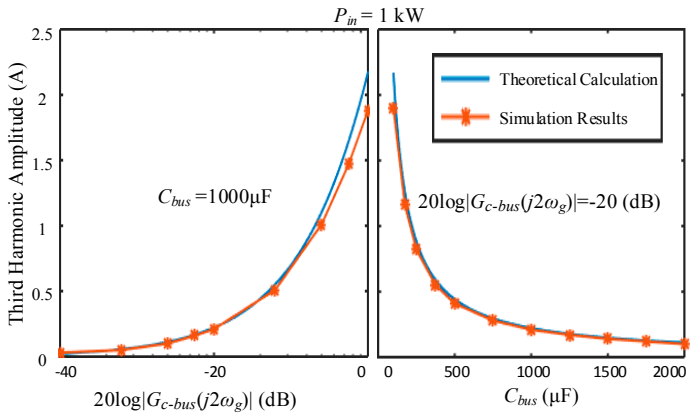

Figure 4. Third harmonic component amplitudes under different system parameters.

The input power of the inverter (P_{in}) is set as 1 kW. For the left diagram, C_{bus} remains unchanged at 1000 μF. The amplitude of the third harmonic increases significantly with increasing the gain of the bus voltage controller ($20\log|G_{c\text{-}bus}(j2\omega_g)|$). The gain of the bus voltage controller is kept constant as −20 dB for the right diagram. The harmonic distortion decreases with the increasing of the DC bus capacitor. The simulation results match calculated values very well for C_{bus} > 250 μF

or $20\log|G_{c\text{-}bus}(j2\omega_g)| < -6$. The difference between the two approaches is owing to fact that the proposed math model uses approximate value of bus voltage and neglects other harmonic sources.

2.2. Grid Current Control System

Similarly, like the bus voltage control system, the DC bus voltage ripple also has a great impact on the grid current control scheme, which is neglected and substituted with unity gain in Section 2.1. To analyze the ripple-caused problems for current control loop, a modified current control scheme, with the consideration of DC-link voltage ripple, is presented in Figure 5a. Where G_{PWM} and $G_f(s)$ denote the transfer function of the PWM section and the output filter. Since the bus voltage ripple is time varying, the transfer function of the dashed box in Figure 5a cannot be derived. As pointed in [22], the nonlinear section becomes a harmonic source. However, for the current control scheme, it is very difficult to quantitatively calculate the amplitudes of the harmonics, which are caused by the bus voltage ripple.

In order to explain the process of harmonic generation, a simplified discrete-time mode is presented in Figure 5b. The reference current and the bus voltage ripple are supposed to be pure sinusoidal, $i_{ref}(n) = I_{ref}\cos(\omega_g nT_s)$, $\Delta v_{bus}(n) = 0.5|\Delta v_{bus}|_{pp} \times \cos(2\omega_g nT_s)$. The output current $i_g(n)$ is created by multiplying the error signal $err(n)$ by the bus voltage $v_{bus}(n)$. For multiplication in the time domain is equivalent to convolution in the frequency domain, the current harmonics are regarded as a convolution of error signals and the ripple signals. By filtering the 5th order harmonic from the feedback signal, a closed-form solution to calculate the amplitudes of the ripple-caused harmonics is proposed in [22]. Nevertheless, the math model cannot be accurate for neglecting the gain variations of the current controller and output filter at different frequency stage, especially when a PR controller is implemented as the current controller.

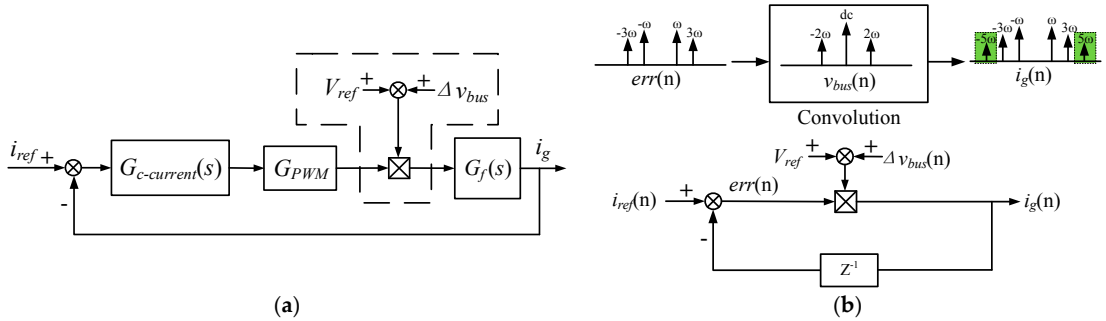

Figure 5. (**a**) Current control scheme considering the DC bus voltage ripple; (**b**) Simplified discrete-time mode.

The PR controller is given by (11). Where $K_{p\text{-}pr}$ and $K_{r\text{-}pr}$ are the proportion gain and resonant gain of the controller, respectively. If a PR controller is used to regulate the grid current, its resonance frequency is in alignment with the fundamental frequency. The PR controllers present different gains at the fundamental frequency and other frequencies [23], which makes the calculation of the ripple-caused harmonic too complicated to be procurable:

$$G_{pr}(s) = K_{p\text{-}pr} + \frac{K_{r\text{-}pr}s}{s^2 + \omega_0{}^2} \tag{11}$$

From the aforementioned analysis, conclusions can be shown as follows:

(1) The 2-f voltage ripple leads to a third harmonic component and a phase shift in the output current. In a similar way, 4-f power pulsation leads to 5th order harmonic current, and so on.

(2) There is a negative correlation between the harmonic distortion (I_{g3}) and the bus capacitor value (C_{bus}). Larger capacitance leads to lower harmonic content, but increases the cost, size and weight of the converter.

(3) There is a positive correlation between the harmonic distortion and the gain of the bus voltage controller ($|G_{c\text{-}bus}(j2\omega_g)|$). With a lower gain, there is less distortion in the grid current. However, a low gain may lead to poor transient response or to instability, two properties that are affected by one main parameter, the loop bandwidth. The bus voltage control loop presents a tradeoff between harmonic distortion and bandwidth, which is controlled by the gain of the controller. Thus, a simple PI controller, which is used as bus voltage controller, is unable to address the ripple-caused difficulties.

(4) The 2-f bus voltage ripple also brings about a nonlinear section in the grid current control scheme, which makes contributions to the increase in harmonic component.

3. Proposed Control Scheme

To minimize the DC bus capacitor, the oscillation on the DC bus should be tolerated. Correspondingly, the control system should have the ability to suppress the ripple-caused distortion. This section introduces the proposed controller, which can achieve excellent steady-state and dynamic performances.

First of all, a second order FIR notch filter is introduced to bus voltage regulator with the purpose of filtering the double frequency ripple. The design of a bus control system including the second order FIR notch filter is discussed. The bus voltage control system is simplified as an approximate linear model. Based on the model, the stability analysis and parameters design for the bus voltage control loop can be carried out. To further improve dynamic response to input transient, an input current estimator using Kalman filter is also established to implement the input power feedforward.

Improvements for the current control loop are also presented in this section. As discussed in Section 2, the ripple-caused nonlinearity, in the grid current control scheme, becomes a harmonic source. To eliminate the nonlinearity, a modulation compensation strategy is proposed. With the implement of this strategy, the current control loop is linearized. The harmonic distortion is reduced, correspondingly. Moreover, a novel synchronous frame scheme is proposed to achieve high performance current tracking for the single-phase grid-connected systems.

3.1. FIR Notch Filter Inserted Bus Voltage Regulator

As described in Section 2.1, decreasing the gain of the bus voltage controller at $2\omega_g$ can reduce the harmonic distortion. Using a second order FIR notch filter, which is tuned at 2-f harmonic, in the bus control loop prevents the 2-f harmonic from polluting the reference current. By filtering the 2-f voltage ripple, the notch filter rejects both the third harmonic and the phase shift to the fundamental current. Moreover, since the grid voltage and grid current may contain undesired harmonic components, 4th and 6th order harmonic ripple components could be found in the DC bus voltage. Therefore, extra FIR notch filters, which are tuned at the 4th and 6th order harmonics, are also needed in some cases.

Since the bus voltage control loop is not linear and not time invariant, it is a great challenge to analyze the stability and dynamic response of the loop. Instead of using the direct and complex feedback signals, the control system is simplified in terms of the average signals. The advantage of the averaged signals method is that it leads to a linear and time invariant model. By averaging instantaneous signals over half of a line cycle (12) and (13), the average signals do not contain second harmonic components. They interact through operators that may be approximated as linear and time invariant [11]. The average DC bus voltage is given as (12). $v_{bus}(t)$ only contains DC component at steady state. We also assume that the harmonic distortion is blocked by the controller, and only

fundamental component in the grid current. Therefore, the average output power $P_g(t)$ is written as (13):

$$v_{bus}(t) = \int_{t-\frac{\pi}{2\omega_g}}^{t+\frac{\pi}{2\omega_g}} v_{bus}(\tau)\mathrm{d}\tau \tag{12}$$

$$P_g(t) = \int_{t-\frac{\pi}{2\omega_g}}^{t+\frac{\pi}{2\omega_g}} p_g(\tau)\mathrm{d}\tau = \frac{V_g}{2} I_g(t) \tag{13}$$

where $I_g(t)$ is the peak value of fundamental grid current. $I_g(t)$ is also assumed be equal to the output of the bus voltage controller (I_{ref}). Since the second order ripple in the output power ($P_g = 0.5 \times V_g I_g + 0.5 \times V_g I_g \cos(2\omega_g t)$) is neglected, a constant gain $0.5 \times V_g$ is used to describe the relationship between $I_g(t)$ and $P_g(t)$. Thus, an approximate linear model of the bus voltage control system is obtained. Figure 6a gives the control block diagram of the FIR notch filter inserted bus voltage regulator ($G_{c\text{-}bus}(z)$), which is comprised of an FIR notch filter ($G_{NF}(z)$) and a loop compensator ($H_c(z)$).

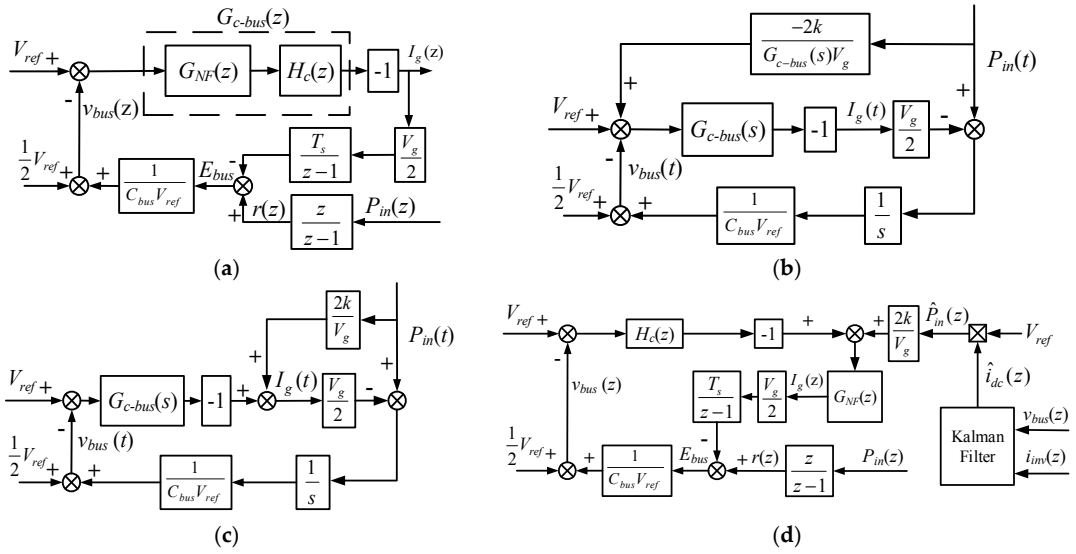

Figure 6. (**a**) FIR notch filter inserted bus voltage regulator; (**b**) Input power feedforward scheme; (**c**) Equivalent model for input power feedforward scheme; and (**d**) FIR notch filter inserted bus voltage regulator with Kalman-filter-based input power feedforward scheme.

Unlike the high order FIR filter used in [11], the second order FIR has a simpler transfer function as follows:

$$G_{NF}(z) = g_0(1 - 2\cos(\delta)\, z^{-1} + z^{-2}) \tag{14}$$

$$\begin{cases} \delta = \frac{2\pi\omega_f}{\omega_s} \\ g_0 = \frac{1}{2-2\cos(\delta)} \\ z_{1,2} = \cos(\delta) \pm j\sin(\delta) \\ BW = \sqrt{2}\left|\frac{1-\cos(\delta)}{\sin(\delta)}\right| \\ Q = \frac{\omega_f|\sin(\delta)|}{\sqrt{2}|1-\cos(\delta)|} \end{cases} \tag{15}$$

The second order FIR notch filter has been successful in the removal of power-line noise from biomedical signals. The major advantage of the FIR notch filter is its simplicity of the pole-zero placement on the unit circle method. The zeroes of the filter are placed on the unit circle at the position

equivalent to the rejected frequency ω_f. For a signal sampled at the frequency ω_s, the zeroes are determined as $z_{1,2}$ [24]. BW is the bandwidth at -3 dB cutoff frequency of the notch filter, which reduces the sensitivity of the grid fundamental frequency variation. BW and the quality factor (Q), which are also given by (15), determine the sharpness of the notch filter.

Figure 7 presents the bode diagrams of the second order FIR notch filters with different sampling frequencies. The filter is manifested as almost unity gain at low frequencies and a notch at the rejected frequency ω_f. However, one thing needs to be noticed is that the magnitude of the filter at the high frequency (higher than ω_f) trends to increase when a high sampling rate is adopted. Typically, the bus voltage control loop is much slower than the current loop and the interactions between the two loops are neglected, thus, the two control loops can be designed independently. Correspondingly, we use different sampling rates for the two controllers. Unlike the current controller, a relative low sampling rate is enough for bus voltage controller in most applications. In order to filter the unnecessary high frequency noises, the bus voltage control system is operating at a low sampling rate, which makes the design of FIR notch filter and the loop compensator simpler.

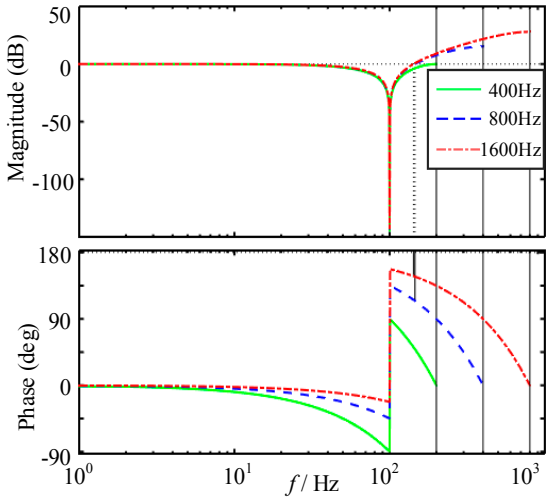

Figure 7. Bode diagrams of the second order FIR notch filters with different sampling frequencies.

To achieve zero steady-state error during a step-up of the injected power, a discrete PI controller is employed as the compensator:

$$H_c(z) = K_p + K_i \frac{T_s z}{z-1} \tag{16}$$

where K_p is the proportional gain, K_i is the integral gain, T_s is the sampling period. Therefore, the modified controller is given by $G_{c\text{-}bus}(z) = G_{NF}(z)H_c(z)$, which has two design parameters K_p and K_i. According to Figure 6a, the open loop transfer function for bus voltage control loop can be obtained as (17). Thus, designing the loop compensator by using the frequency response method is possible:

$$G_{bus\text{-}open}(\mathrm{z}) = \frac{V_g T_s G_{c\text{-}bus}(\mathrm{z})}{2C_{bus}V_{ref}(\mathrm{z}-1)} \tag{17}$$

The above analysis is based on several assumptions. Firstly, the current control loop is fast and robust. Secondly, the interactions between the bus voltage control loop and the current control loop are neglected. Thirdly, the bus voltage control loop is simplified in terms of the average signals to ignore the nonlinearity. However, these assumptions are violated when try to further increase the speed of bus voltage control loop. Since a more accurate math model is hard to establish, the practical approach is to limit the bus voltage control loop bandwidth to a suitable range so as to ensure the stability of the system and decrease the bus voltage fluctuations.

3.2. Kalman-Filter-Based Input Power Feedforward

The input power feedforward control scheme is used to reduce capacitance energy storage requirements and to improve the dynamic response of the system. If the input power can be calculated in real time, the dynamic response to input transients can be improved to satisfy the wide range input change. Figure 6b shows the bus voltage control system with the input power feedforward scheme in continuous time domain. Considering the power loss, a factor k ($0 < k < 1$) is used to adjust the ratio of feedforward power. By moving the feedforward node of the input power $P_{in}(t)$ from the input of the bus voltage controller $G_{c\text{-}bus}(s)$ to the output, an equivalent model is given as Figure 6c.

Due to the lack of direct power measuring methods, a DC bus input current estimator offers an alternative solution for the implement of input power feedforward control scheme. A full order observer, which is based on volt ampere relation of the DC bus capacitor, is proposed to reduce the 2-f ripple in the DC bus voltage for a regenerative cascade inverter [25]. However, the full order observer is very sensitive to the random measuring noise, which leads to a poor performance in real system. The Kalman filter is an optimal state estimator and is usually applied to a dynamic system that involves random noise environment. Thus, it is the suitable choice to detect the DC bus instantaneous input current under the measuring noise. In order to implement the design results into practical digital control systems, the design is directly carried out in discrete domain. The discrete domain system model is shown as below:

$$\begin{cases} \mathbf{x}_k = \mathbf{\Phi}_{k-1}\mathbf{x}_{k-1} + \mathbf{G}_{k-1}\mathbf{u}_{k-1} + \mathbf{\Gamma}_{k-1}\mathbf{w}_{k-1} \\ \mathbf{z}_k = \mathbf{H}_k x_x + \mathbf{v}_k \end{cases} \tag{18}$$

$$\mathbf{\Phi}_k = \begin{bmatrix} 1 & \frac{T_s}{C_{bus}} \\ 0 & 1 \end{bmatrix} \tag{19}$$

where state vector $\mathbf{x}(k) = [v_{bus}(k)\ i_{dc}(k)]^{\mathrm{T}}$, $\mathbf{\Phi}_k$ is the state matrix, input matrix $\mathbf{G}_k = [T_s/C_{bus}\ 0]^T$, input variable $u_k = i_{inv}(k)$; output matrix $\mathbf{H}_k = [1\ 0]$; Output $\mathbf{z}_k = [v_{bus}(k)\ 0]^T$; $\boldsymbol{w}_k$ is the system noise, $\mathbf{\Gamma}_k$ is the noise matrix, $\mathbf{v}_k$ is the measuring noise; $i_{dc}(k)$ and $i_{inv}(k)$ are the input and output current of the DC bus in discrete time. The volt ampere relation of the DC bus capacitor is given as: $v_{bus}(k+1) - v_{bus}(k) = (i_{dc}(k) - i_{inv}(k))T_s/C_{bus}$. The Kalman filter process for this system is given as follows [26]:

$$\begin{cases} \hat{\mathbf{x}}_{k/k} = \hat{\mathbf{x}}_{k/k-1} + \mathbf{G}_{k-1}\mathbf{u}_{k-1} + \mathbf{K}_k[\mathbf{z}_k - \mathbf{H}_k\hat{\mathbf{x}}_{k/k-1}] \\ \hat{\mathbf{x}}_{k/k-1} = \mathbf{\Phi}_k\hat{\mathbf{x}}_{k-1/k-1} \\ \mathbf{K}_k = \mathbf{P}_{k/k-1}\mathbf{H}_k{}^T[\mathbf{H}_k\mathbf{P}_{k/k-1}\mathbf{H}_k{}^T + \mathbf{R}_k]^{-1} \\ \mathbf{P}_{k/k} = \mathbf{P}_{k/k-1} - \mathbf{P}_{k/k-1}\mathbf{H}_k{}^T[\mathbf{H}_k\mathbf{P}_{k/k-1}\mathbf{H}_k{}^T + \mathbf{R}_k]^{-1}\mathbf{H}_k\mathbf{P}_{k/k-1} \\ \mathbf{P}_{k/k-1} = \mathbf{\Phi}_k\mathbf{P}_{k-1/k-1}\mathbf{\Phi}_k{}^T + \mathbf{\Gamma}_k\mathbf{Q}_k\mathbf{\Gamma}_k{}^T \end{cases} \tag{20}$$

where $\mathbf{P}_{k/k}$ is the estimated variance matrix; $\mathbf{K}_k$ is Kalman gain matrix; $\mathbf{Q}_k$ is the variance matrix of the system noise vector; $\mathbf{R}_k$ is the variance matrix of the measurement noise vector; $\mathbf{Q}_k$ and $\mathbf{R}_k$ are positive definite matrix.

The initial estimated variance matrix $\mathbf{P}_0$ and the initial estimated state $\hat{\mathbf{x}}_0$ do not destroy the stability of Kalman filter. However, $\mathbf{P}_0$ and $\hat{\mathbf{x}}_0$ should be set carefully in case of the overflow in calculating $\mathbf{P}_k$ or $\hat{\mathbf{x}}_k$, which is conducted by a finite-word-length microcontroller unit (MCU). $\hat{\mathbf{x}}_0$ is set according to the system state, and $\mathbf{P}_k$ is limited to a suitable range. Arithmetic operations in MCU result in rounding errors, which perhaps cause that $\mathbf{P}_k$ becomes a negative definite matrix and Kalman filter diverges. Thus, a modified $\mathbf{P}'_k(i,j)$ is used to simplify the calculation and to ensure the symmetry of the matrix:

$$\mathbf{P}'_k(i,j) = \mathbf{P}'_k(j,i) = \frac{1}{2}[\mathbf{P}_k(i,j) + \mathbf{P}_k(j,i)] \tag{21}$$

The inverter side current $i_{inv}(k)$ is calculated as follows:

$$i_{inv}(k) = \frac{v_{inv}(k) i_{L1}(k)}{v_{bus}(k)} \tag{22}$$

The inverter output voltage ($v_{inv}(k)$) and the inverter side conductor current ($i_{L1}(k)$) are provided by the grid current control scheme. A proper **R** is used to smooth $\hat{i}_{dc}$, so as to neglect measuring noises and fast oscillations at the input power. Since P_{in} is a constant ($P_{in} = v_{bus} \times i_{dc}$) and v_{bus} includes a 2-f ripple at steady-state, there will also be a slight 2-f ripple in the i_{dc}. The estimated current $\hat{i}_{dc}$ lags the actual current i_{dc}, therefore, P_{in} can't be achieved by multiplying v_{bus} by $\hat{i}_{dc}$. To gain clean reference current signal, V_{ref} instead of v_{bus} is used as the multiplier to calculate the input power, and the feedforward term is also filtered by the FIR notch filter. Finally, Figure 6d presents the control block diagram of the proposed FIR notch filter inserted bus voltage regulator with the Kalman-filter-based input power feedforward scheme.

3.3. Modulation Compensation Strategy for Bus Voltage Ripple

To eliminate the nonlinearity of the current control loop, which is caused by the DC bus voltage ripple, a modulation compensation strategy is proposed in this section. As depicted in Figure 8a, this method simply inserts a term G_{cmp} before the PWM section. When the bus voltage ripple increases, the compensator decreases the modulation index proportionally. As a result, the ripple-caused nonlinearity in the current control scheme is compensated:

$$G_{cmp} = \frac{V_{ref}}{v_{bus}} = \frac{V_{ref}}{V_{ref} + \Delta v_{bus}} \tag{23}$$

With implementing the modulation compensation strategy, an equivalent control model is shown in Figure 8b. By replacing modulator gain v_{bus} with V_{ref}, the current control system is completely linearized.

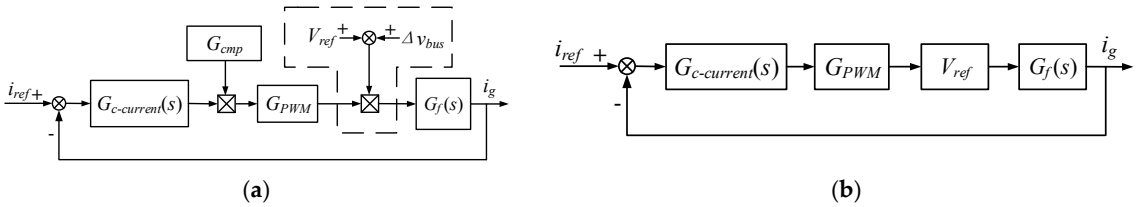

Figure 8. Proposed modulation compensation strategy. (**a**) Current control scheme with the modulation compensation strategy; (**b**) Equivalent current control scheme.

3.4. Novel Synchronous Frame Current Control Scheme for Single-Phase Systems

In order to pursuit precise current tracking and high power quality, a fast and robust current control loop is required. Two common methods for current regulation of single phase grid-connected inverters are: (1) using PR controllers in stationary reference frame; and (2) using virtual vector control in synchronous reference frame.

Figure 9a presents the block diagrams of virtual vector control for current-regulated single-phase grid-connected inverters. Where i_d^* and i_q^*, are the active and reactive reference current; i_α and i_β are the feedback current in stationary frame; v_d, v_q, v_α and v_β are output of controller in synchronous and stationary frame. An orthogonal current (i_β) is created to obtain DC quantities by means of a $\alpha\beta/dq$ transformation. Thus, the PI controllers can be adopted to regulate the dq current, which present infinite control gain at the steady-state operating point and lead to zero steady-state error. In Figure 9, v_α is fed into the PWM modulator, while v_β is discarded. Since the system variables are converted to DC quantities, the control loop has no dependence on the system frequency. The generation of

i_β is described by an equivalent transfer function $O(s)$ [27], in which i_α is shifted 90°. By inserting two opposite frame transformations into Figure 9a, an equivalent block diagram is presented in Figure 9b. Where e_α and e_β are the error signals in stationary frame. Hilbert transform [28], fictive axis emulator [29], time delay [30], all pass filter [31] and second-order generalized integrator [32] are conventional OSG methods. Table 1 lists some OSG methods and the corresponding $O(s)$. Where T_0 and ω_0 are the fundamental period and fundamental frequency. Although these methods provide satisfactory performance at steady-state, they suffer from several drawbacks. The delay to create orthogonal component slows down the system dynamic response. Frequency drifts result in an inaccurate phase shift, which leads to errors in active and reactive power control. Moreover, the OSG block makes the current controller complicated and difficult to analyze the stability. The influence, which is brought about by the interaction between α-axis component and β-axis component, is hard to analyze. Thus, the virtual vector control is seldom implemented for an inverter with an LCL filter.

Table 1. Orthogonal Signal Generation Methods.

Method	Transfer Function
Time delay	$e^{\frac{-T_0 s}{4}}$
All pass filter	$\frac{\omega_0 - s}{\omega_0 + s}$
Hilbert transform	$\frac{-s}{\omega_0}$
Second-order generalized integrator	$\frac{k\omega_0 s}{s^2 + k\omega_0 s + \omega_0^2}$

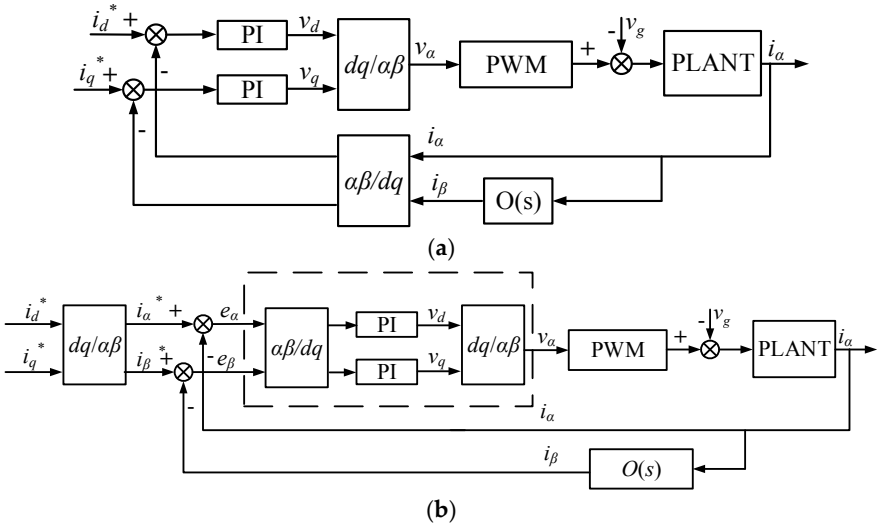

Figure 9. Virtual vector control for current-regulated single-phase grid-connected inverters. (**a**) Conventional virtual vector control; (**b**) Equivalent model.

A droop-Lyapunov-based control technique is proposed for single-phase converters in [33,34]. The control system is designed with respect to the accurate dynamic model of inverter developed in the *d*-*q* rotating frame. A capability curve for the entire operating condition is used to define the positive and negative maximum values for the *d*-*q* components of inverter currents. Excellent performance can be achieved for both stand-alone operating mode and grid-connected operating mode in the presence of nonlinear loads. However, precise circuit parameters are needed by the controller, which makes it challenging to apply the control strategy in practical system.

A novel synchronous frame current controller is proposed in this section. This method cancels the OSG block by assuming that the error signal e_β is equal to zero. Figure 10a presents the block diagram of the proposed control scheme. Using the math model described in [35], the equivalent transfer function in stationary reference frame for the dashed box in Figure 10a is derived as follows.

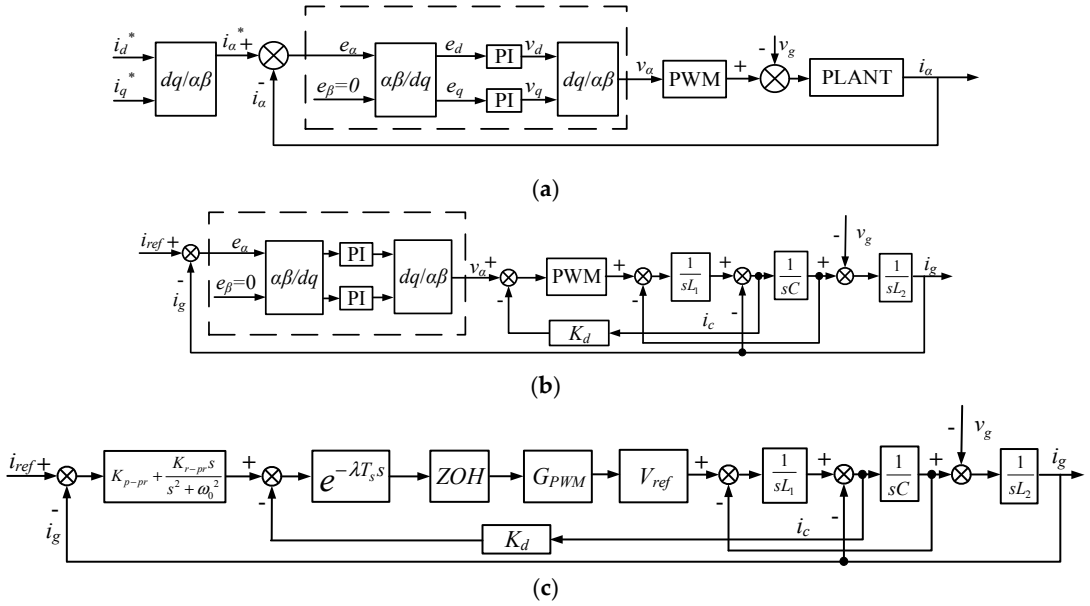

Figure 10. (**a**) Block diagram of the proposed synchronous frame current controller; (**b**) Implementation of the proposed controller for a single-phase grid-connected inverter with an LCL filter; (**c**) Equivalent diagram for the current control scheme in stationary frame.

The equivalent model of proportional controller and integral controller are separately established to analyze their performance in all frequencies. Then, the equivalent model, in stationary frame, for the proposed controller is obtained by summing them up. According to Fourier's theorem, the feedback error signals can be given as:

$$\begin{bmatrix} e_\alpha(t) \\ e_\beta(t) \end{bmatrix} = \begin{bmatrix} E\cos(n\omega_0 t + \varphi) \\ 0 \end{bmatrix} \tag{24}$$

where E is the amplitude of the error signal, and φ is the initial phase angle. $n\omega_0$ represents the angle frequency of the signal. n can be an integer or a decimal ($n \geq 0$). If n is equal to zero, it means the input signals is DC component. Therefore, all possible input error signals in different frequencies are under consideration. The transformation from the stationary to the synchronous frame for an arbitrary quantity is given by:

$$\mathbf{C}_{2s/2r} = \begin{bmatrix} \cos(\omega_0 t) & \sin(\omega_0 t) \\ -\sin(\omega_0 t) & \cos(\omega_0 t) \end{bmatrix} \tag{25}$$

Since K_p is a constant, the proportion controller in synchronous frame is the same as the proportion controller in stationary frame:

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \mathbf{C}_{2s/2r}^{-1} \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \mathbf{C}_{2s/2r}^{-1} K_P \mathbf{C}_{2s/2r} \begin{bmatrix} e_\alpha(t) \\ e_\beta(t) \end{bmatrix} = K_P \begin{bmatrix} e_\alpha(t) \\ e_\beta(t) \end{bmatrix} \tag{26}$$

The integral controller in synchronous frame is given by:

$$\begin{bmatrix} v_d(s) \\ v_q(s) \end{bmatrix} = \frac{K_i}{s} \begin{bmatrix} e_d(s) \\ e_q(s) \end{bmatrix} \tag{27}$$

Signals represented in time domain is:

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = K_i \int \begin{bmatrix} e_d(t) \\ e_q(t) \end{bmatrix} \mathrm{d}t = K_i \int \left\{ \mathbf{C}_{2s/2r} \begin{bmatrix} e_\alpha(t) \\ e_\beta(t) \end{bmatrix} \right\} \mathrm{d}t \tag{28}$$

Substituting (24) and (25) into (26), the output signals of controller are given by:

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \begin{cases} \frac{EK_i}{2} \begin{bmatrix} t\cos(\varphi)\cos(\omega_0 t) - t\sin(\varphi)\sin(\omega_0 t) + \frac{\sin(\omega_0 t)\cos(\varphi)+\cos(\omega_0 t)\sin(\varphi)}{2\omega_0} \\ t\cos(\varphi)\sin(\omega_0 t) + t\sin(\varphi)\cos(\omega_0 t) + \frac{\cos(\omega_0 t+\varphi)}{2\omega_0} \end{bmatrix} & , n = 1 \\ K_i E \begin{bmatrix} \frac{n}{\omega_0(n-1)(n+1)}\cos(n\omega_0 t + \varphi - \frac{\pi}{2}) \\ \frac{-\cos(n\omega_0 t+\varphi)}{\omega_0(n-1)(n+1)} \end{bmatrix} & , n \neq 1 \end{cases} \tag{29}$$

Considering the error signal presented in (24), the relationship between the input and the output signals can be obtained. $G_{I\text{-}eq}(s)$ is the equivalent transfer function in stationary frame for the integral controller in synchronous frame. When n = 1:

$$\begin{aligned} G_{I\text{-}eq}(s) &= \frac{v_\alpha(s)}{e_\alpha(s)} = \frac{K_i}{2} \frac{L\left[t\cos(\varphi)\cos(\omega_0 t) - t\sin(\varphi)\sin(\omega_0 t) + \frac{\sin(\omega_0 t)\cos(\varphi)+\cos(\omega_0 t)\sin(\varphi)}{2\omega_0}\right]}{L[\cos(\omega_0 t+\varphi)]} \\ &= \frac{K_i s}{s^2+\omega_0{}^2} + \frac{K_i}{4} \frac{-\cos(\varphi) + \frac{s}{\omega_0}\sin(\varphi)}{s\cos(\varphi) - \sin(\varphi)\omega_0} \end{aligned} \tag{30}$$

Substituting s by $j\omega_0$, Equations (31) and (32) are obtained. Where e is the Euler's number:

$$\frac{K_i}{4}\left|\frac{-\cos(\varphi) + \frac{j\omega_0}{\omega_0}\sin(\varphi)}{j\omega_0\cos(\varphi) - \sin(\varphi)\omega_0}\right| = \frac{K_i}{4\omega_0}\left|\frac{\mathrm{e}^{i\varphi+\frac{\pi}{2}}}{\mathrm{e}^{i\varphi}}\right| = \frac{K_i}{4\omega_0} \ll \left|\frac{K_i s}{s^2+\omega_0{}^2}\right| \tag{31}$$

$$\left|G_{I\text{-}eq}(s)\right| \approx \left|\frac{K_i s}{s^2+\omega_0{}^2}\right| \tag{32}$$

When $n \neq 1$, substituting $n\omega_0$ by ω:

$$\begin{aligned} G_{I\text{-}eq}(s) &= \frac{v_\alpha(s)}{e_\alpha(s)} = K_i \frac{\omega}{\omega^2-\omega_0{}^2} \frac{L\left[\cos(\omega t+\varphi-\frac{\pi}{2})\right]}{L[\cos(\omega t+\varphi)]} \\ &= \frac{K_i\omega}{\omega^2-\omega_0{}^2} \cdot \frac{\omega\cos\varphi + s\sin\varphi}{s\cos\varphi - \omega\sin(\varphi)} \end{aligned} \tag{33}$$

Substituting s by $j\omega$:

$$|G_{I\text{-}eq}(s)| = \left|\frac{K_i\omega}{\omega^2-\omega_0{}^2} \cdot \frac{\omega\cos\varphi + j\omega\sin\varphi}{j\omega\cos\varphi - \omega\sin(\varphi)}\right| = \left|\frac{K_i\omega}{\omega^2-\omega_0{}^2}\right| = \left|\frac{K_i s}{s^2+\omega_0{}^2}\right| \tag{34}$$

Obviously, no matter whether n is equal to 1 or not, the gain of controller $|G_{I\text{-}eq}(s)|$ is $\left|\frac{K_i s}{s^2+\omega_0{}^2}\right|$ From (29), phase relationship between the input and output signal can be summarized as that the output signal leads the input by 90° for $0 \leq n < 1$ and lags the input by 90° for $n > 1$. Thus, the integral controller in synchronous frame is equal to resonant controller in stationary frame.

A PI controller is regarded as the sum of a proportional controller and an integral controller. Therefore, from the above analysis, the proposed synchronous frame controller $G_c(s)$ is equivalent to a proportion-resonant controller in stationary frame as (35).

$$G_c(s) = K_p + \frac{K_i s}{s^2+\omega_0{}^2} \tag{35}$$

Figure 11a presents Bode diagrams for a PR controller and a resonant controller. Since the resonant term provides very little gain outside the band-pass, an improved PR controller is given by (36) to reduce sensitivity to variations in the interfaced-grid frequency [23]. Where ω_c is the bandwidth

at −3 dB cutoff frequency of the resonant controller. The presence of ω_c seems to allow a degree of freedom in the design of the resonant frequency response. However, as depicted in Figure 11b, increasing ω_c only decreases the peak amplitude of the resonant term at resonant frequency, without affecting the gain at other frequency stage. If there is a variation in reference frequency, a larger resonant gain $K_{r\text{-}pr}$ is required to ensure the performance of the controller. According to the PV power grid code in the China, the PV grid-connected inverters should run smoothly across a wide grid frequency range from 48 Hz to 50.5 Hz [36]. $K_{r\text{-}pr}$ is too large to be unprocurable for such a large frequency variation. In [37], the grid frequency estimated by the PLL is used to adjust the parameters of the PR controller in real time, so as to eliminate difference between the grid frequency and resonant frequency. This control strategy is descripted as the frequency adaptive PR controller. Since the resonant frequency of proposed synchronous frame controller is always in alignment with grid fundamental frequency, a similar control performance as the frequency adaptive PR controller can be achieved by using a simpler approach:

$$G_{pr}(s) = K_{p\text{-}pr} + \frac{K_{r\text{-}pr}s}{s^2 + \omega_c s + \omega_0{}^2} \tag{36}$$

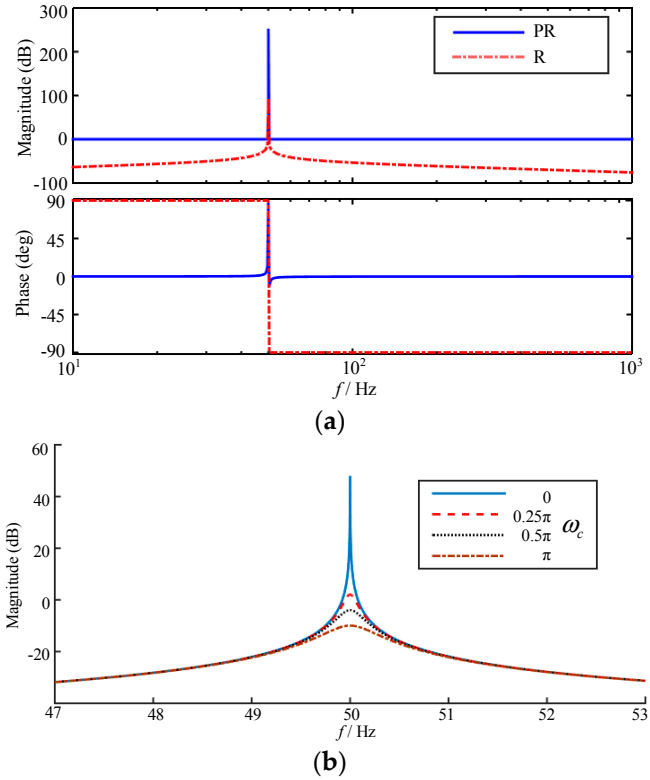

Figure 11. (**a**) Bode diagrams of the PR controller and the R controller, $K_{p\text{-}pr}$ = 1, $K_{r\text{-}pr}$ = 1, ω_0 = 314, ω_c = 0; (**b**) Bode diagrams of the improved resonant term for variation in ω_c, $K_{r\text{-}pr}$ = 1.

As pointed in [35], for a three-phase system, the PI controller in synchronous frame is equivalent to PR controller in stationary frame at fundamental frequency, which has a transfer function as (37). Except for the fundamental frequency, they are not equivalent, and their amplitude characteristics differ greatly in low frequency stage. However, the proposed synchronous frame controller is equivalent to PR controller in stationary frame for all frequency. According to (35) and (37), the equivalent resonant

gain of the proposed controller is only half as high as the one of three-phase system, which is owing to the lack of i_β:

$$G_{3c}(s) = K_p + \frac{2K_i s}{s^2 + \omega_0{}^2} \tag{37}$$

The implementation of the proposed current controller for a single-phase grid-connected inverter with an LCL filter is possible. Figure 10b shows the corresponding control block diagrams. The capacitor current feedback (CCF) active damping method is chosen due to its effective damping performance and simple application [38]. A PR controller, instead of the proposed controller, is used to analyze the system stability. The equivalent control block diagrams are presented in Figure 10c, in which the symbols are adjusted in order to be consistent with context above. A delay of λT_s (T_s is the sampling period, $0 \leq \lambda \leq 1$), which is caused by the digitally controlled system, is also included in the control block diagrams [39]. Usually, the delay of the PWM module is equal to one sampling period T_s ($\lambda = 1$). However, by shifting the sampling instant towards the PWM reference update instant, λ can also be a decimal. λT_s is mainly consist of the analog-to-digital conversion delay and the computation delay.

The PWM is usually modeled as a zero order hold (ZOH), that is:

$$G_{ZOH}(s) = \frac{1 - \mathrm{e}^{-T_s s}}{s} \approx T_s \mathrm{e}^{-0.5 T_s s} \tag{38}$$

Thus, the delay time of the PWM is equal to $0.5T_s$, and the total delay time is $(\lambda + 0.5)T_s$. The time delays have a great influence on the stability of digitally controlled grid-connected inverters with LCL filters. To tune the feedback coefficient K_d, an accurate model is presented in Figure 12.

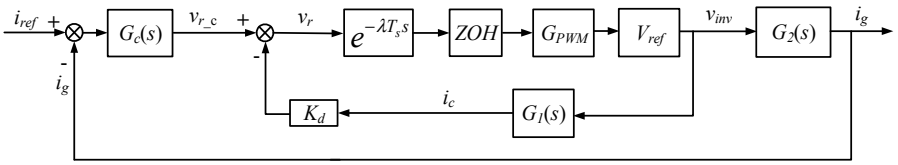

Figure 12. Accurate mathematic model of a digitally controlled single-phase grid-connected inverter with a LCL filter.

$G_1(s)$ is the transfer function from $v_{inv}(s)$ to $i_c(s)$. $G_2(s)$ is the transfer function from $v_{inv}(s)$ to $i_g(s)$. $G_1(s)$ and $G_2(s)$ are given as follows:

$$G_1(s) = \frac{i_c(s)}{v_{inv}(s)} = \frac{sCL_2}{s^2CL_1L_2 + (L_1 + L_2)} = \frac{s}{L_1(s^2 + \omega_r{}^2)} \tag{39}$$

$$\omega_r = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{40}$$

$$G_2(s) = \frac{i_g(s)}{v_{inv}(s)} = \frac{1}{s^3CL_1L_2 + s(L_1 + L_2)} = \frac{1}{L_1L_2Cs(s^2 + \omega_r{}^2)} \tag{41}$$

Applying Z-transform to $G_1(s)$ with ZOH, the open-loop transfer function of the inner active damping loop is given by:

$$\begin{aligned} G_a(z) = \frac{K_d i_c(z)}{v_r(z)} &= K_d G_{PWM} V_{ref} \mathbb{Z}\{\tfrac{1-\mathrm{e}^{-T_s s}}{s} \cdot \mathrm{e}^{-\lambda T_s s} \cdot G_1(s)\} \\ &= K_d G_{PWM} V_{ref} \tfrac{z-1}{z^2} \mathbb{Z}\{\tfrac{G_1(s)}{s} \mathrm{e}^{mT_s s}\} \end{aligned} \tag{42}$$

where $m = 1 - \lambda$, $0 \leq m \leq 1$. $\mathbb{Z}\{\frac{G_1(s)}{s}e^{mT_s s}\}$ in (42) can be obtained using the following property [40]:

$$\mathbb{Z}\{\frac{G_1(s)}{s}\mathrm{e}^{mT_s s}\} = \sum_{i=1}^{n} \mathrm{Res}\left[\frac{zG_1(s)\mathrm{e}^{mT_s s}}{s(z-\mathrm{e}^{T_s s})}\right]_{s=pi} \tag{43}$$

where pi (i = 1, 2, ..., n) are the poles of $G_1(s)/s$ and Res denotes the residue. Thus, (42) can be simplified as:

$$G_a(z) = \frac{K_d G_{PWM} V_{ref}(z-1)}{L_1 \omega_r z} \cdot \frac{z\sin(m\omega_r T_s) + \sin[(1-m)\omega_r T_s]}{z^2 - 2z\cos(\omega_r T_s) + 1} \tag{44}$$

The closed-loop transfer function of the inner active damping loop is expressed as:

$$G_{a\text{-}cl}(z) = \frac{G_a(z)}{1 + G_a(z)} \tag{45}$$

4. System Design and Simulation

4.1. System Design

To validate the feasibility of the proposed control scheme, a two-stage single-phase grid-connected PV system has been constructed. As depicted in Figure 13, it consists of two boost converters and a simple full bridge on the second stage. The two boost converters in the first stage have two operation modes. Firstly, they can be connected to different PV arrays and work independently, which enables the circuit to extract the maximum available power from each array independently for partially shaded conditions. Secondly, they can work as a two-phase interleaved boost converter, which is adopted in this paper. Both simulation and experimental tests have been carried out with the parameters given in Table 2.

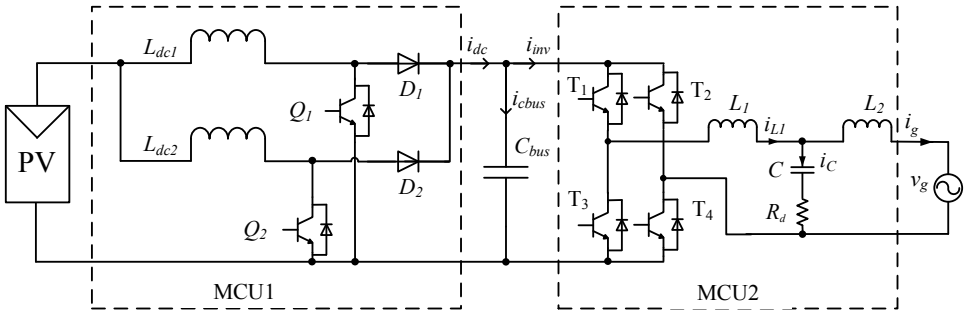

Figure 13. Simulation and experimental power topology.

Table 2. Simulation and Experimental Parameters.

Symbol	Parameters	Values
P_o	Output power	2 kW
C_{bus}	DC bus capacitor	1000 uF
L_1	Inverter side inductor	3.2 mH
L_2	Grid side inductor	1.5 mH
C	Capacitor of LCL filter	10 uF
R_d	Damping resistor	0 Ω
V_{ref}	Bus voltage reference	360 V
f_{sw}	Switch frequency	10 kHz
f_{sbus}	Sampling frequency for bus voltage regulator	400 Hz
$f_{s\text{-}Kalman}$	Sampling frequency for Kalman filter process	2 kHz
f_s	Sampling frequency for current controller	10 kHz
V_g	Grid voltage peak value	311 V
f_g	Grid Frequency	50 Hz

For the FIR notch filter inserted bus voltage regulator, the sampling frequency is 400 Hz. The set of gains are K_p = 0.17, K_i = 5.3. The FIR notch filter is given as $G_{NF}(z) = 0.5(1 + z^{-2})$. By substituting the system parameters shown in Table 2 into (17) the Bode diagram of the bus voltage open-loop transfer function shown in Figure 14 is obtained. The design has a positive phase margin of +52.3° and a cross-over frequency of 12.7 Hz.

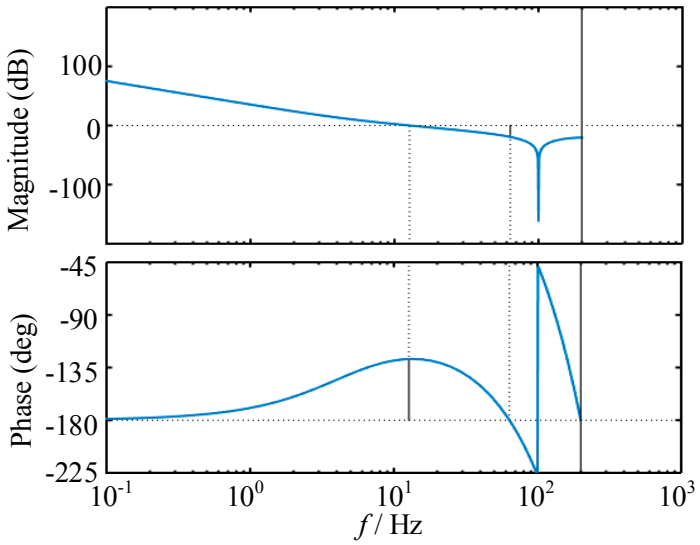

Figure 14. Bode plot of the open-loop transfer function for the proposed bus voltage controller.

The input power feedforward factor k is equal to 0.9. For the Kalman filter, it is very important to determine the values of the Q and R. The value of Q is determined from the noises generated by the PWM inverter and the DC-bus capacitor. The major sources of noise from the PWM inverter come from the current controller. The current controller is not perfect due to the current ripple and the current measuring error. The capacity of the DC bus capacitor may be not equal to its nominal value. The value of R is determined from the noises generated by the DC bus voltage measuring error and fast oscillations at the input power. Unfortunately, the levels of these noises are not exactly known. So the values are mainly determined from the experimental system and should be adjusted by experiment. Thus, it requires some trial-and-errors.

To analyze the influence of different time delays, the grid current control systems are categorized as three typical cases [41], in which the delay time is $0.5T_s$, T_s, $1.5T_s$, respectively. Correspondingly, the PWM module of the MCU is configured in shadow mode with double update, and the sampling instant and duty-ratio update instant are placed at the peak and valley the triangle carrier. The values of m are 1, 0.5 and 0. When m = 1, there is no computation delay, which is unprocurable for practical system. The root loci of the active damping closed-loop transfer function $G_{a\text{-}cl}(z)$ are illustrated in Figure 15. For Figure 15a, m is equal to 0.5. With the increase of K_d, a couple of poles move from the boundary of the unit circle into the inside, meaning that the system stability is improved. However, when K_d goes beyond 0.1, they move outside the unit circle, and the system becomes unstable. For Figure 15b, m is equal to 0. There is a couple of poles located outside the unit circle, indicating that the system is definitely unstable. Obviously, the time delays affect the system significantly, and a large delay time will destroy the stability of the CCF active damping loop.

For the current controller, the sampling frequency is equal to the PWM switch frequency. To simplify the design procedure, m = 0.5 is adopted in this paper. The grid current i_g and capacitor current i_c are sampled at the peak of the PWM carrier, and the PWM reference is updated at the valley. In other words, the analog-to-digital conversion delay and the computation delay should not exceed $0.5T_s$. Luckily, 50 μs is enough for a fast digital processor to achieve the control process. The design of

the PR regulator as current controller is widely discussed, so as to it is not included in this paper [23]. With the compromise of the system stability and resonant damping, $K_{p\text{-}pr}$, $K_{r\text{-}pr}$, and K_d are set as 0.026, 20, 0.03, respectively.

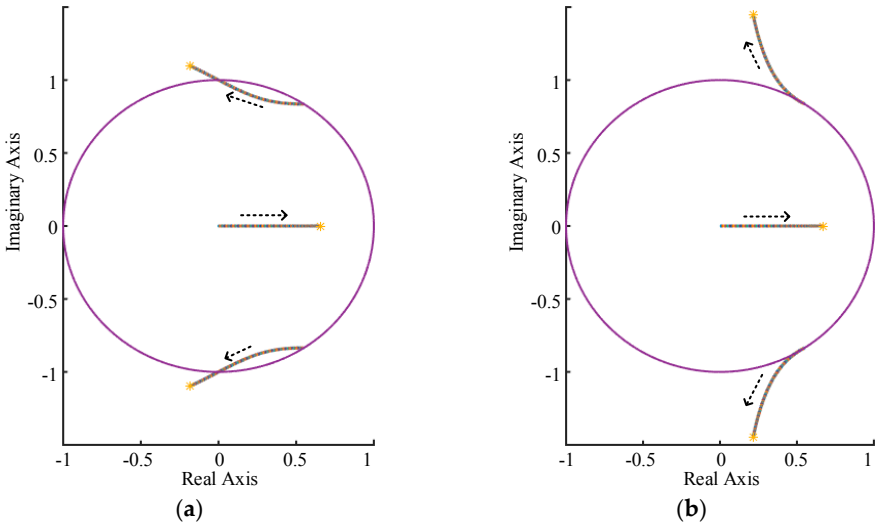

Figure 15. Root loci of the CCF active damping closed-loop transfer function with different parameters. (**a**) $m = 0.5$; $0 < K_d < 0.15$; (**b**) $m = 0$, $0 < K_d < 0.15$.

4.2. Simulation

The simulation results have been obtained by using Matlab Simulink software. First of all, the current control systems are tested independently. The PR controller and the proposed synchronous frame control scheme are both implemented and tested. The PLL is assumed to be perfect in simulation, and the phase angle is given directly. Figure 16 shows the simulation results for the two control methods when the grid voltage undergoes frequency step changes. In Figure 16a, the PR controller presents zero steady-state error when tracing 50 Hz reference signal. However, when the grid frequency steps, steady-state error can be clearly observed. In Figure 16b, the steady error is eliminated for all frequency stage. The output current is highly smooth, meaning that the proposed current controller has an excellent steady-state performance in a single-phase grid-connected inverter with an LCL filter.

The transient response tests are shown in Figure 17. The FIR notch filter inserted bus voltage regulator with the Kalman-Filter-based input power feedforward is used to control the bus voltage. The proposed synchronous frame control scheme with the modulation compensation strategy is implemented as current controller. By changing the operation point of the boost circuit, the input power of the inverter is switched from about 1 kW to 2 kW. Prior to the step, the bus voltage is regulated to its nominal value of 360 V. With a positive power step, the bus capacitor charges. The average bus voltage $v_{bus,avg}$ has a fast response with a reasonable fluctuation of about 10.4 V. The output current maintains high quality (THD is 0.85%).

The performances of the proposed estimator and a full order state observer are presented in Figure 17c,d, respectively. Where $\hat{i}_{dc}$ is the estimated DC bus input current, $\Delta\hat{i}_{dc}$ is the estimation error. For the Kalman filter, the noise variances are set as $Q = 0.01$ and $R = 0.2$. In order to calculate the estimation error, the sampled DC bus input current i_{dc} is filtered by a low pass filter. Before the power jump, both the two methods work well and have small estimation errors. As the input power increasing, $\hat{i}_{dc}$ steps from 2.6 A to 5.4 A in 60 ms, and $\Delta\hat{i}_{dc}$ becomes large for short duration. $\hat{i}_{dc}$, which is obtained by using the proposed estimator, is smoother and more accurate than the one using a full order observer. $\Delta\hat{i}_{dc}$ is lower than $\pm$0.25 A at steady-state for proposed method ($\pm$0.4 A for the full order observer). Clearly, the full order observer is very sensitive to the noises, and the estimation results contain more ripples. The simulation results show that the proposed control scheme has the

merits of good dynamic response and low current harmonics. The estimator using Kalman filter exhibits excellent performance for DC bus input current estimation.

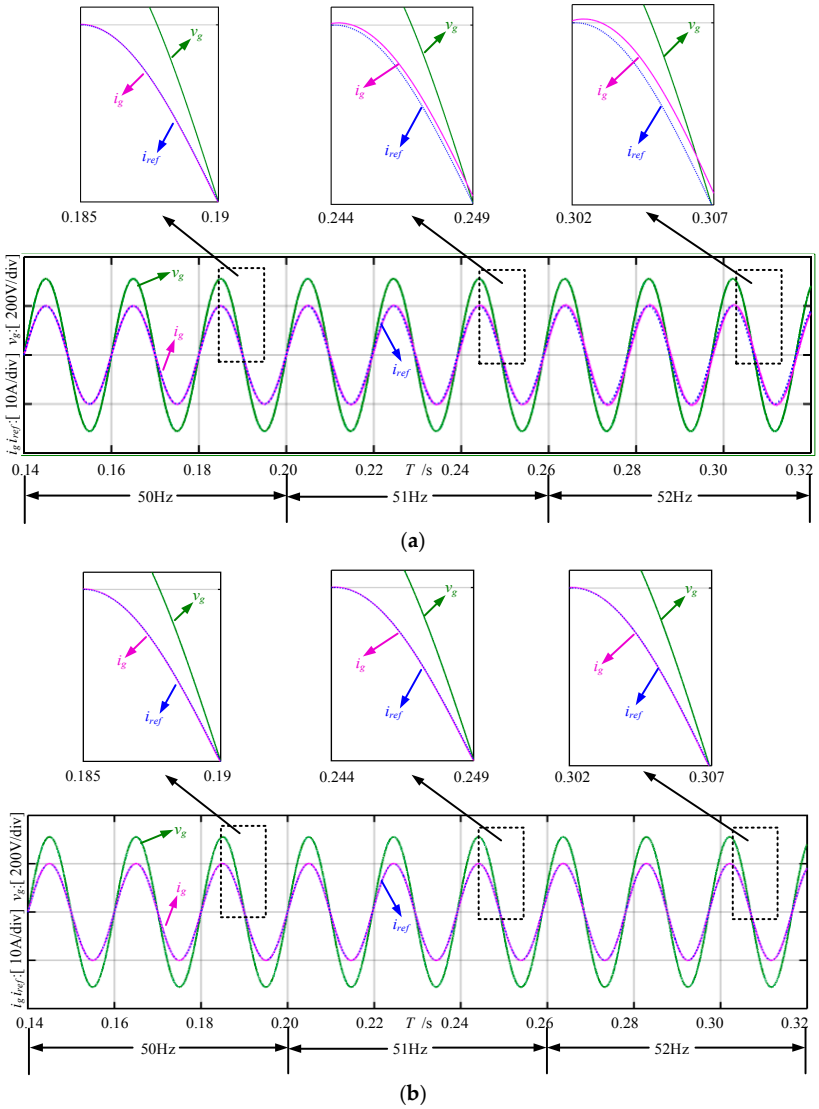

Figure 16. Simulation waveforms of PR controller and the proposed controller when grid voltage under goes frequency step changes. (**a**) PR controller; (**b**) Proposed synchronous frame controller.

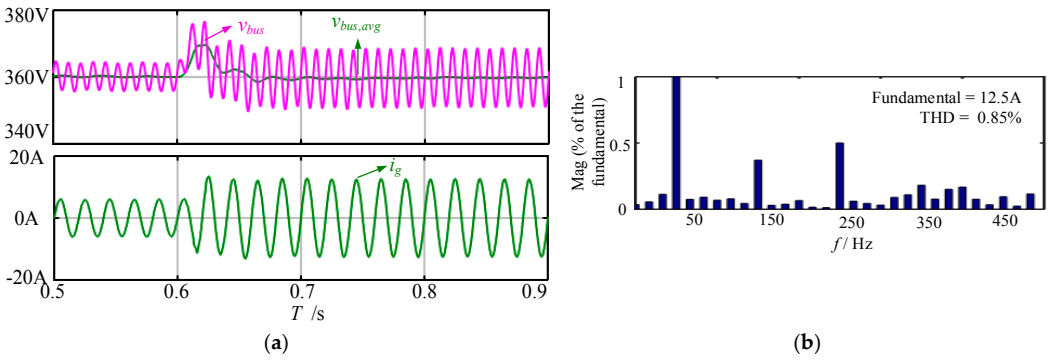

Figure 17. *Cont.*

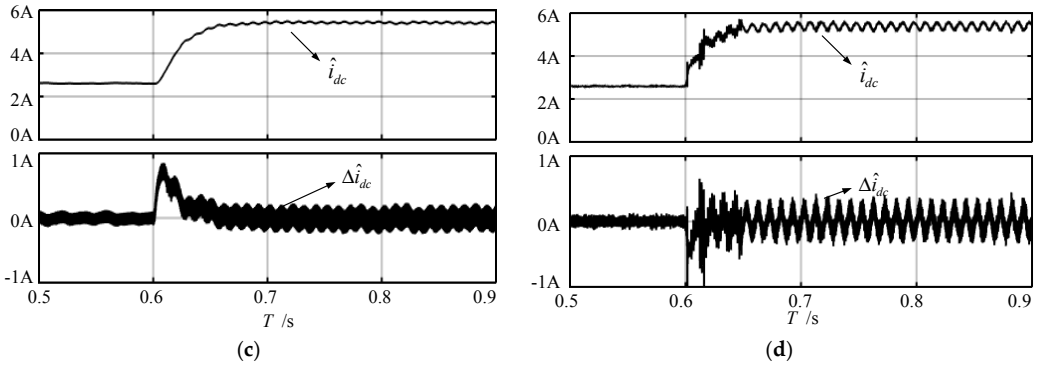

Figure 17. Simulation results of the transient response for a step in input power. (**a**) Waveforms of the bus voltage and grid current; (**b**) Main harmonic components; (**c**) Estimated DC bus input current using the proposed estimator; and (**d**) Estimated DC bus input current using a full order observer.

5. Experimental Results

A 2 kW experiment platform has been set up by taking two 32-bit ARM processors (STM32F303RCT6 from STMicroelectronics) as central processing units. One for the DC-DC converter and the other one for the DC-AC inverter. The inverter circuit parameters are the same with the simulation as shown in Table 2. The dead time of PWM is set as 2 µs. The estimated DC bus input current is outputted by the processor's DAC. To sample DC bus voltage v_{bus}, the ground clip of the oscilloscope probe is connected to a reference potential point of 300 V. Thus, the sampled v_{bus} is offset by 300 V, and can been observed more clearly.

The proposed synchronous frame control scheme is implemented as the current controller. Three bus voltage control schemes are implemented and experimentally tested, namely, PI controller, FIR notch filter inserted bus voltage regulator, and FIR notch filter inserted bus voltage regulator with the Kalman-filter-based input power feedforward. To test the transient response, the input power of the inverter is switched from about 1 kW to 2 kW (i.e., from half power to full power), and vice versa.

5.1. PI Controller

For the PI controller, two designs are tested. The proportional gains (K_p) are set as 0.22 and 0.015 respectively. The integral gains are equal to 2. The experimental results are shown in Figures 18 and 19. When a high proportional gain is employed, the bus voltage is well regulated during the transient, but the distortion is high (THD is 8.68%). The opposite situation occurs with a low proportional gain. The output current is nearly a pure sinusoid with low distortion (THD is 3.08%). However, the transient in the average bus voltage is unacceptably high, and it takes a very long time to reach steady state.

As pointed in Section 2, the amplitude of the third harmonic current varies with the gain of the bus voltage controller at $2\omega_g$. For the two designs, the theoretical calculated amplitudes of the third harmonic current are 0.99 A and 0.004 A, respectively. However, the experimental results are 1.12 A and 0.2 A. Clearly, a lower proportional gain leads to less distortion. The difference between the experimental results and the calculated values mainly due to the additional harmonic sources, which are not included in the calculation, such as PWM dead-time and sensor error. Thus, with a simple PI controller, the tradeoff between low harmonic distortion and high bandwidth seems unsolvable, and the designer must use a large bus capacitor to make the system work.

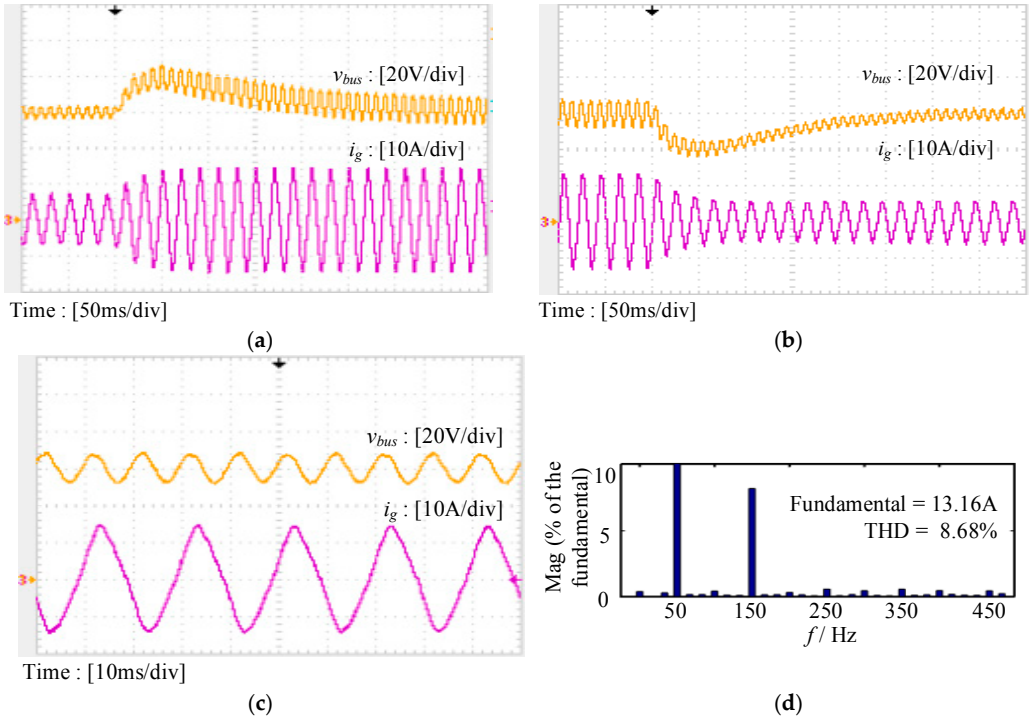

Figure 18. Experimental results of the PI controller with a high proportional gain. (**a**) Transient response when input power steps up from 1 kW to 2 kW; (**b**) Transient response when input power steps down from 2 kW to 1 kW; (**c**) Steady-state waveforms; and (**d**) Main harmonic components.

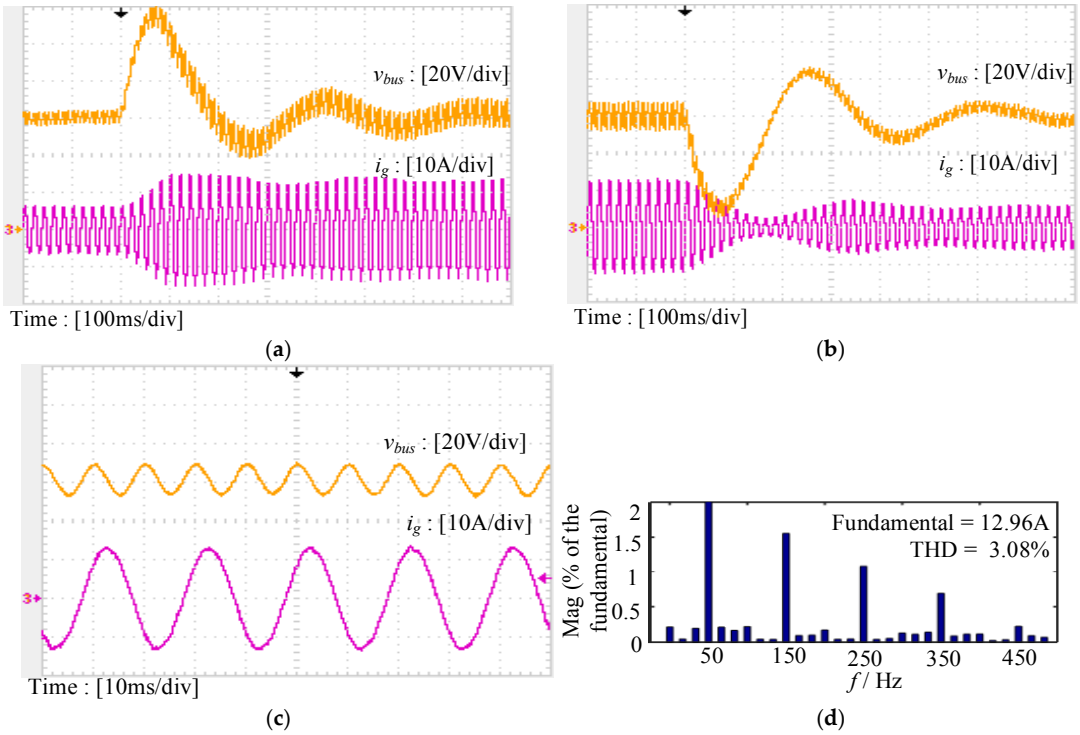

Figure 19. Experimental results of the PI controller with a low proportional gain. (**a**) Transient response when input power steps up from 1 kW to 2 kW; (**b**) Transient response when input power steps down from 2 kW to 1 kW; (**c**) Steady-state waveforms; and (**d**) Main harmonic components.

5.2. FIR Notch Filter Inserted Bus Voltage Regulator

For the FIR notch filter inserted bus voltage controller, the experimental control parameters are the same as in simulation. The experimental results are shown in Figure 20. The 2-f ripple is rejected by the FIR notch filter, so it doesn't create distortion in the grid current. Moreover, since the FIR notch filter exhibits a gain of unity at the low frequency, the bus voltage regulator is designed with high gain and high bandwidth. Consequently, compared with the PI controller with a low proportional gain, the overshoot and undershoot in the average DC bus voltage are significantly reduced, while the output current maintains high quality.

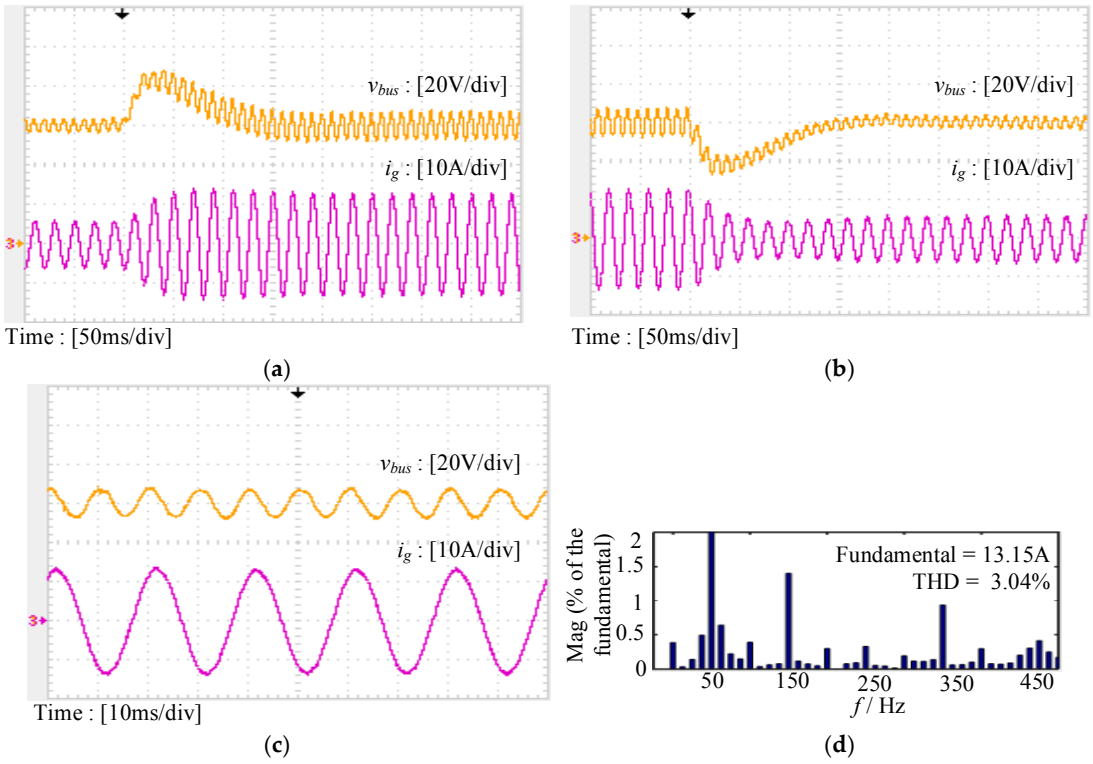

Figure 20. Experimental results of the FIR notch filter inserted bus voltage regulator. (**a**) Transient response when input power steps up from 1 kW to 2 kW; (**b**) Transient response when input power steps down from 2 kW to 1 kW; (**c**) Steady-state waveforms; and (**d**) Main harmonic components.

5.3. FIR Notch Filter Inserted Bus Voltage Regulator with Kalman-Filter-Based Input Power Feedforward

The noise variances of the Kalman filter are determined by experiments. To smoothen the estimated current, a large measurement covariance value is selected, and R is equal to 1.5. The system covariance value (Q) is equal to 0.1. In Figure 21a, after an input power jump, the estimated DC bus input current $\hat{i}_{dc}$ and bus voltage v_{bus} increase simultaneously. It takes 55 ms for $\hat{i}_{dc}$ to reach the steady value. $\hat{i}_{dc}$ is very smooth and quick response to the power jump. In order to compare the performance of proposed estimator, a full order observer is also implemented and tested. The experimental results, which are presented in Figure 22, are well in agreement with simulation results. $\hat{i}_{dc}$, which is obtained by using the full order observer, contains more noises and ripples. The proposed estimator using the Kalman filter has excellent performance over the full order observer to identify the input current amplitude in real-time.

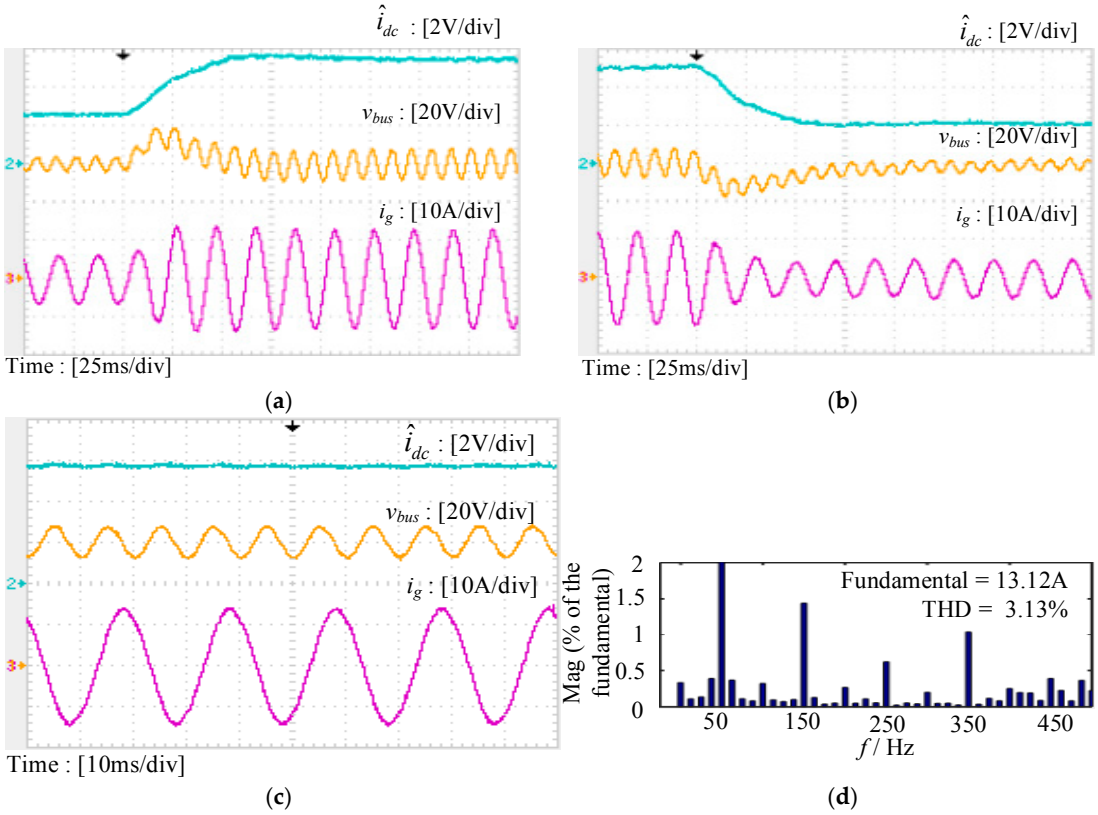

Figure 21. Experiment results of the FIR notch filter inserted bus voltage regulator with Kalman-filter-based input power feedforward. (**a**) Transient response when input power steps up from 1 kW to 2 kW; (**b**) Transient response when input power steps down from 2 kW to 1 kW; (**c**) Steady-state waveforms; and (**d**) Main harmonic components.

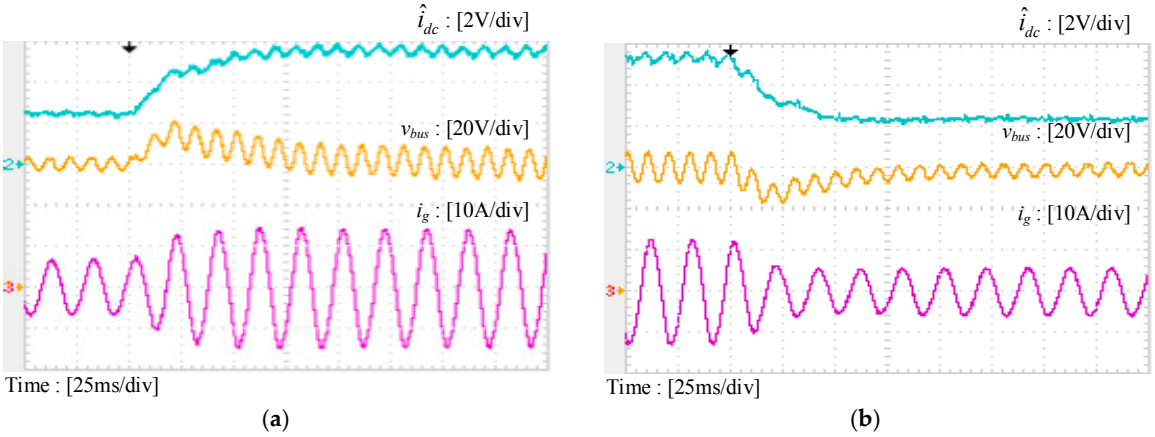

Figure 22. Experimental results for the full order observer (**a**) Transient response when input power steps up from 1 kW to 2 kW; (**b**) Transient response when input power steps down from 2 kW to 1 kW.

As the input power feedforward scheme implemented, fast dynamic response is achieved during input power transient. The overshoot and undershoot in average bus voltage are reduced to 59.4% and 60.7% of the original, respectively, without additional equipment. Moreover, the settle time is significantly reduced, and the quality of output current is nearly not affected. Table 3 lists the comparative experimental results of the four bus voltage control schemes.

Table 3. Comparative Experimental Results.

Method	Overshoot	Undershoot	THD
PI controller with a high proportional gain	18.7 V	19.8 V	8.68%
PI controller with a low proportional gain	56.3 V	50.3 V	3.08%
FIR notch filter inserted controller	23.2 V	22.4 V	3.04%
FIR notch filter inserted controller+ input power feedforward	13.8 V	13.6 V	3.13%

Figure 23 shows the experimental waveforms of grid voltage and current at full load for the FIR notch filter inserted bus voltage regulator with the Kalman-filter-based input power feedforward. Obviously, unity output power factor is achieved. The proposed synchronous frame current control scheme work well in actual system. The total delay time for sampling of the feedback signals and the calculation of the current controller and active damping is about 30 μs, which is less than the allowed $0.5T_s$.

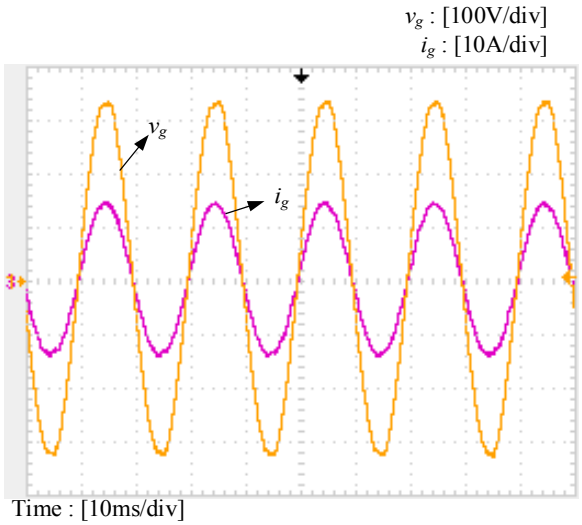

Figure 23. Experimental waveforms of grid voltage and current at full load for the FIR notch filter inserted bus voltage regulator with Kalman-filter-based input power feedforward.

5.4. Modulation Compensation Strategy for Bus Voltage Ripple

An experiment has also been conducted to illustrate the performance of the modulation compensation strategy. The FIR notch filter inserted bus voltage regulator with input power feedforward is used to control bus voltage. The current loop control parameters are the same as the above experiments. The result is given as Figure 24. The THD value of the compensated system is 2.82% compared to 3.13% of uncompensated system. The third harmonic can be observed reduced significantly by comparing Figure 21d with Figure 24.

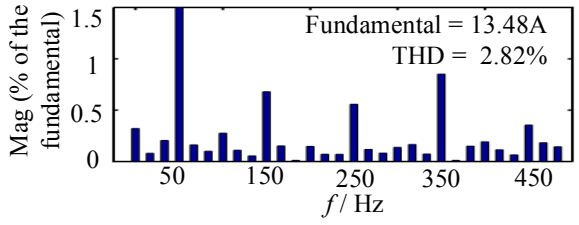

Figure 24. Main harmonic components for compensated system.

6. Conclusions

Design of a two-stage single-phase grid-connected converter with good dynamic response and low distortion is one of the most important topics in renewable grid-connected applications. Due to the presence of a second harmonic ripple across the DC bus voltage, the PI controller, which is conventionally used as DC bus voltage regulator, cannot solve the tradeoff between low harmonic distortion and high bandwidth. This paper presents an accurate math model to analyze the distortion caused by bus voltage ripple for the PI-based bus voltage controller.

To eliminate the tradeoff, a novel bus voltage control scheme is proposed. A second order FIR notch filter is used in the bus voltage control loop to eliminate the distortion in the reference current. Meanwhile, the Kalman-filter-based input power feedforward scheme is implemented to improve transient response. A modulation compensation strategy is also offered to remove the nonlinearity of grid current control loop, which is brought about by bus voltage ripple.

In addition, a synchronous frame current controller for single-phase systems is introduced. The math model in stationary frame, which is equivalent to a PR controller, is obtained through theoretical derivation. With the help of PLL, this control strategy is not sensitive to the grid fundamental frequency variation, while remaining the advantage of zero steady-state error and fast transient response. The implementation of the current controller for a single-phase grid-connected inverter with an LCL filter is also presented. During the design of inner CCF active damping loop, the influences of different time delays, which are caused by the digitally controlled system, are under consideration.

The results of simulations and experiments are provided to demonstrate that the proposed method can remarkably improve the dynamic performance without sacrificing the quality of the grid current. However, the insufficient of this paper is neglecting the interactions between the bus control loop and the current control loop. Further work will aim to establish an accurate math model.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Derivation of (5) and (6).

Equation (4) is rewritten as:

$$\int_0^t [P_{in} - V_g \cos^2(\omega_g t) I_{ref}] \mathrm{d}t \cdot \frac{\left|G_{c\text{-}bus}(j2\omega_g)\right|}{C_{bus} V_{ref}} = a_2 \cos(2\omega_g t + \theta) \tag{A1}$$

$$I_{ref} = a_0 + a_2 \cos(2\omega_g t + \theta) \tag{A2}$$

Calculating the derivative of the Equation (A1):

$$\left\{ P_{in} - \frac{V_g}{2}[1 + \cos(2\omega_g t)][a_0 + a_2 \cos(2\omega_g t + \theta) \right\} \cdot \frac{\left|G_{c\text{-}bus}(j2\omega_g)\right|}{C_{bus} V_{ref}} = -2\omega_g a_2 \sin(2\omega_g t + \theta) \tag{A3}$$

(A3) can be rewritten as:

$$\begin{array}{l} \left\{ [P_{in} - \frac{a_0 V_g}{2} - \frac{a_2 V_g \cos(\theta)}{4}] - \frac{a_0 V_g \cos(2\omega_g t)}{2} - \frac{a_2 V_g}{2} \cos(2\omega_g t + \theta) - \frac{a_2 V_g}{4} \cos(4\omega_g t + \theta) \right\} \\ \cdot \frac{\left|G_{c\text{-}bus}(j2\omega_g)\right|}{C_{bus} V_{ref}} = -2\omega_g a_2 \sin(2\omega_g t + \theta) \end{array} \tag{A4}$$

Considering the power balance, the DC component in (A4) is equal to 0:

$$P_{in} - \frac{V_g}{2}a_0 - \frac{V_g}{4}a_2\cos(\theta) = 0 \tag{A5}$$

(A5) is rewritten as:

$$P_{in} = \frac{V_g}{2}a_0 + \frac{V_g}{4}a_2\cos(\theta) \tag{A6}$$

Neglecting 4th harmonic component in (A4):

$$\left[\frac{a_0 V_g\cos(2\omega_g t)}{2} + \frac{a_2 V_g}{2}\cos(2\omega_g t+\theta)\right]\cdot\frac{\left|G_{c\text{-}bus}(j2\omega_g)\right|}{C_{bus}V_{ref}} \approx 2\omega_g a_2\sin(2\omega_g t+\theta) \tag{A7}$$

Simplifying (A7) as:

$$\begin{aligned}&\cos(2\omega_g t)\cdot\left[\tfrac{a_0 V_g\left|G_{c\text{-}bus}(j2\omega_g)\right|}{2C_{bus}V_{ref}} + \tfrac{a_2 V_g\left|G_{c\text{-}bus}(j2\omega_g)\right|}{2C_{bus}V_{ref}}\cos(\theta) - 2\omega_g a_2\sin(\theta)\right]\\ &= \sin(2\omega_g t)\cdot\left[\tfrac{a_2 V_g\left|G_{c\text{-}bus}(j2\omega_g)\right|}{2C_{bus}V_{ref}}\sin(\theta) + 2\omega_g a_2\cos(\theta)\right]\end{aligned} \tag{A8}$$

Since $\cos(2\omega_g t)$ and $\sin(2\omega_g t)$ is time variant, the following equations are obtained:

$$\begin{cases}\frac{a_0 V_g\left|G_{c\text{-}bus}(j2\omega_g)\right|}{2C_{bus}V_{ref}} + \frac{a_2 V_g\left|G_{c\text{-}bus}(j2\omega_g)\right|}{2C_{bus}V_{ref}}\cos(\theta) - 2\omega_g a_2\sin(\theta) = 0\\ \frac{a_2 V_g\left|G_{c\text{-}bus}(j2\omega_g)\right|}{2C_{bus}V_{ref}}\sin(\theta) + 2\omega_g a_2\cos(\theta) = 0\end{cases} \tag{A9}$$

The DC bus ripple is:

$$\Delta v_{bus}(t)\left|G_{c\text{-}bus}(j2\omega_g)\right| = a_2\cos(2\omega_g t+\theta) \tag{A10}$$

Solve (A9), the coefficients are expressed as:

$$\begin{cases}a_2 \approx \frac{a_0\left|G_{c\text{-}bus}(j2\omega_g)\right|V_g}{4\omega_g C_{bus}V_{ref}\sin(\theta)-\left|G_{c\text{-}bus}(j2\omega_g)\right|V_g\cos(\theta)}\\ \theta = \arctan\left(-\frac{4\omega_g C_{bus}V_{ref}}{\left|G_{c\text{-}bus}(j2\omega_g)\right|V_g}\right)\\ \left|\Delta v_{bus}\right|_{\mathrm{pp}} \approx \frac{2a_2}{\left|G_{c\text{-}bus}(j2\omega_g)\right|}\end{cases}$$

References

1. Blaabjerg, F.; Teodorescu, R.; Liserre, M.; Timbus, A.V. Overview of control and grid synchronization for distributed power generation systems. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1398–1409.
2. Xia, Y.; Ahmed, K.H.A.; Williams, B.W. A New Maximum Power Point Tracking Technique for Permanent Magnet Synchronous Generator Based Wind Energy Conversion System. *IEEE Trans. Power Electron.* **2011**, *26*, 3609–3620. [CrossRef]
3. Esram, T.; Chapman, P.L. Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques. *IEEE Trans. Energy Convers.* **2007**, *22*, 439–449. [CrossRef]
4. Jeong, H.G.; Kim, G.; Lee, K.B. Second-Order Harmonic Reduction Technique for Photovoltaic Power Conditioning Systems Using a Proportional-Resonant Controller. *Energies* **2013**, *6*, 79–96. [CrossRef]
5. Chen, Y.M.; Chang, C.H.; Wu, H.C. DC-Link Capacitor Selections for the Single-Phase Grid-Connected PV System. In Proceedings of the 2009 International Conference on Power Electronics and Drive Systems (PEDS), Taipei, Taiwan, 2–5 November 2009; pp. 72–77.
6. Karimi-Ghartemani, M.; Khajehoddin, S.A.; Jain, P.; Bakhshai, A. A Systematic Approach to DC-Bus Control Design in Single-Phase Grid-Connected Renewable Converters. *IEEE Trans. Power Electron.* **2013**, *28*, 3158–3166. [CrossRef]

7. DeBlasio, R.; Chalmers, S.; Anderson, A.J. *IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems*; IEEE Std. 929-2000; IEEE Standards Association: New York, NY, USA, 2000.
8. Krein, P.T.; Balog, R.S.; Mirjafari, M. Minimum Energy and Capacitance Requirements for Single-Phase Inverters and Rectifiers Using a Ripple Port. *IEEE Trans. Power Electron.* **2012**, *27*, 4690–4698. [CrossRef]
9. Cai, W.; Liu, B.; Duan, S.; Jiang, L. An Active Low-Frequency Ripple Control Method Based on the Virtual Capacitor Concept for BIPV Systems. *IEEE Trans. Power Electron.* **2014**, *29*, 1733–1745. [CrossRef]
10. Khajehoddin, S.A.; Karimi-Ghartemani, M.; Jain, P.K.; Bakhshai, A. DC-Bus Design and Control for a Single-Phase Grid-Connected Renewable Converter with a Small Energy Storage Component. *IEEE Trans. Power Electron.* **2013**, *28*, 3245–3254. [CrossRef]
11. Levron, Y.; Canaday, S.; Erickson, R.W. Bus Voltage Control with Zero Distortion and High Bandwidth for Single Phase Solar Inverters. *IEEE Trans. Power Electron.* **2016**, *1*, 258–269. [CrossRef]
12. Perez, M.A.; Espinoza, J.R.; Rodriguez, J.R.; Lezana, P. Regenerative Medium-Voltage AC Drive Based on a Multicell Arrangement with Reduced Energy Storage Requirements. *IEEE Trans. Ind. Electron.* **2005**, *52*, 171–180. [CrossRef]
13. Andrade, A.M.S.S.; Beltrame, R.C.; Schuch, L.; Martins, M.L.S. PV Module-Integrated Single-Switch DC/DC Converter for PV Energy Harvest with Battery Charge Capability. In Proceedings of the 2014 IEEE International Conference on Industry Applications, Juiz de Fora, Brazil, 7–10 December 2014.
14. Aghdam, F.H.; Hagh, M.T.; Abapour, M. Reliability Evaluation of Two-Stage Interleaved Boost Converter Interfacing PV Panels Based on Mode of Use. In Proceedings of the Power Electronics and Drive Systems Technologies Conference (PEDSTC), Tehran, Iran, 16–18 February 2016; pp. 409–414.
15. Khajehoddin, S.A.; Bakhshai, A.; Jain, P. A Novel Topology and Control Strategy for Maximum Power Point Trackers and Multi-String Grid-Connected PV Inverters. In Proceedings of the Applied Power Electronics Conference and Exposition (APEC), Austin, TX, USA, 24–28 February 2008; pp. 173–178.
16. Zeng, J.; Qiao, W.; Qu, L.; Jiao, Y. An Isolated Multiport DC–DC Converter for Simultaneous Power Management of Multiple Different Renewable Energy Sources. *IEEE J. Emerg. Sel. Top. Power Electron.* **2014**, *2*, 70–78. [CrossRef]
17. Zeng, Z.; Yang, H.; Zhao, R.; Cheng, C. Topologies and control strategies of multi-functional grid-connected inverters for power quality enhancement: A comprehensive review. *Renew. Sustain. Energy Rev.* **2013**, *24*, 223–270. [CrossRef]
18. Du, Y.; Lu, D.D.; James, G.; Cornforth, D.J. Modeling and analysis of current harmonic distortion from grid connected PV inverters under different operating conditions. *Sol. Energy* **2013**, *94*, 182–194. [CrossRef]
19. Fu, X.; Li, S. A Novel Neural Network Vector Control for Single-Phase Grid-Connected Converters with L, LC and LCL Filters. *Energies* **2016**, *9*, 328. [CrossRef]
20. Guo, X.; Guerrero, J.M. General Unified Integral Controller with Zero Steady-State Error for Single-Phase Grid-Connected Inverters. *IEEE Trans. Smart Grid.* **2016**, *7*, 74–83. [CrossRef]
21. Junyent-Ferre, A.; Gomis-Bellmunt, O.; Green, T.C.; Soto-Sanchez, D.E. Current Control Reference Calculation Issues for the Operation of Renewable Source Grid Interface VSCs under Unbalanced Voltage Sags. *IEEE Trans. Power Electron.* **2011**, *26*, 3744–3753. [CrossRef]
22. Du, Y.; Lu, D.D.; Chu, G.M.L.; Xiao, W. Closed-Form Solution of Time-Varying Model and Its Applications for Output Current Harmonics in Two-Stage PV Inverter. *IEEE Trans. Sustain. Energy* **2015**, *6*, 142–150.
23. Zhang, N.; Tang, H.; Yao, C. A Systematic Method for Designing a PR Controller and Active Damping of the LCL Filter for Single-Phase Grid-Connected PV Inverters. *Energies* **2014**, *7*, 3934–3954. [CrossRef]
24. Puchalard, R.; Lorsawatsiri, A.; Loetwassana, W.; Koseeyaporn, J.; Wardkein, P.; Roeksabutr, A. Direct frequency estimation based adaptive algorithm for a second-order adaptive FIR notch filter. *Singal Process.* **2008**, *88*, 315–325. [CrossRef]
25. Qiu, C.; Huang, S.; Wang, E. Direct Active Power Control for Regenerative Cascade Inverter with Reduced AC Power in DC Link. *Automatika* **2014**, *55*, 425–433. [CrossRef]
26. Simon, D. *Optimal State Estimation*; John Wiley & Sons: Hoboken, NJ, USA, 2006; pp. 121–330.
27. Gu, Y.; Wang, Y.; Xiang, X.; Li, W.; He, X. Improved Virtual Vector Control of Single-Phase Inverter Based on Unified Model. *IEEE Trans. Energy Convers.* **2014**, *29*, 611–617. [CrossRef]
28. Saitou, M.; Shimizu, T. Generalized Theory of Instantaneous Active and Reactive Powers in Single-phase Circuits based on Hilbert Transform. In Proceedings of the Power Electronics Specialists Conference, Cairns, Queensland, Australia, 23–27 June 2002; pp. 1419–1424.

29. Bahrani, B.; Rufer, A.; Kenzelmann, S.; Lopes, L.A.C. Vector Control of Single-Phase Voltage-Source Converters Based on Fictive-Axis Emulation. *IEEE Trans. Ind. Appl.* **2011**, *47*, 831–840. [CrossRef]
30. Silva, S.M.; Lopes, B.M.; Filho, B.J.C.; Campana, R.P.; Boaventura, W.C. Performance Evaluation of PLL Algorithms for Single-phase Grid-connected Systems. In Proceedings of the IEEE Industry Applications Conference, Seattle, WA, USA, 3–7 October 2004; pp. 2259–2263.
31. Kim, R.Y.; Choi, S.Y.; Suh, I. Instantaneous control of average power for grid tie inverter using single phase DQ rotating frame with all pass filter. In Proceedings of the IEEE Industrial Electronics Society, Busan, Korea, 2–6 November 2004; pp. 274–279.
32. Song, W.; Deng, Z.; Wang, S.; Feng, X. A Simple Model Predictive Power Control Strategy for Single-Phase PWM Converters with Modulation Function Optimization. *IEEE Trans. Power Electron.* **2016**, *31*, 5279–5289. [CrossRef]
33. Mehrasa, M.; Rezanejhad, M.; Pouresmaeil, E.; Catalao, J.P.S.; Zabihi, S. Analysis and Control of Single-Phase Converters for Integration of Small-Scaled Renewable Energy Sources into the Power Grid. In Proceedings of the 7th Power Electronics, Drive Systems & Technologies Conference, Tehran, Iran, 16–18 February 2016; pp. 384–389.
34. Hosseini, S.K.; Mehrasa, M.; Taheri, S.; Rezanejad, M.; Pouresmaeil, E.; Catalão, J.P.S. A Control Technique for Operation of Single-Phase Converters in Stand-alone Operating Mode. In Proceedings of the IEEE Electrical Power and Energy Conference, Ottawa, ON, Canada, 12–14 October 2016.
35. Zou, C.; Liu, B.; Duan, S.; Li, R. Stationary Frame Equivalent Model of Proportional-Integral Controller in dq Synchronous Frame. *IEEE Trans. Power Electron.* **2014**, *29*, 4461–4465. [CrossRef]
36. GB/T 19964-2012. *Technical Requirements for Connecting Photovoltaic to Power System*; General Administration of Quality Supervision, Inspection and Quarantine of China and Standardization Administration of China: Beijing, China, 2012.
37. Mascioli, M.; Pahlevani, M.; Jain, P.K. Frequency-Adaptive Current Controller for Grid-Connected Renewable Energy Systems. In Proceedings of the IEEE International Telecommunications Energy Conference, Vancouver, BC, Canada, 28 September–2 October 2014.
38. Lorzadeh, I.; Abyaneh, H.A.; Savaghebi, M.; Bakhshai, A.; Guerrero, J.G. Capacitor Current Feedback-Based Active Resonance Damping Strategies for Digitally-Controlled Inductive-Capacitive-Inductive-Filtered Grid-Connected Inverters. *Energies* **2016**, *9*, 642. [CrossRef]
39. Chen, C.; Xiong, J.; Wan, Z.; Lei, J.; Zhang, K. Time Delay Compensation Method Based on Area Equivalence for Active Damping of LCL-Type Converter. *IEEE Trans. Power Electron.* **2017**, *32*, 762–772. [CrossRef]
40. Wang, J.; Yan, J.D.; Jiang, L.; Zou, J. Delay-Dependent Stability of Single-Loop Controlled Grid-Connected Inverters with LCL Filters. *IEEE Trans. Power Electron.* **2016**, *31*, 743–757. [CrossRef]
41. Zhang, X.; Spencer, J.W.; Guerrero, J.M. Small-Signal Modeling of Digitally Controlled Grid-Connected Inverters with LCL Filters. *IEEE Trans. Power Electron.* **2013**, *60*, 3752–3765.