A Comprehensive Study on the Avalanche Breakdown Robustness of Silicon Carbide Power MOSFETs

Asad Fayyaz [1],*, Gianpaolo Romano [2], Jesus Urresti [3], Michele Riccio [2], Alberto Castellazzi [1], Andrea Irace [2] and Nick Wright [3]

[1] Power Electronics, Machines and Control Group, University of Nottingham, Nottingham NG7 2RD, UK; alberto.castellazzi@nottingham.ac.uk

[2] Department of Electrical Engineering and Information Technologies, University of Naples Federico II, Via Claudio 21, 80125 Naples, Italy; gianpaolo.romano@unina.it (G.R.); michele.riccio@unina.it (M.R.); andrea.irace@unina.it (A.I.)

[3] Emerging Technologies and Materials Group, Newcastle University, Newcastle upon Tyne NE1 7RU, UK; jesus.urresti@newcastle.ac.uk (J.U.); nick.wright@newcastle.ac.uk (N.W.)

* Correspondence: asad.fayyaz@nottingham.ac.uk; Tel.: +44-115-9515568

Abstract: This paper presents an in-depth investigation into the avalanche breakdown robustness of commercial state-of-the-art silicon carbide (SiC) power MOSFETs comprising of functional as well as structural characterization and the corresponding underlying physical mechanisms responsible for device failure. One aspect of robustness for power MOSFETs is determined by its ability to withstand energy during avalanche breakdown. Avalanche energy (E_{AV}) is an important figure of merit for all applications requiring load dumping and/or to benefit from snubber-less converter design. 2D TCAD electro-thermal simulations were performed to get important insight into the failure mechanism of SiC power MOSFETs during avalanche breakdown.

Keywords: avalanche breakdown; silicon carbide (SiC); wide band-gap (WBG); power MOSFET; unclamped inductive switching (UIS); failure mechanism; leakage current

1. Introduction

Silicon carbide, (SiC), a wide-bandgap (WBG) semiconductor material, has tremendously outstanding physical material properties when compared to its well established silicon (Si) counterpart. Some physical properties of SiC which have relevance to power conversion are as follows [1]:

(1) Wider bandgap (E_g)—approximately 3.23 eV as compared to 1.1 eV in Si;
(2) Higher critical electrical field (E_C)—approximately 10 times than in Si;
(3) Higher thermal conductivity (λ) at a given temperature—around 3–5 times that of Si.

Over the last 10 years, SiC power MOSFET manufacturing technology has experienced rapid technological advances. As a consequence, they are now a commercial reality, available in different ratings from different manufacturers. Nowadays, SiC power MOSFETs are in the limelight and probably are the most common type of SiC device that are available on the market after Schottky diodes [2,3]. Devices made from SiC relatively offer lower on-state resistance, higher switching frequency and better off-state performance due to small leakage current [4].

Before SiC power MOSFETs can be implemented into power systems at a larger scale to reap the benefits mentioned earlier, it is crucial to characterize these devices for their robustness and

reliability. In order to define the safe operating area (SOA) boundaries for the device, short circuit (SC) and unclamped inductive switching (UIS) tests are widely used within power electronics industry. Indeed, these tests represent really stressful real life events for the device. Over the past few years, various studies have been presented [5–10] which have highlighted the avalanche breakdown (through UIS test) and short-circuit (SC) robustness of SiC power MOSFETs. Though significant maturity has been achieved at device manufacturing level, experimental device characterization results suggests that there is still space for improvement to extend devices' SOA boundaries in order to make them more robust.

Power MOSFETs are widely used in high switching frequency applications with inductive loads such as motor drive applications. Such applications require the devices to be able to withstand a certain duration of avalanche breakdown. A power MOSFET could experience avalanche breakdown between drain and source at turn-off and back EMF (electromagnetic force) is produced by the inductive loads and/or parasitic elements due to sudden interruption of current. In other words, any energy stored in the inductive load during unclamped load dumping would have to be dissipated into the device after device turn-off switching transient. This harsh switching transient condition could also result in failure of the device. Avalanche ruggedness is an important feature for a power device which is determined by its ability to dissipate avalanche energy (E_{AV}) without catastrophic device failure. It also enables snubber-less converter design which could possibly mean reduction in cost, number of components and converter size. Certain automotive applications such as anti-lock braking systems and engine control units (ECUs) require power devices to dissipate more consistent overload transient energy release from inductive loads, typically motors and actuator controlled solenoids [11].

The avalanche breakdown failure mechanism of N-MOS Si power MOSFETs is well-known and mainly linked to the activation of the inherent parasitic NPN BJT. The failure mechanism has been divided into two different classes: current failure and temperature failure. Current failure is linked to the activation of the parasitic BJT (occurs due to small inductor values and parasitic elements which implies high current values) whereas the temperature failure is due to reaching critical junction temperature of the device (for high inductor values and small switched current values). Indeed, various different Si power MOSFET structures evolved along the course of time which targeted the parasitic BJT structure to delay its activation and thus enhance robustness [12]. However, the wider bandgap of SiC makes it highly unlikely for the activation of the parasitic BJT element during typical UIS events (i.e., with typical values of switched currents and ensuing temperature evolution). Previous publications have shown that commercially available SiC MOSFETs exhibit significant intrinsic avalanche ruggedness and could dissipate E_{AV} above 1 J, depending on the test conditions [5–7,13,14]. Even though different studies have presented experimental avalanche robustness, the understanding of its failure mechanism stills remains somewhat unclear and lacking. So, to get more insight into device internal phenomena and the actual failure mechanism, experimental results showing failure have been reproduced with the aid of 2D TCAD physical simulations which are included here and constitutes one of the main methodology of this investigation.

2. MOSFET Avalanche Breakdown

Solid state switches for power electronic applications are normally designed to withstand high voltages, usually represented as the nominal blocking voltage capability (V_{DSmax}). Power electronics applications requiring control of higher power levels such as power distribution and conversion, industrial motor drives and railway traction require devices with larger breakdown voltages.

Semiconductor devices have the ability to support high voltages in the OFF-state, without having a significant drain leakage current (I_{DSS}). The avalanche breakdown mechanism is dependent on the distribution of electric field (E) inside the structure [15]. A structure of a power MOSFET is illustrated in Figure 1. During device design, the doping of N-drift layer (N_{drift}) is carefully chosen to obtain the desired breakdown voltage (V_{BD}). At the same time, the depth of the N-drift layer should be appropriately selected as it should contain the full depletion layer width (W_m) corresponding to V_{BD}

of the device being designed. It is crucial to avoid the depletion region reaching the N+ substrate region as it causes punch through. The analytical device design equations defining the V_{BD} and W_m for non-fully N-depleted region structures are included here as Equations (1) and (2) respectively [15]:

$$V_{BD} = \frac{\varepsilon_s \cdot E_c{}^2}{2q \cdot N_{drift}} \tag{1}$$

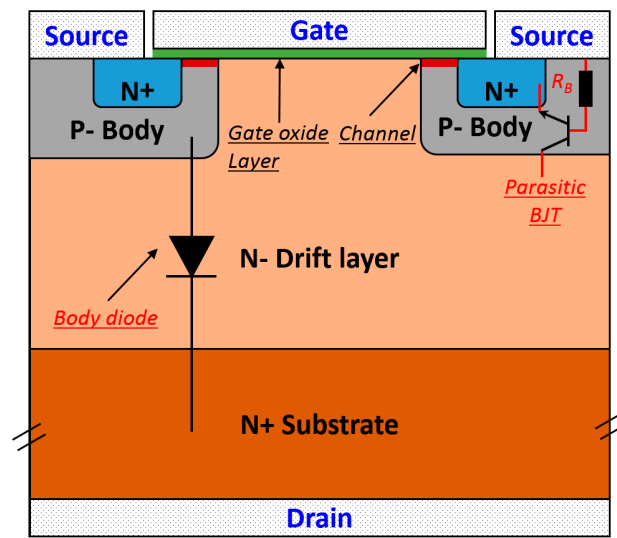$$W_m = \sqrt{\frac{2\varepsilon_s \cdot V_{BD}}{q \cdot N_{drift}}} \tag{2}$$

Figure 1. Structure of an N-channel power MOSFET.

For 4H-SiC, Equations (1) and (2) could be written as a function of N_{drift} only as presented in Equations (3) and (4) below [15]:

$$V_{BD} = 3.0 \times 10^{15} N_{drift}{}^{-3/4} \; \text{(V)} \tag{3}$$

$$W_m = 1.82 \times 10^{11} N_{drift}{}^{-7/8} \; (\mu m) \tag{4}$$

In the presence of high electric field, collision of mobile carriers possessing sufficient energy with the lattice atoms results in creation of electron-hole pairs. This is known as impact ionization. Subsequently, electron-hole pairs generated due to impact ionization result in generation of further electrons and holes pairs. In other words, impact ionization is an augmented process producing a continuous flow of electrons through the depletion region which results in significant flow of current between drain and source during avalanche breakdown. Therefore, the maximum operating voltage for a power device is limited by avalanche breakdown [15].

3. Experimental Results

UIS test circuit, illustrated in Figure 2a, is widely used for assessment of avalanche ruggedness of power devices. An auxiliary 3 kV IGBT from IXYS (IXBH12N300) was used in parallel to ramp up inductor current to the desired value. When the IGBT turns OFF, the device under test (DUT) enters avalanche breakdown since current in the inductor cannot immediately go to zero due to the current continuity condition. Parameters such as IGBT on-time (t_{ON}), inductance (L), input voltage (V_{DD}) and case temperature (T_{CASE}) are normally altered to move outside of the device's SOA until failure is obtained. The representative current (I_D) and voltage (V_{DS}) waveforms are included in Figure 2b.

During the on-time of IGBT, the inductor almost experiences V_{DD} giving rise to linear increase of the inductor current as also defined by Equation (5). On the other hand, during avalanche phase, the current conduction takes place through the reverse body diode of the DUT. Selected experimental results of commercial state-of-the-art SiC power MOSFETs during UIS have been included here. The test results presented here are on a 1200 V 36 A 80 mΩ commercial SiC power MOSFET device (C2M0080120D) in a TO-247 package from CREE [16].

$$V = L\frac{dI}{dt} \tag{5}$$

The results presented here clearly demonstrate the significant intrinsic avalanche ruggedness of these devices. The rated breakdown voltage ($V_{BR(DSS)}$) for these devices is 1200 V but the actual breakdown voltage ($V_{BR(eff)}$) is found to be around 1800 V. As shown in [7,14], failure can occur at different E_{AV} (up to 1 J) based on current profile and T_{CASE}. Here, current value was chosen to align with applications in power converters.
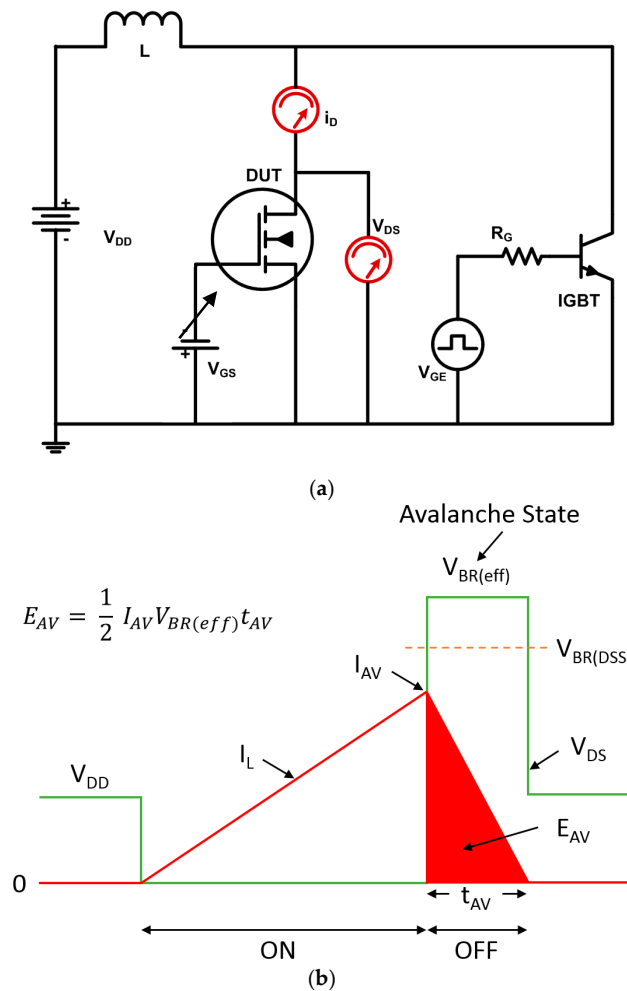

Figure 2. UIS test circuit and waveforms. (**a**) UIS circuit schematic; and (**b**) Representative DUT I_D and V_{DS} waveforms for safe avalanche event.

Different tests were performed at different gate-source voltages (V_{GS}). Figure 3a shows the I_D and V_{DS} waveforms for $V_{GS} = 0$ V for a safe avalanche event, characterized by a return of the current to zero and the voltage to the input voltage (V_{DD}) value. The on-time for the IGBT was gradually increase to increase the peak avalanche current (I_{AV}) until failure was observed as indicated in Figure 3b.
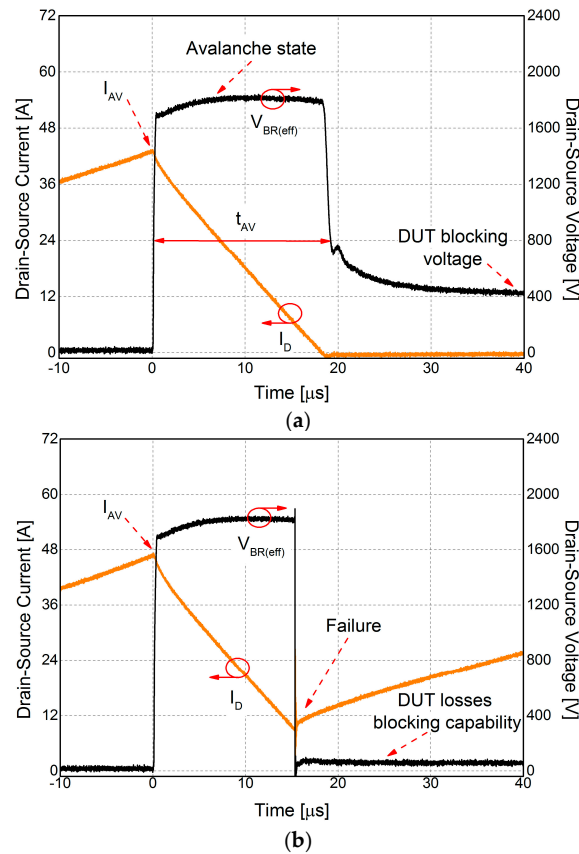
Figure 3. Experimental V_{DS} and I_D waveform; V_{DD} = 400 V; T_{CASE} = 25 °C; V_{GS} = 0 V; L = 500 μH. (**a**) Without Failure; I_{AV}~42 A; (**b**) At Failure; I_{AV}~47 A.

The test was repeated under the same test conditions but changing the V_{GS} to −5 V. The results comparing the I_D and V_{DS} waveforms for V_{GS} = 0 V and −5 V with the same I_{AV} ~47 A are included in Figure 4. Here, an important observation to be made is that the DUT with V_{GS} = −5 V safely completes the avalanche phase and returns to blocking afterwards. On the other hand, the DUT tested for V_{GS} = 0 V failed for I_{AV}~47 A. For a DUT tested at V_{GS} = −5 V, higher I_{AV} ~50 A, i.e., higher E_{AV} was needed before failure was observed as shown in Figure 5. The obtained experimental results demonstrate the avalanche robustness of SiC power MOSFETs is dependent on gate bias (V_{GS}).
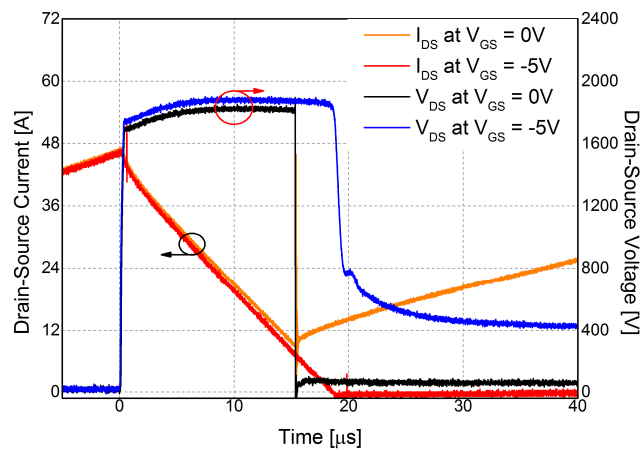

Figure 4. Experimental V_{DS} and I_D waveform; I_{AV}~47 A; V_{DD} = 400 V; T_{CASE} = 25 °C; V_{GS} = 0 V and −5 V; L = 500 μH (Comparison).
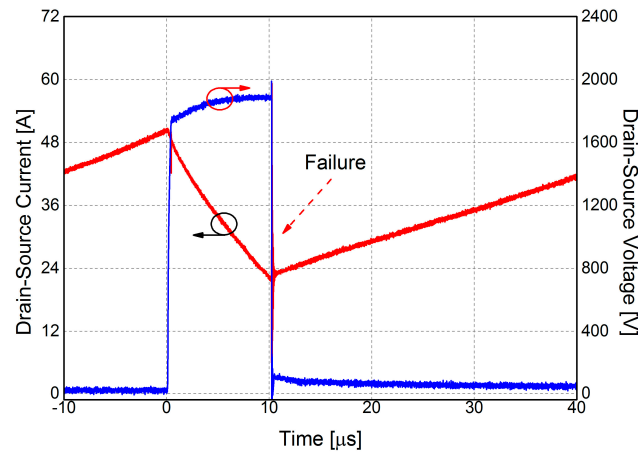
Figure 5. Experimental V_{DS} and I_D waveform; $I_{AV} \sim 50$ A; V_{DD} = 400 V; T_{CASE} = 25 °C; V_{GS} = −5 V; L = 500 μH.

4. TCAD Electro-Thermal Simulations

In order to obtain an insight into device failure mechanism during avalanche state, electro-thermal 2D TCAD simulations were performed in the Sentaurus software from Synopsys. The simulated structure and mixed-mode circuit used for simulation including some parasitic elements are included in Figure 6a,b, respectively. Data from various literatures [15,17,18] was used to define the cell dimensions and doping concentrations (presented in Figure 6a). The cell was refined to acheive a suitable validation of both static and UIS waveforms. The parameters involved to obtain this were the depth and doping of the N-drift region. Even though the simulated cell structure was calibrated to match the behavior of a commercial device but it does not represent the real device sturcture. Here, the N+ drain thickness was chosen to be small (1 μm) as it would not yield any further insight and would unnessarily slow down the simulations.

Figure 7 plots the UIS I_D and V_{DS} waveform at failure. In these simulations, two seperate electrodes were used for p body and N+ source implant. The hole and electron current components respectively for p body and n+ source, together with the overall device current are shown in Figure 8. The failure is defined as the point where the voltage collapse is observed. Because of the simplified nature of the model (without 3D structural elements and field guard rings), the actual failure may take place at a point in time earlier than in simulation. However, the important observation is that the channel current flows. As can be seen in Figure 8, electron current starts to flow into the N+ source region as the t_{AV} lapsed until failure occurred. The current distribution when the channel is conducting during DUT t_{ON} is shown in Figure 9.

Figure 10a presents the current distribution within the whole cell immediately after the device enters avalanche breakdown. Figure 10b, zoomed in region near the corner of the pn region, shows current density at four different t_{AV} instances of increasing order from 1 to 4. A progressive shift of current from reverse diode towards channel is observed. During the first phase of breakdown phenomena (Figure 10b1), current mainly flows through the corner of the P body/N- drift region corresponding to the location where highest electric field density and maximum impact ionization occurs inside the cell. However, as the temperature increases during t_{AV}, the current partially also starts to flow in and below the channel region (Figure 10b2,b3) aided by the reduction of V_{th} with temperature leading to channel activation. At failure (Figure 10b4), all the device current flows in and below the channel region.
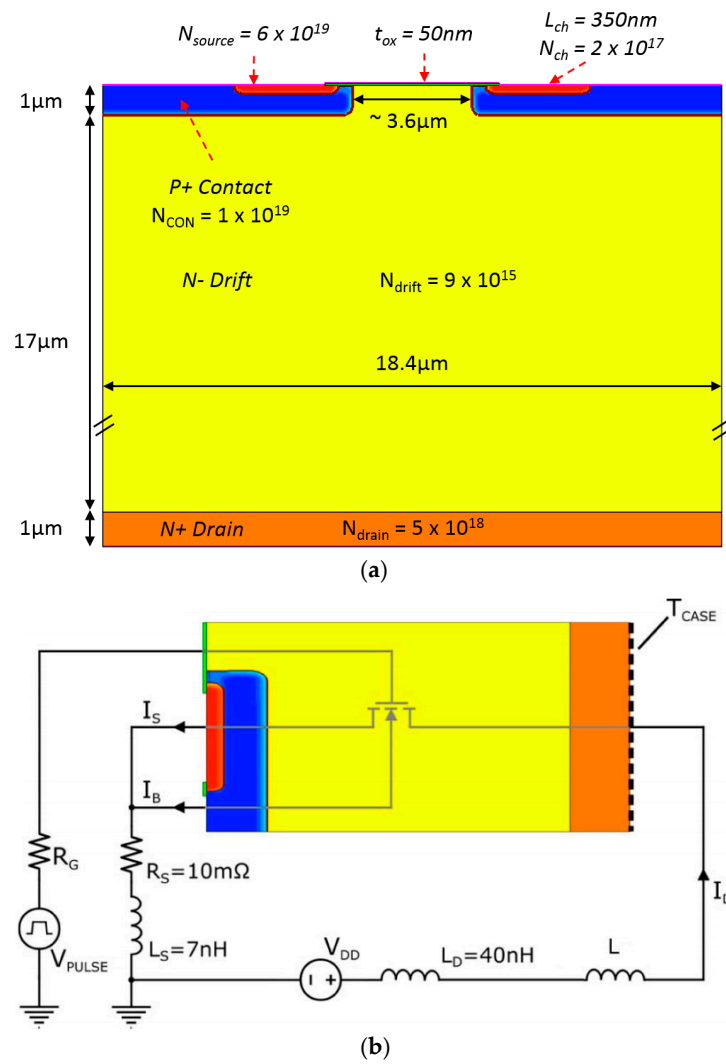
(**a**)

(**b**)

Figure 6. SiC MOSFET structure in Sentaurus TCAD Software. (**a**) Simulated structure (Not to scale); (**b**) Mixed-mode UIS circuit schematic.
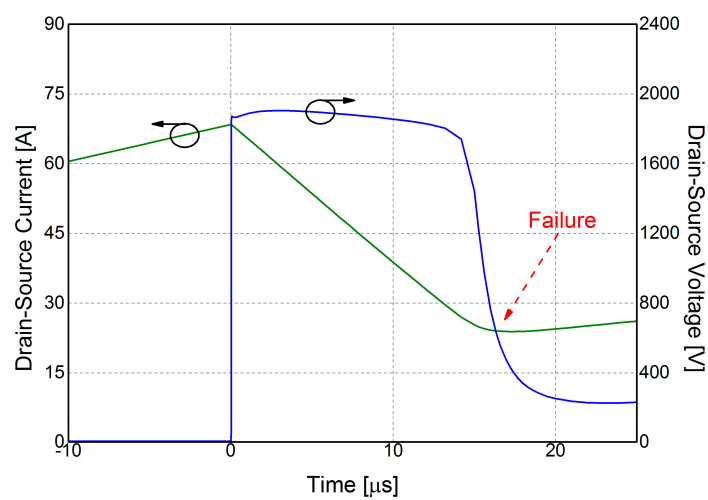

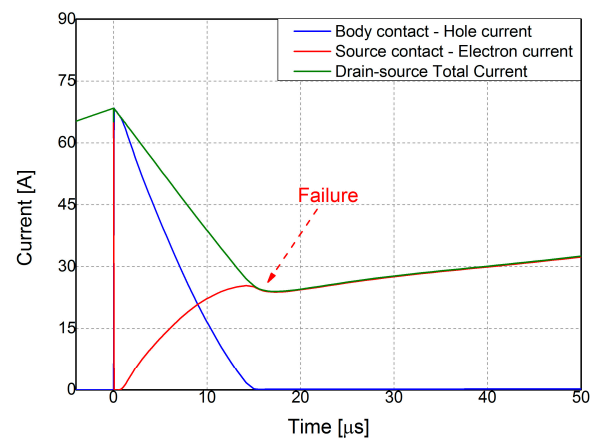**Figure 7.** Simulated V_{DS} and I_D waveform—V_{DD} = 400 V; T_{CASE} = 25 °C; L = 500 μH.

Figure 8. Hole and electron current components along with total current at failure.
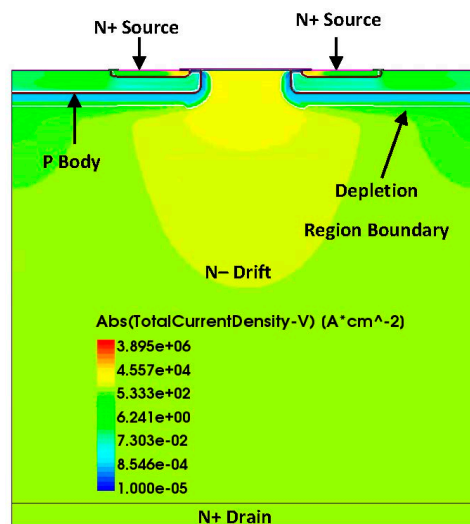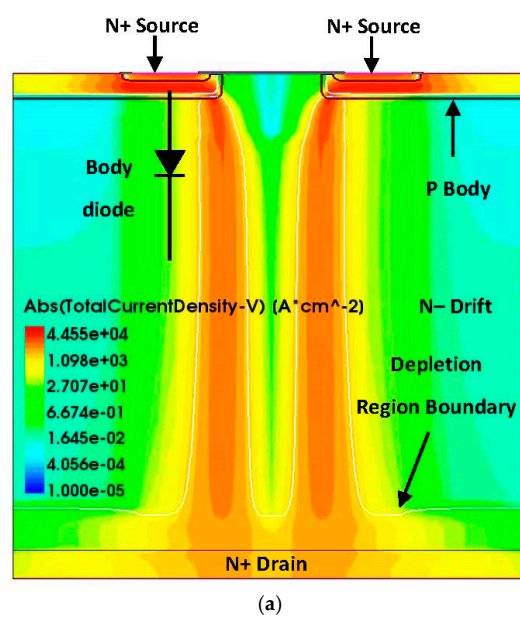

Figure 9. Current distribution during ON state.
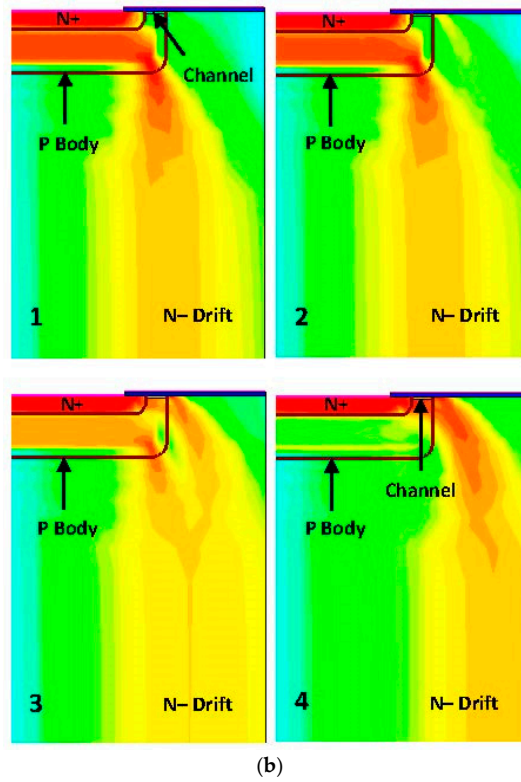

(**a**)

Figure 10. *Cont*.

Figure 10. Current distribution during avalanche breakdown and failure. (**a**) Complete cell; immediately after avalanche breakdown; (**b**) Zoomed in; 1–4 with increasing t_{AV}.

5. Analytical Calculation of Threshold Voltage

Experimental results show that the avalanche capability of SiC power MOSFET has dependence on gate bias voltage. At the same time, electro-thermal simulations have shown that decrease in V_{th} with increasing temperature leads to device failure. Hence, it was important to analytically calculate V_{th} and study the effect of temperature on V_{th}. The V_{th} analytical study is presented below. Gate threshold voltage is determined by:

$$V_{th} = V_{fb} + \phi_s + V_{ox} \tag{6}$$

where V_{fb} is the flat band voltage, ϕ_s is the surface's semiconductor band bending and V_{ox} is the oxide voltage drop. The threshold condition is achieved when:

$$\phi_s = 2\phi_F \tag{7}$$

where ϕ_F is the distance between the intrinsic fermi level and the actual fermi level.

Now, V_{th} equation has to be expanded to identify the temperature dependence:

$$V_{fb} = \phi_{ms} - \frac{qN_{ox}}{C_{ox}} \tag{8}$$

where the work-function difference (ϕ_{ms}) is calculated by:

$$\phi_{ms} = \phi_m - \left(\chi_{SiC} + \frac{E_g}{2} + \phi_F \right) \tag{9}$$

and:

$$V_{ox} = \frac{\sqrt{2\varepsilon_{SiC}qN_A\phi_s}}{C_{ox}} = \frac{\sqrt{2\varepsilon_{SiC}qN_A2\phi_F}}{C_{ox}} \tag{10}$$

Since ε_{SiC}, ε_{SiO2}, ϕ_m and ϕ_s do not change significantly with temperature, it is assumed that these parameters are constant with temperature. Hence, the temperature dependence of the threshold voltage is due to the Bandgap (E_g) and ϕ_F:

$$\phi_F(T) = \frac{kT}{q}ln\left(\frac{N_A}{n_i(T)}\right) \tag{11}$$

where there is a strong temperature dependence of the intrinsic carrier concentration:

$$n_i(T) = \sqrt{N_C(T)N_V(T)}\exp\left(-\frac{E_g}{2kT}\right) \tag{12}$$

The effective density of states in the conduction and valence band (N_C and N_V) are given by:

$$N_C(T) = 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} \tag{13}$$

$$N_V(T) = 2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2} \tag{14}$$

N_C and N_V can be approximated by [18]:

$$N_C(T) = 3.25 \times 10^{15}T^{3/2}\left(\text{cm}^{-3}\right) \tag{15}$$

$$N_V(T) = 4.8 \times 10^{15}T^{3/2}\left(\text{cm}^{-3}\right) \tag{16}$$

Bandgap energy of 4H-SiC can be modelled by [19]:

$$E_g(T) = E_g(0) - 6.5 \times 10^{-4}\frac{T^2}{T + 1300} \tag{17}$$

where [20]:

$$E_g(0) = 3.265 \text{ eV} \tag{18}$$

Thus, taking the following parameters:

- Substrate doping concentration (N_A): 3×10^{17} cm^{-3};
- Gate oxide thickness (t_{ox}): 50 nm;
- Oxide charge density (N_{ox}): 1×10^{10} cm^{-3};
- Oxide permittivity (ε_{SiO2}): 3.45×10^{-11} F/m;
- Silicon carbide permittivity (ε_{SiC}): 8.55×10^{-11} F/m;
- Metal work function (ϕ_m): 4.1 eV for aluminum (Al);
- SiC electron affinity (χ_{SiC}): 3.2 eV.

Therefore, using the above parameters, a plot of ΔV_{th} (with respect to V_{th} value at lowest temperature of 100 K) versus temperature was obtained to give an estimation of the decrease in V_{th} value as temperature increases, which is included in Figure 11. The initial V_{th} of the DUTs tested is ~2.5 V at 300 K. However, due to very small chip size of SiC device (approximately 3 mm × 3 mm) and relatively larger thermal conductivity result in rapid increase of the device temperature (could rise easily well above 1000 K) during such dissipative events. SiC crystals are well-known to withstand very high temperatures due to their characteristics. Hence, V_{th} (function of temperature) can easily decrease below zero as also supported with the analytical calculations of V_{th}.
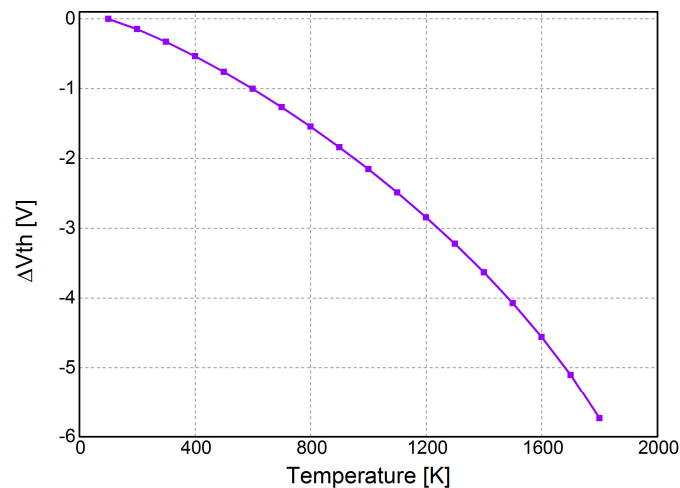
Figure 11. ΔV_{th} versus temperature.

6. Structural Characterization

An advanced infrared (IR) thermography technique, custom design as elaborated in [21], was used on bare die SiC power MOSFET in order to obtain the device's surface temperature during avalanche breakdown conduction phase of the UIS test. This setup features equivalent time sampling method with a frame rate capability of up to 1 MHz which allows acquisition of fast transient dynamics. It is also possible to capture the temperature distribution and thus the current distribution of the device at any time instance during the test using a single shot. The point of capture is chosen carefully to obtain the maximum surface temperature (found to be approximately at 33% of the t_{AV}). Integration time for the IR camera was set to 1 μs and two point calibration procedure was carried out to compensate for the emissivity contrast effect [22]. The surface temperature of the device reached (well above 500 °C) during the test surpassed the calibration range of the camera. So, the thermal images were post-processed to represent a normalized temperature (T_n) distribution (see Equation (19)):

$$T_n = \frac{T - T_0}{T_{max} - T_0} \tag{19}$$

where T_0 is the case temperature and T_{max} is the maximum temperature for the thermal map.

The current and voltage waveform for the UIS test (before and after failure) carried out on a bare die device from CREE are shown in Figure 12. In this test, the V_{DD} was kept the same as the tests on packaged devices (Section 3). The current is almost uniformly distributed for the safe avalanche event as depicted in Figure 13a. The I_{AV} was increased until failure was obtained. The thermal map corresponding to failure is included in Figure 13b. An interesting observation to be made here is the phenomena of localized current crowding taking place inside the device where most of the total current is drawn by a small number of cells in a small locality within the entire active device area. Due to current crowding phenomenon, formation of hot-spot takes place at the edge of the source pad (and the die border) eventually leading to failure. Formation of hot-spots have been also previously reported on Si devices [23].
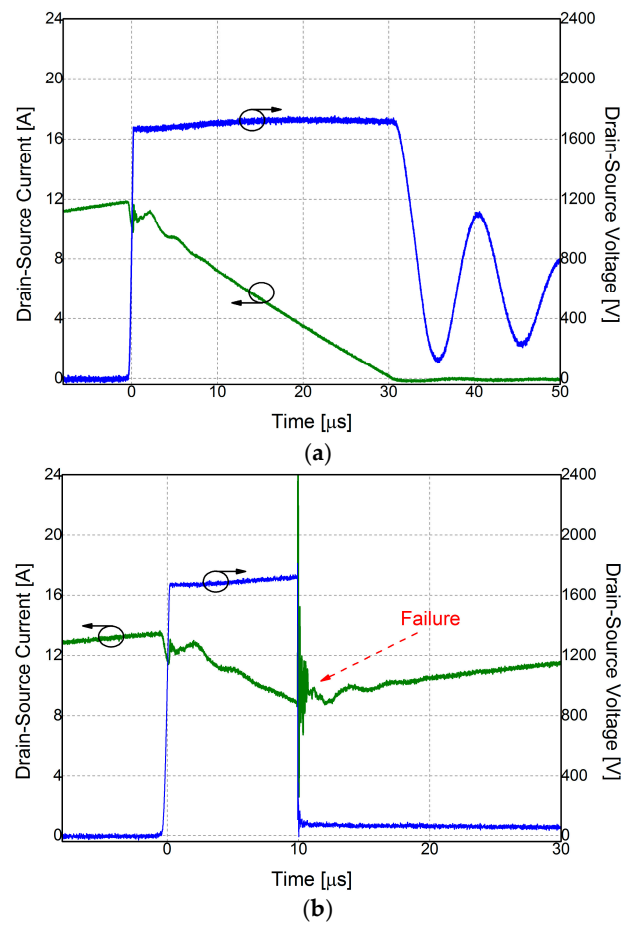
(a)

(b)

Figure 12. Experimental V_{DS} and I_D waveform for CREE (bare die)—V_{DD} = 400 V; T_{CASE} = 75 °C; L = 4600 μH. (**a**) Without Failure; I_0~12 A; (**b**) At Failure; I_0~14 A.
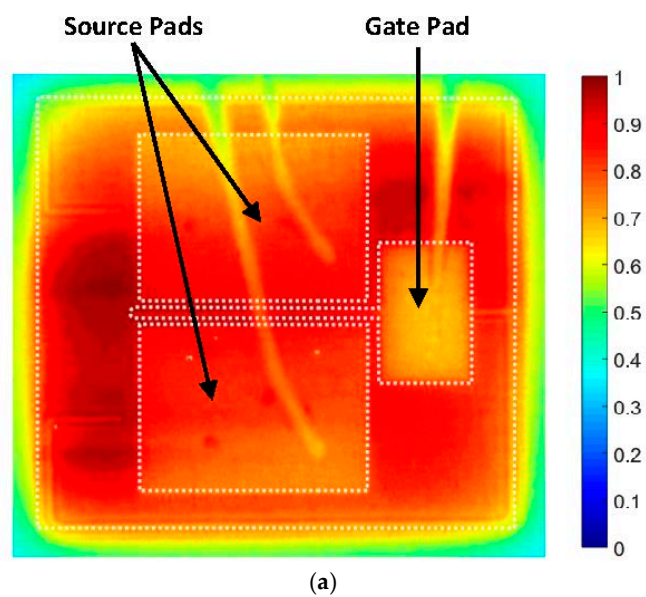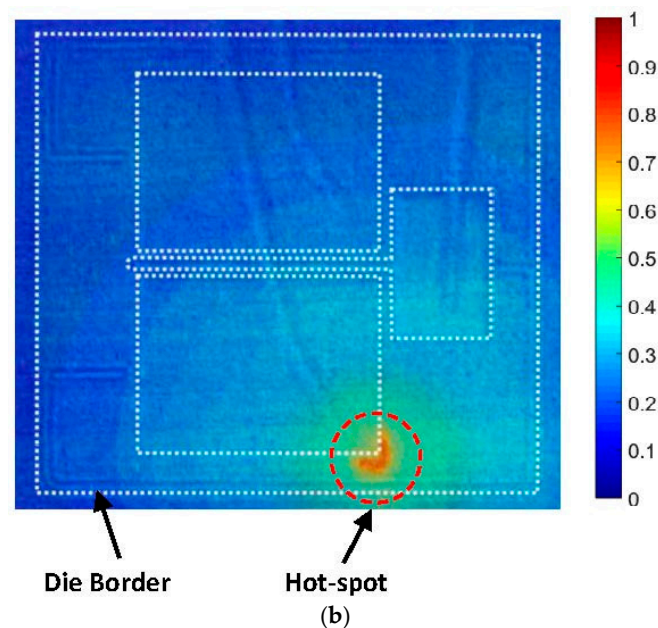

(a)

Figure 13. *Cont.*

Figure 13. Hot-spot formation on bare die SiC MOSFET; V_{DD} = 400 V; T_{CASE} = 75 °C; Normalized temperature scale. (**a**) Thermal map for $I_{AV}{\sim}12$ A; (**b**) Thermal map at failure; $I_{AV}{\sim}14$ A.

7. Conclusions

This paper presents a detailed investigation into the avalanche robustness of commercial avalanche rugged SiC power MOSFETs. SiC MOSFETs with 1200 V rating are available from various manufacturers. Experimental results show that these devices exhibit avalanche capability which is enhanced if the DUT is driven with negative V_{GS}. Simulations show V_{th} reduction with temperature increase leading to device failure which has been supported by V_{th} analytical calculations. The shift of V_{th} also takes place in Si typically at few mV/K (between −2 and −9 mV/K depending on temperature range). However, channel activation during UIS has never been reported in Si devices. The failure mechanism of Si MOSFETs is usually linked to activation of the parasitic BJT. Si MOSFETs can be turned-off with V_{GS} bias of −10 V to −15 V whereas SiC is limited in negative bias. Another point to be noted here is that the simulation investigates first-order effects but second-order effects have not been considered here. Also, the effect of field guard ring is also not taken into account. Finally, as clearly inferable from thermal map (Figure 13b), the eventual failure is still related to the presence of a hot-spot due to current crowding, suggesting that the final failure mechanism is still dominated by bipolar currents, whereas the channel activation only contributes to further increase temperature in some cells.

Author Contributions: Asad Fayyaz, Gianpaolo Romano and Alberto Castellazzi performed all the experimental results on packaged devices. Simulations results were carried out by Asad Fayyaz, Jesus Urresti and Gianpaolo Romano. The simulations results were reviewed and interpreted by Alberto Castellazzi, Andrea Irace and Nick Wright. The thermal mapping of bare die devices were performed by Asad Fayyaz, Gianpaolo Romano, Michele Riccio and Andrea Irace. Analytical calculations analysis for V_{th} was performed by Asad Fayyaz and Jesus Urresti. Finally, all authors contributed to the writing, reviewing and proofreading of the journal paper.

Conflicts of Interest: The authors declare no conflict of interest.

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