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A High-Power-Density Single-Phase Rectifier Based on Three-Level Neutral-Point Clamped Circuits

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Academic Editor: Jose Alves da Silva
Received: 19 March 2017; Accepted: 9 May 2017; Published: 16 May 2017

Abstract: A single-phase three-level converter is suitable for medium-power applications, with an interface voltage that is higher than that of a traditional two-level configuration. The three-level neutral-point clamped converter is adopted using four switches in each bridge arm, which, compared to a two-level rectifier, leads to less voltage stress, a lower switching frequency, and switching loss on switches. The transient current control strategy is designed to control the active power. The single-phase space vector pulse width modulation (SVPWM) with a voltage balance strategy is designed to solve the neutral point voltage fluctuation problem and keep the dc-link voltage stable. A 1.3 kW high-power-density prototype based on SiC MOSFET was built and tested. The experimental results verified the high performance of steady-state and dynamic responses.

Keywords: single-phase rectifier; three-level neutral-point clamped converter; SiC MOSFET; space vector pulse width modulation

1. Introduction

Due to the existence of non-linear loads such as uncontrolled rectifiers, the significant harmonics and reactive power will be generated and flow into the grid, which will reduce the grid power quality, influence power distribution, cause incorrect operation, and even damage electric apparatuses. A controlled rectifier can control the dc-link voltage stable at a constant value, and lower harmonics and lower total harmonic distortion (THD) exists on the grid side. A power electronic converter requires a high power density and a low harmonic. Several main topologies are found and designed in the industrial acceptance, and various multilevel converter topologies, including the three-level neutral point clamped converter (3L-NPC), modular multilevel converter, and cascaded H-bridge, are widely used in power applications [1,2].

The modulation of the converter becomes complicated when the output voltage of the converter increases [3,4]. However, the fluctuation of neutral point voltage in the 3L-NPC exists if no voltage balancing measures are taken. To solve the fluctuation, auxiliary circuits for balancing the multilevel converter neutral point voltage have been proposed in [5–7]. Auxiliary circuits can achieve a voltage balance, but additional hardware costs also arise. The authors of [8], to cancel the auxiliary circuits, used a balance strategy adjusting the duty time of the redundant vector to solve the fluctuation problem. Peng et al. [9] proposed a smooth switching technique to solve the fluctuation.

Along with the development of semiconductor technology, new Wide Band Gap (WBG) semiconductor devices such as SiC devices have gradually come into view [10–14]. SiC devices enjoy a higher bandgap energy, a higher critical electric field, a higher saturation velocity, and superior thermal conductivity directly in comparison with Si devices, which means SiC devices have lower

switching loss and no reverse recovery. Moreover, the great heat dissipation ability of SiC devices can withstand high voltages and high temperatures [15]. Thus, the volume of the power device can be greatly reduced and the efficiency of the system can be greatly improved.

In the traditional traction power supply system, the grid voltage needs to step down from the traction transformer first, and the AC voltage can then be rectified. In the cascade power electronic transformer, the grid voltage is applied directly to the cascade rectifier. The voltage stress of each switching device in two-level topology is larger than that in the three-level topology; it is necessary to adapt a three-level topology to efficaciously decrease voltage stress. Furthermore, SiC devices can withstand high voltage, so SiC MOSFETs are applied in the single-phase three-level topology, and the combination of SiC devices and three-level topology can effectively reduce the number of cascade rectifiers.

According to characteristics of the 3L-NPC and SiC devices, a high-power-density single-phase three-level PWM rectifier based on a SiC MOSFET prototype was designed. This system might work in the unity power factor with relatively high efficiency. This paper introduces the circuit configuration and the control algorithm of the three-level singe-phase rectifier. The performances of the designed rectifier were verified with simulations and experiments.

2. Configuration

The circuit configuration of the single-phase 3L-NPC rectifier is illustrated in Figure 1. It is composed of an input inductance Ls, SiC MOSFET with an anti-parallel diode, clamped diodes, a second-order harmonic filter module, and loads, and the two legs are defined as S_a and S_b. V_{dc1} and V_{dc2} represent the voltage of dc-link capacitors, C_1 and C_2, respectively. As is well known, each 3L-NPC arm can output three-level voltage, then the terminal voltage of an H-bridge circuits can output five-level waveform as shown in Figure 1b. The terminal voltage is divided into four sections: Section I: $V_{dc/2} < U_{AB} < V_{dc}$; Section II: $0 < U_{AB} < V_{dc/2}$; Section III: $-V_{dc/2} < U_{AB} < 0$; Section IV: $-V_{dc} < U_{AB} < V_{dc/2}$.

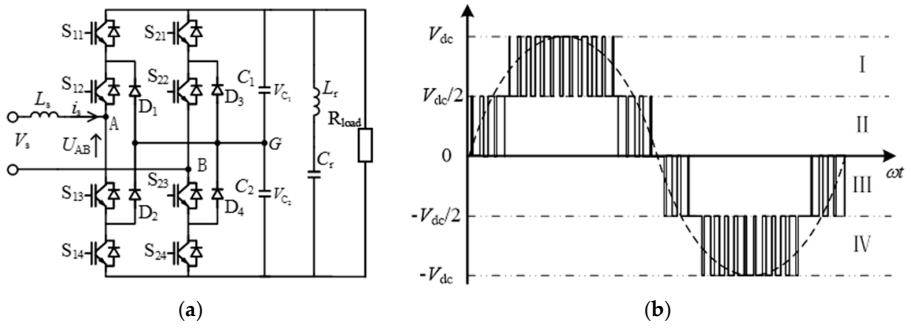

Figure 1. (**a**) Circuit configuration of 3L-NPC; (**b**) five-level waveform of terminal voltage.

According to the circuit operation of Figure 1a, the 3L-NPC converter has nine switching states as illustrated in Figure 2a–i. Assuming that the voltage balance strategy operates properly, the details of each state are summarized as follows.

(a) State 1: Switches S_{11}, S_{12}, S_{21}, and S_{22} are on, while the others are off. The input voltage U_{AB} is zero, and input has no effect on C_1 or C_2. When $i_s > 0$, the current passes through the parallel diode of S_{11} and S_{12} first, and then passes through the S_{21} and S_{22}. When $i_s < 0$, the current passes through the parallel diode of S_{21} and S_{22} first, and then passes through the S_{11} and S_{12}.

(b) State 2: Switches S_{11}, S_{12}, S_{22}, and S_{23} are on, while the others are off. The input voltage U_{AB} is V_{C1}, and C_1 is charged when $i_s > 0$ and discharged when $i_s < 0$, while input has no effect on C_2.

(c) State 3: Switches S_{11}, S_{12}, S_{23}, and S_{24} are on, while the others are off. The input voltage U_{AB} is $V_{C1} + V_{C2}$, and C_1 and C_2 are charged when $i_s > 0$ and discharged when $i_s < 0$.

(d) State 4: Switches S_{12}, S_{13}, S_{21}, and S_{22} are on, while the others are off. The input voltage U_{AB} is $-V_{C1}$, and C_1 is discharged when $i_s > 0$ and charged when $i_s < 0$, while input has no effect on C_2.

(e) State 5: Switches S_{12}, S_{13}, S_{22}, and S_{23} are on, while the others are off. The input voltage U_{AB} is zero, and input has no effect on C_1 or C_2.

(f) State 6: Switches S_{12}, S_{13}, S_{23}, and S_{24} are on, while the others are off. The input voltage U_{AB} is V_{C2}, and C_2 is charged when $i_s > 0$ and discharged when $i_s < 0$, while input has no effect on C_1.

(g) State 7: Switches S_{13}, S_{14}, S_{21}, and S_{22} are on, while the others are off. The input voltage U_{AB} is $-V_{C1}$-V_{C2}, and C_1 and C_2 are discharged when $i_s > 0$ and charged when $i_s < 0$.

(h) State 8: Switches S_{13}, S_{14}, S_{22}, and S_{23} are on, while the others are off. The input voltage U_{AB} is $-V_{C2}$, and C_2 is discharged when $i_s > 0$ and charged when $i_s < 0$, while input has no effect on C_1.

(i) State 9: Switches S_{13}, S_{14}, S_{23}, and S_{24} are on, while the others are off. The input voltage U_{AB} is zero, and input has no effect on C_1 or C_2.

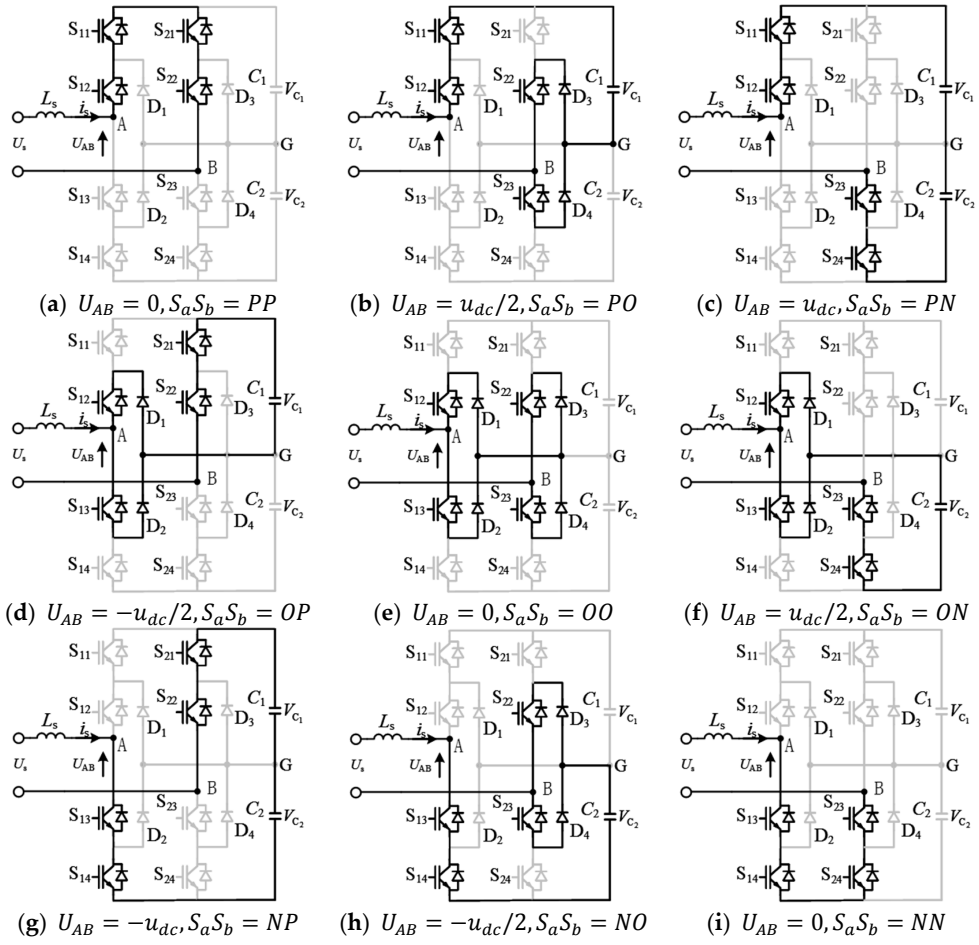

Figure 2. (**a**–**i**) The nine switching states of the single-phase three-level rectifier.

The definition of P is that the two switches of the bridge arm S_i (i = 1, 2)—S_{i1} and S_{i2}—are on, the definition of O is that S_{i2} and S_{i3} are on, and the definition of N is that S_{i3} and S_{i4} are on.

The effect of each state on the two capacitor voltages was analyzed based on nine switching states, and the situation where the grid current $i_s > 0$ is taken as an example, as shown in Table 1. State PO charges Capacitor C_1 only while State PO has no effect on Capacitor C_2, State OP discharges Capacitor C_1 only while State OP has no effect on Capacitor C_2, State ON charges Capacitor C_2 only while State ON has no effect on Capacitor C_1, and State NO charges Capacitor C_2 only while State NO has no

effect on Capacitor C_1. All four of these switching states cause fluctuation of the neutral point voltage. The solution of the fluctuation is discussed in the next section.

Table 1. Switch state and effect on two capacitors. ↑: charge; ↓ : discharge; ↔ : no effect; Z: zero vector; SP: small positive vector; LP: large positive vector; SN: small negative vector; LN: large negative vector.

State	S_a	S_b	U_{AB}	V_{c1}	V_{c2}	Vector Categories
1	P	P	0	↔	↔	Z
2	P	O	V_{c1}	↑	↔	SP
3	P	N	$V_{c1} + V_{c2}$	↑	↑	LP
4	O	P	$-V_{c1}$	↓	↔	SN
5	O	O	0	↔	↔	Z
6	O	N	V_{c2}	↔	↑	SP
7	N	P	$-V_{c1} - V_{c2}$	↓	↓	LN
8	N	O	$-V_{c2}$	↔	↓	SN
9	N	N	0	↔	↔	Z

3. Control Algorithm and Modulation

The configuration of the control system is shown in Figure 3a. The transient current control strategy utilizes the grid current i_s, the input voltage u_s, the dc-link voltage u_{dc}, and the dc-link current i_{dc} to generate the modulation signal U_{AB}. The redundant vector select strategy and SVPWM methods use U_{AB} and the voltages of two capacitors to generate switch signals.

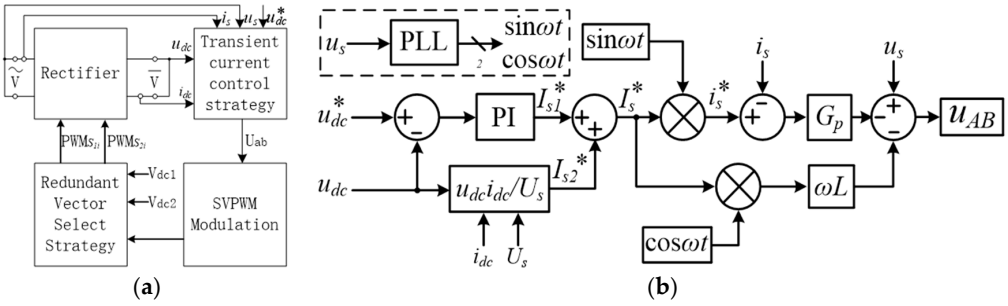

Figure 3. (**a**) Control algorithm; (**b**) transient current control strategy.

3.1. Transient Current Control Strategy

The transient current control diagram is shown in Figure 3b, where u_{dc}^* and u_{dc} are the reference and actual value of the dc-link voltage, and G_p is the gain constant. The phase-locked loop (PLL) is a phase lock procedure, which detects the phase of input voltage.

The voltage control part utilizes a standard PI (Proportional Integral) controller to maintain the dc-link voltage, which should be stable and equal to the reference. When $u_{dc}^* - u_{dc} > 0$, the input current will increase and input power will raise, as shown in Equation (1), so the change in power required is shown by the output of the PI controller, that is, the given value of I_s.

$$I_{s1}^* = K_p(u_{dc}^* - u_{dc}) + K_i/T \int (u_{dc}^* - u_{dc})dt. \quad (1)$$

In order to improve the dynamic characteristics of the PI controller, load current feed-forward control is adopted as in Equation (2), the effective component of a given current is calculated by the input voltage, the dc-link voltage, and the current. The amplitude of the grid current consists of a feed-forward controller output of Equation (2) and the PI controller output of Equation (1), where the feed-forward output is

$$I_{s2}^* = u_{dc} i_{dc} / U_s. \quad (2)$$

Then, the instantons current reference is accumulated as

$$I_s^* = I_{s1}^* + I_{s2}^*. \tag{3}$$

The current control part has a fast response ability. As shown in Equation (4), u_{AB} and u_L compose the u_S, Δi guarantees that the actual current i_s tracks the reference current I_s^* in real-time, and the output is the instruction value of modulation signal u_{AB}.

$$\begin{cases} u_{AB} = u_s - u_L - \Delta i \\ u_L = \omega L_s I_s^* \cos \omega t \\ \Delta i = G_p(I_s^* \sin \omega t - i_s) \end{cases}. \tag{4}$$

3.2. Space Vector Pulse Width Modulation

To choose the proper switching states for the 3L-NPC, the single-phase three-level space vector diagram is divided into four sections. The two voltage vectors are selected to synthesize V_{ref} according to the section in which it is located. As shown in Figure 4a, assuming $U_{AB} = MU_d \cos \omega t$, the voltage U_{AB} is the projection of the vector V_{ref} on the α-axis, and the length of the vector $\left|V_{ref}\right| = MU_d$. The vector is rotated counterclockwise at the angular frequency ω, where M in the range of 0–1 is the modulation ratio.

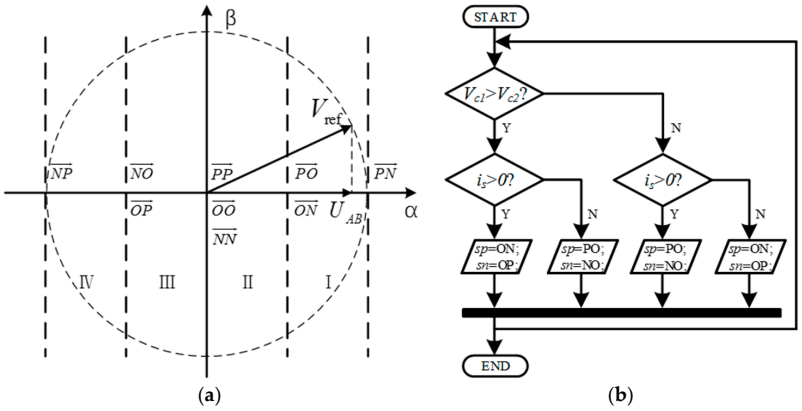

Figure 4. (**a**) SVPWM reference voltage; (**b**) redundant vector selection procedure.

The reference voltage is synthesized by two adjacent vectors. The vector with fewer levels is defined as a small vector V_{min}, and the vector with a large number of levels is defined as a big vector V_{max}. The two adjacent switching state vectors are selected to calculate on-durations via Equation (5) under the volt-second balance principle.

$$\begin{cases} U_{AB}T_S = V_{min}T_1 + V_{max}T_2 \\ T_S = T_1 + T_2 \end{cases}. \tag{5}$$

U_{AB} is the reference voltage of the modulation wave, T_S is the period of the carrier, T_1 is the operational time of V_{min}, T_2 is the operational time of V_{max}.

$$\begin{cases} T_1 = \frac{U_{AB} - V_{max}}{V_{min} - V_{max}} T_S \\ T_2 = T_S - \frac{U_{AB} - V_{max}}{V_{min} - V_{max}} T_S \end{cases}. \tag{6}$$

As shown above in Table 1, the large vector and zero vector will not cause dc-link capacitor voltage unbalance; however, the small vector causes a fluctuation of neutral point voltage. When the small vector is working, one of the two capacitors is charged or discharged, while the other maintains

the same voltage. The small positive vector *PO*(*ON*) and small negative vector *OP*(*NO*) have opposite effects on the neutral point voltage, so the control of the neutral point voltage can be achieved by choosing a redundant vector.

To analyze the direction of the current flowing through the capacitor, a strategy for solving the fluctuation of the neutral point voltage by using different redundant vectors is shown in Table 2 and Figure 4b. According to the capacitor voltage and grid current, there are four kinds of redundant switch state selections. When none of the redundant vectors are working and the terminal voltage is $0.5U_d$, the strategy can choose between States PO and ON(*sp*). Similarly, when terminal voltage is $-0.5U_d$, the strategy can choose between States OP and NO(*sn*). The result of choosing redundant vectors will be put into a register *sp*(*sn*), and the state of the register will be sent to synthesize the switching state finally. When any one of those four redundant vectors is working, the state of register *sp*(*sn*) remains unchanged. For example, in Figure 4b, when the system starts to work, $V_{dc1} > V_{dc2}$ and $i_s > 0$; if the terminal voltage is $0.5U_d$, then sp will be ON; if the terminal voltage is $-0.5U_d$, the sn will be OP.

Table 2. Redundant vector selection.

Terminal Voltage	Relation	Current Direction	Vector Selected	Result
$0.5U_d$	$V_{c1} > V_{c2}$	A→B	$\vec{ON}$	$V_{c1} \downarrow$
		B→A	$\vec{PO}$	$V_{c2} \uparrow$
	$V_{c1} < V_{c2}$	A→B	$\vec{PO}$	$V_{c1} \uparrow$
		B→A	$\vec{ON}$	$V_{c2} \downarrow$
$-0.5U_d$	$V_{c1} > V_{c2}$	A→B	$\vec{OP}$	$V_{c1} \downarrow$
		B→A	$\vec{NO}$	$V_{c2} \uparrow$
	$V_{c1} < V_{c2}$	A→B	$\vec{NO}$	$V_{c1} \uparrow$
		B→A	$\vec{OP}$	$V_{c2} \downarrow$

4. Simulation

In order to verify the system's control strategy adopted above, a 3L-NPC single-phase rectifier shown in Figure 1 is used to conduct a simulation by MATLAB/SIMULINK in this paper, and the simulation parameters are listed in Table 3.

Table 3. System and control parameters.

Parameters	Values
Input AC Voltage	115 V–264 V
Input Current	15 A (Max)
Input AC Voltage Frequency	47 Hz–63 Hz
Output DC Voltage	400 V
Output Power	1.3 kW (Max)
Power Density	0.56 W/cm^3
The Inductance of Input Side	0.4 mH
Filter Circuit	3 mF/0.84 mH
Switching Frequency	30 kHz

The dynamic response of the system is shown in Figure 5. when load is on or off, output voltage recovers to 400 V within 0.15 s. Input voltage and current is in the same phase; that is, the power factor of the system is close to 1. The bottom of Figure 5 is the terminal voltage. As mentioned earlier, the voltage of two dc-side capacitances, if not controlled, would be unbalanced, which in turn would increase the harmonic component in the output voltage and increase the voltage applied on the power switch transistor, even damage the device or dc-side capacitor. Figure 6 shows the changes in

the voltage of the two capacitors. There is no voltage equalizing strategy during the 0–0.3 s period, the maximum value of voltage difference between the two capacitors reached 400 V, and after 0.3 s, the voltage difference gradually disappeared as a voltage equalizing strategy is adopted.

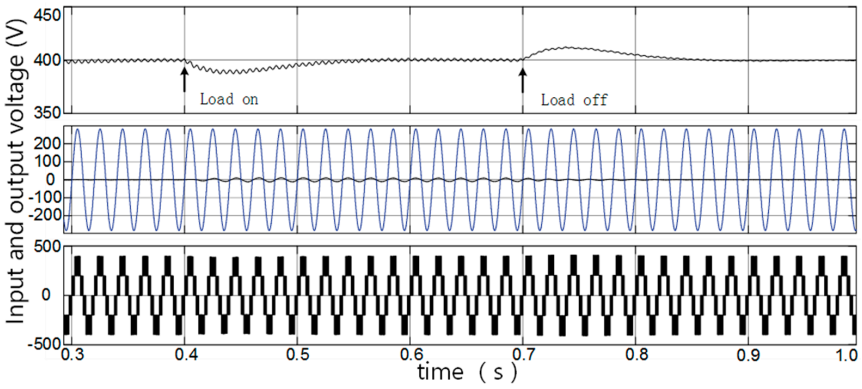

Figure 5. DC-link voltage, input voltage, and current and terminal voltage.

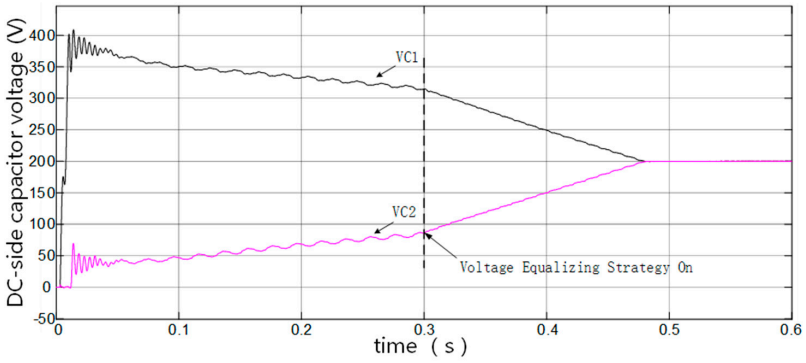

Figure 6. The DC capacitors voltages with and without equalization control.

5. Experiment Results

5.1. Prototype

In order to realize the target mentioned above, which includes a control algorithm and high power density, an experimental prototype of the single-phase three-level rectifier was developed. The system is shown in Figure 7. It is divided into three parts. The first part consists of two SiC MOSFET bridge arms and a drive circuit. The drive circuit is designed to drive SiC MOSFET stably. The second part consists of an input inductor, an EMI filter, a voltage sensor and a current sensor, a relay, and a secondary filter. The input inductor is designed to filter the grid voltage harmonic and store power. The EMI filter is designed to filter out high frequency noise and interference signals contained in the grid while keeping electromagnetic radiation generated by the system from leaking to the grid. The input voltage (u_s), grid current (i_s), and dc-link voltage (u_d) are detected by sensors as the feedback. Each state of the system is transformed precisely through the switching of the relay. The third part is the FPGA control board, which is designed to control the whole system.

We also have protection methods in our program. If the input voltage u_s or grid current i_s are higher or lower than the expected value limits, the output voltage is not in the setting limits, and the system would be shut down in case heat issues or hazards occur.

The configuration of the control system is shown in Figure 3a. All control algorithms are implemented by Verilog-HDL (Hardware Description Language), one of the universal IEEE industry

standard hardware description languages used to describe digital systems and design hardware realization using code methods.

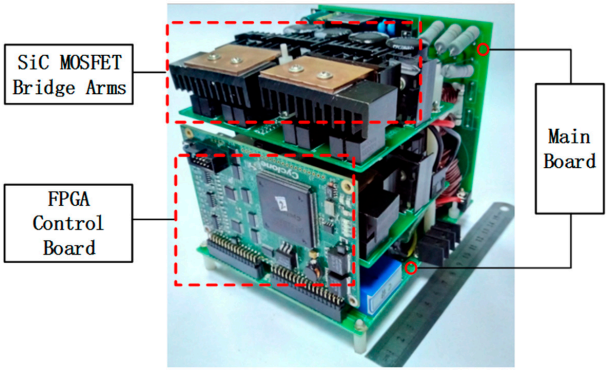

Figure 7. Prototype of the system.

5.2. Experiment Results

In Figure 8a, the dc-link voltage (u_{dc}), terminal voltage (U_{AB}), input voltage (u_s), and grid current (i_s) are illustrated. u_{dc} is stable at 400 V, and u_s and i_s are in the same phase, so the rectifier works within unity-power factor limits. The waveform of i_s presents a low THD in the condition of full load (1.3 kW). Figure 8b presents the ripple of the output voltage, which is lower than 3 V. Figure 8c exhibits the dc-link voltage (u_{dc}), input voltage (u_s), and grid current (i_s) when load step changes happen, the u_{dc} recovers to the reference voltage within 0.8 s after the load step changes. Figure 8d shows that the input voltage (u_s) and grid current (i_s) recover to sinusoidal waveforms immediately after the load step changes. All these experiments illustrate that the system has high dynamic responses.

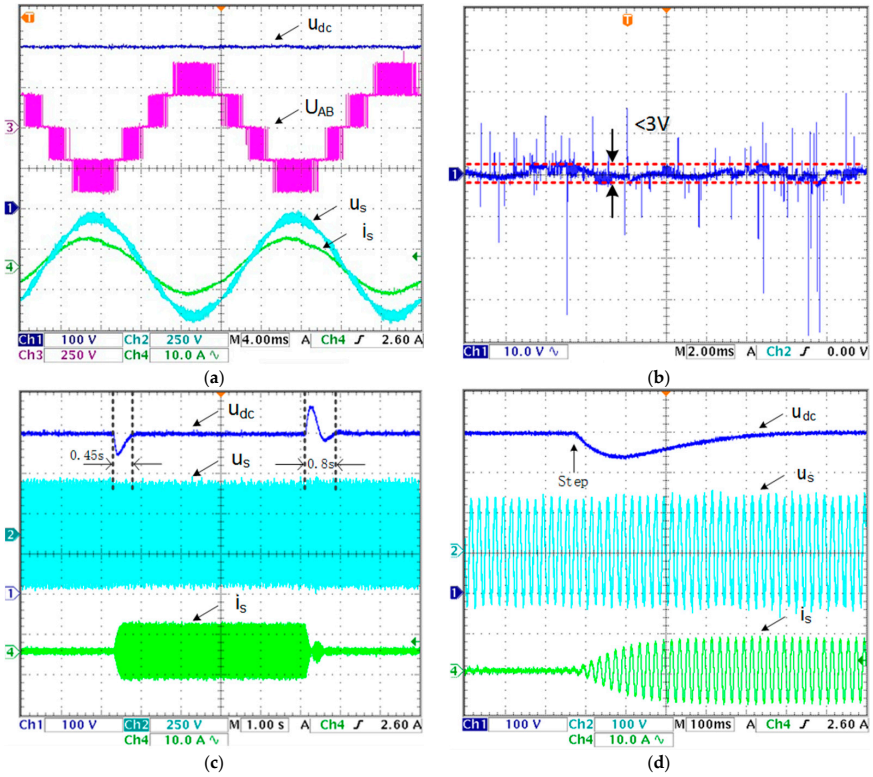

Figure 8. Experiment results. (**a**) State–state waveforms; (**b**) output voltage ripple; (**c**) dynamic waveforms with and without load; (**d**) detail waveforms at load step change.

Figure 9a shows the changes in the power factor (PF) and the efficiency when the rectifier works at two different input voltages (115 V/60 Hz and 230 V/60 Hz). In the first case (115 V/60 Hz), the PF reaches 0.995 at the 30% load. Then, the PF increases gradually as the load increases. The PF comes to the maximum (nearly 0.999) when the rectifier is under full load. As for the efficiency, the PF starts at 94.5% under 30% load, then it declines slightly to the 93.5% with 50% load. After that, the efficiency keeps relatively steady until the load increases to 70%. However, it falls dramatically as the load rises. The efficiency achieves the lowest point at the full load. In the second case (230 V/60 Hz), the PF goes up from 0.965 to 0.993 as the PF of the first case, and the efficiency fluctuates between 0.963 and 0.972 through the process of load changing. Generally, PF increases as the load of the rectifier increases and the PF retains a high value. The efficiency ranges from 0.92 to 0.972, which indicates the efficiency has no strong correspondence with the load changes.

The experiment test has been done under the same power level (1.3 kW), and the result is shown in Figure 9b. The PF drops from 0.999 to 0.99 when the input voltage increases from 115 V to 264 V, which coincides with Figure 9a. As the input voltage gains, the input current decreases correspondingly. As for the THD, the PF starts at 1.7% with a 115 V input voltage. Then, it drops drastically to 1.4% when the input voltage is 120 V. Afterwards, the THD increases to 2.7% when the input voltage increases to 264 V. In terms of the efficiency, the PF begins at 0.92, and then improves sharply to 0.965 when the input voltage reaches 200 V. After the light rolling of the efficiency between 200 and 240 V, a slight drop appears at 264 V input voltage.

Moreover, a comparison experiment between the Si device and the SiC device is developed, and the operation frequency of Si IGBT is 3 kHz, while the operation frequency of SiC MOSFET is 30 kHz. The experiment result is shown in Figure 9c,d. The ITHD of the SiC system is lower than the Si system at the same input voltage with an increased switching frequency, and the PF of the SiC system is higher than that of the Si system and almost close to 1 in different input voltage conditions.

The experiments and the test above verify that the SiC MOSFET single-phase three level rectifier can work with a high efficiency, a low THD, and a unity power factor.

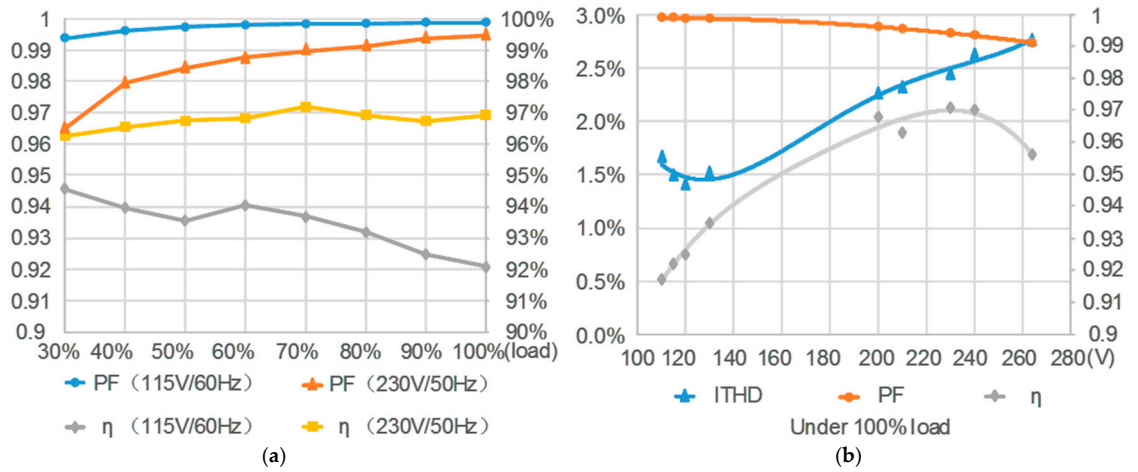

Figure 9. *Cont.*

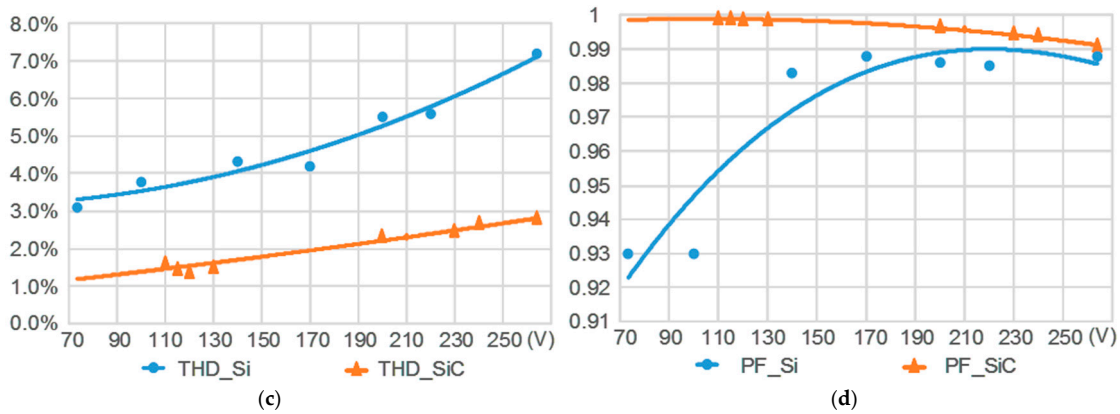

Figure 9. Experimental statistics: (**a**) power factor and efficiency; (**b**) THD, power factor, and efficiency with 100% load; (**c**) THD comparison between Si and SiC devices; (**d**) PF comparison between Si and SiC devices.

6. Conclusions

A high-power-density single-phase 3L-NPC rectifier was built. Its size is shown in Figure 7, and the power density is relatively high. Through the adoption of a transient current control strategy, the SVPWM method, and a redundant vector selection strategy, the goal of a stable dc-link voltage, a high power factor, a low THD, and a relatively high efficiency is achieved. The dynamic characteristics of the system were tested, and the system was found to have a high dynamic response. The grid voltage and current quickly adjust to recover sinusoidal waveforms. The superior advantages of SiC MOSFET in breakdown voltage, heat conductivity, and high temperature compared to Si MOSFET are reflected in the high efficiency of the 3L-NPC rectifier built here.

Acknowledgments: This work was supported by the National Natural Science Foundation of China (Grant Nos. 51377004 and 51477144).

Author Contributions: Tao Zhou and Zeliang Shu designed the control algorithm, the controller, and the main circuits; Tao Zhou, Deng Luo, Xiaoxiao Guo, and Yajun Chen designed the prototype and achieved the experiments; Hongjian Lin analyzed the data.

Conflicts of Interest: The authors declare no conflict of interest.

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