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A Modular Multilevel Converter with Power Mismatch Control for Grid-Connected Photovoltaic Systems

Turgay Duman *, Shilpa Marti, M. A. Moonem, Azas Ahmed Rifath Abdul Kader and Hariharan Krishnaswami

Department of Electrical and Computer Engineering, The University of Texas at San Antonio, One UTSA Circle, San Antonio, TX 78249, USA; shilpa.marti@utsa.edu (S.M.); m.a.moonem@gmail.com (M.A.M.); mailmerifath@gmail.com (A.A.R.A.K.); hariharan.krishnaswami@utsa.edu (H.K.)

* Correspondence: turgay.duman@utsa.edu; Tel.: +1-210-452-4165

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Abstract: A modular multilevel power converter configuration for grid connected photovoltaic (PV) systems is proposed. The converter configuration replaces the conventional bulky line frequency transformer with several high frequency transformers, potentially reducing the balance of systems cost of PV systems. The front-end converter for each port is a neutral-point diode clamped (NPC) multi-level dc-dc dual-active bridge (ML-DAB) which allows maximum power point tracking (MPPT). The integrated high frequency transformer provides the galvanic isolation between the PV and grid side and also steps up the low dc voltage from PV source. Following the ML-DAB stage, in each port, is a NPC inverter. *N* number of NPC inverters' outputs are cascaded to attain the per-phase line-to-neutral voltage to connect directly to the distribution grid (i.e., 13.8 kV). The cascaded NPC (CNPC) inverters have the inherent advantage of using lower rated devices, smaller filters and low total harmonic distortion required for PV grid interconnection. The proposed converter system is modular, scalable, and serviceable with zero downtime with lower foot print and lower overall cost. A novel voltage balance control at each module based on power mismatch among *N*-ports, have been presented and verified in simulation. Analysis and simulation results are presented for the *N*-port converter. The converter performance has also been verified on a hardware prototype.

Keywords: dual active bridge; maximum power point tracking (MPPT); multilevel; neutral-point clamped; utility scale photovoltaic (PV) system

1. Introduction

Grid-connected large-scale photovoltaic (PV) systems have to consider challenges such as energy yield, power conversion efficiency, power density, reliability and cost which includes solar panels, power electronics and balance of systems (BOS) cost. Utility scale PV plants use single or multiple centralized inverters rated from 500 kW or higher to output power at a three phase voltage level of 480 V or less. Some megawatt (MW) scale PV inverters are designed for a higher input dc voltages such as 2500 V [1] in order to reduce the dc BOS cost and increase efficiency up to 99.5% [1,2]. Large PV plants still rely on line frequency (i.e., 50 or 60 Hz) transformers because of its high efficiency to isolate and step-up the inverter's output voltage to the distribution voltage level of 11 to 13 kV for interconnection with the utility grid. In the MW power range, transformer cost is more than one-third of the inverter cost and occupies close to one-third of the footprint of a 1 MW inverter station. A price comparison has been shown in a report prepared by the U.S. Idaho National Laboratory in May 2012 [3] and these prices may vary widely depending on market fluctuations, manufacturer, windings

material, features, etc. The average cost of a 500 kVA GE transformer operating at 60% load with a power factor of 0.85 is 11.92 ¢/watt for 99% efficiency [3]. The total cost including transportation, installation, other transformer related balance of system costs and regular maintenance cost make this ¢/watt estimate more than twice of the transformer price. A 500 kVA 12 kV/400 V 60 Hz transformer weighs roughly 1~2.5 tons based on the type and manufacturing material which is a concern for transportation and installation. The proposed *N*-port converter uses smaller and lightweight medium frequency transformers integrated within the dc-dc converter at each identical port.

Research has been going on to eliminate the bulky line frequency transformers at the grid interface using different converter topologies and configurations [4–8]. Various topologies, standards and evolution of PV converters are reviewed in literature [4,9,10]. Optimum choice in topology, components and operating parameters can increase energy injected into the grid by 9–15% and lowering the levelized cost of energy (LCOE) up to 17% for grid connected PV system [11]. One of the major challenges in achieving medium or high voltage in a PV converter is the limitation of switching device (i.e., IGBT, Diode) and associated components' voltage handling capability. A 15 kV silicon-carbide (SiC) switching device performance is reported in [12] and up to 6.5 kV IGBTs are commercially available. Multilevel topologies can overcome shortcomings in solid-state switching device ratings so that they can be applied to higher voltage systems, and additionally they provide low total harmonic distortion (THD) and lower dv/dt. Commonly used multilevel topologies are neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB). NPC topology is an effective way to eliminate the leakage current for transformer-less PV inverters [13]. CHB offers the flexibility in choosing the number of modules to be cascaded based on the voltage and power requirement. In the proposed topology *N*-nos. of phase-shifted NPC inverters are cascaded at the output of each port to yield the desired voltage level. This cascaded NPC (CNPC) topology provides $(4N + 1)$ levels at the cascaded output voltage where the CHB provides $(2N + 1)$ levels for *N* cascaded ports which is advantageous in terms for lower dv/dt and lower device voltage ratings in comparison to the CHB topology.

Modular multilevel converter (MMC or M^2LC or M^2C) topology has been proposed in [14] and it is used in a 26.5 kV 36 MW grid intertie system. For PV applications modularity at the input side with two stage power conversion is advantageous as shown in a study on a commercially available large-scale PV inverter that replaces the PV side dc combiners with dc-dc converters at string-level along with maximum power point tracking (MPPT) which increases the energy yield by 34–46% in comparison to a single central inverter for certain shading conditions [15]. A multilevel-multistring configuration with CHB topology has been proposed in [16] which increases the PV system capacity and improves the power quality. A 3 MW 12 kV modular CHB for grid-connected PV system is proposed in [17] where the dc-dc conversion stage is a two-level dual active bridge (DAB) and multiple of such dc outputs are added to feed an inverter module in the cascade. In [18] a common high-frequency link transformer is used to isolate the cascaded inverter modules which also minimizes the voltage imbalance and common mode issue. A multi-port multi-level topology for PV application has been proposed in [8] where the dc-ac stage uses four-quadrant switches instead of dc-dc and dc-ac conversion stages. In terms of the number of semiconductor switches used in dc-ac converter, this is the same as separate dc-dc and dc-ac converters. In [19,20], 15 kV SiC IGBTs have been used instead of cascading to reach higher voltages. The high voltage, however, poses several challenges in handling high dv/dt parasitic at high frequencies and THD requirement for PV-grid interconnection. A high-frequency-link based grid-tied PV system is proposed in [21]. The innovations are in the small dc bus link capacitor thereby improving the reliability of the system by replacing electrolytic capacitors with film capacitors. Capacitor voltage unbalance among different modules is a common issue for CHB inverter topology. Various control algorithms have been discussed in literature to address these voltage and power balancing issues [17,22–25].

The state-of-the art utility scale PV power converters continue to address size and cost challenges through modularity and innovative. Specifically, in this paper an *N*-port power electronic converter

architecture with integrated high-frequency transformer is presented, which eliminates the line frequency transformer and reduces the overall cost for grid-connected PV plants. The proposed architecture is modular from the PV source up to the grid before cascading and each module consists of a dc-dc and a dc-ac power conversion stage. MPPT control is decoupled from the voltage and power balance control. MPPT is performed at the front end dc-dc multilevel DAB (ML-DAB) stage using the phase-shift control. The ML-DAB also independently controls any voltage mismatch between two clamping capacitors used in the NPC bridge as the dc-link. This ML-DAB not only provides isolation between PV and grid side, it also boosts up the PV side dc voltage for the next inverter stage. The proposed dc-dc three-level NPC DAB stage allows one to synthesize the same number of voltage levels at the high voltage bridge of ML-DAB that can be produced using two cascaded two-level conventional DABs, so the ML-DAB is saving one high frequency transformer in comparison with two cascaded H-bridges while performing the same voltage step-up operation similar to two CHBs. The *N*-port converter allows for a direct medium-voltage (e.g., 13.8 kV) interconnection without the need of a bulky line frequency transformer. Modularity provides serviceability with zero downtime. Presented design is also highly scalable. Despite medium to high voltages, the converter can be realized by lower voltage rated devices. Due to the cascaded multilevel configuration at the ac output stage, the *N*-port converter has the inherent advantage of low THD required for PV grid interconnection. The building blocks of the proposed *N*-port converter are shown in Section 2. A study on cost-effectiveness of proposed *N*-port in comparison to a standard 1 MW PV power system having central inverter has also been shown in Section 2. MPPT, voltage balancing control of clamping capacitors at the inverter input and power mismatch control among different ports are described in Section 3. Section 4 consists of simulation and experimental results.

2. Proposed *N*-Port Converter Architecture

The proposed *N*-port converter architecture is shown in Figure 1. The *N*-port converter consists of *N* numbers of modular dc-dc and dc-ac power conversion stages in between PV and grid interface. Each port includes a dc-dc multilevel dual active bridge (ML-DAB) converter followed by a NPC inverter. The high voltage bridge of the dc-dc ML-DAB has a three-level NPC configuration which is connected in a back-to-back manner with the NPC inverter having the common neutral point "o" as shown in Figure 2. The PV dc voltage is stepped up in two stages, first in the dc-dc ML-DAB stage and then in the NPC inverter stage by cascading which yields the overall voltage up to 13.8 kV three-phase line-to-line rms. Each ML-DAB supplies a three-level NPC-bridge inverter and all the *N* inverters are cascaded to produce a single-phase line-to-neutral voltage of 7.96 kV (Figure 2). The following sub-sections describe the building blocks of this *N*-port converter in detail.

2.1. dc-dc Power Conversion Stage

Various transformer-less and transformer-isolated dc-dc power conversion topologies have been proposed for grid-connected PV applications [4,16,26]. In the proposed topology, ML-DAB is the first power conversion stage that boosts up the dc voltage obtained from the PV array and also provides isolation between PV and the grid. The concept of DAB was initially proposed in [27]. Since then DAB is being used for transformer isolated dc-dc conversion in medium and high power applications. In the conventional two-level DAB, two active bridges across a high frequency transformer produce two square waves which are phase-shifted to control the power flow. On the advances in DAB, [28] proposes a semi-dual active bridge (S-DAB) dc-dc converter for unidirectional power flow (e.g., PV application) where the load-side bridge has two switches and two diodes instead of four active switches used in conventional DAB. Operating principle and characteristic advantages are similar to conventional DAB but the S-DAB lacks a multilevel topology (e.g., a NPC stage) suitable for medium or high-voltage applications. The proposed ML-DAB topology for the *N*-port converter (Figure 2.) consists of the PV side primary bridge (switches S_1 to S_4) which produces a two-level square wave v_{AB} and the secondary bridge which is composed of two 3-level (3L) neutral point clamped (NPC) legs

produces a leg-to-leg 5-level (5L) V_{AB} staircase waveform as shown in Figure 3. Conventionally, NPC legs are used in multi-level inverter applications. In the proposed ML-DAB application, each of the switches in the NPC bridge (S_{a1} to S_{a4} and S_{b1} to S_{b4}) is subjected to a maximum voltage stress of $V_p/2$ while the five-level voltage V_{ab} across the transformer has maximum peak voltage V_p.

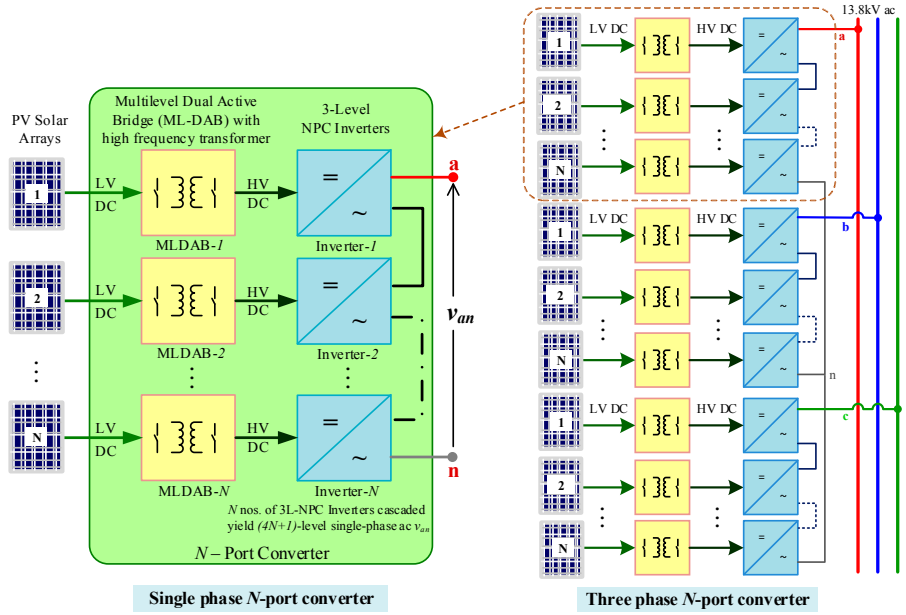

Figure 1. Block-diagram of proposed *N*-port converter for grid-connected PV system.

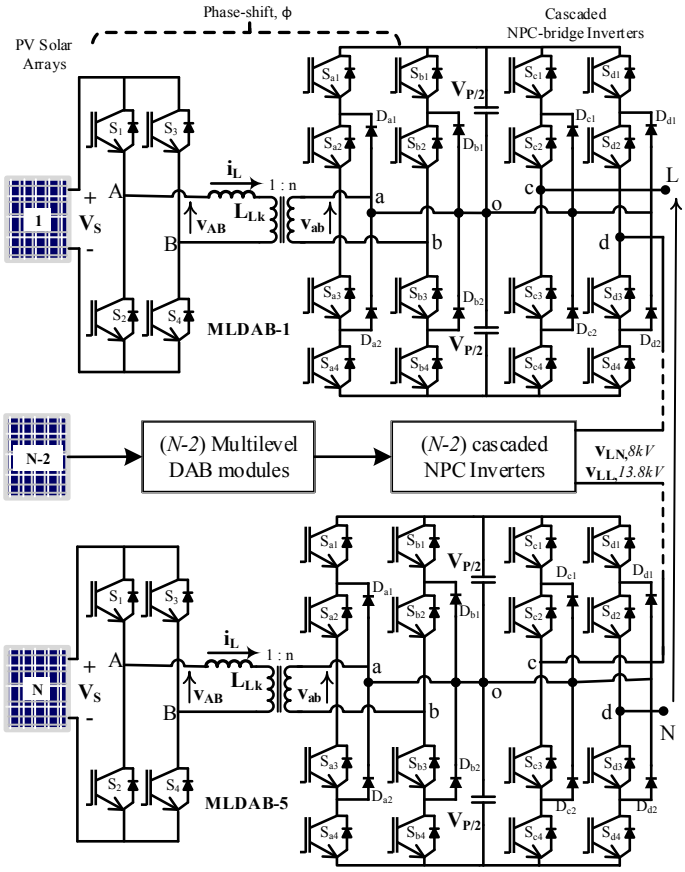

Figure 2. Schematic of the proposed single-phase *N*-port PV converter.

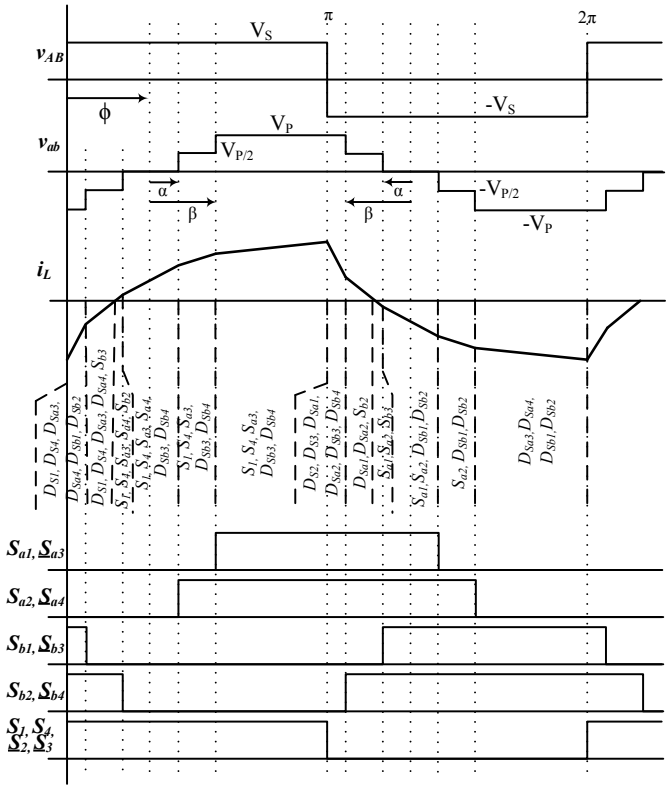

Figure 3. Key waveforms at the dc-dc ML-DAB stage.

In order to synthesize the 5L voltage v_{ab}, switching pulses and resulting voltage waveforms are defined with respect to angular distances (i.e., α,β) instead of the duty cycle. These angles α,β are measured symmetrically at zero, π and 2π within a switching period (Figure 3). The zero and π are considered at the mid-point of the zero voltage level of the 5L voltage v_{ab}. Defining v_{ab} in such a symmetrical way is advantageous in terms of the minimum number of parameters (α, β) required. This provides a straightforward method for derivation of a simple mathematical expression for power flow in the ML-DAB [29]. Parameters α and β shape the multilevel voltage waveform and are used in voltage balancing of the clamping capacitors. The phase-shift angle ϕ is independent of α, β and acts as the control parameter to control the power flow in the ML-DAB.

The novelty of such an NPC based ML-DAB is that it can handle a higher output dc voltage (V_p) due to the multilevel topology which reduces both the voltage stress on switches and the dv/dt. The 5L voltage waveform (v_{ab}) across the high frequency transformer also reduces the THD in comparison to conventional 2L DAB. On the other hand, a higher dc voltage (V_p) is achieved in one ML-DAB module (1-port in Figure 2) using one single-phase transformer, whereas doing the same with two cascaded 2L DABs would require at least two high-frequency transformers and more semiconductor switches.

2.1.1. Power Flow through the dc-dc ML-DAB

Power flow from the PV dc bus to the high voltage dc bus is based on the phase-shift between two active bridges. The phase-shift ϕ is defined based on the phase difference between the fundamental of the primary side 2L v_{ab} and NPC bridge output 5L v_{ab} as shown in Figure 3.

In this topology, 3L NPC diode clamped legs form the high voltage side multilevel (5L) bridge. Sector-wise inductor current (i_{DAB}) at all different switching transitions has been analyzed in terms of α, β and ϕ in order to find the power-flow expression. From the fundamental relation of inductor voltage and current we get:

$$v_L = L\frac{di_L}{dt} \tag{1}$$

Here, $i_L = i_{DAB}$ = current through transformer's leakage inductance:

$$i_L(\theta) = \frac{1}{\omega L}\int_{\theta_1}^{\theta_2} v_L.d\theta;\ \text{where}\ \theta = \omega t \tag{2}$$

Now writing this $i_L(\theta)$ equation for each segment of i_L(i.e., i_{DAB}) from 0 to π and equating $i_L(\pi) = -i_L(0)$ as shown in Figure 3 we get:

$$i_L(0) = \frac{V_P}{n\omega L}.\left(\frac{\pi}{2} - \phi\right) - \frac{V_s}{\omega L}.\left(\frac{\pi}{2}\right) \tag{3}$$

The average power flow equation from primary bridge to secondary bridge through the leakage inductance can be written as follows:

$$P_o = \frac{1}{\pi}\int_0^{\pi} v_{AB}(\theta).i_L(\theta).d\theta. \tag{4}$$

Putting the expression of $i_L(0)$ in $i_L(\theta)$ at different segment (Figure 3) we get the power flow equation for the condition of $\beta < \phi < \frac{\pi}{2}$ as:

$$P_o = \frac{V_P V_s}{n\omega L}.\left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right). \tag{5}$$

$$P_o = m\frac{V_s^2}{\omega L}\left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right). \tag{6}$$

In the above Equations (5) and (6), P_o is the transferred power through the high frequency transformer, V_s is the PV side dc voltage, V_P is the inverter side dc voltage, $\omega = 2\pi f_s$ where f_s is the switching frequency, n is the transformer turns ratio, m is the voltage conversion ratio defined as $m = \frac{V_P}{nV_s}$ and $L\ (= L_{Lk})$ is the primary referred leakage inductance used at the high frequency link.

2.1.2. Soft-Switching Operation of ML-DAB

The conventional two level DAB topology can achieve zero voltage switching (ZVS) for all switches in the entire power range when m is equal to unity. The switching pulses for the 2 L-to-5 L DAB switches are shown in Figure 3. It is possible to achieve the same in the primary bridge (S_1 to S_4) with the condition of $i_L(0) < 0$. ZVS happens in the switches S_{a1}, S_{a4}, S_{b1}, S_{b4} of the NPC bridge during turn-on at $m = 1$. The rest of the switches (S_{a2}, S_{a3}, S_{b2}, S_{b3}) are also turned on when the current through the switch is already zero. S_{a1} and S_{a4} are to be turned-on at ZVS when $i_L(\phi + \beta) > 0$ S_{b1} and S_{b4} are to be turned-on at ZVS when $i_L(\phi - \alpha) \geq 0$. In order to avoid the short circuit condition between D_{a1}, D_{a2} (7) and D_{b1}, D_{b2} (8) zero crossing of i_L should be avoided in the following regions:

$$(\pi + \phi + \alpha) \leq \theta \leq (\pi + \phi + \beta)\ \&\ (\phi + \alpha) \leq \theta \leq (\phi + \beta) \tag{7}$$

$$(\phi - \beta) \leq \theta \leq (\phi - \alpha)\ \&\ (\pi + \phi - \beta) \leq \theta \leq (\pi + \phi - \alpha) \tag{8}$$

By choosing an optimum range of α, β, ϕ ZVS turn-ON can be achieved in eight out of twelve switches. The above analysis of soft-switching operation in ML-DAB becomes important if the IGBTs are replaced by SiC Mosfets operating at higher switching frequencies. Recent development in silicon carbide (SiC) Mosfets, at the voltage level of 1200 V or higher, offer significantly lower switching loss—as much as 90% compared with silicon IGBTs, due to the absence of tail current and fast recovery characteristics of the body diode [30]. Using SiC based switching devices the switching frequency can be in the order of hundred kHz, which in turn reduces the size of reactive components used in the converter.

2.1.3. Transformer Design

The medium/high frequency transformer is used within the dc-dc ML-DAB stage which isolates the PV side from the grid. The transformer frequency is essentially same as the switching frequency used for the 12 switches used in the primary and secondary bridges in the ML-DAB. Higher switching frequency provides lower inductor size. But there is a trade-off while selecting the switching frequency, as higher frequency provides higher switching loss and also higher transformer core loss. Considering the operating frequency and loss profile, various core materials, such as silicon steel, amorphous alloy and nanocrystalline, are used as the transformer core. For frequencies less than 10 kHz, the amorphous Metglas material shows better performance. Based on the prototype voltage and power level a switching frequency of 5 kHz has been chosen as the Metglas Amorphous alloy core is suitable for even higher operating frequencies. Also the IGBTs (Infineon Technologies AG, Neubiberg, Germany, FF100R12YT3, dual) chosen for the ML-DAB also shows a good switching loss profile at that frequency range. Amorphous metglas alloy 2605SA1 material has also shows high permeability, low core losses, high saturation flux density and narrow hysteresis curve. The design of a 3.4 kVA transformer core and winding wires has been calculated using the area-product method as shown below. The transformer core area product is defined as:

$$A_p = A_{core}A_{window} = \frac{k_{conv}(V_1 I_{1_{rms}} + V_2 I_{2_{rms}})}{k_w B_{mx} J_{mx} f_s} \quad (9)$$

where $V_1 \approx V_s = 292$ V, $V_2 \approx V_P = 1667$ V, switching frequency $f_s = 5$ kHz, $I_{1_{rms}} = 16.2$ A, $I_{2_{rms}} = 2.9$ A (RMS values calculated from simulation results), $k_{conv} = 0.5$ (this factor value is chosen based on the converter topology), $k_w = 0.4$ (this is the fill-factor having values usually within range of 0.3 to 0.6), $B_{mx} = 1$ T (chosen based on the maximum saturation flux density being 1.56 T), $J_{mx} = 6$ A/mm^2 (peak current density with the use of litz wire). From Equation (9), we get $A_p = 398,650$ mm^4 By using Metglass 2605SA1 AMCC-50 core specification, we get, $A_p = 462,000$ mm^4, $A_{core} = 330$ mm^2, $A_w = 1400$ mm^2.

The conductor cross-section can be found as $A_{cond_1} = \frac{I_{1_{rms}}}{J_{mx}} = 2.7$ mm^2, *and* $A_{cond_2} = 0.48$ mm^2. The number of turns in the transformer is calculated as, $N_1 = \frac{k_{conv}V_1}{A_{core}f_s B_{mx}} = 89$ turns, similarly $N_2 = 509$ turns AWG 12 259/36 and AWG 20 38/30 Type 2 litz wire have been chosen for transformer primary and secondary windings, respectively. Figure 4 shows a transformer and its components used in the 3.34 kVA ML-DAB.

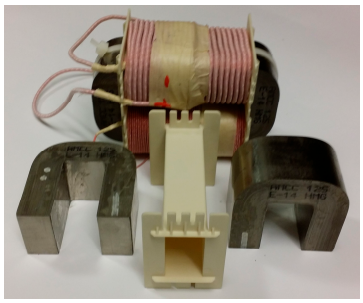

Figure 4. A 3.34 kVA HF Transformer and its components used in the ML-DAB.

2.2. Three-Level NPC Bridge Inverter

Each port of the cascaded NPC (CNPC) inverter (Figure 2) is switched to provide a leg-to-leg 5-level ac output (i.e., V_P, $\frac{V_P}{2}$, 0, $-\frac{V_P}{2}$, $-V_P$). N number of CNPC inverters produce outputs that are phase-shifted from each other by an angle $\frac{180^\circ}{N}$ to yield a $(4N + 1)$ level ac output as discussed later in Section 3. In CHB modulation, the number of levels for N cascaded H-bridges is $(2N + 1)$. So, CNPC provides lower THD than CHB because of having more levels in the cascaded output voltage

waveform. Figure 5 shows how the THD is improved with the increase in number of ports (N) and how the CNPC provides better THD than CHB for any number of cascaded ports. In comparison to cascaded H-bridge (CHB) inverter stage, the CNPC bridge uses double the number of switches with lower voltage rating. It is also advantageous in terms of low dv/dt and less harmonic distortion inherent to the multilevel topology.

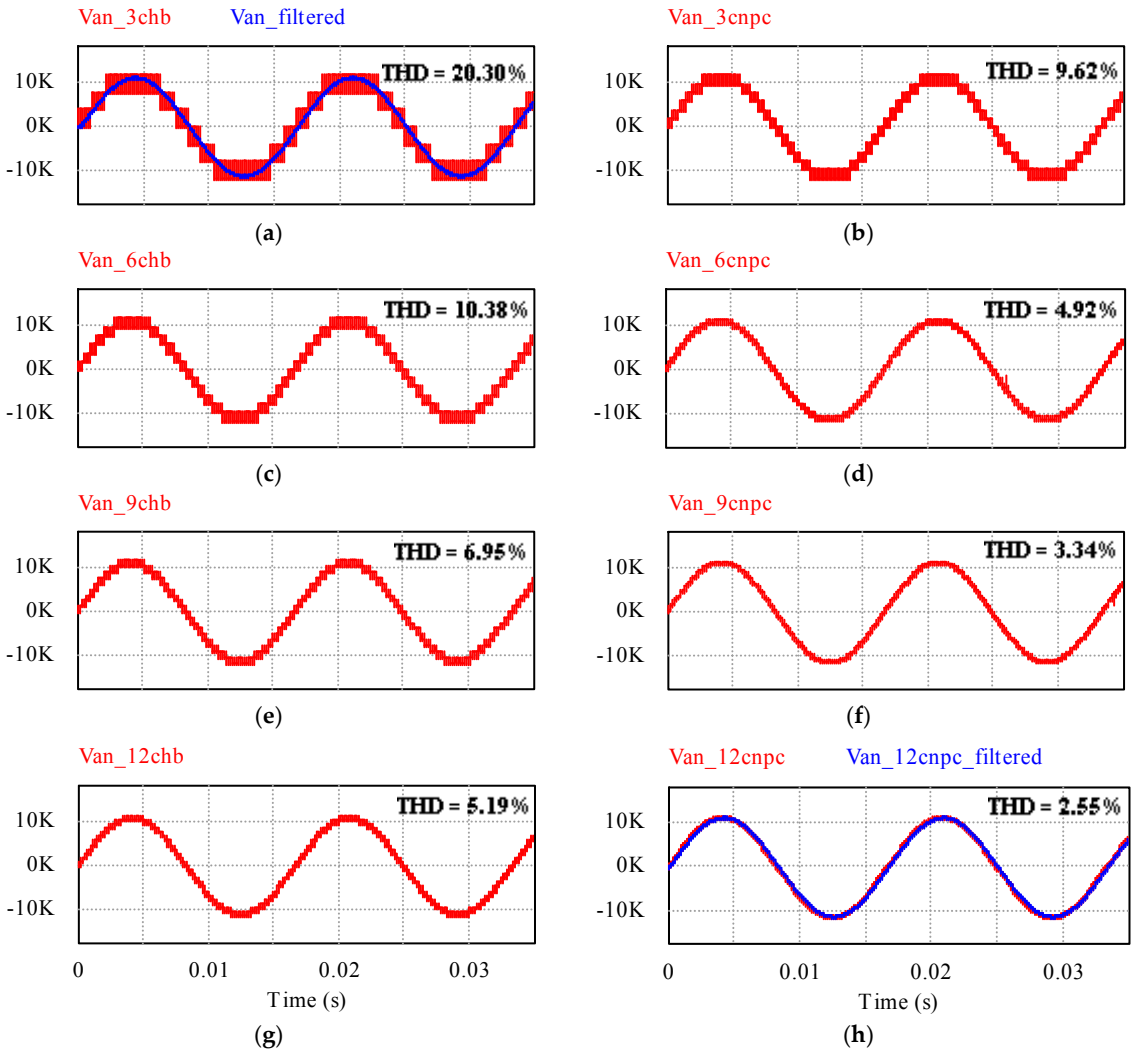

Figure 5. Left and right columns show the THD values at the cascaded unfiltered voltage output for CHB and CNPC configurations respectively. (**a**) V_{an} for 3 cascaded H-bridge; unfiltered THD = 20.30%; (**b**) V_{an} for 3 cascaded NPC-bridge; unfiltered THD = 9.62%; (**c**) V_{an} for 6 cascaded H-bridge; unfiltered THD = 10.38%; (**d**) V_{an} for 6 cascaded NPC-bridge; unfiltered THD = 4.92%; (**e**) V_{an} for 6 cascaded H-bridge; unfiltered THD = 10.38%; (**f**) V_{an} for 9 cascaded NPC-bridge; unfiltered THD = 3.34%; (**g**) V_{an} for 12 cascaded H-bridge; unfiltered THD = 5.19%; (**h**) V_{an} for 12 cascaded H-bridge; unfiltered THD = 2.55%.

Figure 6 shows how the gate signals are generated for one leg (i.e., leg-*c* in Figure 2). The signal generation is done by comparing two level-shifted triangular carriers with a sinusoidal modulating waveform. The other NPC leg (i.e., leg-*d*) has also similar pattern of gate pulses where the modulating signal is shifted by 180°. The carrier frequency has been chosen as 1.5 kHz for easy visualization, though the simulation and hardware experiments have been performed using higher switching frequency. The simulation and hardware output waveforms are shown under Sections 3 and 4.

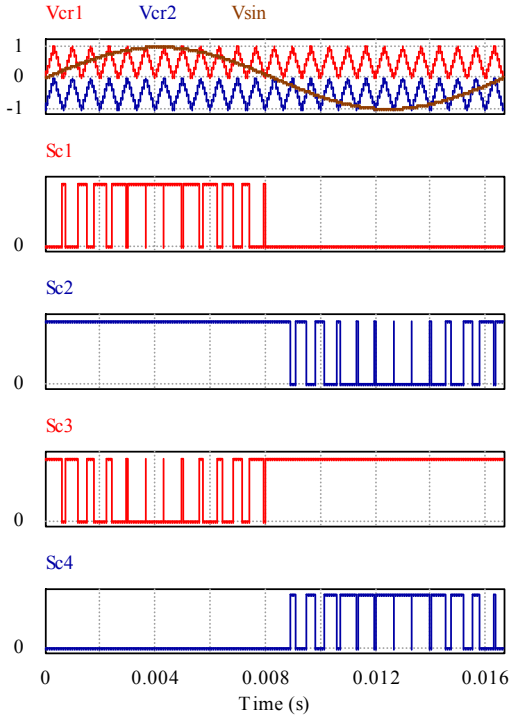

Figure 6. (from top to bottom): Level-shifted carriers (1.5 kHz) and modulating sine waveform (60 Hz), gate signals for NPC inverter leg-*c* as shown in Figure 2.

2.3. Calculation of Power Stage Paramaters

In order to validate the control and power flow in the proposed converter configuration, a 500 $kW_{3\text{-ph}}$ converter has been chosen for design purpose. In that case, the per-phase power output should be:

$$P_{1\phi} = \frac{500\text{ kW}}{3} = 166.67\text{ kW} \tag{10}$$

Assuming the converter having N ports in each phase, each port should process:

$$P_{1port} = \frac{166.67}{N}\text{kW} \tag{11}$$

The 500 kW 3-phase (i.e., 166.67 kW 1-phase) converter is considered to be connected to the 3-phase utility grid at the 13.8 kV $(V_{l-l\ rms})$ voltage level. The voltage level of the converter at every point has been calculated based on 13.8 kV grid voltage and the per-phase line-to-neutral peak voltage at grid interface for one phase (i.e., phase-*a*) is:

$$\hat{V}_{aN} = \frac{13.8\text{ kV}}{\sqrt{3}} \cdot \sqrt{2} = 11.27\text{ kV} \tag{12}$$

Assuming a 4% reserve the nominal dc voltage at the input of N inverter ports should be:

$$V_{dc_{Nport}} \geq 1.04 * \hat{V}_{aN} = 11.72\text{ kV} \tag{13}$$

For a N-port design of the overall single-phase converter (Figure 2), the input voltage at each inverter port is:

$$V_P = \frac{V_{dc_{Nport}}}{N}\text{kV} \tag{14}$$

This dc voltage is the output from the 1-port ML-DAB. For example, if N = 9 the dc-link voltage $V_P = \frac{11.72\ kV}{9} = 1.3$ kV Due to the NPC configuration, the switches on the output side bridge of ML-DAB will withstand half of this voltage, i.e., $V_{c1} = V_{c2} = \left(\frac{V_P}{2}\right) = 650$ V as shown in Figure 2.

The primary bridge dc voltage of the ML-DAB is actually the output voltage from the PV array. Large scale PV installations usually generate PV power at a voltage level up to 600 V or 1000 V dc. This maximum PV voltage is usually constrained by the PV panel characteristics. Considering the SunPower®, E20-435 (SunPower Corporation, San Jose, CA, USA) (435 W, 72.9 V, 5.97 A) solar panel, 45 panels are required at each port for N = 9. So, 9 series connected panels should make one string with $(72.9 \times 9) = 656$ V output. Five such strings should be connected in parallel to make a 19 kW array of 45 PV panels. In this case PV array voltage is:

$$V_s = V_{PV} = 72.9\text{ V } \times \text{ 9 panels in series} = 656\text{ V} \tag{15}$$

2.4. Selection of Semiconductor Switches

2.4.1. Choosing Semiconductor Switches for the NPC Inverter

In comparison to CHB inverter stage, the CNPC bridge uses double the number of switches with half the voltage rating (e.g., 1700 V rated IGBTs instead of 3300 V). It is also advantageous in terms of low dv/dt inherent to the multilevel topology. In the kV voltage levels, typically lower the voltage rating cheaper the semiconductor switches cost. For example, an Infineon 1.7 kV, 340 A dual IGBT module (Part #FF225R17ME3) costs $124.58 each and from the same manufacturer Infineon, a 3.3 kV, 330 A dual IGBT module (Part #FF200R33KF2C) costs $648.56 [31]. At higher voltage and higher current level this price difference gets more and it becomes a key factor while choosing semiconductor switches for a cost-effective converter design.

In early 1900 it has been discovered that cosmic rays cause random failure of high voltage semiconductor devices which depends on the blocking voltage of the device, junction temperature and altitude. In order to select the proper switching devices (e.g., IGBT, Diode) in the kV range the cosmic ray effect on device failure must be considered for reliable operation. For IGBT modules with voltage rating higher than 1700 V, a DC Stability voltage (V_{CED} for Infineon®) or device commutation voltage ($V_{com@100FIT}$) is mentioned in the manufacturer datasheet. 100 FIT means 100 failures within 10^9 h of time. This failure is influenced by the device blocking voltage, junction temperature and altitude although the effect of junction temperature and altitude is negligible at room temperature and sea level [32]. As per Equation (16) the dc stability voltage at 100 FIT has been calculated for 1.7 kV, 2.5 kV, 3.3 kV, 4.5 kV and 6.5 kV IGBTs:

$$V_{CE@100\text{ FIT}} = C_1 - C_2 / \ln\left(\frac{100\text{ FIT}}{C_3}\right) \tag{16}$$

Here C_1, C_2, C_3 are parameter values found from [32]. Based on this $V_{CE@100\text{ FIT}}$ voltage value, another metric named "device voltage utilization factor (DVUF)" can be defined to choose an IGBT for cost-efficient design [18]. DVUF is defined as:

$$\text{DVUF} = \frac{V_{CES_{rated}}}{V_{CE@100\text{ FIT}}} \tag{17}$$

Here, $V_{CES_{rated}}$ is the maximum rated voltage mentioned in the IGBT manufacturer datasheet. In order to choose an IGBT module higher DVUF percentage is preferred for an optimum design of the converter. This factor not only optimizes the device utilization efficiency it also reduces the cost of IGBTs in most of the cases. The following Table 1 summarizes the required IGBT voltage rating for both CHB and CNPC inverters for N = 3 to 12.

Table 1. IGBT Selection for CHB and CNPC Inverters for N = 3 to N = 12.

No. of Modules per Phase (N)	Assuming N-Nos. of CHB Modules per Phase				Assuming N-Nos. of CNPC Modules per Phase			
	V_{dc} at Each Port of CHB Inverter (V)	Required IGBT $V_{CES_{rated}}$ (kV)	$V_{CE@100FIT}$ (V)	DVUF (%)	$V_{dc/2}$ at Each Port of CNPC Inverter (V)	Required IGBT $V_{CES_{rated}}$ (kV)	$V_{CE@100FIT}$ (V)	DVUF (%)
3	3906	>6.5	-	-	1953	4.5	2899	67.37
4	2930	6.5	3865	75.81	1465	3.3	1794	81.66
5	2344	4.5	2899	80.86	1172	2.5	1289	90.92
6	1953	4.5	2899	67.37	977	1.7	1072	91.14
7	1674	3.3	1794	93.31	837	1.7	1072	78.08
8	1465	3.3	1794	81.66	733	1.7	1072	68.38
9	1302	3.3	1794	72.58	651	1.2	No FIT data	90.42
10	1172	2.5	1289	90.92	586	1.2	available.	81.39
11	1065	1.7	1072	99.35	533	1.2	Assuming 720 V	74.03
12	977	1.7	1072	91.14	489	1.2	(60% of V_{CES})	67.92

2.4.2. Choosing Semiconductor Switches for the ML-DAB

For the ML-DAB dc-dc converter the NPC-bridge IGBTs have the same voltage rating as calculated for the NPC inverter in Table 1. The primary bridge of the ML-DAB is a 2-level full-bridge. Usually the PV voltage lies within 1000 V dc limit. If the input voltage is within 720 V (assuming 60% of the V_{CES} of 1.2 kV IGBTs), 1200 V IGBTs can be chosen for primary ML-DAB full-bridge.

For PV voltages in 720 V to 1000 V range, 1700 V IGBTs are a good choice for the same full-bridge. The parameter values obtained for designing a 3-phase 500 kW N-port (i.e., N = 3, 5, 8, 12) PV converter are summarized in Table 2 below. The PV output voltage (V_s) has been chosen based on the string combination of SunPower® E20-435 (SunPower Corporation, San Jose, CA, USA) panels. Based on the power requirement more parallel strings can be combined to form a suitable PV array.

Table 2. ML-DAB Parameter Values for a 500 kW 3-phase N-port Converter.

For a 500 kW 3-ph 13.8 kV Converter	N = 3 Ports/Phase	N = 5 Ports/Phase	N = 8 Ports/Phase	N = 12 Ports/Phase
Power rating of 1 ML-DAB	55.6 kW	33.4 kW	20.8 kW	13.9 kW
PV output voltage, V_s (for 10 or more parallel strings)	947.7 V to 1000 V	583.2 to 1000 V	364.5 V to 1000 V	291.6 V to 1000 V
ML-DAB output voltage, V_P	6.67 kV	4 kV	2.5 kV	1.67 kV
HF transformer turns ratio, $n = V_P/V_s$	7.035 or less	6.858 or less	6.858 or less	5.716 or less
Leakage inductor L (for minimum V_s & f_s = 5 kHz)	0.32 mH	0.20 mH	0.12 mH	0.122 mH
ML-DAB primary IGBTs V_{ce}	1700 V	1200 V	600 V	600 V
ML-DAB secondary IGBTs V_{ce}	4.5 kV	3.3 kV	1700 V	1200 V

In choosing the no. of ports for this N-port converter design, the required voltage levels have been considered based on commercially available medium voltage IGBTs (e.g., 1.2 kV, 1.7 kV, 2.5 kV, 3.3 kV, 4.5 kV and 6.5 kV). The diodes and capacitors used in the converter is rated as per the IGBT rating associated with those diodes and capacitors. Some high voltage silicon carbide (SiC) based IGBTs have been discussed in literature [33–35] which would be helpful in reducing no. of ports and thus improving the power density of the overall converter.

2.5. Cost-Effectiveness of the Proposed N-Port Converter

Based on the proposed design of the N-port converter and a 3.34 kW hardware prototype, an effort has been made to estimate the proposed converter cost and compare it with a commercially available utility-scale overall PV system. In order to prepare a cost comparison with a conventional 1 MW PV system, authors got the support from a private utility scale PV system contractor in the state of Texas. Due to more number of ports per phase the proposed N-port converter alone is likely to

be costlier than the central inverter. The conventional transformer cost is not there in the proposed converter since it eliminates the line frequency transformer with smaller high frequency transformers integrated in dc-dc stage. Still the converter alone is not cheaper than the combination of central inverter and transformer. Most of the cost in the proposed converter comes from the HF transformer. The overall gain can be achieved from balance of systems (BOS) cost. Due to internal higher voltages the corresponding current gets much lower in comparison to the central inverters. This lower current saves money by saving a good amount of copper cable, conduit and switchgear. A summary, with some key components in a 1 MW PV system, has been shown in Table 3. It appears that the proposed *N*-port converter can be \$0.13/watt cheaper than a conventional central inverter in the 1 MW scale. The comparison has been made based on central inverter solution. All the item costs have been estimated based on present market price which may vary as per design, place, manufacturer and other market conditions.

Table 3. Cost of the proposed *N*-port Converter based on 1 MW PV system.

Components	Proposed *N*-Port Inverter
Inverters	\$0.2000
Transformers	Included in Inverter Cost
Copper Cable	\$0.0252
PVC conduit	\$0.0085
AC switchgear	\$0.0337
Combiners	\$0.0060
Concrete	\$0.0059
Key items above:	\$0.2000
Assuming rest of the project cost is same for both central and *N*-port inverter	
Overall \$/watt	\$1.72

It was also observed that the proposed *N*-port converter has more than 40% lower footprint in comparison to the combination of central inverter and line frequency transformer.

2.6. Global Efficiency of the Proposed N-Port Converter

The efficiency of a system is defined as the ratio of the output power P_{out}, and input power P_{in}. Since the proposed *N*-port converter consists of N number of cascaded ports, the global efficiency for the proposed *N*-port converter is the ratio between output power and the total input power which is the summation of individual *N*-port input power. Hence, the global efficiency of the system is the average efficiency of the cascaded ports. The global efficiency of the 12-port converter is 96.42% based on the obtained simulation results:

$$\eta = \frac{P_{out}}{\sum_1^N P_{inN}} \tag{18}$$

3. Control of *N*-Port Converter

Since the *N*-port converter is designed for PV application, the front-end ML-DAB ensures to get the maximum power available from PV array using the MPPT control. MPPT and power mismatch control in the *N*-port converter will be discussed in the following sub-sections.

3.1. PV Modelling and MPPT Control

In large scale PV solar system, MPPT is commonly implemented on the inverter stage. In this converter MPPT, using perturb and observe (P&O) method, is achieved by controlling the phase-shift (ϕ) between the two active bridges in each ML-DAB [36]. The MPPT has also been verified in Simulink® using the incremental conductance algorithm. Based on the variation of insolation, the PV strings generate different currents. To draw the maximum current achievable, thus the maximum power

from PV panels, the PV voltage and current are sensed and the derived control signal is translated to desired phase-shift (ϕ). Figure 7 shows the block diagram of the grid connected PV system with P&O algorithm implemented in NI myRIO-1900® (National Instruments Corporation, Austin, TX, USA).

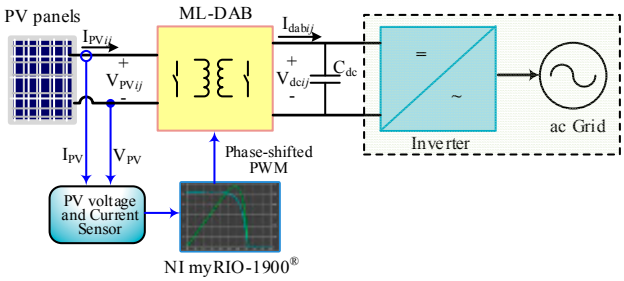

Figure 7. MPPT control at each ML-DAB module using NI myRIO-1900®.

Voltage and current sensors are used to sense the slope of PV power curve. A control voltage from the PI controller will accordingly vary the phase shift of ϕ (5). A P&O algorithm is implemented to achieve the MPPT control and implemented on LabVIEW® (National Instruments Corporation, Austin, TX, USA) in real time. Phase shifted PWM pulses are generated in LabVIEW FPGA. Once the PV power output is connected to the MPPT circuit the open circuit voltage instantly drops to a new value which is dependent on the impedance of the load. The control algorithm implemented on the NI-myRIO sends corresponding switching pulses to the ML-DAB converter to move the new operating point to the maximum power point (MPP). The detailed MPPT results from hardware are shown in Section 3.

3.2. Capacitor Voltage Mismatch Control at the ML-DAB

Ideally the ML-DAB should not experience any unbalance between clamping capacitor voltages V_{c1} & V_{c2} (Figure 8), where the dc-link voltage $V_{dc_{ij}} = V_{c1_{ij}} + V_{c2_{ij}}$, here $i = 1, 2, \ldots, N$ ports and $j = a, b, c$ three phases. Figure 7 shows the dc-link voltage $V_{dc_{ij}}$ as a series combination of $V_{c1_{ij}}$ & $V_{c2_{ij}}$ across $C_{1_{ij}}$ & $C_{2_{ij}}$ respectively without showing the common neutral point "o" between ML-DAB NPC bridge and NPC inverter. Due to any load disturbance or converter non-ideality capacitor voltages become unbalanced i.e., $V_{c1} \neq V_{c2}$ During unbalanced condition a non-zero average neutral-point current i_{np} flows to/away from the neutral point "o" (Figure 7).

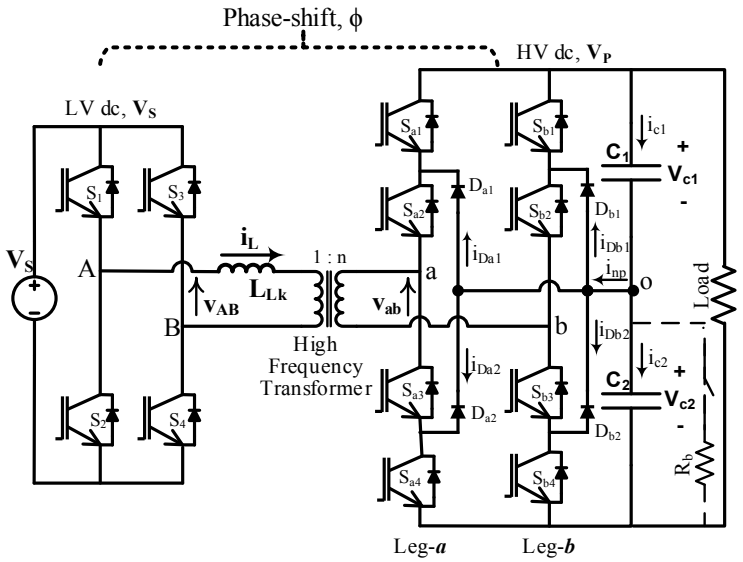

Figure 8. Schematic of ML-DAB only showing NPC bridge currents in one port.

From Figure 8 we get the neutral point and clamping diode current relations as follows:

$$i_{np} = i_{c1} - i_{c2} \tag{19}$$

$$i_{np} = i_{D_{a1}} - i_{D_{a2}} + i_{D_{b1}} - i_{D_{b2}} \tag{20}$$

In order to control the switching cycle average of i_{np}, the diode currents ($D_{a1}$to D_{b2}) can be controlled by changing the α & β, which modulates corresponding NPC switch gate pulses accordingly. For example, if during any unbalance $i_{c1} > i_{c2}$ then switching-cycle average of i_{c1} ($\overline{i_{c1}}$) should be reduced and $\overline{i_{c2}}$ should be increased. In order to implement this control, we need to delay S_{a1}& S_{b1} and start earlier S_{a2}& S_{b2} by an amount of $\Delta\theta$ as shown in Figures 9–11 as "*Theta_Control*" in degrees. During simulation the gain $K = 0.018$ and time-constant $T = 0.01413$ have been used to validate the control algorithm using a PI controller. A similar capacitor voltage balancing control has been described in [37]. As shown in Figure 11, an intentional imbalance between $V_{c1}$and V_{c2} has been created bypassing a part of the i_{c2} through R_b (Figure 8) at t = 0.02.

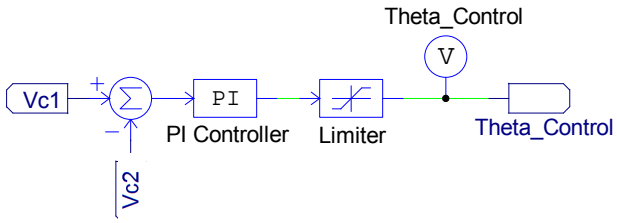

Figure 9. Block diagram showing the capacitor voltage imbalance control.

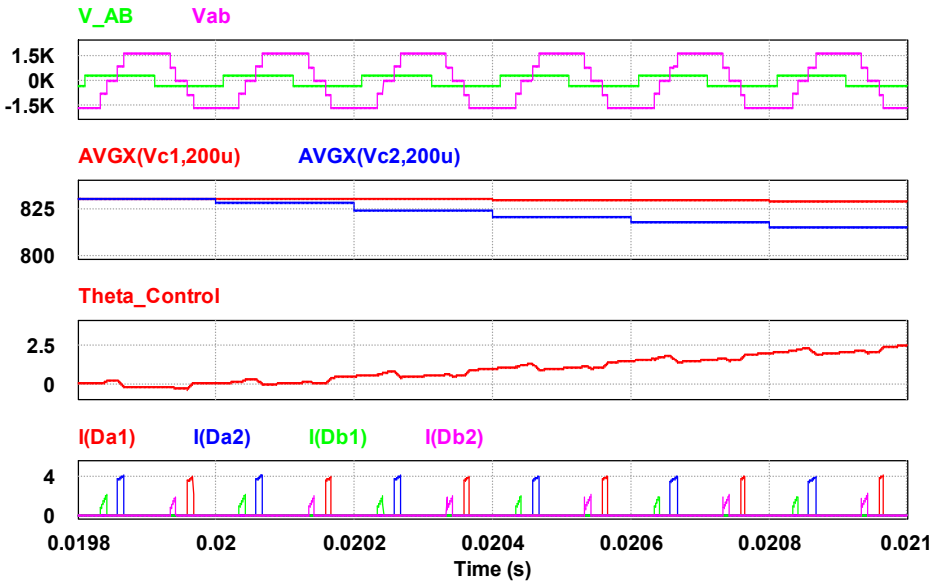

Figure 10. After t = 0.02s, $V_{c1} \neq V_{c2}$ and the control signal "*Theta_Control*" starts compensating the imbalance by modulating diode currents ON-time duration ($I_{D_{a1}}$*to* $I_{D_{b2}}$).

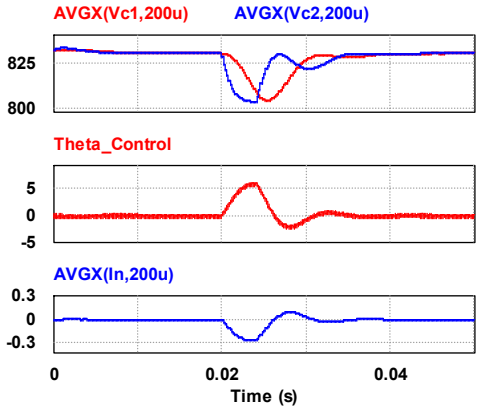

Figure 11. Capacitor voltage balancing using a PI controller ($I_n = i_{np}$).

3.3. dc-Link Voltage Control Using Power Mismatch among N Ports

Voltage imbalance and power mismatch among the different ports are control challenges for a multiport cascaded converter topology. Various control strategies have been described in literature in order to regulate such unbalance for cascaded inverters in solid state transformer (SST) applications [22,25]. The overall control structure has been designed, in this paper, based on the input PV power mismatch among the various ports in all three phases. Maximum power point current I_{mpp} and corresponding voltage V_{mpp} can be obtained from the MPPT control. The product of V_{mpp} and I_{mpp} is the output power P_{PV} from the solar PV panels which is fed into the dc-dc ML-DAB converter. Assuming η_{dab} as the efficiency for ML-DAB dc-dc stage conversion, we get:

$$P_{dab_{ij}} = \eta_{dab}.P_{PV_{ij}};\ \text{where } i = 1, 2, \ldots, N \text{ ports and } j = a, b, c \text{ three phases} \tag{21}$$

For N numbers of ports per phase, the total power to be processed in three phases should be:

$$\begin{aligned} \sum P_{dab_{ij}} &= P_{dab_{1a}} + P_{dab_{2a}} + \ldots + P_{dab_{Na}} + P_{dab_{1b}} + \ldots + P_{dab_{Nb}} + P_{dab_{1c}} + \ldots + P_{dab_{Nc}} \\ &= \eta_{dab} * \left(P_{PV_{1a}} + P_{PV_{2a}} + \ldots + P_{PV_{Na}} + P_{PV_{2b}} + \ldots + P_{PV_{Nb}} + P_{PV_{1c}} + \ldots + P_{PV_{Nc}}\right) \end{aligned} \tag{22}$$

The dc-dc ML-DAB power equation for one port is as follows. Here α, β are assumed to be constant and ϕ varies according to MPPT control (Figure 3):

$$P_{dab_{ij}} = \frac{V^*_{dc_{ij}}.\, V_{PV_{ij}}}{n\omega L} \cdot \left(\phi_{ij} - \frac{\phi_{ij}^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right) = \eta V_{PV_{ij}} I_{PV_{ij}} = V^*_{dc_{ij}} I_{dab_{ij}} \tag{23}$$

ML-DAB output current $\left(I_{dab_{ij}}\right)$ can be obtained by using the variables such as ϕ, α, β, n, w, L and V_{PV} as follows:

$$I_{dab_{ij}} = \frac{V_{PV_{ij}}}{n\omega L} \cdot \left(\phi_{ij} - \frac{\phi_{ij}^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right) \tag{24}$$

As there will be difference in power from the PV panels connected to different ports, it is necessary to find the ratio $\left(r_{ij}\right)$ of the individual port's PV power to the total PV power:

$$r_{ij} = \frac{P_{dab_{ij}}}{\sum\limits_{\substack{i = 1, ..N; \\ j = a, b, c}} P_{dab_{ij}}} \tag{25}$$

The respective ratio of the individual ports is multiplied by d-axis grid current i_d and d-axis grid voltage e_d, obtained from $abc - dq$ transformation, to calculate the inverter input power for the

respective port of the N-port converter (Figures 12 and 13). In order to establish the decoupled control of active power $P_{g_{ij}}$ through control of i_d, and reactive power $Q_{g_{ij}}$ through i_q in the grid voltage-oriented control, where e_q is zero and e_d equals $\sqrt{\frac{3}{2}}$ times the amplitude of the grid phase voltage:

$$P_{g_{ij}} = r_{ij}.\left(e_d \cdot i_d + e_q \cdot i_q\right) = r_{ij} e_d i_d \tag{26}$$

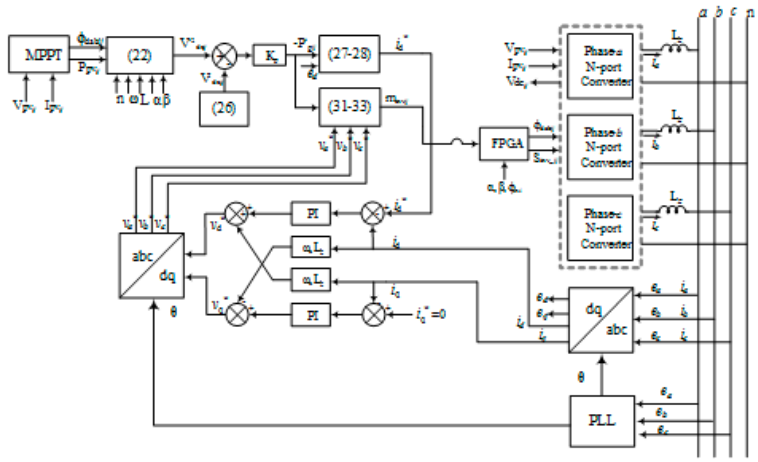

Figure 12. Block diagram showing the capacitor voltage imbalance control.

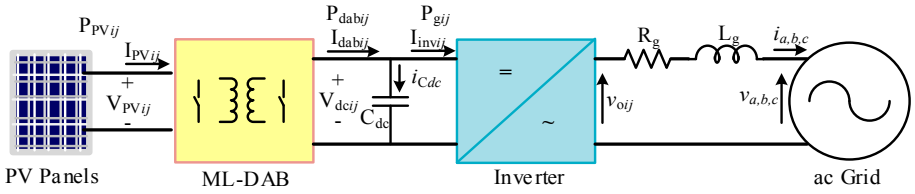

Figure 13. Block diagram showing key parameters and power flow from PV panels to the grid.

An approach to control the dc-link voltage has been described in [24] for a doubly fed induction generator (DFIG). This can be modified in the proposed N-port converter for balancing the power mismatch among different ports. The energy stored in a small time period dt in the dc-link capacitor C_{dc} can be expressed as the power difference between $P_{dab_{ij}}$ and $P_{g_{ij}}$ at any instant (Figure 13). The reference DC bus voltage $(V_{dc_{ij}})$ can be obtained from Equation (27):

$$\frac{1}{2} C_{dc} \frac{d}{dt}\left(V_{dc_{ij}}^2\right) = P_{dab_{ij}} - P_{g_{ij}} \tag{27}$$

Considering $V_{dc_{ij}}^2$ as the control variable and assuming $P_{dab_{ij}}$ as constant (i.e., perturbation in $P_{dab_{ij}}$ to be zero), the small signal model can be derived from Equation (27), as shown in Equation (28):

$$\frac{V_{dc_{ij}}^2(s)}{-P_{g_{ij}}(s)} = 2\frac{1}{sC_{dc}} \tag{28}$$

The controller parameters can be found from Equation (28). The square of measured dc-link voltage $V_{dc_{ij}}^2$ is compared with the reference $V_{dc_{ij}}^{*2}$ obtained from Equation (23) to regulate the dc-link voltage. This yields the active power reference $P_{g_{ij}}^*$ (Figure 12). This power gives the reference for i_d^* as

shown in Equation (29), where e_d is the d-axis component of grid voltage and $\sum P^*_{g_{ij}}$ is calculated from Equation (30) to Equation (31):

$$i^*_d = -\frac{\sum_{\substack{i=1,.,N \\ j=a,b,c}} P^*_{g_{ij}}}{e_d} \tag{29}$$

$$\left.\begin{aligned} \sum_{i=1,..,N} P^*_{g_{ia}} &= P^*_{g_{1a}} + P^*_{g_{2a}} + \ldots + P^*_{g_{Na}} \\ \sum_{i=1,..,N} P^*_{g_{ib}} &= P^*_{g_{1b}} + P^*_{g_{2b}} + \ldots + P^*_{g_{Nb}} \\ \sum_{i=1,..,N} P^*_{g_{ic}} &= P^*_{g_{1c}} + P^*_{g_{2c}} + \ldots + P^*_{g_{Nc}} \end{aligned}\right\} \tag{30}$$

$$\sum_{\substack{i=1,.,N \\ j=a,b,c}} P^*_{g_{ij}} = \sum_{\substack{i=10 \\ ,\ldots,N}} P^*_{g_{ia}} + \sum_{i=1,..,N} P^*_{g_{ib}} + \sum_{i=1,..,N} P^*_{g_{ic}} \tag{31}$$

The ac output voltage from every single inverter port can be obtained by multiplying the reference grid phase voltage (e.g., v^*_a) with the respective negative power reference ($-P^*_{g_{ia}}$) ratio as shown in Equation (32):

$$v_{o_{ia}} = v^*_a \cdot \frac{P^*_{g_{ia}}}{\sum P^*_{g_{ia}}} \tag{32}$$

Similarly, the ac output from all other ports can be obtained for phases b and c as shown below:

$$v_{o_{ib}} = v^*_b \cdot \frac{P^*_{g_{ib}}}{\sum P^*_{g_{ib}}} \tag{33}$$

$$v_{o_{ic}} = v^*_c \cdot \frac{P^*_{g_{ic}}}{\sum P^*_{g_{ic}}} \tag{34}$$

The sum of the output voltages from each of N-port inverters appears across the respective phase of the grid (i.e., v_{an}, v_{bn}, v_{cn}):

$$\left.\begin{aligned} v_{an} &= \sum_{i=1,..,N} v_{o_{ia}} = v_{o_{1a}} + v_{o_{2a}} + \ldots + v_{o_{Na}} \\ v_{bn} &= \sum_{i=1,..,N} v_{o_{ib}} = v_{o_{1b}} + v_{o_{2b}} + \ldots + v_{o_{Nb}} \\ v_{cn} &= \sum_{i=1,..,N} v_{o_{ic}} = v_{o_{1c}} + v_{o_{2c}} + \ldots + v_{o_{Nc}} \end{aligned}\right\} \tag{35}$$

The current flowing towards the grid (i_a, i_b, i_c) can be found using equations (36) to (38), where e_a, e_b are respective grid voltages and R_g, L_g are the lumped resistance and inductance respectively at the grid interface:

$$v_{an} = i_a \cdot R_g + L_g \cdot \frac{di_a}{dt} + e_a \tag{36}$$

$$v_{bn} = i_b \cdot R_g + L_g \cdot \frac{di_b}{dt} + e_b \tag{37}$$

Assuming balanced grid currents, the sum grid currents i_a, i_b, i_c is zero:

$$i_c = -(i_a + i_b) \tag{38}$$

Using $abc - dq$ transformation, grid currents i_a, i_b, i_c are transformed into i_d and i_q (Figure 12). Current i_d is compared with the corresponding reference current i^*_d, and i_q is assumed to be zero. The output of the d-phase PI controller is summed up with the product of ω_s, L_g and i_q current and the resultant is the d-phase reference voltage v^*_d. v^*_q can be obtained similarly as shown in

Figure 12. After the $dq - abc$ transformation reference voltages v_a^*, v_b^*, v_c^* can be obtained. These reference voltages are used as the modulating signal for the level-shifted PWM to generate the corresponding gate pulses ($S_{inv_{ij}}$) for the IGBTs used in the NPC inverters. The phase-shift control parameter ($\phi_{dab_{ij}}$) has been derived independently from the MPPT control which generates the gate pulses for the ML-DAB primary bridge switches ($S_{1_{ij}}$ to $S_{4_{ij}}$) corresponding to the required phase-shift ($\phi_{dab_{ij}}$) between two bridges.

3.4. (N − 1) Redundancy

The overall converter has been studied for $(N-1)$ redundancy. That means, if a single port out of the N numbers of total ports per phase fails, the whole converter should not stop functioning. Because of one port failure, each of the remaining ports has to deal with a higher voltage to still maintain the grid voltage at the output. In order to safeguard the IGBTs from excessive voltage this redundancy design is feasible for higher number of ports (e.g., N = 9 or more). The parameter values have been considered from Table 2 with $N = 12$ to study the effect of 1-port failure among the N numbers of ports. For $N = 12$, $N_{new} = (N-1) = 11$ And the ML-DAB output voltage $V_{P_N} = 1667$ V and $V_{P_{N-1}} = \frac{1667*12}{11} = 1820$ V; and $V_{s_{N-1}} = 292$ V $= V_{s_N}$ The total power (i.e., $N \times P_{g_{1port}}$) at the inverter output will be reduced to $((N-1) \times P_{g_{1port}})$ due to 1-port failure. The current through the cascaded NPC bridges at the inverter output stage will be reduced to comply with this reduction in total power. Assuming power from every single ML-DAB port remains the same and it is obtained from PV MPPT control. $V_{s_{N-1}}$ (for 1-port) should also remain same as before since V_s $(= V_{PV})$ is controlled by the MPPT controller to achieve maximum available power from the PV panels. Only $V_{P_{N-1}}$ will go high to maintain constant grid voltage. The turns ratio n and leakage inductance L_{Lk} of the high frequency transformer will also remain the same as this is a parameter value obtained from hardware design. The switching frequency f_s is also kept constant. The phase-shift between the outputs of the CNPC inverters change from $\left(\frac{180^\circ}{N}\right)$ to $\left(\frac{180^\circ}{N-1}\right)$ in the case of 1 port failure. Assuming 12 number of ports per phase (i.e., N = 12), Table 4 summarizes the calculated parameter values for a single port converter in case of 1 port failure (i.e., $N-1$ = 11).

Table 4. $(N-1)$ Redundancy for a 3.34 kW Prototype design with all 1200V IGBTs assuming N = 12.

Item Description	Each Port (for N = 12)	Each Port (for $N-1$ = 11)
Power Rating of 1 single DAB module P_o	3.34 kW	3.34 kW
$V_s(= V_{PV})$	291.6 V	291.6 V
$V_P(= V_{dc})$	1667 V	1820 V
DAB high frequency transformer's turn ratio, n	5.716	5.716
$I_{PV}(= I_{DAB_{ln}})$	11.43 A	10.48 A
$I_{dab}(= I_{inv_{in}})$	2 A	1.835 A
Phase-shift among CNPC inverter outputs	$(N/180)$ =15°	$((N-1)/180)$ = 16.37°

4. Simulation and Experimental Results

Each port (i.e., ML-DAB and NPC inverter) has been designed to process 3.34 kW of power for simulation and hardware experiments. Table 1 shows the voltage levels and parameter values for one port, which has been derived assuming the output of the cascaded NPC (CNPC) bridge is connected to the 13.8 kV utility grid. In order to realize the switching and conduction losses Infineon FF100R12YT3 dual IGBT module and IXYS DSEP 30-12AR clamping diodes are modeled in PSIM® thermal module simulation software. The same IGBTs and diodes are used in the hardware prototype also. The voltage conversion ratio m in the ML-DAB is chosen as unity resulting in the turns ratio $n = 5.7$ The switching frequency f_s is set at 5 kHz. Figure 14 shows the simulated steady state voltage and current waveforms across the high frequency transformer in the ML-DAB where $V_s = 292$ V, $V_P = 1668$ V, $\alpha = 10^\circ$, $\beta = 30^\circ$.

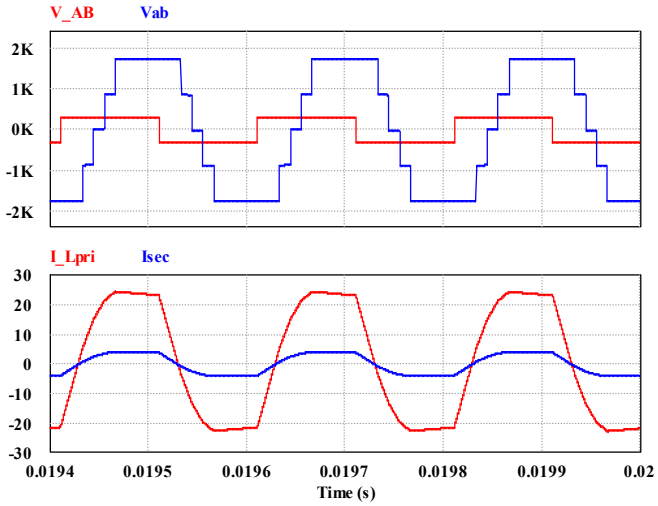

Figure 14. (from top to bottom)—PV-side bridge voltage, v_{AB}, v_{ab} and current i_{Lpri} and i_{sec} of 1-port ML-DAB.

A scaled down laboratory prototype of the proposed converter (ML-DAB and NPC inverter) has been built for validating the MPPT and power flow control and to observe the key waveforms at different stages of power conversion assuming open loop operation. Each ML-DAB and NPC inverter hardware has been designed to process a maximum 3.34 kW of power. The value of ϕ varies according the control signal received from the MPPT sub-circuit. Figure 15 shows the experimental waveforms of the ML-DAB for $V_s = 125$ V, $V_P = 650$ V, $\alpha = 10°$, $\beta = 30°$, $\phi = 70°$.

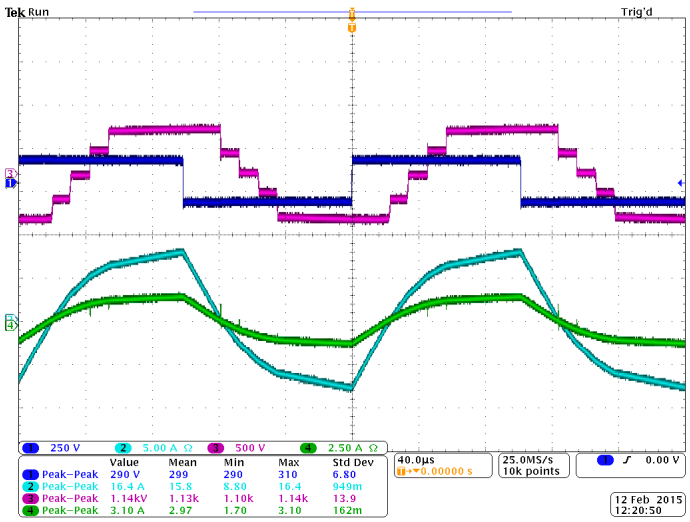

Figure 15. Experimental output for ML-DAB 2-level voltage v_{AB}, 5-level voltage v_{ab} and currents through the transformers i_{Lpri}, i_{sec}; where $V_s = V_{PV} = 125$ V, $V_P = V_{dc} = 650$ V, $n = 5.71$, $\alpha = 10°$, $\beta = 30°$, $\phi_{ini} = 70°$.

Figures 16 and 17 show the simulated and experimental input-output currents at ML-DAB. MPPT control in ML-DAB adjusts the phase shift ϕ to obtain the maximum power available at the PV panels. The ML-DAB input voltage (V_s) is obtained from four PV panels in series. The PV parameters have been calculated based on the SunPower® E20-435W, 72.9 V, 5.97 A solar panel datasheet. Figure 18 shows the effect of MPPT control and phase-shift modulation when PV current changes due to the change in solar irradiance for both Perturb and Observe (P&O) and Incremental Conductance algorithm.

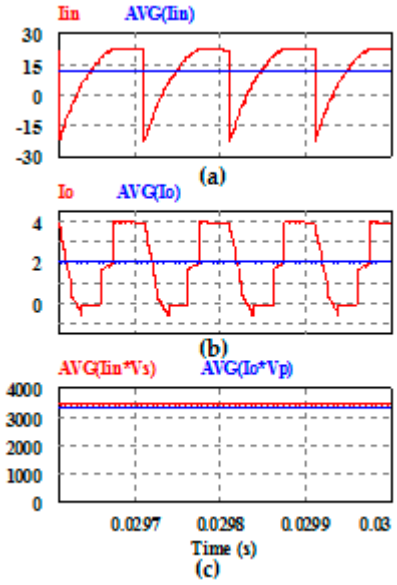

Figure 16. (From top to bottom)—(**a**) ML-DAB input current and its average; (**b**) output current and its average; and (**c**) Average input and output power; efficiency = 96.42%.

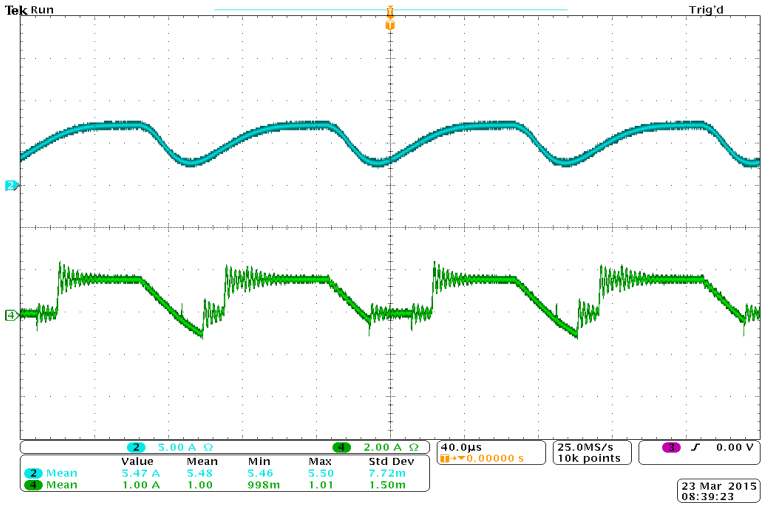

Figure 17. Experimental output for ML-DAB input (top–blue) and output (bottom–green) dc currents respectively.

NI-myRIO® (National Instruments Corporation, Austin, TX, USA) has been used to provide MPPT control signals for ML-DAB converter. The MPPT algorithm and the phase-shift PWM scheme is built, debugged and run with the help of LabVIEW development software. A voltage transducer (SCK-MU-1500V) has been used at the point where the PV module output is connected to the input of the DAB converter to measure the dc input voltage. A current transducer (CR5410-20) measures the PV generated current of the PV module on each operating point. The MPPT algorithm provides the required phase-shift (ϕ) which gives the gate-pulse for the ML-DAB primary bridge switches. This phase shift allows the required amount of power, generated from PV MPPT, to flow through the ML-DAB to the inverter and the load. Figure 19 shows the MPPT results obtained from hardware using MAGNA Power® XR200-10 (MAGNA Power Electronics Inc., Flemington, NJ USA) PV source emulator and NI myRIO-1900® FPGA (National Instruments Corporation, Austin, TX, USA) (Figure 20).

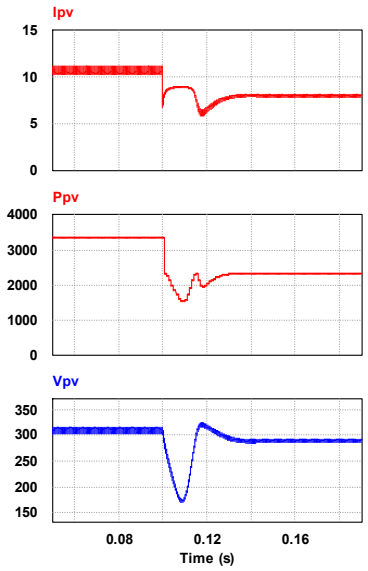

Figure 18. MPPT, using P&O algorithm, controls the power flow when PV generation changes due to change in insolation from 1000 W/m^2 to 800 W/m^2 at t = 0.1 s.

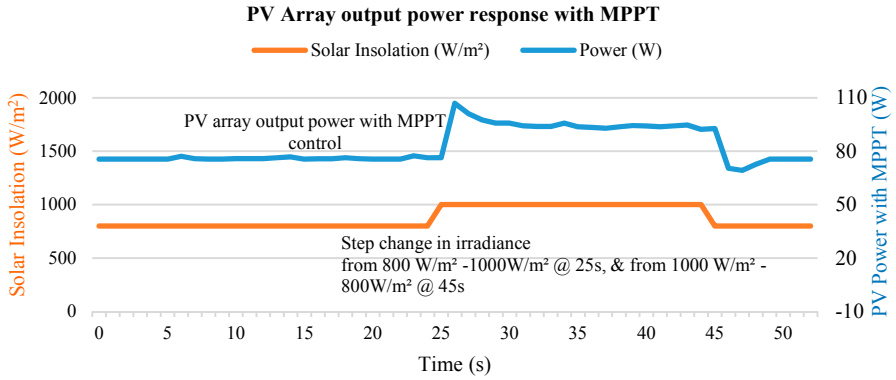

Figure 19. The graph obtained from experimental data shows how the PV output power is controlled by the MPPT algorithm using MAGNA Power® XR200-10 PV source emulator and NI myRIO-1900®.

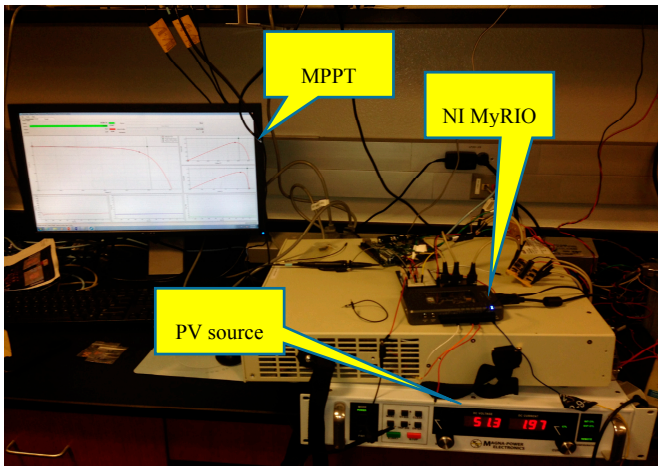

Figure 20. Hardware setup for the MPPT control using MAGNA Power® XR200-10 PV source emulator and NI myRIO-1900® along with LabVIEW.

MPPT efficiency is determined, as the ratio of power measured with the MPPT controller and the true power, the PV module produces without the MPPT controller:

$$\eta_{MPPT} = \frac{\int_0^t P_{with\ MPPT}(t)dt}{\int_0^t P_{true}(t)dt} \tag{39}$$

The true power of PV array at irradiance 1000 W/m^2 and 800 W/m^2 from PV source emulator is given as 96.3 W and 75.35 W respectively. Thus the MPPT efficiency is 97.6% for 1000 W/m^2 and 98.2% for 800 W/m^2.

The current control for grid-connected N-port converter has been performed in Simulink® (The MathWorks Inc., Natick, MA, USA). For clarity in the waveforms to present in this paper, five ports ($N = 5$) per phase have been considered. The control scheme uses PLL to provide a phase reference and establish the frequency at the inverter terminals. Figure 21a shows the PLL response of a three phase system synchronized with the grid at the frequency of 60 Hz. The PV power input to different ports has been changed at two time instants (i.e., at t = 0.04 s and at t = 0.08 s) to observe the control performance as shown in Figure 21b. Figures 22 and 23 show the dc-link voltage control using two CHB inverters per phase. Details of this control algorithm has been described in Section 3.3.

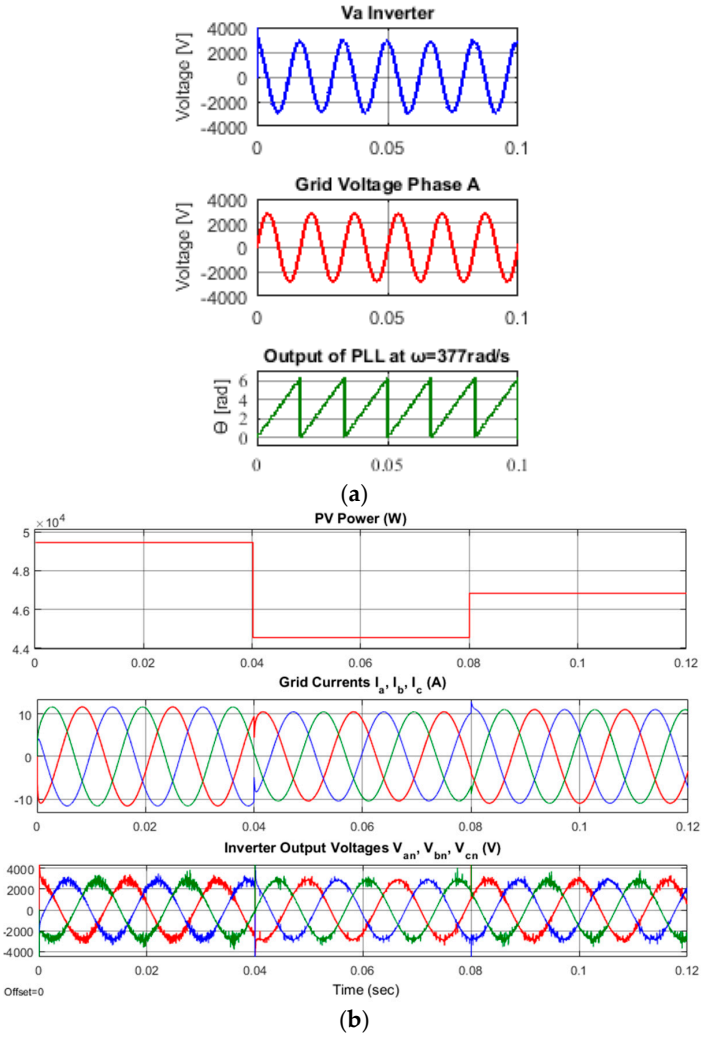

Figure 21. (**a**) Response of three-phase closed loop PLL system that tracks the phase of grid voltage $V_a = V_m \cos\theta$, $V_m = 2000 \times \sqrt{2}$ V; (**b**) Current control of the N-port three-phase grid-connected PV converter for varying total PV input power; here P_{PV} is dropped 10% at t = 0.4 s and increased 5% at t = 0.08 s.

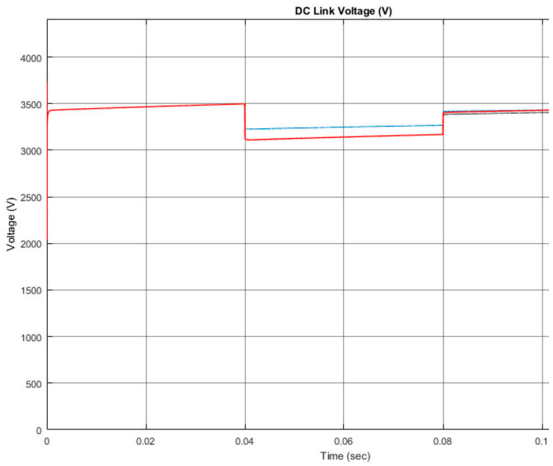

Figure 22. Based on power mismatch different dc-link voltages appear at corresponding inverter inputs.

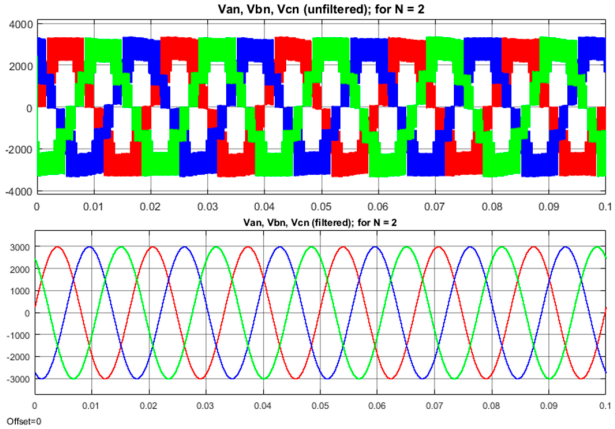

Figure 23. Despite different dc-link voltages the output phase voltages are controlled for grid synchronization.

Figures 24 and 25 show how the NPC inverter ports improve the output ac waveform in terms of THD. The experimental results, obtained from two 3.34 kW prototypes cascaded, are shown in Figures 26 and 27.

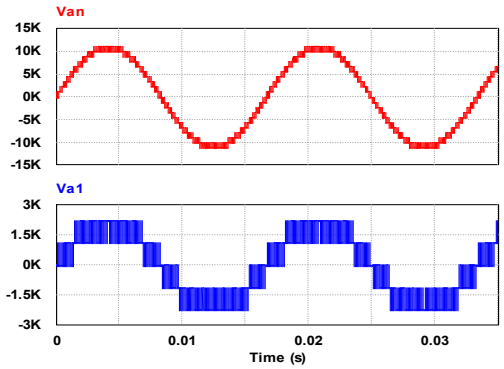

Figure 24. (From top to bottom) 5-port cascaded NPC bridge output waveform v_{an} having 21 levels (THD = 5.76%), 1-port NPC bridge inverter output waveform v_{a1} having five levels (THD = 27.74%); THD values are obtained from simulation.

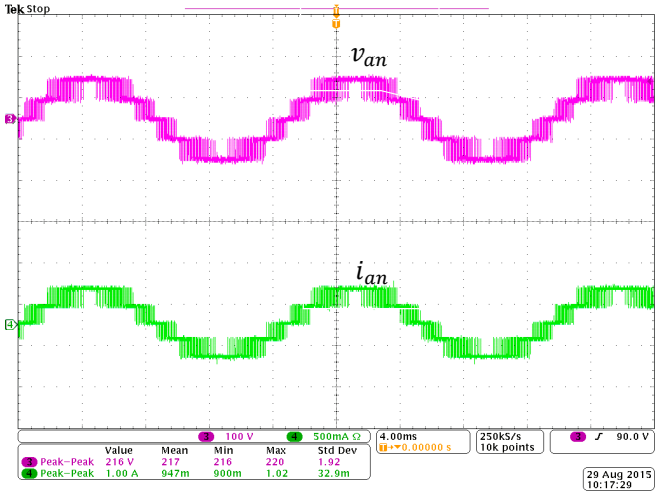

Figure 25. Experimental Output ac voltage (60 Hz, unfiltered) from one NPC inverter (N = 1) port to producing a five ($4N$ + 1) level v_{an}, and corresponding current, i_{an} through a resistive load $R = 500\ \Omega$, where $V_s = V_{PV} = 100$ V.

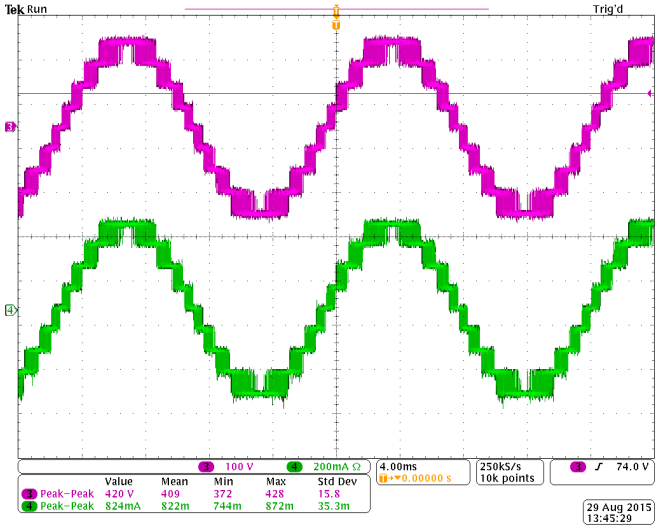

Figure 26. Experimental Output ac voltage and current (60 Hz, unfiltered) when two NPC inverters (N = 2) are cascaded to produce a nine ($4N$ + 1) level v_{an}, and corresponding current, i_{an} through a resistive load $R = 500\ \Omega$, where $V_s = V_{PV} = 100$ V.

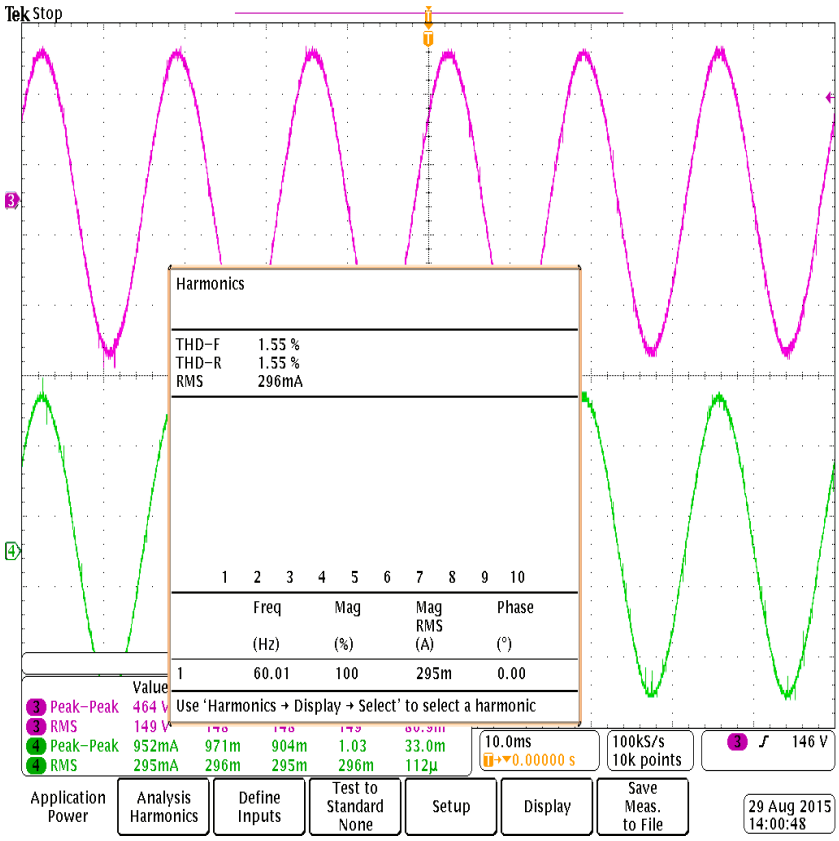

Figure 27. Experimental output ac voltage and current (60 Hz, filtered) when two NPC inverters (N = 2) are cascaded v_{an}, and corresponding current, i_{an} through a resistive load $R = 500\ \Omega$, $L_a = 500$ mH, where $V_s = V_{PV} = 100$ V.

The hardware set-up for one port of 3.34 kW prototype converter (ML-DAB and NPC inverter) is shown in Figure 28 with a resistive-inductive load. The experiments have been performed at a scaled-down power level with a maximum ML-DAB input dc voltage (V_s) of 125 V. The hardware components used in one port of the proposed converter are summarized in Table 5 below.

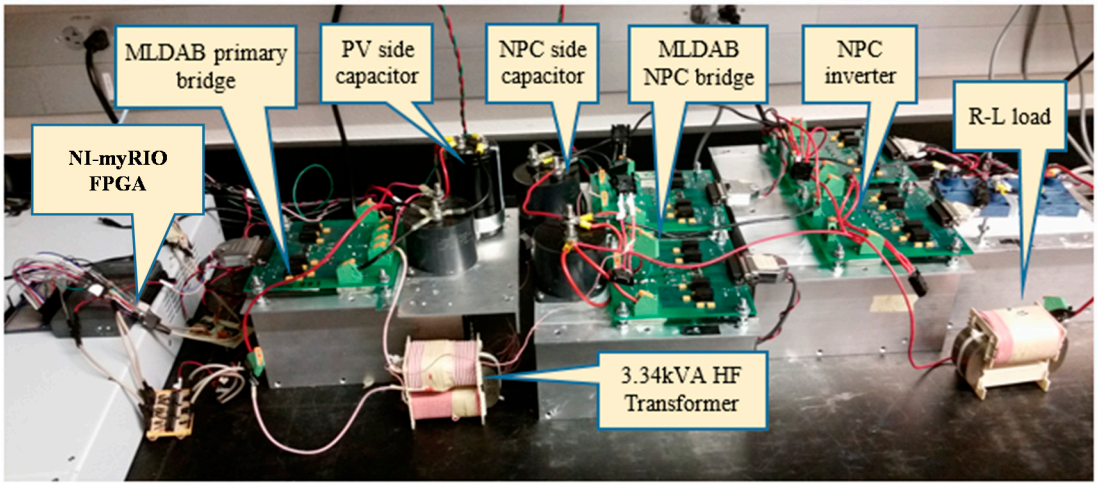

Figure 28. Hardware setup for one port of the ML-DAB and NPC inverter with a resistive-inductive (R-L) load.

Table 5. Hardware component specification for one port of the proposed converter.

Hardware Component		Item Description	Quantity per Port
PV source Emulator		MAGNA Power XR200-10	1
Voltage transducer		SCK-MU-1500V	1
Current Transducer		CR5410-20	1
MPPT controller		NI myRIO-1900®, LabVIEW	1
ML-DAB primary bridge	IGBT (Dual)	Infineon FF100R12YT3	2
	Capacitor	550 V, 1200 µF	1
High frequency transformer	Core Material	Metglass amorphous alloy 2605SA1 AMCC-125	1
	Winding turns ratio	89:509	-
	Winding wire (Round Litz Wire)	Primary: AWG 12-259/36, Secondary: AWG 20-38/30	-
ML-DAB secondary NPC bridge	IGBT (Dual)	Infineon FF100R12YT3	4
	Capacitor	1200 V, 100 µF	2
	Clamping Diode	IXYS DSEP30-12AR	4
NPC Inverter bridge	IGBT (Dual)	Infineon FF100R12YT3	4
	Clamping Diode	IXYS DSEP30-12AR	4
Gate pulse generator	ML-DAB&Inverter	NI myRIO-1900®, LabVIEW	1
Load at output	R-L load	R = 500 Ω, L = 500 mH	1
Waveform measurement	Signal Oscilloscope	Tektronix MSO-4034	1

5. Conclusions

A distributed modular *N*-port converter configuration, using neutral point diode clamped multilevel DAB and cascaded NPC-bridge inverters with high frequency transformer integration, has been presented for utility scale grid-connected PV system. A novel dc-dc multi-level DAB with MPPT scheme is presented as an intermediate dc-dc converter stage. Detailed design of the power stage parameters is shown and the control strategy based on power mismatch among the various ports has been proposed and verified in simulation in PSIM® and Simulink®. Experimental outputs are obtained from two ports of hardware prototype running under laboratory test condition. The steady-state analysis of the converter has been performed both in simulation and using hardware prototypes to validate the power flow and overall performance of the converter.

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Author Contributions: Hariharan Krishnaswami conceived the concept; M.A. Moonem, Turgay Duman performed analysis; Turgay Duman designed and performed the experiments; Shilpa Marti and Hariharan Khrisnaswami analyzed the data; Azas Ahmed Rifath Abdul Kader verified mismatch control algorithm; Hariharan Khrisnaswami mentored students M.A. Moonem, Turgay Duman, Shilpa Marti, and Azas Ahmed Rifath Abdul Kader; M.A. Moonem, and Turgay Duman wrote the paper. All authors approved the final manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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