

Article

A High-Efficiency Isolated LCLC Multi-Resonant Three-Port Bidirectional DC-DC Converter

Cheng-Shan Wang, Wei Li, Yi-Feng Wang * , Fu-Qiang Han [†] and Bo Chen [†]

School of Electrical and Information Engineering, Tianjin University, Tianjin 300072, China;

cswang@tju.edu.cn (C.-S.W.); liweitju@tju.edu.cn (W.L.); hanxinyu@tju.edu.cn (F.-Q.H.); cb92614@126.com (B.C.)

* Correspondence: wayif@tju.edu.cn; Tel.: +86-022-2740-1479

[†] These authors contributed equally to this work.

Received: 13 May 2017; Accepted: 3 July 2017; Published: 5 July 2017

Abstract: In this paper, an isolated multi-resonant three-port bidirectional direct current-direct current (DC-DC) converter is proposed, which is composed of three full bridges, two inductor-capacitor-inductor-capacitor (LCLC) multi-resonant tanks and a three-winding transformer. The phase shift control method is employed to manage the power transmission among three ports. Relying on the appropriate parameter selection, both of the fundamental and the third order power can be delivered through the multi-element LCLC resonant tanks, and consequently, it contributes to restrained circulating energy and the desirable promoted efficiency. Besides, by adjusting the driving frequency under different load conditions, zero-voltage-switching (ZVS) characteristics of all the switches of three ports are guaranteed. Therefore, lower switching loss and higher efficiency are achieved in full load range. In order to verify the feasibility of the proposed topology, a 1.5 kW prototype is established, of which the maximum efficiencies under forward and reverse operating conditions are 96.7% and 96.9% respectively. In addition, both of the bidirectional efficiencies maintain higher than 95.5% when the power level is above 0.5 kW.

Keywords: three-port; bidirectional DC-DC converter; multi-resonant; soft switching

1. Introduction

Nowadays, facing the increasingly severe energy crisis and pollution issues, considerable attention is being focused on renewable power sources to figure out promising solutions [1–3]. However, owing to the time-varying and intermittent output features of some renewable sources, energy storage plays an indispensable role to improve the stability and energy utilization rate of the distributed energy generation system (DEGS) [4–6]. In existing DEGS, the renewable energy sources, storage units and loads are connected together by their independent converters. Therefore, the large number of converters leads to complexity in the DEGS architecture. This issue is addressed by adopting three-port converters, where the efficiency, the cost and the power density are optimized. As a consequence, three-port bidirectional DC-DC converters (TP-BDCs) have become a competitive alternative in recent years.

Based on the connections, the TP-BDCs are simply categorized into three types, namely the non-isolated, the partly-isolated and the isolated converters [7]. For the non-isolated topology, although the direct connection is beneficial for its reduced number of components and compact architecture, this kind of TP-BDC suffers from limited voltage gain, since the voltage conversion ratio can only be adjusted by controlling the duty-ratio of switches [8–10]. In the partly-isolated structures, a transformer is used to isolate one port from the other two ports. Owing to the added transformer, is easier to obtain higher voltage gain with the partly-isolated TP-BDC [11–14]. However, neither non-isolated or partly-isolated TP-BDCs are suitable for applications where the three ports must be completely isolated. Therefore, it is necessary to consider the isolated-type TP-BDC [15,16].

The isolated TP-BDC exhibits pronounced advantages over its two counterparts, since the three-port power exchanges are realized through a three-winding high-frequency transformer, and the completely galvanic isolation is also ensured. Further, among the numerous previously published references [17–24] about isolated TP-BDCs, two more detailed main sub-classifications are used: the triple-active-bridge (TAB) converter shown in Figure 1a and the series-resonant TP-BDC (SR-TP-BDC) in Figure 1b.

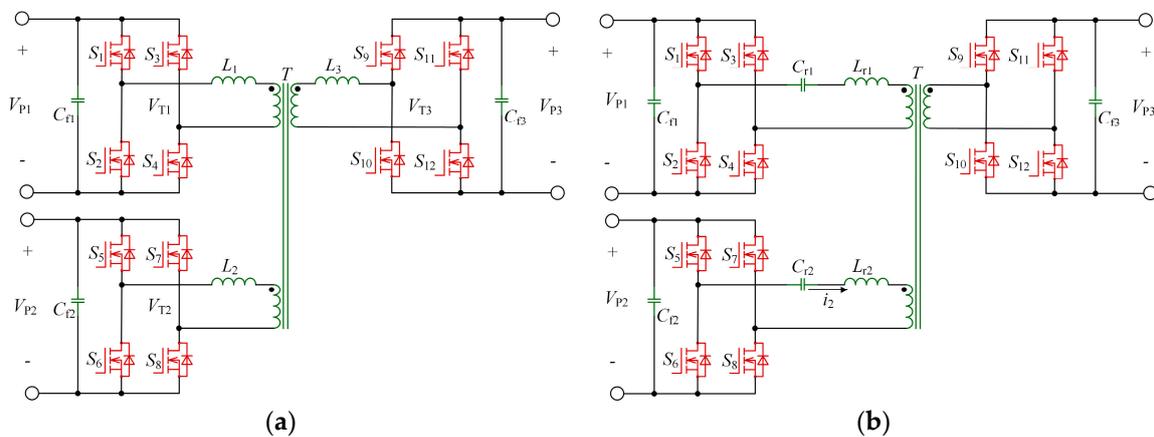


Figure 1. Topology of the isolated TP-BDCs: (a) TAB; (b) TP-SR-BDC.

The TAB converter, a research hotspot, is composed of three active bridges, three inductors and a three-winding transformer [17–21]. It possesses advantages such as galvanic isolation, bidirectional power flow, ZVS operation and phase shift control with fixed switching frequency, while the power coupling among the three ports makes the decoupling matrix essential in its control loop, which is sophisticated and can be detrimental to the reliability of TAB. Moreover, the power transmission in TAB topology is in inverse proportion of the impedance of L_1 – L_3 , and L_1 – L_3 are inherent greater than the leakage inductors of transformer. Consequently, the switching frequency has to be reduced in case of high power levels. In [19–21] the driving frequencies are all 20 kHz, and this will be detrimental for the desired high power density.

The other sub-classification is the series-resonant TP-BDC (SR-TP-BDC) as Figure 1b shows. Compared to TAB, the SR-TP-BDC introduces two additional series-resonant tanks into the primary sides. For one thing, it maintains the main advantages of TAB such as galvanic isolation, bidirectional operation, ZVS features and constant switching frequency [22–24]. For another, the decoupling of the power transmissions successfully relieves the difficulty of control issue. Additionally, another benefit of SR-TP-BDC is that the impedance of SR tanks can be regulated by C_{r1} , L_{r1} , C_{r2} , L_{r2} and the driving frequency together, thus, it can operate with a higher switching frequency with realizable component values under high power level. In [23,24], renewable source, battery and load are integrated to a three-port SR BDC. The driving frequency rises to 100 kHz, which is apparently higher than 20 kHz of TAB [19–21].

In spite of the benefits discussed above, the SR-TP-BDC still needs to be modified due to the loss of ZVS at light load. Since the phase shift angle is small under light load conditions, the energy stored in the series-resonant tanks is unable to fully discharge the switches' output capacitors. In order to improve the operating characteristics of series resonant converter under light load conditions, many studies have been conducted [25–30]. In [29], an additional capacitor is added to the resonant storage to solve the regulation problem in which the output voltage increases as the load current decreases. Moreover, all the advantages of typical inductor-inductor-capacitor (LLC) series-resonant converter (SRC) are maintained in this article. In [30], additional unidirectional switch and pulse width modulation (PWM) are introduced to the traditional half-bridge SRC to limit the operating frequency under light load. Then the light-load efficiency is elevated as the following result. Nevertheless,

both these methods mentioned above are based on the single input and single output converter with frequency modulation method (PFM), and cannot extend to the application of TP-BDCs with the phase shift control method. Another serious drawback of SR-TP-BDC is that the series-resonant storage can only transfer the fundamental power, while the higher order harmonic power, inducing the reactive power, will bring in circulating power and hence sacrifices the nominal efficiency.

To alleviate the aforementioned drawbacks, a novel isolated multi-resonant TP-BDC (MR-TP-BDC) is developed in this article. The LCLC resonant storage exploited in this article has three resonant frequencies, namely a 2nd harmonic parallel resonant frequency and two series resonant frequencies. These two series resonant points, arranged 1st and 3rd, respectively, guarantee the active power deliveries for the fundamental and the third order, by which the circulating energy is constrained. Besides, through properly adjusting the operating frequency for diverse load states, the proposed MR-TP-BDC obtains the fruitful ZVS traits for all the switches of the three ports among whole load range. Finally, a prototype platform is fabricated to verify the theoretical analyses. The article is organized as followings: the operating principles of the proposed converter is given in Section 2. The steady-state analysis is introduced in Section 3. Parameters optimization design is presented in Section 4. Finally, the experimental results are presented in Section 5, and the conclusion is drawn in Section 6. The features of the proposed isolated MR-TP-BDC are:

- (1) The three-port power exchanges are multi-directional, and the centralized phase shift control method is utilized to manage the power flows.
- (2) The transportation of the extra 3rd power contributes to the reduced circulating power.
- (3) ZVS characteristics of all switches in the three ports are guaranteed within the whole load range.
- (4) The proposed converter is proved to have high efficiency among entire load range. High efficiencies of over 95.5% is acquired for bidirectional operation on the condition that the power level is above 0.5 kW. Meanwhile, the highest efficiencies of the forward and reverse modes are 96.7% and 96.9% respectively.

2. Operating Principle of the Proposed Converter

The proposed MR-TP-BDC is presented in Figure 2, and it is made up of four main parts including a three-winding transformer, three full bridges, two MR tanks and three filter capacitors C_{F1} – C_{F3} . Phase shift control method is implemented, the amount and direction of transmitted power is controlled by the phase shift angles. Two switches of the same bridge leg conduct complementarily with fixed duty ratio of 50%. The operating frequency f_s is above the resonant frequency of MR tanks to ensure the converter works only in continuous current mode.

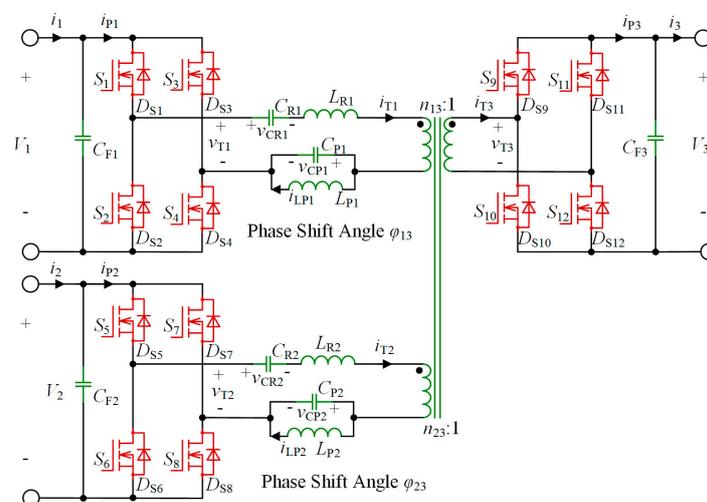


Figure 2. Topology of the proposed isolated MR-TP-BDC.

To simplify the analysis, we assume the voltages of three ports to be constant dc. Therefore, v_{T1} , v_{T2} and v_{T3} are square-waves with amplitudes of $\pm V_1$, $\pm V_2$ and $\pm V_3$, respectively. The phase shift angles of port 1 and 2 are defined as φ_{13} and φ_{23} , and they control the phase shifts among the square wave outputs of the three active bridges. φ_{13} and φ_{23} are defined as positive if v_{T1} and v_{T2} lead v_{T3} , and conversely, φ_{13} and φ_{23} are considered negative.

The MR tanks are made up of C_R , L_R , C_P and L_P , and in order to simplify the parameter design, resonant parameters of port 1 and 2 are set identical. The MR tanks have two series resonant frequencies (SRFs), which are defined as f_r and f_{r3} respectively, and a notch resonant frequency (NRF) f_{r2} . The first SRF f_r helps to deliver the fundamental component energy. To avoid additional power circulation, NRF should be designed at even times of the nominal resonant frequency f_r , and $2f_r$ is selected. The second SRF, placed at $3f_r$, ensures the transfer of the 3rd harmonic power and thus shows significance on circulating energy reduction and efficiency saving.

The parameters are defined as follows: V_1 - V_3 are the voltages of three ports, v_{T1} - v_{T3} are the voltages of the square wave outputs of three active bridges, i_1 - i_3 are the currents of three ports, i_{T1} - i_{T3} are the resonant currents of three ports, i_{P1} - i_{P3} are the currents of three full bridges; v_{CR1} - v_{CR2} are the voltages of C_{R1} and C_{R2} ; v_{CP1} - v_{CP2} are the voltages C_{P1} and C_{P2} ; i_{LP1} - i_{LP2} are the currents of L_{P1} and L_{P2} and P_1 - P_3 are the power of three ports. The positive direction of each value is shown in Figure 2.

Limited by the length of the article, only the operating principle for a certain case is presented, for instance, where the power flows from port 1 and 2 to port 3. In this condition, $\varphi_{13} > \varphi_{23} > 0$, and the theoretical waveforms are as shown in Figure 3.

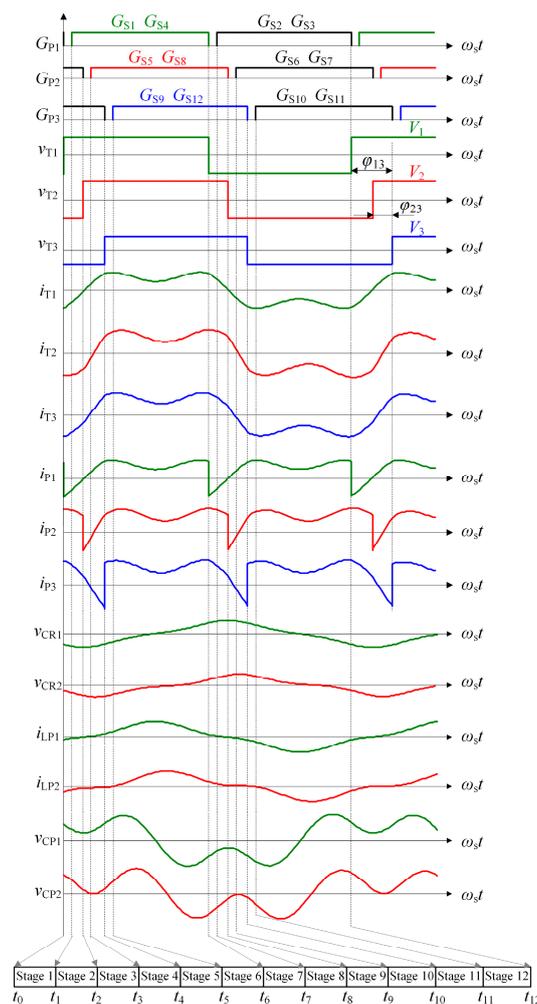


Figure 3. Theoretical waveforms of the proposed MR-TP-BDC.

The dead time is taken into consideration, while the short intervals of the charging and discharging of switches' parasitic output capacitors are neglected. Totally, there are 12 different intervals existing in one switching cycle, and the equivalent circuits of each stage are shown in Figure 4:

Stage 1 (t_0-t_1): This interval begins at the t_0 when S_2 and S_3 are turned off, and it is dead time of port 1. During this interval, S_6 and S_7 , S_{10} and S_{11} are on. Since i_{T1} is negative, it flows through D_{s1} and D_{s4} , the anti-parallel diodes of S_1 and S_4 . i_{T2} flows through S_6 and S_7 , i_{T3} flows through S_{10} and S_{11} . The current flow paths and directions of three ports are shown in Figure 4a. This stage ends at t_1 , when S_1 and S_4 are turned on.

Stage 2 (t_1-t_2): During this stage, S_1 and S_4 , S_6 and S_7 , S_{10} and S_{11} are on. i_{T1} , i_{T2} and i_{T3} flow through S_1 and S_4 , S_6 and S_7 , S_{10} and S_{11} respectively, as shown in Figure 4b. D_{s1} and D_{s4} conduct prior to the main switches of S_1 and S_4 , thus, S_1 and S_4 are turned on with ZVS. This stage ends at t_2 , when S_6 and S_7 are turned off.

Stage 3 (t_2-t_3): This stage is dead time of port 2, S_1 and S_4 , S_{10} and S_{11} are on. i_{T1} and i_{T3} flow through S_1 and S_4 , S_{10} and S_{11} respectively. i_{T2} is negative, so i_{T2} flows through the anti-parallel diodes of S_5 and S_8 . The current flow paths and directions of three ports are shown in Figure 4c, while the current directions of port 1 and 3 change in this interval, so only the current paths of i_{T1} and i_{T3} are given. This interval ends at t_3 , when S_5 and S_8 are turned on.

Stage 4 (t_3-t_4): During this stage, S_1 and S_4 , S_5 and S_8 , S_{10} and S_{11} are on. i_{T1} , i_{T2} and i_{T3} flow through S_1 and S_4 , S_5 and S_8 , S_{10} and S_{11} respectively. D_{s5} and D_{s8} conduct prior to the main switches of S_5 and S_8 , thus, S_5 and S_8 are turned on with ZVS. The operating states of three ports are shown in Figure 4d. In this stage the direction of i_{T2} changes, so only the current path of port 2 are given. This stage ends at t_4 , when S_{10} and S_{11} are turned off.

Stage 5 (t_4-t_5): During this stage, S_1 and S_4 , S_5 and S_8 are on, and this interval is dead time of port 3. i_{T1} and i_{T2} flow through S_1 and S_4 , S_5 and S_8 respectively. i_{T3} is positive, so it flows through the anti-parallel diodes of S_9 and S_{12} . The operating states of three ports are shown in Figure 4e. This interval ends at t_5 , when S_9 and S_{12} are turned on.

Stage 6 (t_5-t_6): During this stage, S_1 and S_4 , S_5 and S_8 , S_9 and S_{12} are on. As shown in Figure 4f, i_{T1} , i_{T2} and i_{T3} flow through S_1 and S_4 , S_5 and S_8 , S_9 and S_{12} respectively. D_{s9} and D_{s12} conduct prior to the main switches of S_9 and S_{12} , thus, S_9 and S_{12} are turned on with ZVS. This stage ends at t_6 , when S_1 and S_4 are turned off.

Stage 7 (t_6-t_7): This stage is dead time of port 1. During this interval, S_5 and S_8 , S_9 and S_{12} are on. Since i_{T1} is positive, it flows through D_{s2} and D_{s3} , the anti-parallel diodes of S_2 and S_3 . i_{T2} flows through S_5 and S_8 , i_{T3} flows through S_9 and S_{12} . The current flow paths and directions of three ports are shown in Figure 4g. This stage ends at t_7 , when S_2 and S_3 are turned on.

Stage 8 (t_7-t_8): During this stage, S_2 and S_3 , S_5 and S_8 , S_9 and S_{12} are on. As shown in Figure 4h, i_{T1} , i_{T2} and i_{T3} flow through S_2 and S_3 , S_5 and S_8 , S_9 and S_{12} respectively. D_{s2} and D_{s3} conduct prior to the main switches of S_2 and S_3 , thus, S_2 and S_3 are turned on with ZVS. This stage ends at t_8 , when S_5 and S_8 are turned off.

Stage 9 (t_8-t_9): This stage is dead time of port 2. During this interval, S_2 and S_3 , S_9 and S_{12} are on. Since i_{T2} is positive, it flows through D_{s6} and D_{s7} , the anti-parallel diodes of S_6 and S_7 . i_{T1} flows through S_2 and S_3 , i_{T3} flows through S_9 and S_{12} . The operating states of three ports are shown in Figure 4i, while the current directions of port 1 and 3 change in this interval, so only the current paths of i_{T1} and i_{T3} are given. This interval ends at t_9 , when S_6 and S_7 are turned on.

Stage 10 (t_9-t_{10}): During this stage, S_2 and S_3 , S_6 and S_7 , S_9 and S_{12} are on. As shown in Figure 4j, i_{T1} , i_{T2} and i_{T3} flow through S_2 and S_3 , S_6 and S_7 , S_9 and S_{12} respectively. In this stage the direction of i_{T2} changes, so only the current path of port 2 is given. D_{s6} and D_{s7} conduct prior to the main switches of S_6 and S_7 , thus, S_6 and S_7 are turned on with ZVS. This stage ends at t_{10} , when S_9 and S_{12} are turned off.

Stage 11 ($t_{10}-t_{11}$): This stage is dead time of port 3. During this interval, S_2 and S_3 , S_6 and S_7 are on. Since i_{T3} is negative, it flows through D_{s10} and D_{s11} , the anti-parallel diodes of S_{10} and S_{11} .

i_{T1} flows through S_2 and S_3 , i_{T2} flows through S_6 and S_7 . The operating states of three ports are shown in Figure 4k. This interval ends at t_{11} , when S_{10} and S_{11} are turned on.

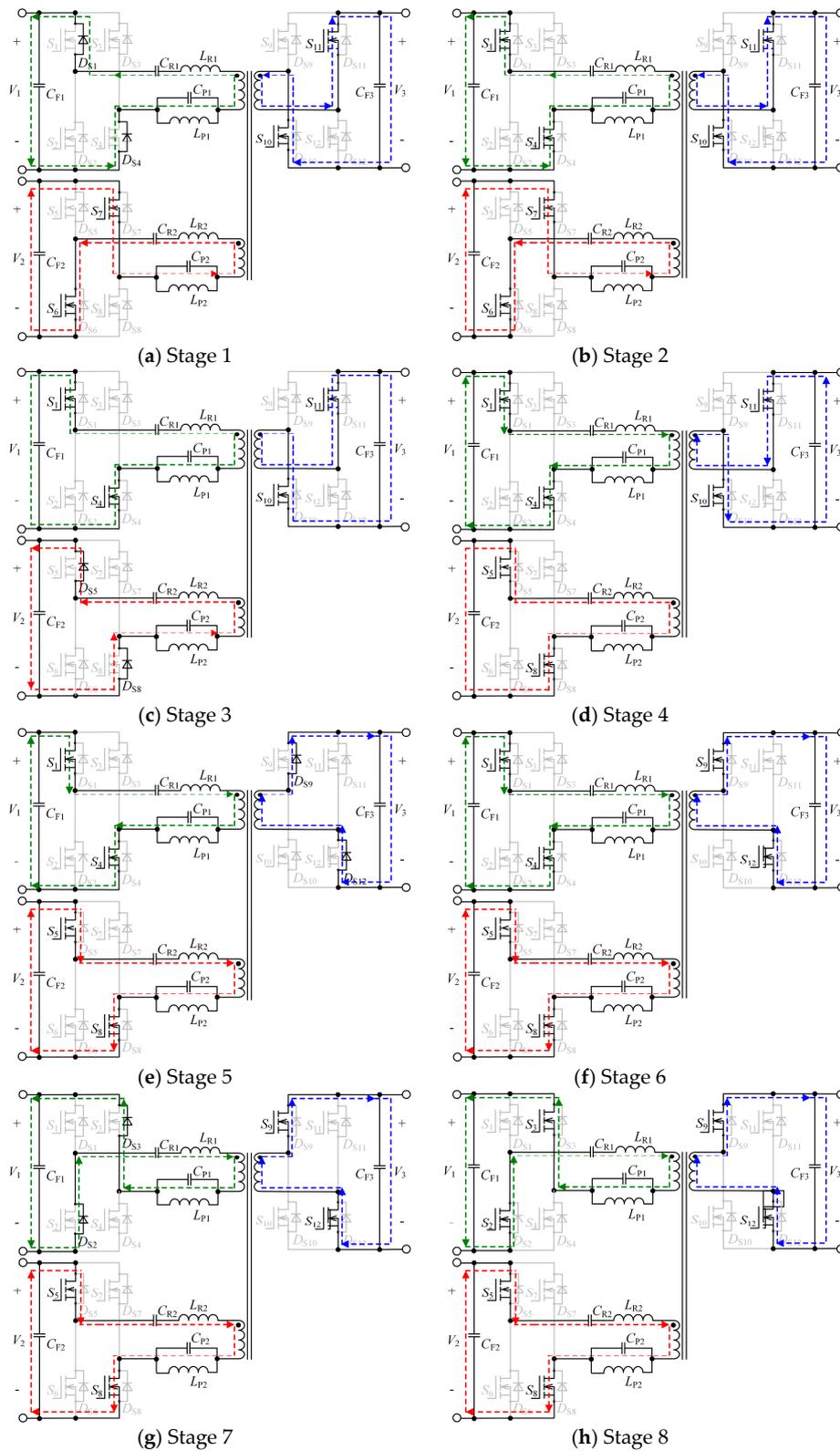


Figure 4. Cont.

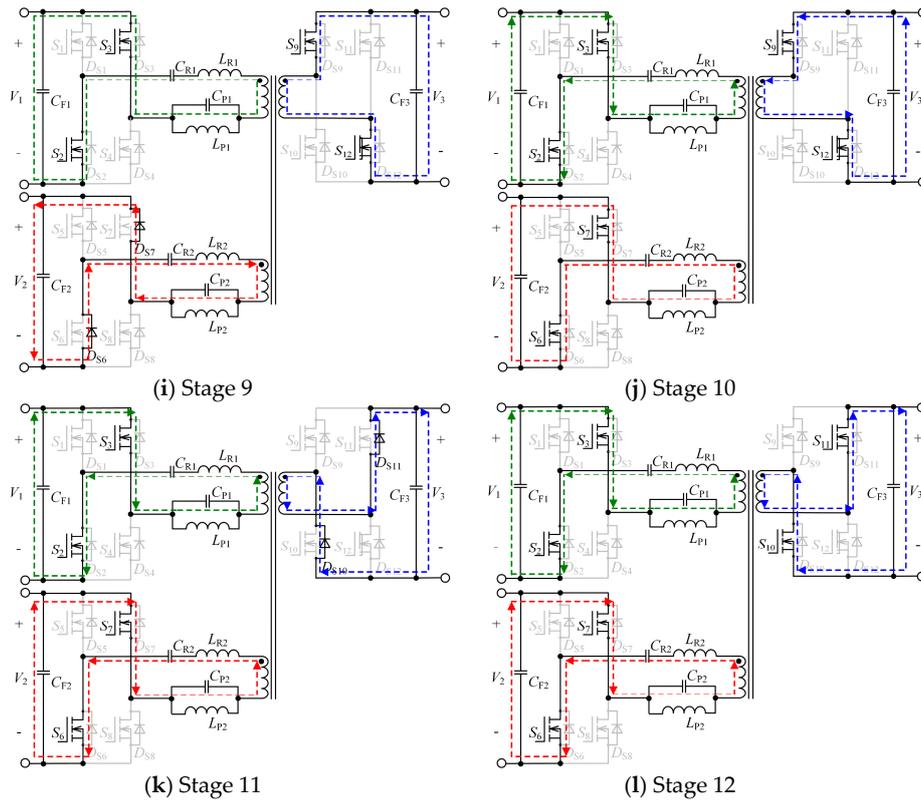


Figure 4. Equivalent circuits of each stage.

Stage 12 (t_{11} – t_{12}): During this stage, S_2 and S_3 , S_6 and S_7 , S_{10} and S_{11} are on. As shown in Figure 4l, i_{T1} , i_{T2} and i_{T3} flow through S_2 and S_3 , S_6 and S_7 , S_{10} and S_{11} respectively. D_{s10} and D_{s11} conduct prior to the main switches of S_{10} and S_{11} , thus, S_{10} and S_{11} are turned on with ZVS. This stage ends at t_{12} , when S_2 and S_3 are turned off.

3. Steady-State Analysis

In this section, the steady-state analysis is conducted for the proposed isolated MR-TP-BDC, including expressions of resonant currents, voltages of resonant capacitors, power transmission among three ports and voltage gains under resistive loads.

3.1. Normalization and Definitions

To simplify the circuit analysis and parameter design, the resonant parameters of port 1 and 2 are assumed to be identical, that is $C_{R1} = C_{R2} = C_R$, $L_{R1} = L_{R2} = L_R$, $C_{P1} = C_{P2} = C_P$ and $L_{P1} = L_{P2} = L_P$. Besides, to facilitate the explanation of the parameter design, all the equations presented are normalized on the basis of Equation (1):

$$V_B = V_3 \quad P_B = P_3 \quad Z_B = V_3^2 / P_B \quad I_B = V_B / Z_B \quad (1)$$

The normalized driving frequency is shown as Equation (2), where ω_s and ω_r are the corresponding angular velocities of f_s and f_r , respectively:

$$F = \frac{\omega_s}{\omega_r} = \frac{f_s}{f_r} \quad (2)$$

The impedance of MR storage under two SRFs (f_r and f_{r3}) are 0, and impedance under NRF (f_{r2}) is infinite. Moreover, the relationships of the three resonant frequencies are: $f_{r2} = 2f_r$, $f_{r3} = 3f_r$.

Thus, the impedance of MR storage under f_r , f_{r2} and f_{r3} are defined as X_{r1} , X_{r2} and X_{r3} , and are deduced in Equation (3):

$$\begin{cases} X_{r1} = \omega_r L_R - \frac{1}{\omega_r C_R} + \frac{\omega_r L_P}{1 - \omega_r^2 L_P C_P} = 0 \\ X_{r2} = 2\omega_r L_R - \frac{1}{2\omega_r C_R} + \frac{2\omega_r L_P}{1 - 4\omega_r^2 L_P C_P} = \infty \\ X_{r3} = 3\omega_r L_R - \frac{1}{3\omega_r C_R} + \frac{3\omega_r L_P}{1 - 9\omega_r^2 L_P C_P} = 0 \end{cases} \quad (3)$$

From (3), the relationship between four resonant parameters are deduced as:

$$C_R = \frac{5}{3}C_P, L_R = \frac{16}{15}L_P, 4\omega_r^2 = C_P L_P \quad (4)$$

The impedance of MR storage under angular velocity ω is:

$$X = \frac{16}{15}\omega L_P - \frac{12\omega^2 L_P}{5\omega} + \frac{4\omega^2 \omega L_P}{4\omega^2 - \omega^2} \quad (5)$$

Combining Equations (4) and (5), the impedance of MR storage under f_s and $3f_s$ can be expressed as Equation (6).

$$\begin{cases} X_{s1,pu} = Q(\frac{16}{15}F - \frac{12}{5F} + \frac{4F}{4-F^2}) \\ X_{s3,pu} = Q(\frac{16}{5}F - \frac{4}{5F} + \frac{12F}{4-9F^2}) \end{cases} \quad (6)$$

where Q is defined as:

$$Q = \frac{\omega_r L_P}{Z_B} \quad (7)$$

3.2. Operating Characteristics with Voltage Source Load

The equivalent circuit of the proposed MR-TP-BDC is presented in Figure 5a, where the three square-wave v_{T1} , v_{T2} and v_{T3} represent the outputs of the active bridges. By transferring all parameters of port 1 and port 2 to port 3, the equivalent circuit can be further simplified as Figure 5b shows. The superscript “'” indicates the transferred parameters. On account of the complexity of MR tank, the proposed MR-TP-BDC has a plurality of resonant components and operating modes. It will be difficult to analyze the circuit with traditional time-domain analysis method. Therefore, Fourier equivalent method is adopted in the following analysis procedure. The accuracy of the calculation is verified by the experimental results.

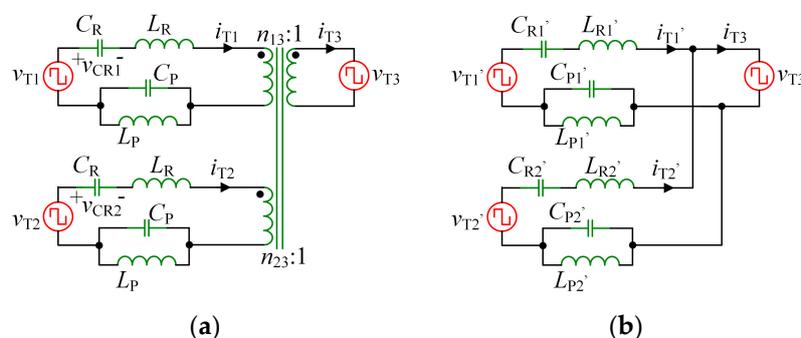


Figure 5. Equivalent circuits for analysis: (a) equivalent circuit of proposed isolated MR-TP-BDC; (b) transformer equivalent model.

In the proposed MR-TP-BDC, all harmonics except the fundamental and third order components of all voltages and currents are neglected. After Fourier decomposition, v'_{T1} , v'_{T2} and v_{T3} are shown as:

$$\begin{cases} v'_{T1,pu}(t) = \frac{4M_1}{\pi} \left[\sin(\omega_s t + \varphi_{13}) + \frac{1}{3} \sin(3\omega_s t + 3\varphi_{13}) \right] \\ v'_{T2,pu}(t) = \frac{4M_2}{\pi} \left[\sin(\omega_s t + \varphi_{23}) + \frac{1}{3} \sin(3\omega_s t + 3\varphi_{23}) \right] \\ v_{T3,pu}(t) = \frac{4}{\pi} \left[\sin \omega_s t + \frac{1}{3} \sin(3\omega_s t) \right] \end{cases} \quad (8)$$

M_1 and M_2 are the voltage gains between port1 and port 3, port 2 and port 3 respectively, and are given by Equation (9):

$$\begin{cases} M_1 = \frac{V_1}{n_{13}V_B} \\ M_2 = \frac{V_2}{n_{23}V_B} \end{cases} \quad (9)$$

Assume the transformer to be ideal, and the transformer voltage is clamped by the voltage of port 3. The currents of port 1 and 2 are decided by their voltage and phase shift angles respectively. The resonance currents shown in Figure 5b are derived as:

$$\begin{cases} i'_{T1,pu}(t) = \frac{4n_{13}^2}{\pi} \left[\frac{\cos(\omega_s t) - M_1 \cos(\omega_s t + \varphi_{13})}{X_{s1,pu}} + \frac{\cos(3\omega_s t) - M_1 \cos(3\omega_s t + 3\varphi_{13})}{3X_{s3,pu}} \right] \\ i'_{T2,pu}(t) = \frac{4n_{23}^2}{\pi} \left[\frac{\cos(\omega_s t) - M_2 \cos(\omega_s t + \varphi_{23})}{X_{s1,pu}} + \frac{\cos(3\omega_s t) - M_2 \cos(3\omega_s t + 3\varphi_{23})}{3X_{s3,pu}} \right] \\ i_{T3,pu}(t) = i'_{T1,pu}(t) + i'_{T2,pu}(t) \end{cases} \quad (10)$$

The normalized impedance of C_R under f_s and $3f_s$ are expressed as Equation (11):

$$\begin{cases} X_{CR1,pu} = \frac{1}{\omega_s C_R Z_B} \\ X_{CR3,pu} = \frac{1}{3\omega_s C_R Z_B} \end{cases} \quad (11)$$

By combining Equations (10) and (11), the voltages of series resonant capacitors are deduced as:

$$\begin{cases} v_{CR1,pu}(t) = \frac{4n_{13}}{\pi} \left[\frac{M_1 \sin(\omega_s t + \varphi_{13}) - \sin(\omega_s t)}{X_{s1,pu}} X_{CR1,pu} + \frac{M_1 \sin(3\omega_s t + 3\varphi_{13}) - \sin(3\omega_s t)}{3X_{s3,pu}} X_{CR3,pu} \right] \\ v_{CR2,pu}(t) = \frac{4n_{23}}{\pi} \left[\frac{M_2 \sin(\omega_s t + \varphi_{23}) - \sin(\omega_s t)}{X_{s1,pu}} X_{CR1,pu} + \frac{M_2 \sin(3\omega_s t + 3\varphi_{23}) - \sin(3\omega_s t)}{3X_{s3,pu}} X_{CR3,pu} \right] \end{cases} \quad (12)$$

For switches in port 1, the ZVS realizing condition is that the resonant storage current lags its applied square wave voltage. For S_1 and S_4 , ZVS will be achieved only on the condition that their currents at the conduction time are negative, while for S_2 and S_3 , resonant current at the conduction time should be positive to guarantee ZVS operating. The ZVS constraint conditions of port 1 are expressed as Equation (13):

$$\begin{cases} i'_{T1,pu} \left(\frac{-\varphi_{13}}{\omega_s} \right) < 0 \quad S_1/S_4 \\ i'_{T1,pu} \left(\frac{-\varphi_{13} + \pi}{\omega_s} \right) > 0 \quad S_2/S_3 \end{cases} \quad (13)$$

According to the properties of the cosine function, the ZVS constraint formulas of the four switches in port 1 are completely equivalent. As a consequence, simple analysis on the ZVS condition for S_1 is enough for port 1. Similarly, ZVS conditions of S_5 and S_9 indicate the ZVS conditions of port 2 and 3. To sum up, the ZVS constraint expressions of three ports are shown in Equation (14):

$$\begin{cases} i'_{T1,pu} \left(\frac{-\varphi_{13}}{\omega_s} \right) = \frac{4n_{13}^2}{\pi} \left[\frac{\cos(\varphi_{13}) - M_1}{X_{s1,pu}} + \frac{\cos(3\varphi_{13}) - M_1}{3X_{s3,pu}} \right] < 0 \\ i'_{T2,pu} \left(\frac{-\varphi_{23}}{\omega_s} \right) = \frac{4n_{23}^2}{\pi} \left[\frac{\cos(\varphi_{23}) - M_2}{X_{s1,pu}} + \frac{\cos(3\varphi_{23}) - M_2}{3X_{s3,pu}} \right] < 0 \\ i_{T3,pu}(0) = \frac{4n_{13}^2}{\pi} \left[\frac{1 - M_1 \cos(\varphi_{13})}{X_{s1,pu}} + \frac{1 - M_1 \cos(3\varphi_{13})}{3X_{s3,pu}} \right] + \frac{4n_{23}^2}{\pi} \left[\frac{1 - M_2 \cos(\varphi_{23})}{X_{s1,pu}} + \frac{1 - M_2 \cos(3\varphi_{23})}{3X_{s3,pu}} \right] > 0 \end{cases} \quad (14)$$

Since the instantaneous output voltages and currents of three active bridges are shown in equations (8) and (10), respectively, the output active power of three ports are shown in Equation (15).

$$\begin{cases} P_{1,pu} = \frac{1}{2\pi} \int_0^{2\pi} v'_{T1,pu}(t) i'_{T1,pu}(t) d(\omega_s t) \\ P_{2,pu} = \frac{1}{2\pi} \int_0^{2\pi} v'_{T2,pu}(t) i'_{T2,pu}(t) d(\omega_s t) \\ P_{3,pu} = P_{1,pu} + P_{2,pu} \end{cases} \quad (15)$$

By substituting Equations (8) and (10) into (15), the output power of three ports are shown in Equation (16):

$$\begin{cases} P_{1,pu} = \frac{8M_1 n_{13}^2}{\pi^2} \left[\frac{\sin \varphi_{13}}{X_{s1,pu}} + \frac{\sin(3\varphi_{13})}{9X_{s3,pu}} \right] \\ P_{2,pu} = \frac{8M_2 n_{23}^2}{\pi^2} \left[\frac{\sin \varphi_{23}}{X_{s1,pu}} + \frac{\sin(3\varphi_{23})}{9X_{s3,pu}} \right] \\ P_{3,pu} = \frac{8M_1 n_{13}^2}{\pi^2} \left[\frac{\sin \varphi_{13}}{X_{s1,pu}} + \frac{\sin(3\varphi_{13})}{9X_{s3,pu}} \right] + \frac{8M_2 n_{23}^2}{\pi^2} \left[\frac{\sin \varphi_{23}}{X_{s1,pu}} + \frac{\sin(3\varphi_{23})}{9X_{s3,pu}} \right] \end{cases} \quad (16)$$

Equation (16) indicates that the powers of port 1 and port 2 are only relative to φ_{13} and φ_{23} , while $P_{3,pu}$ are effected by both φ_{13} and φ_{23} . Figure 6a shows the relationship between $P_{1,pu}$ and φ_{13} , Figure 6b shows the relationship between $P_{2,pu}$ and φ_{23} , while Figure 6c shows $P_{3,pu}$ with varying φ_{13} and φ_{23} .

Equation (16) and Figure 6 indicate that when φ_{13} and φ_{23} are positive, power is transferred from port 1 and port 2 to port 3, while at the converse situation, the power flow is negative. Furthermore, the values of transferred power increases with the increment of phase shift angles.

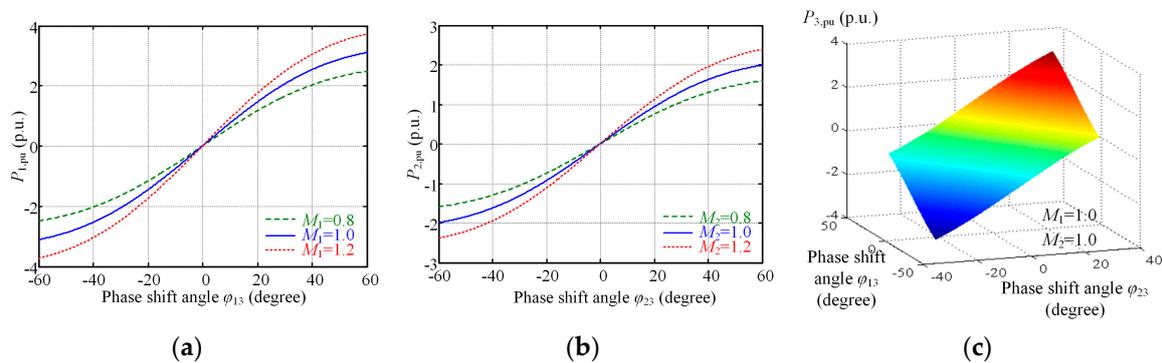


Figure 6. Output power versus phase shift angles: (a) $P_{1,pu}$ versus φ_{13} ; (b) $P_{2,pu}$ versus φ_{23} ; (c) $P_{3,pu}$ versus φ_{13} and φ_{23} .

3.3. Voltage Gain with Resistive Load

In the analysis above, the operating characteristics of the proposed converter under given port voltages are deduced. This section explains the relationship of voltage gain, power transmission and phase shift angles with a resistive load. The voltage gain analyses are divided into two cases.

In the first case, port 1 and 2 are connected to voltage sources of V_1 and V_2 , port 3 is connected to resistive load, and the resistive value is defined as R_3 . At this time, the power is transferred from port 1 and port 2 to port 3, and both φ_{13} and φ_{23} are positive. The power of port 3 is $P_3 = V_3^2 / R_3$. Combing Equation (16), the power of port 3 will be derived as:

$$P_3 = (P_{1,pu} + P_{2,pu}) \frac{V_B^2}{Z_B} = \frac{V_3^2}{R_3} \quad (17)$$

Since the base values for normalization in Equation (1) are the operating parameters of port 3, Equation (17) uses the actual electric values rather than the normalized ones. Combining (16) and (17), the output power in this condition can be expressed as Equation (18):

$$V_3 = \frac{8n_{13}V_1R_3}{\pi^2} \left[\frac{\sin \varphi_{13}}{X_{s1}} + \frac{\sin(3\varphi_{13})}{9X_{s3}} \right] + \frac{8n_{23}V_2R_3}{\pi^2} \left[\frac{\sin \varphi_{23}}{X_{s1}} + \frac{\sin(3\varphi_{23})}{9X_{s3}} \right] \quad (18)$$

where X_{s1} and X_{s3} are the impedance values of MR tanks under fundamental frequency and third order frequency, respectively, and $X_{s1} = X_{s1,pu} \times Z_B$, $X_{s3} = X_{s3,pu} \times Z_B$.

In another case, port 3 is connected to a voltage source, and resistive loads R_1 and R_2 are connected to port 1 and 2, respectively. In this condition, power is transferred from port 3 to port 1 and 2, and both φ_{13} and φ_{23} are negative. The power of port 1 and 2 are expressed as: $P_1 = V_1^2/R_1$ and $P_2 = V_2^2/R_2$. By combining Equation (16), P_1 and P_2 are derived as:

$$\begin{cases} P_1 = P_{1,pu} \times \frac{V_B^2}{Z_B} = \frac{V_1^2}{R_1} \\ P_2 = P_{2,pu} \times \frac{V_B^2}{Z_B} = \frac{V_2^2}{R_2} \end{cases} \quad (19)$$

where $V_1 = n_{13}M_1V_B$, $V_2 = n_{23}M_2V_B$. Then the voltage gains of port 1 and 2 in this condition are deduced as:

$$\begin{cases} M_1 = \frac{8R_{1,pu}}{\pi^2} \left[\frac{\sin|\varphi_{13}|}{X_{s1,pu}} + \frac{\sin|3\varphi_{13}|}{9X_{s3,pu}} \right] \\ M_2 = \frac{8R_{2,pu}}{\pi^2} \left[\frac{\sin|\varphi_{23}|}{X_{s1,pu}} + \frac{\sin|3\varphi_{23}|}{9X_{s3,pu}} \right] \end{cases} \quad (20)$$

and $R_{1,pu} = R_1/Z_B$, $R_{2,pu} = R_2/Z_B$.

4. Design Parameter Optimization

Same as the other resonant converters, the optimization for the resonant parameters is of great importance, since the operating characteristics of the proposed converter are mainly affected by these parameters. The design requirements of the proposed converter are shown as follows:

Port 1: $V_1 = 200$ V, $P_1 = 1000$ W;

Port 2: $V_2 = 160$ V, $P_2 = 500$ W;

Port 3: $V_3 = 400$ V, $P_3 = 1500$ W.

The parameters which need to be optimized include the transformer ratio, values of resonant components and driving frequency. The optimization objectives are ZVS range, peak value of resonant currents, voltage stress of resonant capacitors and cutoff current of switches. And the parameters are optimized in detail in the following.

Since the voltage of transformer is clamped by the voltage of port 3, there is no direct power interaction between port 1 and port 2. It is feasible to decompose the proposed MR-TP-BDC into two single input MR-BDCs, and the design principles of port 1 and port 2 are identical. To simplify the analysis, the operating characteristics of single input MR-BDC are analyzed in this section.

4.1. Transformer Ratio Optimization

The transformer turn ratio affects voltage gain M_1 and M_2 as shown in Equations (8) and (9). Furthermore, Equation (14) indicates the voltage gains directly influence the ZVS realization ranges of three ports. Since there is no direct power interaction between port 1 and port 2, the ZVS realization ranges of port 1 and 3 under single input condition are efficient to analyze the relationship between voltage gain and ZVS region.

The ZVS constraint conditions of three ports are given in (14). In the condition of single input, the ZVS realization conditions of port 1 and 3 are $i'_{T1,pu}(-\varphi_{13}/\omega_s) < 0$ and $i'_{T1,pu}(0) > 0$ respectively. The ZVS regions of port 1 and port 3 under varying M_1 are shown in Figure 7a,b.

Figure 7a indicates that when M_1 is less than or equal to 1, all the switches in port 1 can realize ZVS. When M_1 is greater than 1, switches in port 1 cannot realize ZVS unless φ_{13} (output power) is greater than a certain value. While for port 3 shown in Figure 7b, conditions are exactly contrary to port 1. When M_1 is less than 1, switches in port 3 can only realize ZVS only when the phase shift angle is greater than a certain value. It can be obtained that, the ZVS realization regions of port 1 and port 3 change reversely under varying M_1 , so during the design process, M_1 should be as close to 1 as possible, and $M_1 = 1$ is the best choice to achieve ZVS for all the switches of port 1 and 3.

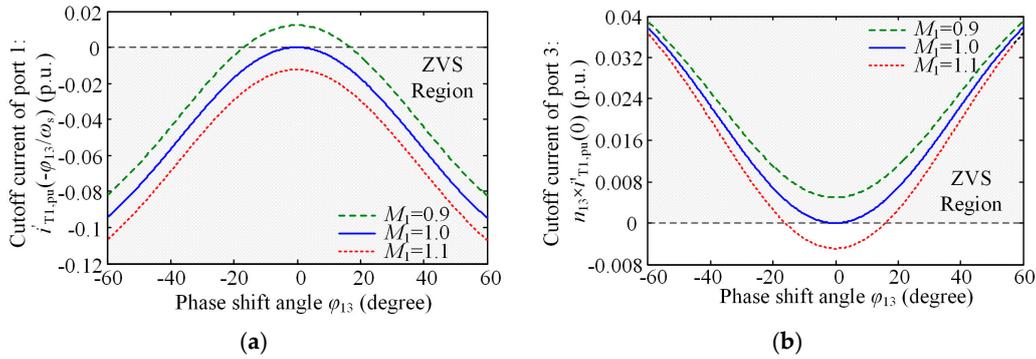


Figure 7. ZVS realization regions of port 1 and port 3 under varying M_1 : (a) port 1; (b) port 3.

Conditions of port 2 are exactly the same with port 1, and $M_1 = M_2 = 1$ are the optimal voltage gains to guarantee ZVS operation of all switches of proposed isolated MR-TP-BDC. According to the given voltages of three ports and voltage gains, turn ratios of transformer are defined as: $n_{13}:n_{23}:1 = 0.5:0.4:1$.

4.2. Resonant Components Optimization

The MR storage in the proposed converter consists of four resonant elements: resonant capacitors C_R and C_P , resonant inductors L_R and L_P . While there are constraint relations between the four resonant elements as shown in Equation (4). This will greatly reduce the difficulty of parameters design. In the following parameters design process, L_P is selected as the optimization variable. In the considered single-input converter, $P_{1,pu} = P_{3,pu}$, $i_{T1,pu}(t) = i'_{T1,pu}(t)/n_{13}$, $i'_{T1,pu}(-\varphi_{13}/\omega_s) = -i_{T3,pu}(0)$.

With given voltage gains, resonant parameters and driving frequency, the phase shift angle φ_{13} , which can provide certain $P_{1,pu}$, will be derived by solving Equation (16). Then substitute φ_{13} into (10), the corresponding cutoff current is expressed as $i_{T1,pu}(-\varphi_{13}/\omega_s) = i'_{T1,pu}(-\varphi_{13}/\omega_s)/n_{13}$. Through using the function of seeking maximum value in MATLAB (Mathworks, Natick, MA, USA), the peak value of resonant current is acquired, and expressed as $I_{T1max,pu} = \max[i'_{T1,pu}(t)]/n_{13}$.

Figure 8 shows the peak value of resonant current $I_{T1max,pu}$, peak value of resonant capacitor voltage $V_{CR1max,pu}$ and cutoff current of port 1 $i_{T1,pu}(-\varphi_{13}/\omega_s)$ versus $P_{1,pu}$ under varying L_P . In the designing process, $P_1 = 1000\text{ W}$, $P_B = P_3 = 1500\text{ W}$, therefore, the maximum value of $P_{1,pu}$ is 0.67.

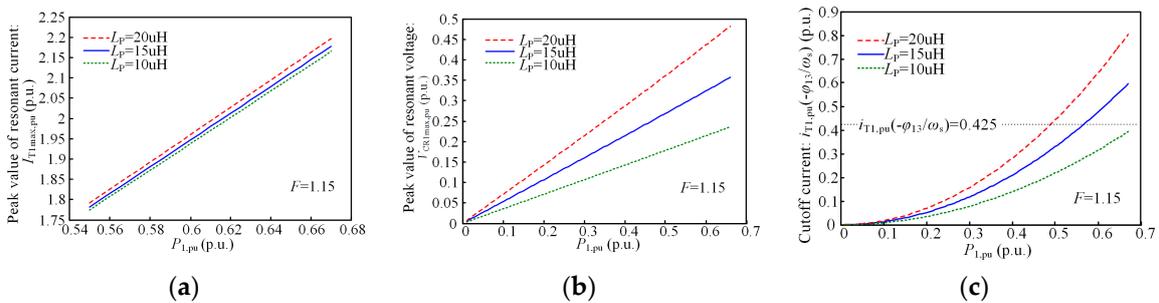


Figure 8. Circuit operating characteristics versus $P_{1,pu}$ under varying L_P : (a) $I_{T1max,pu}$; (b) $V_{CR1max,pu}$; (c) $i_{T1,pu}(-\varphi_{13}/\omega_s)$.

Figure 8 indicates that the peak value of resonant current, peak value of resonant capacitor voltage and cutoff current increase L_P increases. From the point of view of reducing the power loss of proposed MR-TP-BDC, L_P should be chosen as small as possible. Meanwhile, the converter will lose its ZVS property when the cutoff current is very small. In this condition, the energy stored in the MR storage is not enough to get the output capacitor of metal-oxide-semiconductor field effect transistor (MOSFET) completely discharged. Therefore, the critical cutoff current value, which guarantee ZVS of converter, should be deduced.

The analysis above indicates that $M_1 = M_2 = 1$ are the optimal voltage gains to guarantee ZVS operation of all switches of proposed isolated MR-TP-BDC. Equation (14) shows the ZVS constraint expressions of three ports. While, the aforementioned conclusions are all based on ideal MOSFETs and the output capacitors of MOSFETs are neglected. However, in the actual experimental processes, the energy stored in the resonant tanks must be enough to get the output capacitors fully discharged during the dead time. Hence the cutoff current must be high enough to achieve ZVS condition.

When the MOSFETs are turned off, their drain-source voltages are equal to their respective port voltages. On the basis of the utilized design method, port 3 has the highest voltage of 400 V, and thus the output capacitors of MOSFETs in ports 3 store most energy in their cut-off stage. Besides, port 3 has the highest voltage, which means a smaller winding current. Hence the ZVS realization conditions of switches in port 3 are the most difficult. Moreover, the discharging current of the switch parasitic output capacitor of port 3 decreases when power is transferred from port 3 to port 1. Figure 9 shows the critical ZVS condition of switches in port 3 under the most severe situation. In this condition, output capacitor of S_9 is just completely discharged when the resonant current decreases to zero. The corresponding cutoff current is defined as I_{tomin} , which is the minimum cutoff current to guarantee ZVS operation of port 3.

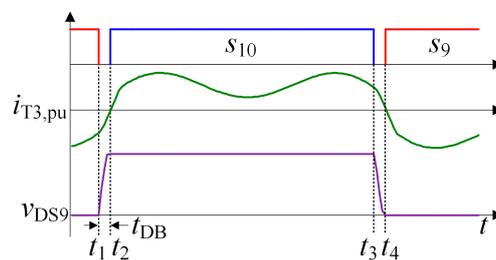


Figure 9. Critical ZVS realization process of switches in port 3.

In Figure 9, t_1-t_2 and t_3-t_4 are the dead time of port 3. At t_3 , S_{10} is turned off, and the output capacitors of S_9 and S_{10} begin to get discharged and charged, respectively. The values of charging and discharging current of S_9 and S_{10} are all $i_{T3,pu}(t)/2$. During t_3-t_4 , $i_{T3,pu}(t)$ is assumed to be decrease linearly. According to the discharging formula of capacitor, the voltage changing process of S_9 can be expressed as:

$$v_{DS9}(t_4) - v_{DS9}(t_3) = -\frac{1}{2C_{oss}} \int_{t_3}^{t_4} i_{T3,pu}(t) dt \quad (21)$$

Thus, the critical ZVS condition of S_9 shown in Figure 9 is derived as:

$$V_3 = \frac{1}{2C_{oss}} \times \frac{1}{2} I_{tomin} \times t_{DB} \quad (22)$$

where C_{oss} is the parasitic output capacitor of switches and t_{DB} represents the dead time. For the MOSFET selected in this article, the value of parasitic output capacitor under 0–400 V voltage range is 150 pF. The dead time is chosen as 200 ns. By substituting C_{oss} and t_{DB} into (22), I_{tomin} is derived as

1.2 A. Since the power distribution among three ports are: $P_1:P_2:P_3 = 2:1:3$, then the minimum cutoff current assigned to port 1 is approximated as:

$$I_{tomin1,pu} = \frac{2}{3n_{13}} \frac{I_{tomin}}{I_B} = 0.425 \quad (23)$$

To ensure the converter efficiency under rated power state, the cutoff current should be minimized on the premise of realizing ZVS. Figure 8c shows that, when $L_P = 10 \mu\text{H}$, the cutoff current of port 1 is $i_{T1,pu}(-\varphi_{13}/\omega_s) = 0.40$ and it doesn't satisfy the ZVS constraint shown in (23). When $L_P = 15 \mu\text{H}$, $i_{T1,pu}(-\varphi_{13}/\omega_s) = 0.59$, ZVS operation can be guaranteed. What's more, the peak value of resonant current and resonant capacitor voltage are $I_{T1max,pu} = 2.18$ and $V_{CR1max,pu} = 0.37$ respectively, and both of them are in a reasonable range. To sum up, $L_P = 15 \mu\text{H}$ is selected in the proposed isolated MR-TP-BDC.

4.3. Driving Frequency Optimization

Equation (6) indicates that the MR storage impedances under fundamental and third order frequencies change under varying F . The operating characteristics of the proposed converter should be compared under different F . The peak value of resonant current $I_{T1max,pu}$, peak value of resonant capacitor voltage $V_{CR1max,pu}$ and cutoff current of port 1 $i_{T1,pu}(-\varphi_{13}/\omega_s)$ are plotted by MATLAB and are shown in Figure 10.

Figure 10 shows that the effects of F on $I_{T1max,pu}$ and $V_{CR1max,pu}$ are small and can be neglected. While the cutoff current $i_{T1,pu}(-\varphi_{13}/\omega_s)$ increases obviously with the increase of F . The ZVS constraint deduced in 4.2 is also shown in Figure 10c. If $F = 1.15$ is adopted in the full load range, ZVS properties will be missed. Therefore, to ensure optimal efficiency under full load range, driving frequency should increase with the decrease of power level. Values of F under the rated and half load conditions are selected as 1.15 and 1.35, respectively.

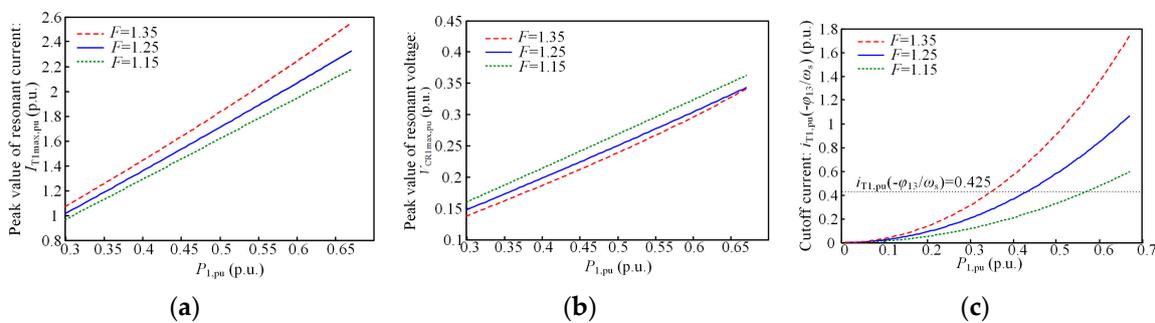


Figure 10. Circuit operating characteristics versus $P_{1,pu}$ under varying F : (a) $I_{T1max,pu}$; (b) $V_{CR1max,pu}$; (c) $i_{T1,pu}(-\varphi_{13}/\omega_s)$.

5. Experimental Results

To verify the feasibility of the proposed topology and the accuracy of the theoretical analysis, a 1.5 kW prototype is built and tested in the laboratory. The MOSFETs adopted in the system is C3M0065090D manufactured by CREE (Durham, NC, USA). The DSP TMS320F28379D from Texas Instruments (Dallas, TX, USA) is employed as the digital controller. The optimized parameters of the proposed converter are selected and shown in Table 1. In the experiments P_1 , P_2 and P_3 are defined as positive when power flows from port 1 and port 2 to port 3, and vice versa.

Table 1. Parameters of the proposed system.

Converter Parameter	Value
Port 1 voltage/power	200 V/1000 W
Port 2 voltage/power	160 V/500 W
Port 3 voltage/power	400 V/1500 W
Transformer turns ratio $n_{13}:n_{23}:1$	0.5:0.4:1
Series resonant inductor L_R	16 μ H
Notch resonant inductor L_P	15 μ H
Series resonant capacitor C_R	80 nF
Notch resonant capacitor C_P	48 nF
Resonant frequency f_r	95 kHz
Driving frequency f_s	110~130 kHz

5.1. Forward Operating Mode

Experimental results under rated and half load positive conditions are evaluated. In the rated positive mode, port 1 and 2 are connected to voltage sources of 200 V and 160 V, respectively. A resistive load of 106 Ω is connected to port 3. In this experiment, power flows from port 1 and 2 to port 3, v_{T1} and v_{T2} lead v_{T3} . The specific data of this experiment are given as follows: input voltage $V_1 = 200$ V, $V_2 = 160$ V; output voltage $V_3 = 398$ V; driving frequency $f_s = 110$ kHz, $\varphi_{13} = 14.2^\circ$, $\varphi_{23} = 11.1^\circ$; $P_1 = 1015$ W, $P_2 = 497$ W, $P_3 = 1455$ W. The efficiency is 96.2%.

Waveforms of output voltage and current of port 3 are shown in Figure 11a. i_{T1} , i_{T2} and i_{T3} are currents of three transformer windings and are presented in Figure 11b. Figure 12a–d show the operating waveforms of port 1, such as i_{T1} , and the drain-source voltages and the driving signals of S_1 and S_3 $v_{DS,S1}$, $v_{G,S1}$, $v_{DS,S3}$ and $v_{G,S3}$. Figures 12e–h and 12i–l show waveforms of port 2 and port 3 respectively. Figure 12b,d,f,h,j,l are zoomed-in versions of Figure 12a,c,e,g,i,k. It can be obtained from the zoom-in figures that the drain-source voltages of MOSFETs decrease to zero before their driving signals turn to positive. Furthermore, $v_{G,S1}$ and $v_{G,S5}$ turn positive when i_{T1} and i_{T2} are negative, $v_{G,S3}$ and $v_{G,S7}$ turn positive when i_{T1} and i_{T2} are positive. $v_{G,S9}$ turns positive when i_{T3} is positive, and $v_{G,S11}$ turns positive when i_{T3} is negative. The above-mentioned facts prove that S_1 and S_3 of port 1, S_5 and S_7 of port 2 and S_9 and S_{11} realize ZVS successfully, which means all the three-port switches achieve the desirable ZVS feature.

Figures 13 and 14 show waveforms under half load positive mode. In this condition, voltage sources of 200 V and 160 V are supplied to port 1 and port 2, respectively. The load resistance connected to port 3 is 213 Ω . In this experiment, output voltage $V_3 = 399$ V; driving frequency $f_s = 130$ kHz, $\varphi_{13} = 15.8^\circ$, $\varphi_{23} = 10.3^\circ$; $P_1 = 549$ W, $P_2 = 230$ W, $P_3 = 747$ W; the efficiency is 95.8%.

Waveforms of output voltage and current of port 3 are shown in Figure 13a. Figure 13b shows waveforms of three transformer windings. Figure 14a,b, Figure 14c,d and Figure 14e,f demonstrate waveforms of port 1, port 2 and port 3. Like the experimental results shown in Figure 12, ZVS is achieved for all switches of the three ports.

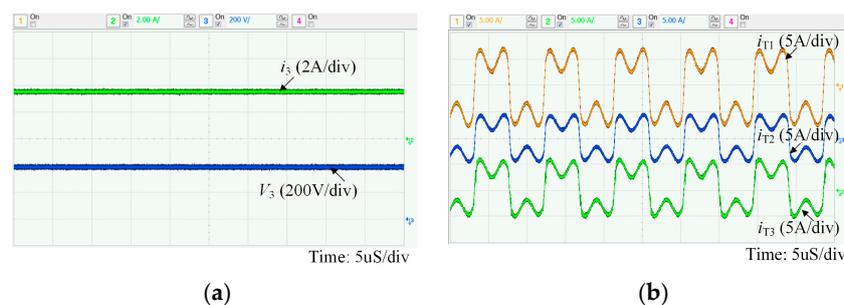


Figure 11. Experimental results of MR-TP-BDC under forward rated condition: (a) output voltage and current of port 3; (b) resonant currents of three ports.

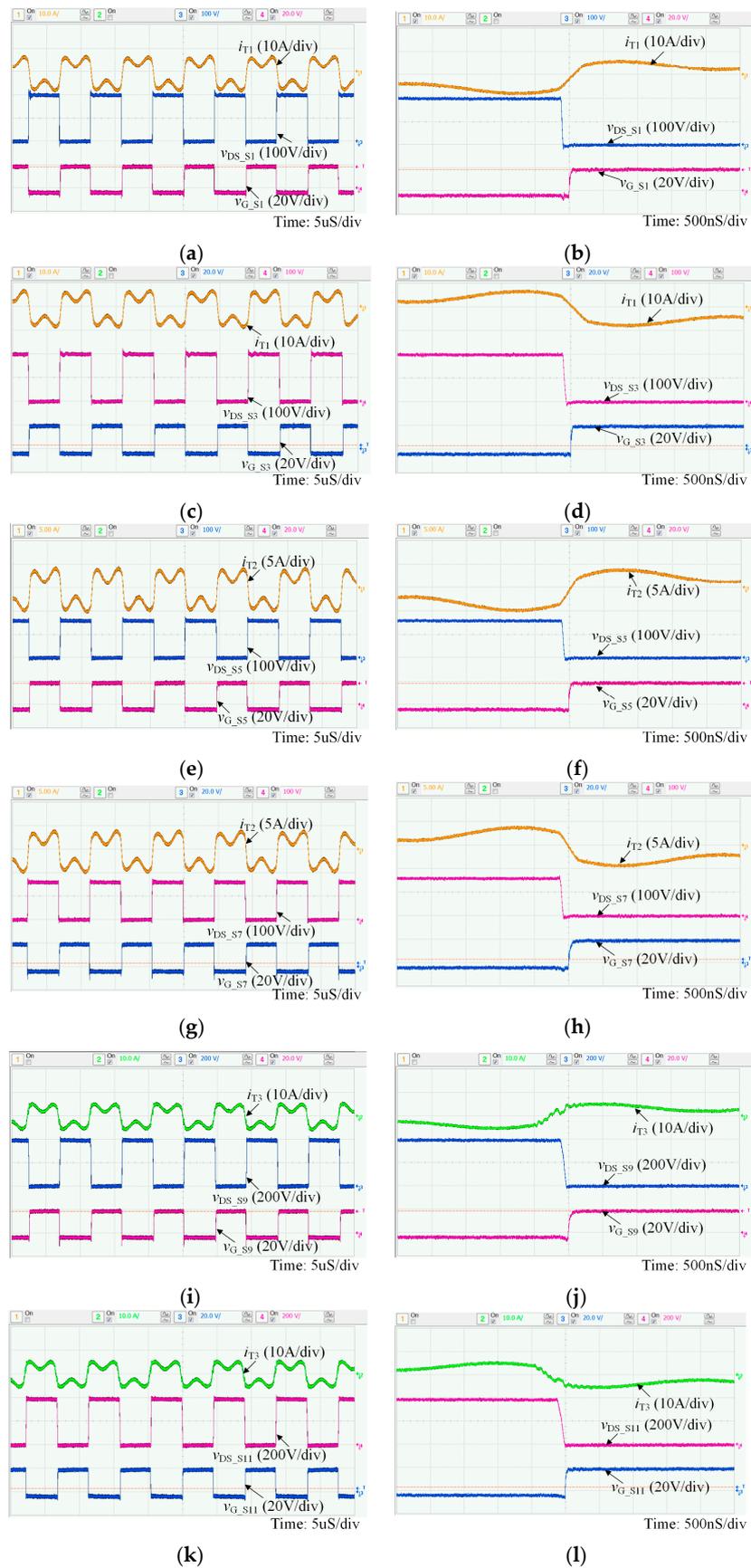


Figure 12. Experimental results of MR-TP-BDC under forward rated condition: (a–d) port 1; (e–h) port 2; (i–l) port 3.

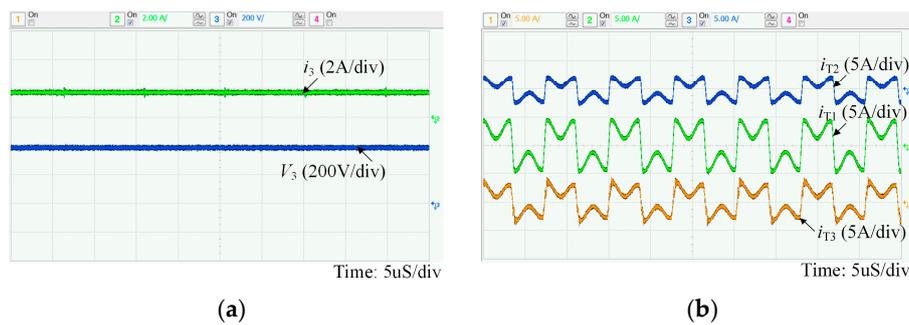


Figure 13. Experimental results of MR-TP-BDC under forward half load operating mode: (a) output voltage and current of port 3; (b) resonant currents of three ports.

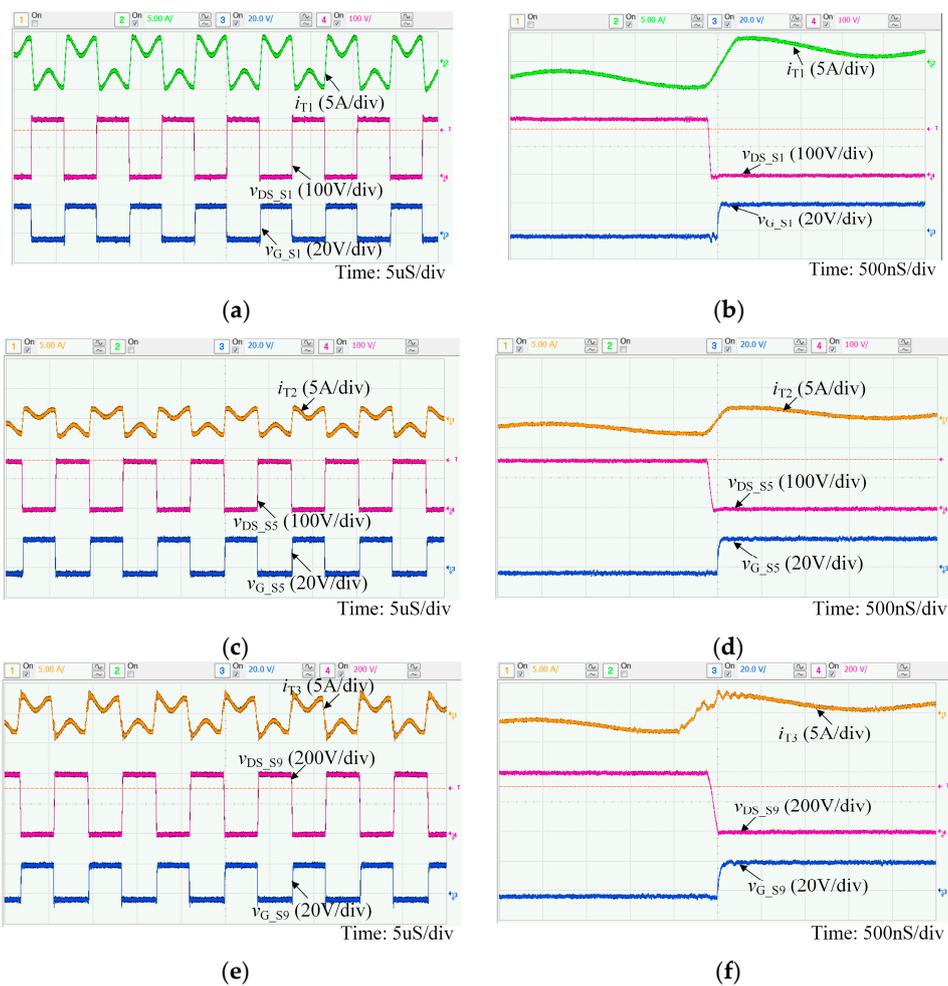


Figure 14. Experimental results of MR-TP-BDC under forward half load operating mode: (a,b) port 1; (c,d) port 2; (e,f) port 3.

5.2. Reverse Operating Mode

In the negative operating mode, 400 V voltage source is supplied to port 3 and resistive loads are connected to port 1 and port 2. Power is transferred from port 3 to port 1 and port 2, and both φ_{13} and φ_{23} are negative. Experimental results under rated and half load conditions are illustrated.

Under the rated power condition, resistances of port 1 and port 2 are 40 Ω and 50 Ω , respectively. The experimental results are listed as: output voltages $V_1 = 198$ V, $V_2 = 159$ V; driving frequency $f_s = 110$ kHz, $\varphi_{13} = -13.9^\circ$, $\varphi_{23} = -11.4^\circ$; $P_1 = -965$ W, $P_2 = -502$ W, $P_3 = -1520$ W; efficiency is 96.5%.

Figure 15a gives the waveforms of output voltage and current of port 1 and 2. Figure 15b shows the waveforms of resonant currents of three ports.

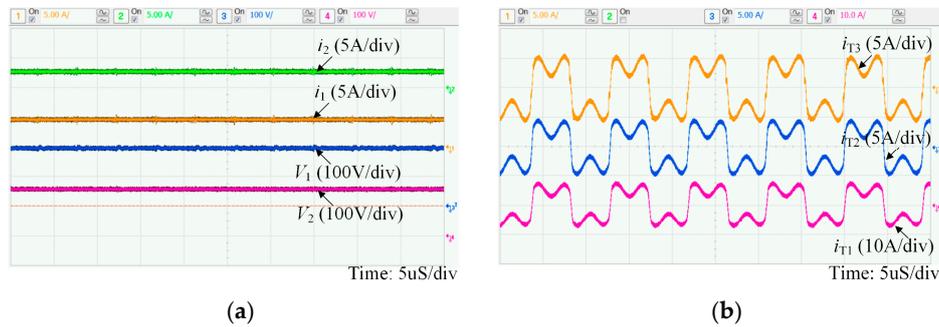


Figure 15. Experimental results of MR-TP-BDC under reverse rated operating mode: (a) output voltage and current of port 1 and port 2; (b) resonant currents of three ports.

Figure 16a demonstrates i_{T1} , v_{DS_S1} and v_{G_S1} of port 1. Figure 16c illustrates i_{T2} , v_{DS_S5} and v_{G_S5} of port 2. Figure 16e shows i_{T3} , v_{DS_S9} and v_{G_S9} of port 3. Figure 16b,d,f are zoomed-in waveforms of Figure 16a,c,e. The waveforms of three ports are consistent with the analysis above, and ZVS is achieved for all MOSFETs of the three ports.

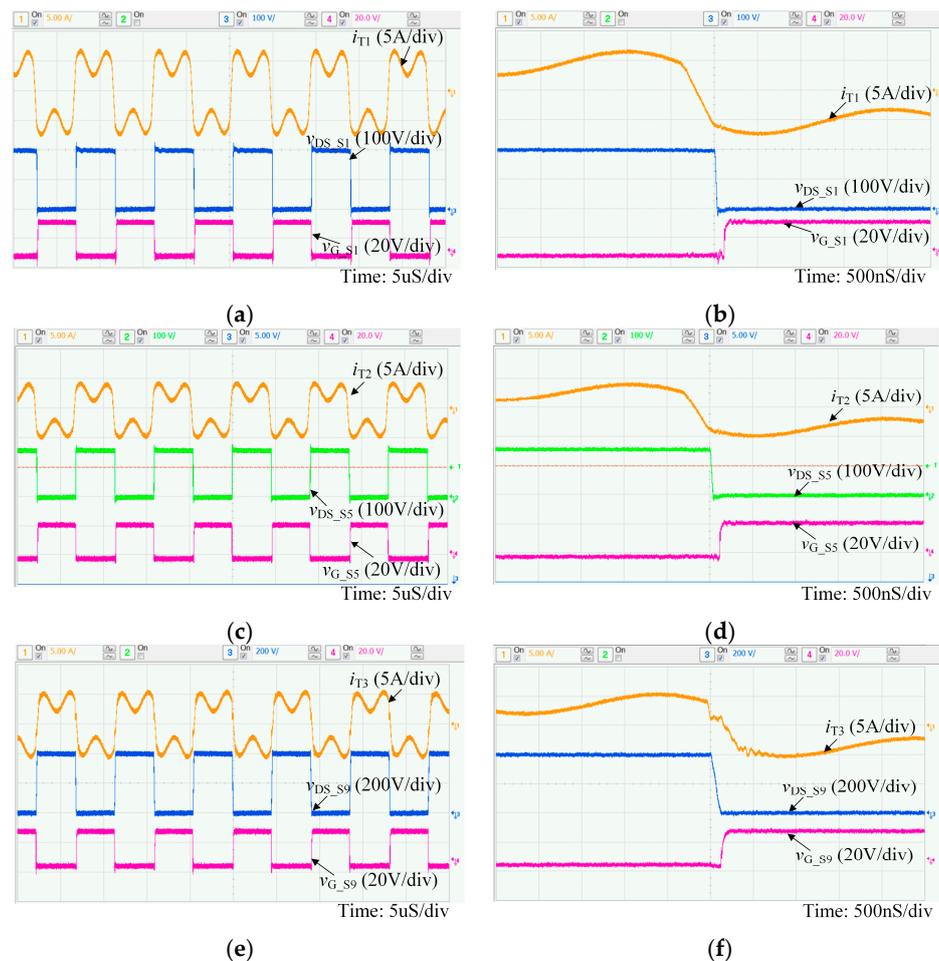


Figure 16. Experimental results of MR-TP-BDC under reverse rated condition: (a,b) port 1; (c,d) port 2; (e,f) port 3.

Under the half power condition, resistances of port 1 and port 2 are $80\ \Omega$ and $100\ \Omega$, respectively. The experimental results are listed as: output voltages $V_1 = 197\ \text{V}$, $V_2 = 159\ \text{V}$; driving frequency $f_s = 130\ \text{kHz}$, $\varphi_{13} = -15.0^\circ$, $\varphi_{23} = -11.3^\circ$; $P_1 = -484\ \text{W}$, $P_2 = -250\ \text{W}$, $P_3 = -764\ \text{W}$; efficiency is 96.0%.

Waveforms of output voltage and current of port 1 and 2 are shown in Figure 17a. Figure 17b shows the waveforms of three transformer windings. The waveforms illustrated in Figure 18 are same those in Figure 16. ZVS is achieved for all the MOSFETs.

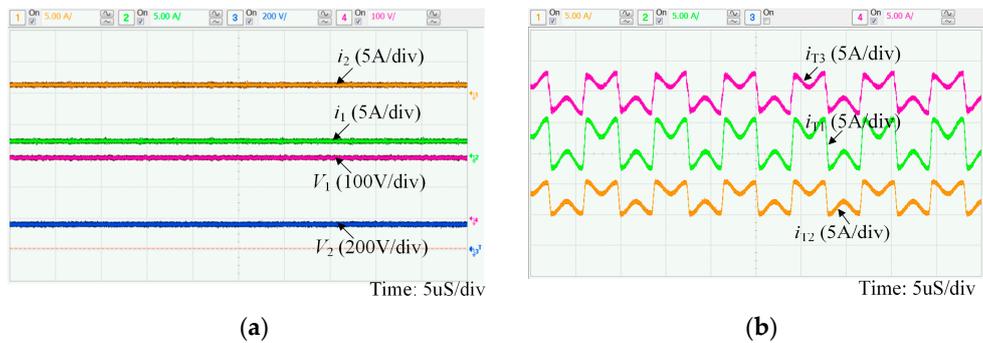


Figure 17. Experimental results of MR-TP-BDC under reverse half load operating mode: (a) output voltage and current of port 1 and port 2; (b) resonant currents of three ports.

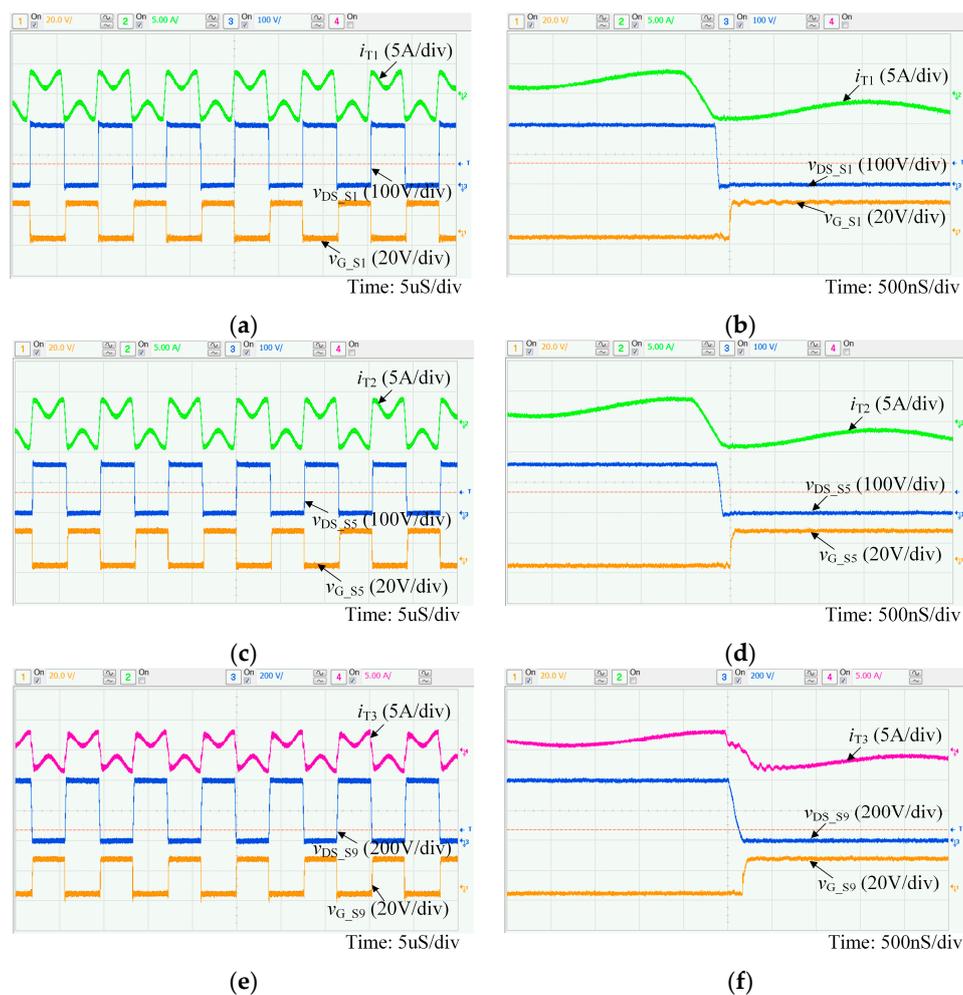


Figure 18. Experimental results of MR-TP-BDC under reverse half load condition: (a,b) port 1; (c,d) port 2; (e,f) port 3.

The comparisons of phase shift angles obtained from theoretical calculation and experiment are given in Table 2. It can be seen that all the values match reasonably close to each other, and this proves the accuracy of the theoretical analysis.

Table 2. Comparison of phase shift angles from theoretical calculation and experiment.

Power Level	Method	ϕ_{13}	ϕ_{23}
Positive 100% (1500 W)	Theory	12.5°	9.7°
	Experiment	14.2°	11.1°
Positive 50% (750 W)	Theory	14.6°	11.2°
	Experiment	15.8°	10.3°
Negative 100% (1500 W)	Theory	−12.5°	−9.7°
	Experiment	−13.9°	−11.4°
Negative 50% (750 W)	Theory	−14.6°	−11.2°
	Experiment	−15.0°	−11.3°

Finally, the measured efficiency curves under positive and negative conditions is shown in Figure 19. The efficiency under rated bidirectional conditions are 96.2% and 96.5%, respectively. The highest efficiency under forward condition is 96.7% at 1.25 kW, and 96.9% under 1 kW in reverse mode. Furthermore, when the power is above 0.5 kW, the efficiencies of both directions are higher than 95.5%. The proposed converter is proved to have high efficiency within entire load range.

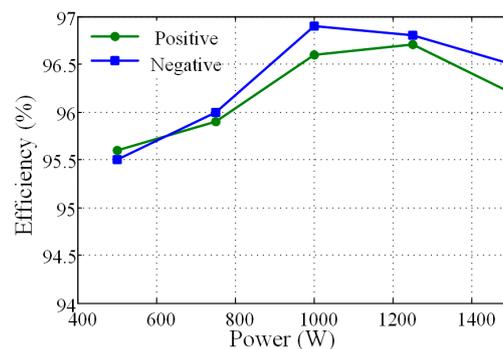


Figure 19. Waveforms of resonant currents of three ports and transformer port voltages.

6. Conclusions

In this paper, a three-port LCLC multi-resonant bidirectional DC-DC converter is developed. Through parameter design, the LCLC possesses two SRFs (f_r and $3f_r$) and a NRF ($2f_r$). Hence, the energy of first and third orders can be delivered through the MR tank, and circulating energy of the resonant tanks is reduced. What's more, by adjusting the driving frequency under different load conditions, ZVS characteristics for all three-port switches are guaranteed among entire load range. Besides, a design procedure with normalized variables is presented. At last, a 1.5 kW prototype is implemented to validate the feasibility and practicability of the proposed converter. Experimental results indicate that the proposed converter presents high efficiency within whole load range. When the power is above 0.5 kW, the bidirectional efficiencies maintains as high as over 95.5%, and the highest efficiencies under forward and reverse conditions are 96.7% and 96.9% respectively.

Acknowledgments: This research was supported by the National High Technology Research and Development Program of China (863 Program) (Grant: 2015AA050603) and supported by Tianjin Municipal Science and Technology Commission (Grant: 14ZCZDGX00035). The authors would also like to thank the anonymous reviewers for their valuable comments and suggestions to improve the quality of the paper.

Author Contributions: Cheng-Shan Wang, Wei Li and Yi-Feng Wang designed the main parts of the study, including the circuit simulation model, topology innovation and simulation development. Fu-Qiang Han and Bo Chen helped in the hardware development and experiment.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Kang, E.C.; Lee, E.J.; Ghorab, M.; Yang, L.; Entchev, E.; Lee, K.-S.; Lyu, N.-J. Investigation of energy and environmental potentials of a renewable trigeneration system in a residential application. *Energies* **2016**, *9*, 760. [[CrossRef](#)]
2. Pérez-Ortiz, M.; Jiménez-Fernández, S.; Gutiérrez, P.; Alexandre, E.; Hervás-Martínez, C.; Salcedo-Sanz, S. A review of classification problems and algorithms in renewable energy applications. *Energies* **2016**, *9*, 607. [[CrossRef](#)]
3. Kim, J.Y.; Kim, H.M.; Kim, S.K.; Jeon, J.H.; Choi, H.K. Designing an energy storage system fuzzy pid controller for microgrid islanded operation. *Energies* **2011**, *4*, 1443–1460. [[CrossRef](#)]
4. Hu, J.; Cheng, K.W.E. Predictive control of power electronics converters in renewable energy systems. *Energies* **2017**, *10*, 515. [[CrossRef](#)]
5. Xu, Q.; Hu, X.; Wang, P.; Xiao, J.; Tu, P.; Wen, C.; Lee, M.Y. A Decentralized Dynamic Power Sharing Strategy for Hybrid Energy Storage System in Autonomous DC Microgrid. *IEEE Trans. Ind. Electron.* **2016**, *64*, 5930–5941. [[CrossRef](#)]
6. Kollimalla, S.K.; Mishra, M.K.; Ukil, A.; Gooi, H.B. DC Grid Voltage Regulation Using New HESS Control Strategy. *IEEE Trans. Sustain. Energy* **2016**, *8*, 772–781. [[CrossRef](#)]
7. Zhang, N.; Sutanto, D.; Muttaqi, K.M. A review of topologies of three-port DC–DC converters for the integration of renewable energy and energy storage system. *Renew. Sustain. Energy Rev.* **2016**, *56*, 388–401. [[CrossRef](#)]
8. Wu, H.; Sun, K.; Ding, S.; Xing, Y. Topology derivation of nonisolated three-port dc–dc converters from DIC and DOC. *IEEE Trans. Power Electron.* **2013**, *28*, 3297–3307. [[CrossRef](#)]
9. Zhu, H.; Zhang, D.; Zhang, B.; Zhou, Z. A nonisolated three-port dc–dc converter and three-domain control method for PV-battery power systems. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4937–4947. [[CrossRef](#)]
10. Chien, L.J.; Chen, C.C.; Chen, J.F.; Hsieh, Y.-P. Novel Three-Port Converter with High-Voltage Gain. *IEEE Trans. Power Electron.* **2014**, *29*, 4693–4703. [[CrossRef](#)]
11. Qian, Z.; Rahman, O.A.; Al-Atrash, H.; Batarseh, I. Modelling and control of three-port DC/DC converter interface for satellite applications. *IEEE Trans. Power Electron.* **2010**, *25*, 637–649. [[CrossRef](#)]
12. Wu, H.; Chen, R.; Zhang, J.; Xing, Y.; Hu, H.; Ge, H. A family of three-port half-bridge converters for a stand-alone renewable power system. *IEEE Trans. Power Electron.* **2011**, *26*, 2697–2706. [[CrossRef](#)]
13. Hu, Y.; Xiao, W.; Cao, W.; Ji, B.; Morrow, D.J. Three-Port DC–DC Converter for Stand-Alone Photovoltaic Systems. *IEEE Trans. Power Electron.* **2015**, *30*, 3068–3076. [[CrossRef](#)]
14. Sun, X.; Shen, Y.; Li, W. A Novel LLC Integrated Three-port DC-DC Converter for Stand-alone PV/Battery System. In Proceedings of the 2014 IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific), Beijing, China, 31 August–3 September 2014; pp. 1–6.
15. Song, Y.; Wang, B. Survey on reliability of power electronic systems. *IEEE Trans. Power Electron.* **2013**, *28*, 591–604. [[CrossRef](#)]
16. Yang, S.; Bryant, A.; Mawby, P.; Xiang, D.; Ran, L.; Tavner, P. An industry-based survey of reliability in power electronic converters. *IEEE Trans. Ind. Appl.* **2009**, *47*, 1441–1451. [[CrossRef](#)]
17. Duarte, J.L.; Hendrix, M.; Simões, M.G. Three-Port Bidirectional Converter for Hybrid Fuel Cell Systems. *IEEE Trans. Power Electron.* **2007**, *22*, 480–487. [[CrossRef](#)]
18. Fontana, C.; Buja, G.; Bertoluzzo, M.; Kumar, K.; Wang, Q. Power and control characteristics of an isolated three-port DC-DC converter under DCM operations. In Proceedings of the IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, Italy, 24–27 October 2016; pp. 4211–4216.
19. Phattanasak, M.; Gavagsaz-Ghoachani, R.; Martin, J.; Nahid-Mobarakeh, B.; Pierfederici, S.; Davat, B. Control of a Hybrid Energy Source Comprising a Fuel Cell and Two Storage Devices Using Isolated Three-Port Bidirectional DC–DC Converters. *IEEE Trans. Ind. Appl.* **2015**, *51*, 491–497. [[CrossRef](#)]

20. Wang, L.; Wang, Z.; Li, H. Asymmetrical Duty Cycle Control and Decoupled Power Flow Design of a Three-port Bidirectional DC-DC Converter for Fuel Cell Vehicle Application. *IEEE Trans. Power Electron.* **2012**, *27*, 891–904. [[CrossRef](#)]
21. Ling, Z.; Wang, H.; Yan, K.; Gan, J. Optimal Isolation Control of Three-Port Active Converters as a Combined Charger for Electric Vehicles. *Energies* **2016**, *9*, 715. [[CrossRef](#)]
22. Li, X.; Bhat, A.K.S. Analysis and Design of High-Frequency Isolated Duan-Bridge Series Resonant DC/DC Converter. *IEEE Trans. Power Electron.* **2010**, *25*, 850–862.
23. Krishnaswami, H.; Mohan, N. Three-Port Series-Resonant DC-DC Converter to Interface Renewable Energy Sources with Bidirectional Load and Energy Storage Ports. *IEEE Trans. Power Electron.* **2009**, *24*, 2289–2297. [[CrossRef](#)]
24. Shreelekha, K.; Arulmozhi, S. Multiport Isolated Bidirectional DC-DC Converter Interfacing Battery and Supercapacitor for Hybrid Energy Storage Application. In Proceedings of the 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, India, 3–5 March 2016; pp. 2763–2768.
25. Lee, I.O.; Moon, G.W. Phase-Shifted PWM Converter with a Wide ZVS Range and Reduced Circulating Current. *IEEE Trans. Power Electron.* **2013**, *28*, 908–919. [[CrossRef](#)]
26. Kim, J.W.; Kim, D.Y.; Kim, C.E.; Kim, M.-Y.; Moon, G.-W. Switching control method for light load efficiency improvement in phase shifted full bridge converter. In Proceedings of the 2013 IEEE ECCE Asia Downunder, Melbourne, Australia, 3–6 June 2013; pp. 165–169.
27. Kim, J.W.; Kim, D.Y.; Kim, C.E.; Moon, G.-W. A Simple Switching Control Technique for Improving Light Load Efficiency in a Phase-Shifted Full-Bridge Converter with a Server Power System. *IEEE Trans. Power Electron.* **2013**, *29*, 1562–1566. [[CrossRef](#)]
28. Lee, I.O. Hybrid DC–DC Converter with Phase-Shift or Frequency Modulation for NEV Battery Charger. *IEEE Trans. Ind. Electron.* **2016**, *63*, 884–893. [[CrossRef](#)]
29. Yeon, C.O.; Kim, J.W.; Park, M.H.; Lee, I.-O.; Moon, G.-W. Improving the Light-Load Regulation Capability of LLC Series Resonant Converter Using Impedance Analysis. *IEEE Trans. Power Electron.* **2017**, *32*, 7056–7067. [[CrossRef](#)]
30. Jang, Y.; Kim, J.H.; Kim, K.W.; Kang, B.; Park, M.; Moon, G.-W. A high efficiency half-bridge series resonant converter with pulse width modulation under light load condition. In Proceedings of the 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, China, 22–26 May 2016; pp. 3489–3494.



© 2017 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).