





Modeling and Analysis of the Common Mode Voltage in a Cascaded H-Bridge Electronic Power Transformer

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Abstract: Electronic power transformers (EPTs) have been identified as emerging intelligent electronic devices in the future smart grid, e.g., the Energy Internet, especially in the application of renewable energy conversion and management. Considering that the EPT is directly connected to the medium-voltage grid, e.g., a10 kV distribution system, and its cascaded H-bridges structure, the common mode voltage (CMV) issue will be more complex and severe. The CMV will threaten the insulation of the entire EPT device and even produce common mode current. This paper investigates the generated mechanism and characteristics of the CMV in a cascaded H-bridge EPT (CHB-EPT) under both balanced and fault grid conditions. First, the CHB-EPT system is introduced. Then, a three-phase simplified circuit model of the high-voltage side of the EPT system is presented. Combined with a unipolar modulation strategy and carrier phase shifting technology by rigorous mathematical analysis and derivation, the EPT internal CMV and its characteristics are obtained. Moreover, the influence of the sinusoidal pulse width modulation dead time is considered and discussed based on analytical calculation. Finally, the simulation results are provided to verify the validity of the aforementioned model and the analysis results. The proposed theoretical analysis method is also suitable for other similar cascaded converters and can provide a useful theoretical guide for structural design and power density optimization.

Keywords: electronic power transformer; cascaded H-bridge; common mode voltage; carrier phase shift modulation; electrical insulation; dead time; fault condition

1. Introduction

Recently, renewable energy sources (RESs), e.g., photovoltaic and wind power, with a rising penetration in the modern power grid, have attracted more attention and been exploited widely due to their renewable and environmentally friendly nature relative to traditional fossil fuel energy. Distributed generations and micro-grids are regarded as promising directions and technologies for the reasonable development and utilization of RESs [1,2]. Moreover, with the concept of 'Energy Internet' proposed [3], RESs and related technologies are expected to be more widely applied.

However, as the fundamental elements in the legacy grid, traditional line-frequency transformers are not well suited for the exploitation and utilization of RESs. Therefore, a multifunctional grid interface or energy router is required for the Energy Internet.

Electronic power transformers (EPTs) [4,5], also called solid state transformers (SSTs) or power electronic transformers (PETs) [6,7], has been investigated in recent years and identified as an emerging intelligent electronic device to meet the aforementioned requirements for the future smart grid or Energy Internet [8,9]. Unlike a line-frequency transformer, an EPT is generally composed of power

electronic converters and medium frequency transformers (MFTs) [10]. Therefore, the controllability and multi-object operation can be implemented flexibly such as active power transmission and voltage level conversion, fast and continuous on-load voltage regulation [11], reactive power compensation and current harmonics suppression, fault current limitation, interface to RESs, and so on.

When an EPT is connected to a high or medium voltage power grid, e.g., a 10 kV distribution system, due to the limit of blocking the voltage rating of insulated gate bipolar transistors (IGBTs) or other switching devices, a series-input/cascaded structure has been the most reasonable and popular choice for EPTs [5,6,12], e.g., the 10 kV cascaded H-bridge EPT (CHB-EPT) industrial prototype presented in the literature [5].

It is well known that pulse width modulation (PWM) converters always generate common mode voltage (CMV) [13,14], also called zero-sequence voltage. Especially, a high common mode dv/dt will be generated at a switching instant, when the converter operates at a high switching frequency, which would bring many problems to converter devices, both internal and external. For instance [15–17]:

- Due to the long power cables connecting to the grid or motors, the traveling high-rise-rate CMV
 wave reflected by the terminals of cables will further result in overvoltage for terminal devices
 and cause bearing currents that reduce the life of the motors.
- High dv/dt may cause leakage currents through the parasitic capacitances, which also damage the insulation of elements in the devices, e.g., power cables; in addition, it also creates electromagnetic interference problems, which will interfere with the control systems of devices.

Since an EPT is composed of cascaded H-bridges on the high-voltage side, the aforementioned CMV phenomenon and problems will exist as well and would be more serious and complex, which directly affects the insulation performance and safety operation of the EPT.

For the CMV in traditional two-level PWM converters or grid-connected photovoltaic inverters, since the generation mechanism and analysis are relatively simple, much literature deals with it by improving PWM strategy and employing common mode filters or improved topologies [18–21]. As for the analysis and reduction of the CMV in cascaded converters, due to the significant damage to the insulation and bearing current of motors, much of the literature and research focuses on medium-voltage adjustable speed drive (MV-ASD) systems. The literature [13] analyses systematically the CMV in the MV-ASD and establishes a common mode equivalent circuit, then suppresses the CMV by means of an improved modulation scheme. In the literature [22], the characteristics and paths of common mode current (CMI) in cascaded-multilevel-inverter-based photovoltaic system are analyzed, and suppression filters are designed. As for EPTs, related analysis of the CMV in the previously mentioned literature cannot be applied to them directly, due to their different topologies and control strategies. So far, few papers discuss the CMV or CMI in EPTs. The literature [23,24] presents the CMV and CMI phenomenon in the SST with a solidly grounded neutral point on the high-voltage side and designs common mode chokes to suppress the CMI based on the CMI equivalent circuit. However, the generation mechanisms and distribution characteristics of the CMV in the EPT have not been discussed analytically in the literature. In addition, other factors, e.g., dead time and grid fault condition, are not considered as well.

In this paper, the analysis of the generation mechanism and the characteristics of the CMV in the CHB-EPT, for both the under balanced and fault grid conditions, are presented, based on the simplified circuit model of CHB-EPT and the corresponding PWM strategy, which can provide theoretical guidance for the insulation design and power density optimization of cascaded converters. The analysis method is also applicable for other cascaded converters, e.g., CHB-STATCOM and CHB-inverters.

Section 2 introduces the CHB-EPT system considered in this paper and establishes its equivalent simplified circuit model on the high-voltage side. Section 3 gives the analytical calculation of the CMV in the EPT using the Fourier series analysis method. In Section 4, the results of the analytical calculations are verified by a simulation in MATLAB.

2. Description of the CMV in a CHB-EPT

In this section, the configuration of the considered CHB-EPT system and its internal CMV are introduced.

2.1. CHB-EPT System

Figure 1 shows a distribution system configured with a 10 kV/400 V EPT and the topology of the CHB-EPT considered in this paper, which is designed in a modular fashion and consists of single-phase sub-units that include high-voltage power cells (HVPCs), medium frequency transformers (MFTs), and low-voltage power cells (LVPCs) [5]. Since MFTs provide galvanic isolation and voltage conversion [10], the main circuit also can be divided into high-voltage and low-voltage sides. At the high-voltage side, *h* back-to-back H-bridges are cascaded to sustain a high grid phase voltage and three phases are Y-connection with a floating neutral point. Unipolar double frequency sinusoidal pulse width modulation (SPWM) and carrier phase shift (CPS) modulation technology [25] are adopted in the H-bridge rectifier; then $2hf_s$ kHz equivalent switching frequency can be obtained when the IGBTs work at f_s kHz switching frequency. Note that the voltage reference G in Figure 1b, constructed by three 10 kV potential transformers (PTs), is meant to offer a reference ground for CMV in this paper. These descriptions form the basis for the subsequent analysis of CMV.



Figure 1. Schematic diagram of (**a**) an Electronic power transformer (EPT)-based distribution system; and (**b**) a 10 kV/400 V cascaded H-bridge EPT (CHB-EPT).

2.2. The CMV at the High-Voltage Side in the EPT System

This paper mainly focusses on the CMV problem at the high-voltage side of EPT. Although the CMV appears at the low-voltage side as well, it is not significant relative to the high-voltage side in terms of insulation design. In addition, due to the isolation stage embedded MFTs, which block the mutual transmission and influence of the CMVs on both sides, the CMV at the low-voltage side will not be considered in this paper.

At the high-voltage side, the CHB rectifier connects to the MV grid directly. Especially when a long connecting power cable is employed, the CMV problem will be more complicated and worse due to voltage reflection phenomena and cable to ground capacitance, which will result in overvoltage, even resonance [16,17]. Obviously, higher insulation design requirements should be taken into account in EPT devices. In view of this, the analysis of the CMV at the high-voltage side will be presented in the following.

2.2.1. Voltages Generated by the HVPC

Figure 2a shows the circuit of a high-voltage power cell (HVPC). Each HVPC consists of a high-voltage rectifier and a front-end voltage source converter (VSC) in the isolation stage. Note that the dc-link midpoint (marked with o) between the upper and lower capacitors in Figure 2 is virtual, just to facilitate the definition and calculation of related voltages generated in the HVPC.

Referring to the left VSC H-bridge in Figure 2a, the input differential mode voltage $v_{aa'}$ is defined as the difference between the two PWM voltages across each phase input terminal, a and a', to the dc-link midpoint o, which can be expressed as:

$$v_{aa'} = v_{ao} - v_{a'o} \tag{1}$$

where v_{ao} and $v_{a'o}$ are determined by the PWM strategy and the dc-link voltage. Figure 3 illustrates the operating principle of the unipolar SPWM modulation strategy employed by the left H-bridge in Figure 2a, where v_{SA} and $-v_{SA}$ are the reference sinusoidal waves for the left and right H-bridge arms respectively and v_r is triangular carrier.



Figure 2. (a) The topology of a high-voltage power cells (HVPC); (b) Equivalent circuit model of HVPC for common mode voltage (CMV) analysis.



Figure 3. Unipolar sinusoidal pulse width modulation (SPWM) modulation strategy for an H-bridge.

Figure 2b shows the equivalent circuit model (ECM) of a single HVPC, in which the voltage potential of the midpoint with respect to ground can reflect the variation of voltages in HVPC. Due to the bipolar modulation strategy generally employed by the back-end H-bridge [5], we have:

$$v_{Tcm} = \frac{v_{T1} + v_{T2}}{2} = 0 \tag{2}$$

where v_{Tcm} represents the CMV with respect to the midpoint for MFT primary windings. If neglecting the voltage sources v_{T1} and v_{T2} , the equivalent voltage model for CMV analysis can be further simplified, as is shown in Figure 2b.

2.2.2. The CMV at Neutral Point

Referring to the modeling methods and equivalent circuits in [13,22,23], a simplified three-phase equivalent circuit for the high-voltage side of the EPT illustrated in Figure 1b is exhibited in Figure 4. Note that the grid is converted equivalently to a star-connected voltage source for the analysis and calculation of CMV.



Figure 4. Equivalent circuit for common mode voltage analysis in three-phase CHB-EPT.

In Figure 4, each phase stack has *h* ECMs of HVPC in series, and three-phase stacks are symmetric with a common unearthed neutral point *N*. It should be noted that the relevant parasitic capacitances in each HVPC are not drawn in Figure 4 to highlight the generation mechanism and characteristics of the CMV.

The CMV between point *N* and ground is defined as v_{cm} , shown in Figure 4. Considering that the MV grid, i.e., the 10 kV distribution system, often operates without grounding (e.g., a distribution system in Figure 1a), even in the case of the occurrence of a single-phase earth fault, the EPT will continue to operate for the line-to-line voltages continue to be balanced as well and the relay protection

of the grid would not trip to make an outage immediately. Whether on the normal or single-phase to ground fault condition, the control strategy for the operating of EPT is not affected. However, the corresponding voltages between point *N* and ground are different.

- Normal grid: For the three-phase balanced power grid, the voltage between the virtual grid neutral g (see the location in Figure 4) and ground can be assumed as zero so the neutral point of the grid can be chosen as the reference ground directly; then we have $v_{cm} = v_{Ng}$.
- Single-phase to ground fault: The voltage between the neutral point g of the grid and ground will shift up to phase voltage when a single-phase to ground fault occurs. For a balanced EPT, the CMV at neutral point N with respect to ground will be shifted synchronously. Then we have:

$$v_{cm}' = v_{Ng} + v_{g-ground} \tag{3}$$

where $v_{g-ground}$ is the voltage between the neutral point of the grid in Figure 4 and ground.

In addition, other types of grid faults will not be considered because they are not within the normal operating range of the EPT.

2.2.3. Voltages with Respect to Ground in HVPCs

Taking phase A for example, from Figure 4, it can be seen that the voltage between O_{xL} ($L = 1, 2 \dots h$) and N can be expressed as:

$$v_{AoN}^{L} = v_{ALB} + \sum_{i=1}^{L-1} v_{aa'}^{i}$$
(4)

where *L* is the sequence number of the corresponding HVPC. Then the voltage v_{Aog}^L with respect to ground in HVPC *L* can be obtained from:

$$v_{Aog}^L = v_{AoN}^L + v_{cm} \tag{5}$$

As seen from Figure 4 and Equationss (4) and (5), the voltage at each midpoint o in the corresponding HVPC will change following the variation of the switching transitions in its lower HVPCs, i.e., the equivalent voltage sources v_T and v_B . Thus, the voltage potential at each HVPC not only contains a DM component but also contains the CM component, i.e., the CMV at the neutral point.

3. Analytical Calculation of Voltages in EPT

3.1. Principle and Method to Calculate Voltages in EPT System

In this section, an analytical method for calculating the CMV at neutral points and the voltage potential of HVPCs in an EPT system is proposed. The proposed analytical procedure is described as follows:

- (1) Calculate the CMV at neutral point N with respect to ground, i.e., v_{cm} .
- (2) Calculate the voltage between O_{xL} and N, that is:

$$v_{xoN}^L = v_{xoN}^{L-1} + v_{x(L-1)T} + v_{xLB}$$
(6)

where $x = \{A, B, C\}, L = 1, 2 \dots h$.

(3) Finally, obtain the voltage potential with respect to ground v_{Aog}^L in HVPC *L* based on Equation (5).

3.2. Derivation and Calculation of the CMV at Neutral Point and Voltage Potential of HVPCs

3.2.1. The CMV with Respect to Ground at a Neutral Point

For the input stage of the EPT, there are following relationships:

$$e_{AN} - v_{AN} = R_{L_S} i_A + L_s \frac{di_A}{dt} \tag{7}$$

$$e_{BN} - v_{BN} = R_{L_S} i_B + L_s \frac{di_B}{dt} \tag{8}$$

$$e_{\rm CN} - v_{\rm CN} = R_{L_S} i_{\rm C} + L_s \frac{di_{\rm C}}{dt} \tag{9}$$

where R_{L_S} and L_S are the per phase equivalent resistance and inductance of the input boost inductor; v_{AN} , v_{BN} , and v_{CN} are the high-voltage side converter pole voltages with respect to point N (note that the number of levels of the pole voltages will be up to 2h + 1 when the modulation ratio M is close to 1, where h is the number of HVPCs); e_{AN} , e_{BN} , e_{CN} and i_A , i_B , i_C are the grid voltages and currents, respectively. In addition, the grid voltages under normal conditions can be expressed as:

$$e_{xN} = e_{xg} - v_{cm} \tag{10}$$

where $x = \{A, B, C\}$. Summing Equations (7) to (9), we have:

$$(e_{AN} + e_{BN} + e_{CN}) - (v_{AN} + v_{BN} + v_{CN}) = \left(R_{L_S} + L_s \frac{d}{dt}\right)(i_A + i_B + i_C)$$
(11)

Under the balanced utility grid conditions, $e_{Ag} + e_{Bg} + e_{Cg} = 0$ and $i_A + i_B + i_C \approx 0$, substituting (10) into (11), we obtain:

$$v_{cm} = -\frac{1}{3}(v_{AN} + v_{BN} + v_{CN}) \tag{12}$$

Taking phase A, for example, the reference sinusoidal wave v_{SA} can be expressed as:

$$v_{SA}(t) = M\cos(\omega_s t + \varphi_s) \tag{13}$$

where *M* is the modulation ratio of the CHB rectifier in the input stage of EPT and ω_s and φ_s are the frequency and initial phase of the modulation waveform, respectively. Since *h* HVPCs are cascaded and a unipolar CPS-SPWM strategy with a particular phase-shift angle of π/h based on a natural-sampling method is employed using a similar Fourier series analysis method to that in [25,26], the output voltages of the front-end H-bridge in Figures 2a and 3 can be obtained as follows:

$$v_{ao}^{L} = \frac{V_{dc}}{2}M\cos(\omega_{s}t + \varphi_{s}) + \frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_{n}\left(\frac{Mm\pi}{2}\right)\sin[(m+n)\frac{\pi}{2}]\cos[m(\omega_{c}t + \varphi_{L}) + n(\omega_{s}t + \varphi_{s})]$$
(14)

$$v_{a'o}^{L} = -\frac{V_{dc}}{2}M\cos(\omega_{s}t + \varphi_{s}) + \frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_{n}\left(\frac{Mm\pi}{2}\right)\sin[(m+n)\frac{\pi}{2}]\cos[m(\omega_{c}t + \varphi_{L}) + n(\omega_{s}t + \varphi_{s} + \pi)]$$
(15)

where ω_c and φ_c are the angular frequency and initial phase of the carrier; $\varphi_L = \varphi_c + \frac{\pi}{h}(L-1)$; $L = 1, 2 \dots h$; and, hereinafter assuming that $\varphi_s = \varphi_c = 0$ for simplicity, which will not introduce error for the calculation results, V_{dc} is the dc-link voltage of the H-bridges and $J_n(\cdot)$ is the n-order Bessel function, with the expression $J_n(x) = \sum_{m=1}^{\infty} (-1)^m \frac{x^{n+2m}}{2^{n+2m}m!(n+m)!}$. Note that the dead time is not considered in this section for simplicity.

Then, the voltage between the two input terminals of the front-end H-bridge can be given by:

$$v_{aa'}^{L} = v_{ao}^{L} - v_{a'o}^{L} = MV_{dc}\cos(\omega_{s}t + \varphi_{s}) + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{I_{2n-1}(Mm\pi)}{m} \cos[(m+n-1)\pi]\cos[2m(\omega_{c}t + \varphi_{L}) + (2n-1)\omega_{s}t] .$$
 (16)

Finally, the phase A stack output voltage can be given by:

$$v_{AN} = \sum_{L=1}^{h} v_{aa'}^{L}$$

$$= hMV_{dc} \cos \omega_{s} t + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{I_{2n-1}(hmM\pi)}{m} \cos[(hm+n-1)\pi] \cos[2hm\omega_{c} t + (2n-1)\omega_{s} t].$$
(17)

Similarly, for phases B and C, the corresponding expression can be obtained by replacing φ_s with $\varphi_s \mp \frac{2}{3}\pi$, respectively. Substituting three phase output voltage expressions into (12), we have:

$$v_{cm} = -\frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_{6n-3}(hmM\pi)}{m} \cos[(m+3n-2)\pi] \cos[2hm(\omega_{c}t+\varphi_{c})+(6n-3)\omega_{s}t]$$
(18)

When single-phase to ground fault occurs, e.g., phase C to ground fault, according to Equation (3), Equation (18) should be rewritten as:

$$v_{cm}' = -e_{CN} - \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_{6n-3}(hmM\pi)}{m} \cos[(m+3n-2)\pi] \cos[2hm(\omega_{c}t+\varphi_{c}) + (6n-3)\omega_{s}t]$$
(19)

3.2.2. The Voltage with Respect to N at Point o_{xL}

Still taking phase A for example, for H-bridge *L* in Figures 2 and 4, the voltages between the input terminals with respect to the dc-link midpoint O_{xL} have been derived in Equations (14) and (15). Define the right second term of Equations (15) as function H(L), in which the variable is *L*.

Therefore, the voltage v_{AoN}^1 between the midpoint O_{A1} and the neutral point N of the HVPC located at the bottom of the phase A stack can be given by:

$$v_{AoN}^{1} = v_{A1B} = -v_{a'o}^{1} = \frac{V_{dc}}{2} M \cos \omega_{s} t + v_{AoNh}^{1}$$
(20)

where $v_{AoNh}^1 = H(1)$. Similarly, the voltage v_{AoN}^2 of the second HVPC can be obtained as follows:

$$v_{AoN}^2 = v_{A2B} + v_{aa'}^1 = \frac{3V_{dc}}{2} M \cos \omega_s t + v_{AoNh}^2$$
(21)

where v_{AoNh}^2 is:

$$v_{AoN}^2 = \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_{2n-1}(Mm\pi)}{m} \cos[(m+n-1)\pi] \cos[2m(\omega_{\rm c}t+\varphi_{\rm L}) + (2n-1)\omega_{\rm s}t] + H(2)$$
(22)

The other voltages between the midpoints and *N*, i.e., v_{AoN}^3 , ..., v_{AoN}^h , have the same structure.

3.2.3. Voltage Potential of HVPCs

According to Equations (5) and (18), the CMV with respect to ground at point O_{xL} on the balanced utility grid condition can be written as:

$$v_{Aog}^{L} = \frac{2L - 1}{2} M \cos \omega_s t + v_{Aogh}^{L}$$
⁽²³⁾

where $v_{Aogh}^{L} = v_{AoNh}^{L} + v_{cm}, L = 1, 2 ... h.$

Similarly, for phase B and C, by replacing φ_s with $\varphi_s \mp \frac{2}{3}\pi$, the corresponding expression can be obtained.

In the case of the occurrence of a single-phase earth fault, Equation (23) just needs to have the corresponding fault phase-voltage subtracted.

3.3. Analysis of the Voltages

The analysis of the above mathematical expressions will be presented in this section.

3.3.1. Analysis of the CMV with Respect to Ground at Neutral Point

From Equation (18), the significant feature is that the fundamental frequency component does not appear in v_{cm} . As for the harmonics component, the groups of sideband harmonics arrange around the even multiples of the equivalent carrier $h\omega_c$, the angular frequency and amplitude value of which are $2mh\omega_c \pm (6n-3)\omega_s$ and $\frac{2V_{dc}}{\pi} \frac{J_{6n-3}(hmM\pi)}{m}$ ($m = 1, 2, 3 \dots, n = 0, \pm 1, \pm 2 \dots$), respectively. Obviously, the amplitude of harmonics depends on the modulation ratio and the harmonics order. Note that the amplitude here does not necessarily decrease with an increase in the harmonics order, and the sideband harmonics also do not decrease symmetrically, which can be seen from the following analysis.

Assuming that h, f_s , and V_{dc} are 6 kHz, 1 kHz, and 1500 V, respectively, some analysis results can be obtained as follows:

(1) The relationship between the amplitude of the CMV harmonics component and the modulation ratio *M*

Equation (18) shows that the lowest harmonic group corresponds to m = 1, and the variable x of an n-order Bessel Function is $x = hmM\pi = 6M\pi$. Then the n-order Bessel Function curves can be plotted as in Figure 5.



Figure 5. The relationship between Bessel $|J_n(x)|$ and modulation *M*.

As shown in Figure 5, when m = 1, the modulation ratio M changes from 0 to 1, the corresponding order of the maximum amplitude harmonic is varied. For example, when M is 0.9, the order of the maximum amplitude harmonic is 240 ± 15 .

(2) The relationship between the amplitude of CMV harmonics and its order

Figure 6 shows the relationship between the amplitude of CMV harmonics and its order, where *M* is set as 0.9. It can be seen that the amplitude here does not necessarily decrease with an increase in the harmonics order. This point should be considered as especially involved in suppressing the CMIs in the EPT.



Figure 6. Relationship between the amplitude of CMV harmonics and its order.

3.3.2. Analysis of the Voltage with Respect to Ground at Midpoint o_{xL}

From (23), it can be found that the expression of the voltage with respect to ground at the midpoint o_{xL} , contains the fundamental frequency component, and its amplitude increases with the characteristics of an arithmetic series. As for the harmonics component, it can be divided into two parts; one part is the high-order harmonics generated at the neutral point *N*, the other part is generated by the corresponding H-bridge due to using a unipolar double frequency modulation strategy.

It should be noted that the fundamental component appearing in Equation (23) is an effective component in the output voltage generated by the cascaded H-bridges; in other words, it cannot be eliminated by means of improving the PWM strategies.

When the values of the dc-link voltage and the modulation ratio *M* in HVPCs are 1500 V and 1, respectively, the amplitudes of the fundamental component of the voltage potential of HVPC 1 to 6 are 750 V, 2250 V, 3750 V, 5250 V, 6750 V, and 8250 V, respectively. It can be seen that the amplitude of the fundamental component of the voltage potential in the top HVPC will reach 8250 V, which is much higher than its dc-link voltage of 1500 V and also higher than the amplitude of the grid phase voltage, which is 8165 V. Furthermore, the voltage potential at the upper input terminal of the MFT primary windings connected with the top HVPC should add on 750 V ($V_{dc}/2$); then it can even reach 9000 V. Especially when the single-phase to ground fault of an input grid occurs, the value will be higher, which results a huge threat to the insulation of HVPCs and MFTs in the EPT.

3.4. Effects of SPWM Dead Time on the CMV

The effects of SPWM dead time on the CMV are not considered in the above analysis and results for the sake of simplifying the calculation and highlighting the distribution characteristics of the CMV. It should be pointed out that, in practice, the dead time T_d , e.g., a few microseconds, generally must be inserted into the switching signals of the IGBTS or other switching devices to prevent a short circuit. Hence, in this section, the impact of SPWM dead time on the CMV in the EPT will be discussed and analyzed.

The practical output voltage of phase A stack v_{AN}^* can be divided into two parts; an ideal part, i.e., the output voltage expressed in Equation (17) without dead time, and a correction part caused by dead time. Equation (17) can be rewritten as:

$$v_{AN}^{*} = \sum_{L=1}^{h} v_{aa'}^{L*} = \sum_{L=1}^{h} \left(v_{aa'}^{L} + v_{err_aa'}^{L} \right)$$
(24)

where $v_{err_aa'}^L$ is the error voltage caused by the dead time. The total error voltage v_{err_A} of the phase A stack can be obtained by employing the DFIA method in [25].

$$v_{err_A} = \sum_{L=1}^{h} v_{err_aa'}^{L} = \sum_{L=1}^{h} \left[v_{err_a}^{L} - v_{err_a'}^{L} \right] \\ = 2h \sum_{n=1}^{\infty} \left[A_{0,n} \cos(n(\omega_{s}t + \varphi_{s})) + B_{0,n} \sin(n(\omega_{s}t + \varphi_{s})) \right] \\ + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left\{ \begin{array}{c} 2A_{m,n} \sum_{L=1}^{h} \cos[2m(\omega_{c}t + \varphi_{L}) + (2n - 1)\omega_{s}t] \\ + 2B_{m,n} \sum_{L=1}^{h} \sin[2m(\omega_{c}t + \varphi_{L}) + (2n - 1)\omega_{s}t] \end{array} \right\}$$
(25)
$$= 2h \sum_{n=1}^{\infty} \left[A_{0,n} \cos(n(\omega_{s}t + \varphi_{s})) + B_{0,n} \sin(n(\omega_{s}t + \varphi_{s})) \right] \\ + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left\{ \begin{array}{c} 2A_{m,n} \cos[2hm\omega_{c}t + (2n - 1)\omega_{s}t] \\ + 2B_{m,n} \sin[2hm\omega_{c}t + (2n - 1)\omega_{s}t] \end{array} \right\}$$

where $A_{m,n}$ and $B_{m,n}$ are the Fourier coefficients [25]. Similarly, for phases B and C, the corresponding expression can be obtained by replacing φ_s with $\varphi_s \mp \frac{2}{3}\pi$. Then, the total CMV at point *N*, considered dead time, can be given by:

$$\begin{aligned}
 & v_{cm}^{*} &= -\frac{1}{3} \Big(v_{AN}^{*} + v_{BN}^{*} + v_{CN}^{*} \Big) \\
 &= v_{cm} - \frac{1}{3} (v_{err_A} + v_{err_B} + v_{err_C}) \\
 &= v_{cm} - 2h \sum_{n=1}^{\infty} [A_{0,3n} \cos(3n(\omega_{s}t + \varphi_{s})) + B_{0,3n} \sin(3n(\omega_{s}t + \varphi_{s}))] \\
 &- \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \begin{cases} 2A_{m,n} \cos[2hm\omega_{c}t + (6n - 3)\omega_{s}t] \\
 +2B_{m,n} \sin[2hm\omega_{c}t + (6n - 3)\omega_{s}t] \end{cases}
 \end{aligned}$$
 (26)

From Equations (18) and (26), it can be seen that the dead time does not bring a fundamental component to the CMV at the neutral point *N*. However, it will affect the harmonics component. The analysis in the case of the occurrence of a single-phase earth fault is similar to Equation (19).

4. Simulation Results

To display the waveforms and characteristics of the CMV directly and illustrate the correctness of the analysis presented in Section 3, simulations have been carried out in MATLAB/SIMULINK.

A model of three-phase 10 kV/400 V 1 MVA EPT with the same structure as shown in Figure 1b, which consists of six HVPCs and six LVPCs per phase, is built. The main parameters are given in Table 1.

Parameter	Value
Number of cascaded H-bridges	6 per phase
Number of paralleled H-bridges	6 per phase
Rated high voltage dc-link	1500 V
Rated low voltage dc-link	360 V
Capacitance in one high-voltage dc-link	2200 μF
Capacitance in one low-voltage dc-link	56 mF
Inductance of rectifier	30 mH
Filter inductance of the inverter	0.2 mH
Filter capacitance of the inverter	250 μF
Rated ratio of the MFIT	4.17:1
Switching frequency at high-voltage side	1 kHz
Switching frequency at low-voltage side	4 kHz

In addition, SPWM natural sampling is employed in the simulation, and the SPWM dead time is set as 4 μ s. The modulation ratio *M* is close to 0.9 in the simulation.

Figure 7 shows the waveform of the phase A stack output voltage with 13 levels, and it was calculated in Equation (17).



Figure 7. Phase A stack output voltage.

Figure 8 shows the waveforms of the CMV between the neutral point *N* and reference ground with or without the dead time of 4 µs inserted into the switching signals. As can be seen, both CMVs have almost the same waveforms and harmonic performance. The absolute maximum instantaneous values in both waveforms can reach up to 1000 V. The ordinate value at the right side of Figure 8 is the magnitude of the 50 Hz fundamental component and harmonic voltages. According to the conclusion in Section 3.3.1, the harmonic group should appear around $2mh\omega_c$, where $m = 1, 2, 3 \dots$, h = 6, $\omega_c/\omega_s = 20$, i.e., 240th, 480th, 720th \dots , which is consistent with the fast Fourier transformation (FFT) analysis results on the right side of Figure 8. More agreement relations between the proposed mathematical model and the simulation results can be obtained for further analysis. In addition, there are significant differences between the low-order harmonics appearing in Figure 8a,b, i.e., the low-order harmonics have a higher magnitude in latter compared with those in the former, which is consistent with the discussion in Section 3.4 and with the results when SPWM dead time is considered. Thus, the accuracy of the aforementioned model can be proved.



Figure 8. The waveforms and corresponding the fast Fourier transformation (FFT) analysis of the CMV between *N* and reference ground: (**a**) without SPWM dead time; (**b**) with SPWM dead time.

Figure 9 exhibits a comparison of the magnitude values of CMV harmonics between the theoretical calculation and simulation results, where the theoretical values are obtained from Equation (18) and the simulation results are obtained directly by employing the FFT tool in MATLAB/SIMULINK. From the comparison in Figure 9, it can be found that the maximum error value between the theoretical and the simulation results is 8.67%, appearing at 507th harmonic, and the minimum error is lower than 0.39%, appearing at 225th harmonic. Although the relative errors of the high-order harmonics are slightly larger, their absolute amplitudes are lower. Therefore, the difference between the two results is very small, which also verifies the validity of the proposed CMV mathematical model.



Figure 9. A comparison of magnitude values of CMV harmonics in the theoretical calculation and the simulation results.

Figure 10 shows the CMV at a neutral point (in Figure 4) and the voltage potential with respect to ground of the cascaded HVPCs at the high-voltage side in phase A under balanced grid voltage conditions and single-phase to ground fault in phase C, respectively. From 0.06 s to 0.10 s, the EPT is operating under normal grid conditions. It can be clearly seen from the figure that the characteristics of the voltages are consistent with the analysis in Sections 3.2.3 and 3.3.2, e.g., the top HVPC in Figure 1b has to sustain the highest voltage potential with respect to ground, reaching up to 9000 V. At 0.10 s, a single-phase to ground fault occurs in phase C of the 10 kV grid. Since the line-to-line voltages of 10 kV also maintain the balance in this fault, the EPT continues to operate to provide high quality electricity for the loads in the secondary side. However, the voltages in Figure 10 change abruptly at 0.10 s, i.e., each voltage potential with respect to ground of each HVPC. In the worst case, the RMS of the voltage potential of the top HVPC is close to the line-voltage of the grid. This brings a great challenge to the insulation design of the HVPC and MFT. All of the aforementioned analysis can offer a theoretical basis for insulation design.



Figure 10. Cont.



Figure 10. Simulation results: Related voltages under normal and fault conditions. (**a**) The CMV at a neutral point; (**b**) the voltage potential between the midpoints of the HVPCs and ground (From top to bottom: $v_{Aog'}^6 v_{Aog'}^3$ and v_{Aog}^1).

5. Conclusions

This paper has investigated the generated mechanism of the CMV in a CHB-EPT, presented the characteristics of the CMV by using an analytical calculation method, and validated them with simulation results. The main analysis results can be concluded as follows:

- The CMV at the neutral point *N* under normal and balanced grid voltage conditions mainly consists of high-order harmonics with relatively high d*v*/d*t* voltage stress for the high-voltage side of the EPT. The EPT has to sustain a higher fundamental component of the CMV, i.e., the voltage of the fault phase, when it operates under a fault grid condition (single-phase to ground fault).
- The voltage potential at each equivalent midpoint of the HVPC with respect to ground, not only includes the high-order harmonics components, but also contains the line-frequency fundamental component. Furthermore, the magnitude of the latter will increase with an increase of the sequence number of the HVPC. Obviously, the highest electrical stress will appear in the top HVPC, which provides a theoretical guide for the structural design and further power density optimization of the EPT.
- SPWM dead time has little effect on the magnitude of the CMV. In addition, it will not bring a fundamental component to the CMV at the neutral point.

In conclusion, through the analysis of the CMV in the EPT, a theoretical guide can be put forward for insulation design and power density optimization. In addition, the proposed analysis method can also be applied to other cascaded converters, e.g., CHB-STATCOM and CHB-inverters.

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References

- 1. Yan, B.; Wang, B.; Zhu, L. A novel, stable, and economic power sharing scheme for an autonomous microgrid in the energy internet. *Energies* **2015**, *8*, 12741–12764. [CrossRef]
- 2. Liserre, M.; Sauter, T.; Hung, J.Y. Future energy systems: Integrating renewable energy sources into the smart power grid through industrial electronics. *IEEE Ind. Electron. Mag.* **2010**, *4*, 18–37. [CrossRef]
- 3. Huang, A.Q.; Crow, M.L.; Heydt, G.T.; Zheng, J.P.; Dale, S.J. The future renewable electric energy delivery and management (FREEDM) system: The energy internet. *Proc. IEEE* **2011**, *99*, 133–148. [CrossRef]
- 4. Yang, Y.; Mao, C.; Wei, T.; Wang, D.; Tian, J. Multi-function combined operation and control strategy of electronic power transformer for power quality improvement. *IEEJ Trans. Electr. Electron.* **2017**. [CrossRef]
- 5. Wang, D.; Tian, J.; Mao, C.; Lu, J.; Duan, Y.; Qiu, J.; Cai, H. A 10-kV/400-V 500-kVA electronic power transformer. *IEEE Trans. Ind. Electron.* **2016**, *63*, 6653–6663. [CrossRef]
- 6. She, X.; Huang, A.Q.; Burgos, R. Review of solid-state transformer technologies and their application in power distribution systems. *IEEE J. Emerg. Sel. Top. Power Electron.* **2013**, *1*, 186–198. [CrossRef]
- 7. Brando, G.; Dannier, A.; del Pizzo, A.; Rizzo, R. Power electronic transformer for advanced grid management in presence of distributed generation. *Int. Rev. Electr. Eng.* (*IREE*) **2011**, *6*, 3009–3015.
- Kolar, J.W.; Ortiz, G. Solid-state-transformers: Key components of future traction and smart grid systems. In Proceedings of the International Power Electronics Conference-ECCE Asia (IPEC 2014), Hiroshima, Japan, 18–21 May 2014.
- 9. She, X.; Huang, A.Q. Solid state transformer in the future smart electrical system. In Proceedings of the IEEE Power and Energy Society General Meeting, Vancouver, BC, Canada, 21–25 July 2013; pp. 1–5.
- 10. Huang, P.; Mao, C.; Wang, D. Electric field simulations and analysis for high voltage high power medium frequency transformer. *Energies* **2017**, *10*, 3. [CrossRef]
- 11. Yang, J.; Mao, C.; Wang, D.; Lu, J.; Fu, X.; Chen, X. Fast and continuous on-load voltage regulator based on electronic power transformer. *IET Electr. Power Appl.* **2013**, *7*, 499–508. [CrossRef]
- 12. Zhao, C.; Dujic, D.; Mester, A.; Steinke, J.K.; Weiss, M.; Lewdeni-Schmid, S.; Chaudhuri, T.; Stefanutti, P. Power electronic traction transformer—Medium voltage prototype. *IEEE Trans. Ind. Electron.* **2014**, *61*, 3257–3268. [CrossRef]
- Rendusara, D.A.; Cengelci, E.; Enjeti, P.N.; Stefanovic, V.R. Analysis of common mode voltage-'neutral shift' in medium voltage PWM adjustable speed drive (MV-ASD) systems. *IEEE Trans. Power Electron.* 2002, 15, 1124–1133. [CrossRef]
- 14. Tang, X.; Lai, C.; Liu, Z.; Zhang, M. A SVPWM to eliminate common-mode voltage for multilevel inverters. *Energies* **2017**, *10*, 715. [CrossRef]
- Aoki, N.; Satoh, K.; Nabae, A. Damping circuit to suppress motor terminal overvoltage and ringing in PWM inverter-fed ac motor drive systems with long motor leads. *IEEE Trans. Ind. Appl.* 1999, 35, 1014–1020. [CrossRef]
- 16. Jiang, Y.; Wu, W.; He, Y.; Chung, S.H.; Blaabjerg, F. New passive filter design method for overvoltage suppression and bearing currents mitigation in a long cable based PWM inverter-fed motor drive system. *IEEE Trans. Power Electron.* **2017**, *32*, 7882–7893. [CrossRef]
- Lai, R.; Todorovic, M.H.; Sabate, J. Analysis and suppression of a common mode resonance in the cascaded H-bridge multilevel inverter. In Proceedings of the Energy Conversion Congress and Exposition (ECCE), Atlanta, GA, USA, 12–16 September 2010; pp. 4564–4568.
- Hava, A.M.; Ün, E. Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters. *IEEE Trans. Power Electron.* 2009, 24, 241–252. [CrossRef]
- Lai, Y.S.; Shyu, F.S. Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects—Part I: Basic development. *IEEE Trans. Ind. Appl.* 2004, 40, 1605–1612. [CrossRef]
- 20. Julian, A.L.; Oriti, G.; Lipo, T.A. Elimination of common-mode voltage in three-phase sinusoidal power converters. *IEEE Trans. Power Electron.* **1999**, *14*, 982–989. [CrossRef]
- 21. Yang, B.; Li, W.; Gu, Y.; Cui, W.; He, X. Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system. *IEEE Trans. Power Electron.* **2012**, 27, 752–762. [CrossRef]

- 22. Zhou, Y.; Li, H. Analysis and suppression of leakage current in cascaded-multilevel-inverter-based PV systems. *IEEE Trans. Power Electron.* 2014, 29, 5265–5277. [CrossRef]
- 23. Huber, J.E.; Kolar, J.W. Common-mode currents in multi-cell solid-state transformers. In Proceedings of the 2014 International Power Electronics Conference (IPEC), Hiroshima, Japan, 18–21 May 2014; pp. 766–773.
- 24. Guillod, T.; Huber, J.E.; Ortiz, G.; De, A.; Franck, C.M.; Kolar, J.W. Characterization of the voltage and electric field stresses in multi-cell solid-state transformers. In Proceedings of the 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, USA, 14–18 September 2014; pp. 4726–4734.
- 25. Li, Y.; Wang, Y.; Li, B.Q. Generalized theory of phase-shifted carrier PWM for cascaded H-bridge converters and modular multilevel converters. *IEEE J. Emerg. Sel. Topics Power Electron.* **2016**, *4*, 589–605. [CrossRef]
- 26. Holmes, D.; Lipo, T. *Pulse Width Modulation for Power Converters: Principles and Practice*, 1st ed.; Wiley: Hoboken, NJ, USA, 2003; pp. 99–119.



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