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# A Simple Method for Reducing THD and Improving the Efficiency in CSI Topology Based on SiC Power Devices

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Received: 14 September 2018; Accepted: 16 October 2018; Published: 17 October 2018



**Abstract:** Silicon carbide (SiC)-based switching devices provide significant performance improvements in many aspects, including lower power dissipation, higher operating temperatures, and faster switching; compared with conventional Si devices, all these features contribute to these devices generating interest in applications for electric traction systems. The topology that is frequently used in these systems is the voltage source inverter (VSI), but the use of SiC devices in the current source inverter topology (CSI), which is considered as an emerging topology, generates interest. This paper presents a method for improving total harmonic distortion (THD) in the currents of output and efficiency in SiC current source inverter for future application in an electric traction system. The method that is proposed consists of improving the coupling of a bidirectional converter topology, voltage current (V-I) and CSI. The V-I converter serves as a current regulator for the CSI, and allows for the recovery of energy. The method involves an effective selection of the switching frequencies and phase angles for the carrier signals that are present in each converter topology. With this method, it is expected to have a reduction of the total harmonic distortion, THD in the output currents. In addition, a comparative analysis between converters with all-SiC technology and converters with hybrid technology is realized, to verify the impact of the SiC devices in the power converters efficiency.

**Keywords:** current source inverter (CSI); silicon carbide (SiC); power converter, DC–AC converter, total harmonic distortion (THD)

## 1. Introduction

The constant growth of hybrid and electric vehicles (EHV/EV) promotes new challenges to achieve the total integration of these vehicles in the transportation field. High power density and high efficiency powertrains are among other important drawbacks in the EHV/EV designs. The electric traction systems play an important role for addressing these issues. Therefore, the new technologies study, and the search for alternatives to traditional power converters and switching devices, and control are important within the design requirements of electric traction systems for EHV/EV.

Silicon carbide devices (SiC) are a mature technology, and examples are widely found in the market [1–4]. Recent research has shown the advantages and disadvantages of the SiC devices. These elements possess better characteristics than silicon devices, such as low switching losses, higher switching frequencies, and higher temperature operation ranges [4–8]. Accordingly, the SiC devices allow for the design of power converters with high-power densities and high efficiencies.

In [9–12], several studies of power converter topologies with SiC devices for electric traction systems are presented. The switching frequency ranges that are used in the different studies are

between 50 kHz and 100 kHz. Accordingly, in the design of electric traction systems with SiC devices, the frequency must be greater than 50 kHz and less than 100 kHz. On the other hand, if the switching frequency is increased, the efficiency can be affected. This is shown clearly in [13], where at 200 kHz of operation frequency, the efficiency of the converter drops to 85%.

On the other hand, state of the art studies have widely shown the effects caused in electrical machines by high total harmonic distortion (THD) in the currents and voltages at different frequency ranges. The research [14] presents an analysis on the impact of the switching frequency impact in the power converters, and the harmonic power losses effect on surface permanent magnet motors. The reduction of harmonics in the current allows for improvement the torque and reducing of the THD in the current. This reduced the magnetic saturation in the stator, improving the losses and the torque. The harmonics effects of the carrier in the motor operation are important, when considering the additional losses in the windings and the iron laminations caused by eddy currents.

Accordingly, power converters and control techniques are required to achieve currents and voltages with low THD, but adjusting the switching frequency to not significantly increase the switching losses. The voltage source inverter (VSI) topology is more commonly used in electric traction systems for driving the electric motor. Nevertheless, this topology requires a very high performance capacitor in the direct current (DC) link that is expensive and bulky in the most cases [15]. As an alternative, the current source inverter (CSI) is a considered and emerging topology within electric traction systems, due to several advantages such as high voltage capability, auto short-circuit protection, and a better sinusoidal output voltage, because of alternating current AC capacitor effects [16–18]. In addition, the inductors used in CSI converters offer a longer lifetime than the capacitors used in VSI converters. However, even with the previously mentioned characteristics, the CSI converter has several drawbacks, which limit the design of high-performance power converters.

In [19], the authors present the topology of CSI with a DC/DC V-I power converter that controls the stabilization of the current of input, and the return of energy. For the implementation of this topology, insulated gate bipolar transistors (IGBTs) with reverse-blocking (RB) capability are used for a low frequency of switching, 15 kHz for a V-I power converter, and 7.5 kHz for CSI. The result shows that the THD is improved, but the results could be enhanced if SiC devices are used, because the switching frequency can be increased. Others works can be found in the literature, which are focused on the control techniques and the analysis of the switching frequency effect. In addition, in [20,21], optimization techniques are presented to achieve output currents with high quality. However, the works are also based on traditional switching devices and low switching frequency.

In accordance with the above, the switching frequency is important for the CSI converter design. Meanwhile, the control technique applied in CSI converters and the V-I converter to achieve a DC current can affect significantly the THD of this current. Thus, the modulation design for both converters' conditions and the synchronization between modulations is of high interest.

This paper has two important contributions. First, the work presents a new method that consists of synchronizing the modulation control of the V-I and CSI converters based on SiC devices. Due to the controls being based on pulse-width modulation (PWM) techniques, two carriers are used to generate the pulses of the transistors. The method includes the search of the optimal operating frequency and a better shift angle between carries as well. The main purpose of this method is for improving the THD in the CSI outputs current at high frequencies. Second, the paper demonstrates a coordinated modulation improvement and the consequent reduction of harmonics, allowing for a better efficiency in the motor and inverter system to be obtained. Finally, a comparison between converters with all-SiC technology and converters with hybrid technology is realized to verify the impact of the SiC devices in the power converter's efficiency.

The paper is organized as follows: first, the topology studied and the proposed method is presented in Section 2. Section 3 focuses on the operation of CSI, and validation through simulations. After that, a study of losses and efficiency, the sizing estimation of the heatsink and analysis of the

efficiency between converters with all-SiC devices and converters with hybrid technology devices are developed in Section 4. Finally, Section 5 concludes this paper.

## 2. Power Converters Analysis and Description of the Proposed Method

### 2.1. V-I Converter and CSI Inverter Analysis

The proposed converter topology shown in Figure 1 uses a V-I converter to regulate the current input. Also, a CSI inverter that generates three-phase currents of output with SiC devices is proposed.

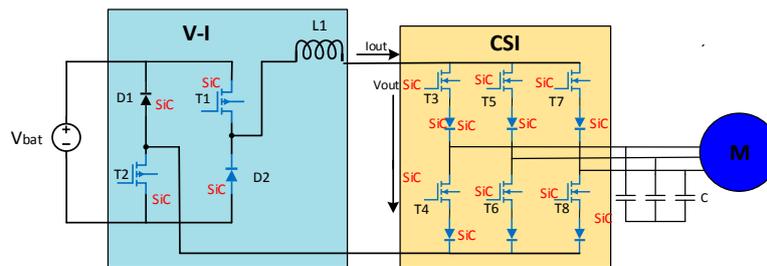


Figure 1. Topology proposed for the study.

Based on the previous analyses presented in [20,21], this topology can be analyzed in two modes, as shown in Figure 2. It is assumed that the output current  $I_{out}$  maintains a constant for a one state of the converter control. In the first mode, the SiC MOSFETs  $T_1$  and  $T_2$  are turned ON, and a DC voltage delivered by a battery is applied to the converter. The inductor  $L_1$  converts to storage energy. Current returns through the activation of SiC MOSFETs  $T_2$ , during  $T_{off}$  modulation state and the diodes  $D_1$ , and  $D_2$  are in reverse bias; therefore, they are not activated. A current  $I_{out}$  and a voltage  $V_{out}$  are obtained in the V-I converter output where  $V_{Bat}$  depends on the converter control. In the second mode (Figure 2b) the MOSFETs are turned off, and the current flows through the diodes  $D_1$  and  $D_2$ , this mode can be implemented in the case when the CSI current converter returns the energy to recharge the high voltage battery  $V_{out} = -V_{Bat}$ .

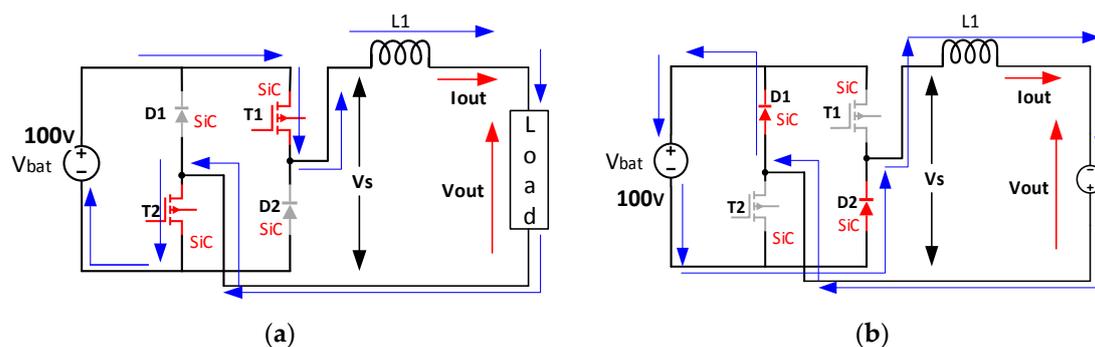


Figure 2. Current trajectory in V-I and CSI converter V-I. (a) First state of operation; (b) second state of operation.

The model dynamic of V-I converter is governed by (1):

$$L \frac{dI_{DC}}{dt} = V_s - V_{in} \tag{1}$$

where the output voltage  $V_{out}$  of the V-I converter can take three values: the battery voltage ( $V_{out} = V_{Bat}$ ) when the V-I converter operates in the first state, also,  $V_{out} = 0$  when  $T_1$  and  $T_2$  are OFF, or  $V_{out} = -V_{Bat}$ . To maintain a desired level of the dc choke current, the V-I converter alternates between the first state and ON-OFF of  $T_1$  or  $T_2$ .

The CSI inverter has six transistors and six Schottky diodes connected in series; all devices are made of silicon carbide. Depending on the modulation technique implemented, the CSI inverter is responsible for directing the current through the load by the ON and OFF control of each transistor.

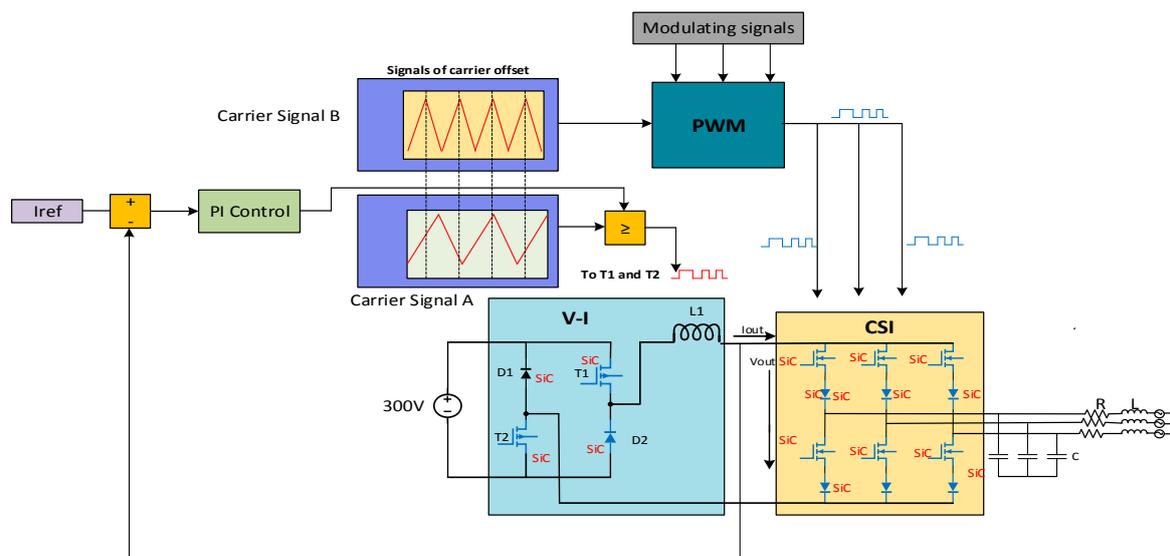
For the operation of the CSI topology, it is necessary to generate typical patterns, and to add short-circuit pulses to obtain the activation signals; for this reason it is necessary for the use of the (SPWM) sine-wave modulation technique, which generate pulses for the activation of power transistors. These pulses create a short circuit through one leg of the inverter, whenever either top or all bottom switches are open.

## 2.2. Proposed Method Description

An important challenge of the topology shown in Figure 1 is the synchronization between the two modulations of the converters for achieving high performance and low THD. As previously mentioned, the CSI required a controlled output current with as low ripple as possible. Besides, the CSI required a control to deliver an AC output current.

Therefore the method proposed has two stages, the first stage consists of implementing a control to regulate the output current of the V-I converter, taking into account the requirements of the CSI. In addition, a PWM control was designed for the CSI, and adapted with the V-I converter conditions.

The CSI used a PWM technique, which required two carriers A and B for generating the pulse of the transistors, as depicted in Figure 3. Accordingly, the second stage of the method consisted of searching for the best operating frequency in both V-I and CSI converters, and also to determinate the angle between, to achieve synchronization between the two controls.



**Figure 3.** Schematic of operation and synchronization of power converters.

For the first part, the control technique used was a proportional-integrator control (PI). The design of the control PI for the current in the V-I converter is summarized as follows: the circuit shown in Figure 4 describes the behavior of the currents and voltages generated when it is placed with an RLC load. Also, for the analysis, the internal resistances of the SiC MOSFETs ( $R_{ds} = R_{on}$ ), inductance (RL), and capacitance (RC) (first state) were considered.

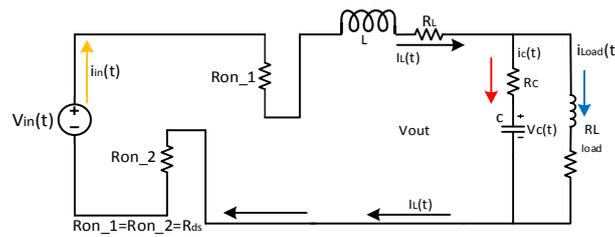


Figure 4. V-I converter: first state of operation circuit (supplying energy).

The equations obtained in the function of the circuit shown in Figure 4 are described in (2) and (3):

$$L \frac{di_L(t)}{dt} = V_{in}(t) - 2R_{ds}i_L(t) - R_L i_L(t) - V_o \tag{2}$$

$$\frac{dV_C(t)}{dt} = \frac{R_{Load}}{R_{Load} + R_C} i_L(t) - \frac{1}{R_{Load} + R_C} V_C(t) \tag{3}$$

From Equations (2)–(5) can be represented a state space system:

$$\dot{X}(t) = AX(t) + B \tag{4}$$

$$Y(t) = CX(t) + D \tag{5}$$

These equations can be expressed in the matrix form:

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dV_C(t)}{dt} \end{bmatrix} = \begin{bmatrix} \frac{2R_{ds} + R_L + \frac{R_{Load}R_C}{R_{Load} + R_C}}{L} & -\frac{R_{Load}}{R_{Load} + R_C} \\ \frac{R_{Load}}{R_{Load} + R_C} & -\frac{1}{R_{Load} + R_C} \end{bmatrix} \begin{bmatrix} i_L(t) \\ V_C(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in}(t) \tag{6}$$

$$\begin{bmatrix} \frac{V_o(t)}{dt} \\ I_{in}(t) \end{bmatrix} = \begin{bmatrix} \frac{R_{Load}R_C}{R_{Load} + R_C} & \frac{R_{Load}}{R_{Load} + R_C} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ V_C(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{in}(t) \tag{7}$$

Then, with the previous analysis, the transfer function could be calculated. After that, a PI controller was designed and tuned for achieving the expected outputs. The simulation results of the PI controller tuning of the system are shown in Figure 5.

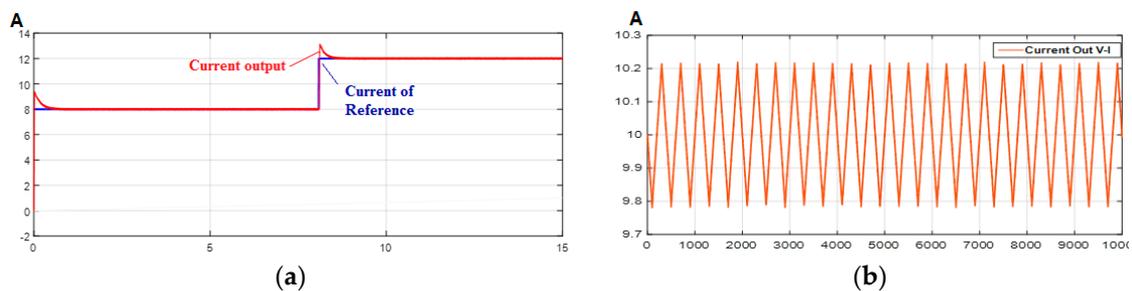
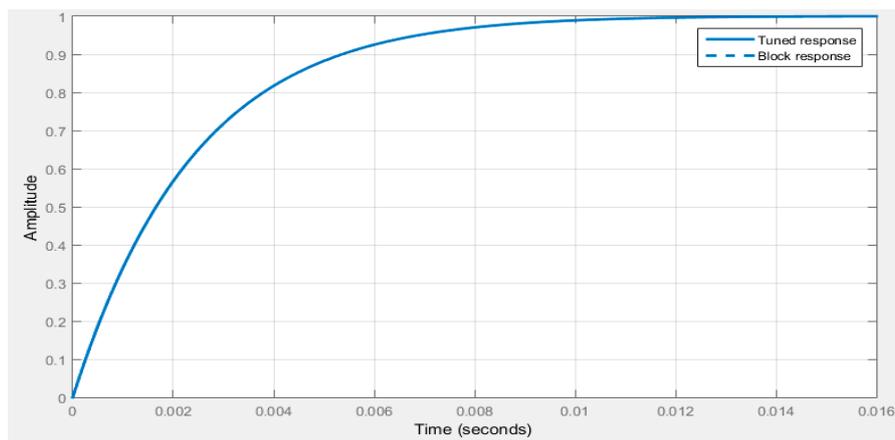


Figure 5. Simulation results of the PI controller. (a) Output current response, (b) detail of the current reference at 10 A.

For the tuning of the PI controller, the auto-tuning tool of the proportional-integrator-derivate block (PID) of Simulink was used. The results are shown in Figure 6 and Table 1.



**Figure 6.** Tuning of the PI controller for the V-I converter response to a step.

**Table 1.** Parameters of simulations of the PI control.

Parameter	Values
$K_p$	4.75769580834167
$K_i$	460.186624758197
Rise time	0.00488 s
Settling time	0.00838 s
Overshoot	0.0198%
Peak	1
Phase margin	889 deg @ 439 rad/s

The second stage for the control development began with the search of the switching frequency for each converter. For doing the search, a random frequency ( $f_s$ ) was assigned, and with this frequency, three conditions for the analysis were established by (8):

$$f_s = \begin{cases} f_{s(vi)} = f_{s(csi)} \\ f_{s(vi)} = 2f_{s(csi)} \\ 2f_{s(vi)} = f_{s(csi)} \end{cases} \quad (8)$$

The first condition assigned the same value of the switching frequency for the V-I power converter and the CSI. The second condition indicated that the value of the switching frequency of the CSI was the double that of the V-I converter. Finally, the third condition indicated that the switching frequency of V-I converter was double of the CSI. Considering these three conditions, the analysis followed the flowchart shown in Figure 7.

Regarding state-of-the-art methods, the switching frequencies in applications with SiC devices are around 50 kHz to 200 kHz. However, even with the low losses achieved using silicon carbide devices, it is important that a compensation is made between the switching frequency and switching losses. Thus, after a study, the switching frequency of the V-I converter was fixed at 35 kHz in all simulation cases, A, B, and C. Meanwhile, the switching frequency for the CSI converter was set at 70 kHz. Later a THD analysis of the output currents was performed and the THD value for each option was obtained. This analysis consisted of defining the two carrier signals of each converter. The carrier signal of the V-I was considered as the reference signal (Figure 8). Subsequently, it displaced the angle of the signals carrier between a range of  $0^\circ$  to  $180^\circ$ , in steps of 30 degrees. With the results obtained, a new THD analysis was carried out. Besides, if the value of THD was further reduced for some phase angle, the condition was validated and the tuning was done.

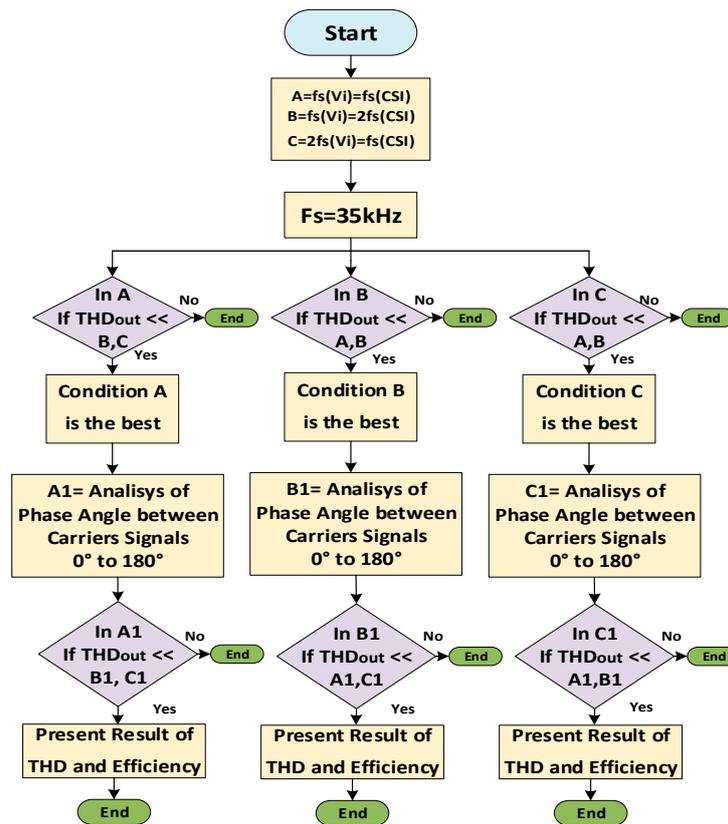


Figure 7. Flowchart of method proposed.

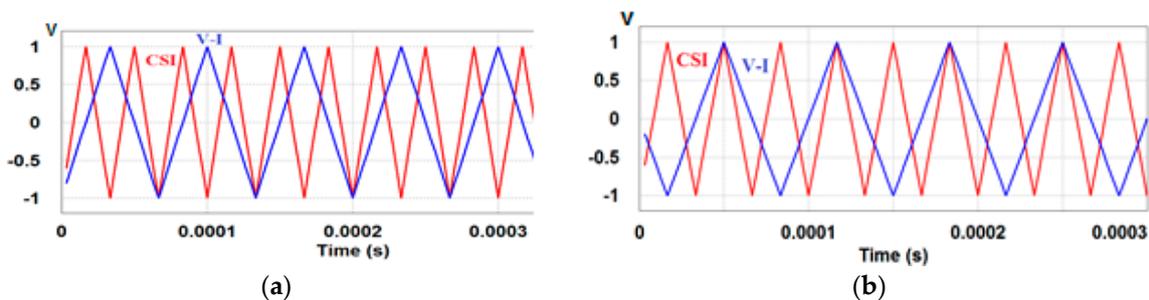


Figure 8. Signals carriers to different frequencies and angles. (a)  $F_{s(V-I)} = 15$  kHz,  $F_{s(CSI)} = 30$  kHz, angle =  $0^\circ$ ; (b)  $F_{s(V-I)} = 15$  kHz,  $F_{s(CSI)} = 30$  kHz angle =  $90^\circ$ .

### 3. Operation of CSI and Validation

This section presents the implementation of the proposed method. The operation of combined modulations and synchronization of the topologies were analyzed and validated by simulations. The transistors of CSI were activated using a PWM modulation technique under conditions that will be explained later.

#### 3.1. Technique of Modulation

In the designed PWM, some conditions were defined. First, a constant current source must be guaranteed at all times. Second, the transistors must work in such a way that an open circuit in the DC link or a short circuit in the output capacitors is avoided. Any sudden loss of the current results in a large  $dv/dt$  value, due to the DC-link inductor; this would cause damage to the components. Third, only two switches will be activated at any time. If more than two are activated, the waveforms of the PWM current cannot be defined.

To comply with these conditions, the modulation technique presented in [22,23] was used. It consisted of four main blocks (Figure 9) that satisfied the required constraints, and extended the duality between VSI and CSI beyond the power circuit topology [23]. Using this technique allows us to guarantee a continuous current input to the CSI inverter.

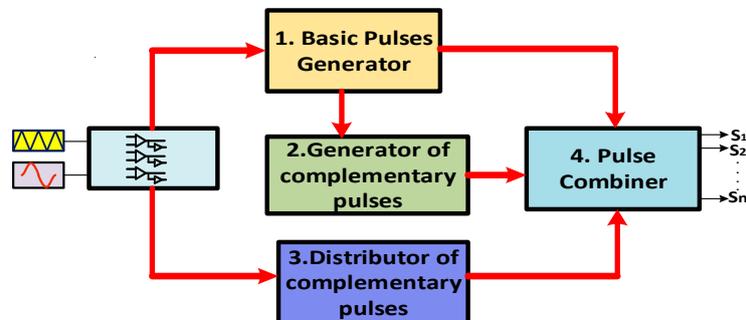


Figure 9. Gating signal generation.

The map gating signals obtained in the simulation of the PWM technique used, is present in Figure 10.

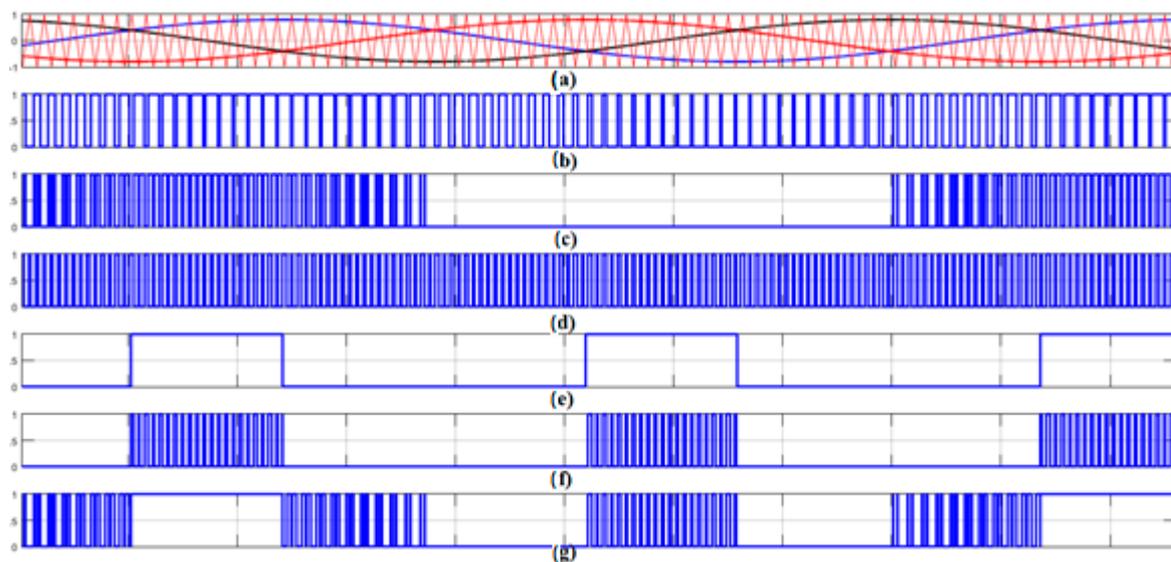


Figure 10. Map gating signals generations. (a) Carrier and modulating signals; (b) pulse generator conventional pulse-width modulation (PWM); (c) commutation basic; (d) pulses of short circuit; (e) pulses of distribution; (f) signal of distribution; (g) signals of gating.

### 3.2. Implementation of the Proposed Method

The converter topology driven by the method proposed was simulated using the MATLAB-SIMULINK toolbox. The parameters for the simulation are shown in Table 2. The  $F_s$  value was selected as 35 kHz, and the THD was analyzed under the three conditions A, B, and C, as previously defined. The results are shown in Figure 11, which indicate that condition B has less THD harmonic distortion than the other two conditions. Thus, it can be concluded that a better response was obtained when the CSI works at a higher frequency than the V-I converter.

Once the modulations condition C was selected ( $f_{svi} = 35$  kHz and  $f_{scsi} = 70$  kHz), an analysis was performed to validate this selection. This pretended to demonstrate the switching pattern that followed, to obtain a current output in V-I with less harmonic content. The analysis is shown in Figure 12.

Table 2. Parameters of simulations.

Parameter	Values
$V_{dc}$	100 V
Current	10 A
Inductor $L_1$	10 mH
Frequency $F_s$	35 kHz
Capacitor C1, C2, C3	1.5 $\mu$ F
Index of Modulation $m$	0.8
L Load	1.5 mH
R Load	1.3 $\Omega$

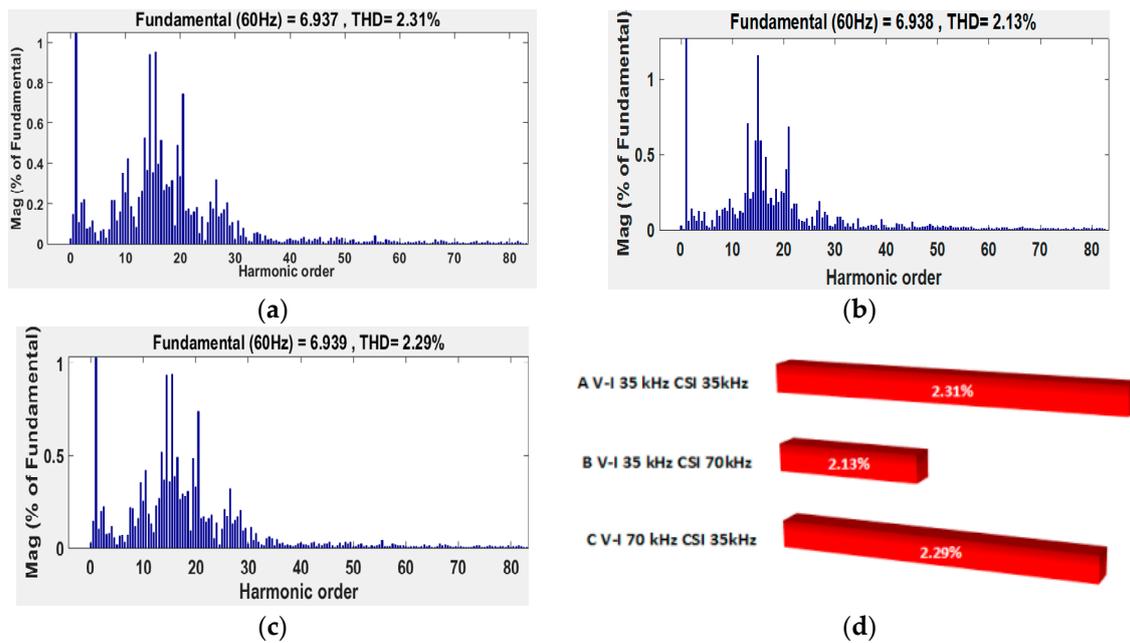


Figure 11. Total harmonic distortion (THD) spectrum results. (a) THD spectrum for situation A, (b) THD spectrum for situation B, (c) THD spectrum for situation C, (d) comparative results graph.

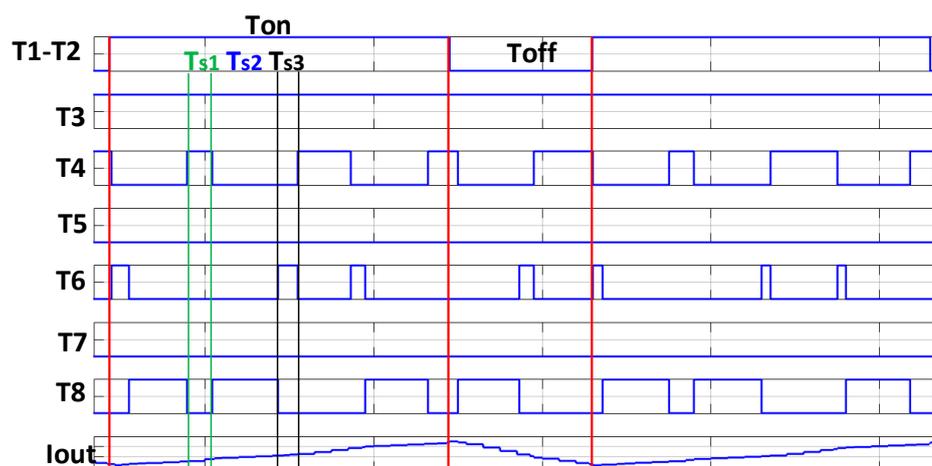


Figure 12. Switching pattern signals for V-I-CSI to  $f_{svi} = 35$  kHz and  $f_{scsi} = 70$  kHz.

The two states ON/OFF of the V-I have a time duration  $T_{on}$  and  $T_{off}$ , in which several commutations occur in the CSI converter. The current of the CSI was short-circuited when two transistors of one leg were switched at the same time ( $T_3$  and  $T_4$  in  $T_{s1}$ ). In  $T_{s2}$ , two transistors were closed in the upper and lower aspects of different branches ( $T_3$  and  $T_8$ ), and the current flowed through

the load connected to the CSI. This occurred as long as transistors of V-I and  $T_1$ – $T_2$  were turned on ( $T_{on}$ ). In time,  $T_{s3}$ , the conduction of the current, continued, but now it passed through  $T_3$ , which was in the upper part of the branch, and through  $T_6$ , which belonged to the lower part of the leg 2, and also through the load that of CSI. These sequences were repeated, whereas the V-I converter was in the ON state. If the transistors were open, the current descended and presented a slope of fall for the duration of  $T_{off}$ , as shown in Figure 12.

Under modulation conditions of B, the frequency of V-I was double that of CSI, and the current of CSI was again short-circuited, when two transistors of one leg were switched at the same time ( $T_{s1}$ ), the current having a slope positive. In the next period  $T_{s2}$ , the current flowed by transistors of two different legs ( $T_3$ – $T_8$ ), and closed for the load that was connected to CSI, then having a positive ramp but a lower slope. This happened as long as the transistors of V-I  $T_A$ – $T_B$  were turned on ( $T_{on}$ ) (Figure 13).

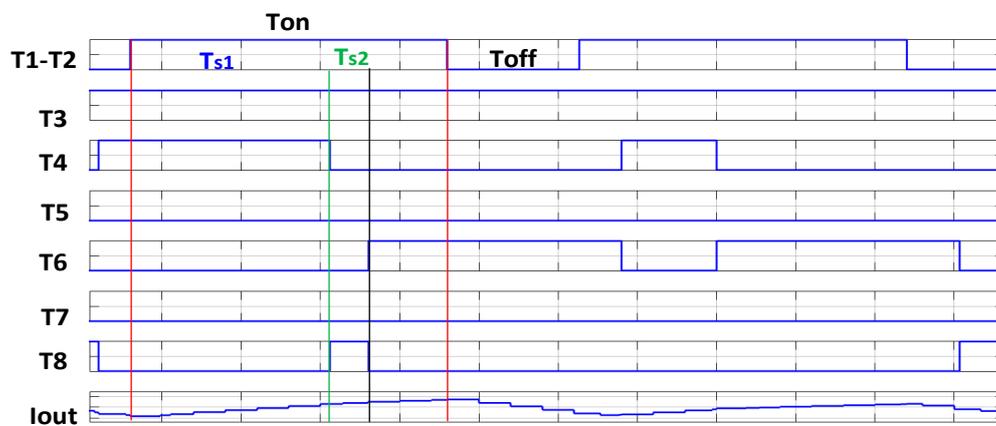


Figure 13. Switching pattern signals in V-I-CSI to  $f_{svi} = 70$  kHz and  $f_{scsi} = 35$  kHz.

These two cases were compared, and the THD of the V-I output current was analyzed with a DC component. The results obtained were shown in Figure 14. As shown, somewhat less distortion with a higher harmonic order appeared in case B, i.e., the CSI switching frequency was double the V-I one.

The next step was to develop an analysis that consisted of moving the angle-shift for the carrier signals of the converters. The displacement was a range of  $0^\circ$  to  $180^\circ$  in steps of  $30$  grades. After that, performing a calculation of THD for each set point of phase-shift with the previously selected frequency values regarding the result shown in Figure 15, the THD was reduced to 1.98% when the shifting between the carrier signals was  $90^\circ$ .

To understand the THD related to the phase change between carrier signals, the CSI and V-I activation signal map was analyzed. Also, the conduction and short-circuit sequence were established for each instant of turning ON and OFF the V-I converter. For the situation of  $0^\circ$  degrees of phase shift, the signal activation map of CSI and V-I is shown in Figure 16.

Where C is the situation of conduction, and \* is the situation of the short circuit. The sequence for this situation is C\*CC\*CC|C\*CC\*CC, and it is repeated for all cycles. The signals map for the phase angles of  $90^\circ$  and  $120^\circ$  are shown in Figure 17; in these situations, the highest and lowest value of THD is produced.

In the first situation, (a) it was observed that there were two short-circuit states with short durations when the V-I converter was in the OFF state, and two short-circuits with a short times of duration in the ON state. In (b) situation, it was observed that there were three short-circuit states for each ON and OFF state of the V-I. From this analysis, it can be concluded that the more short-circuit states a with minor time of duration in the CSI, the higher a THD is generated, and when there are less short-circuit states with minor times, a reduction in the THD is obtained. Finally, the duration time of the short-circuit also increments the THD for the same number of short-circuit states. Table 3 shows

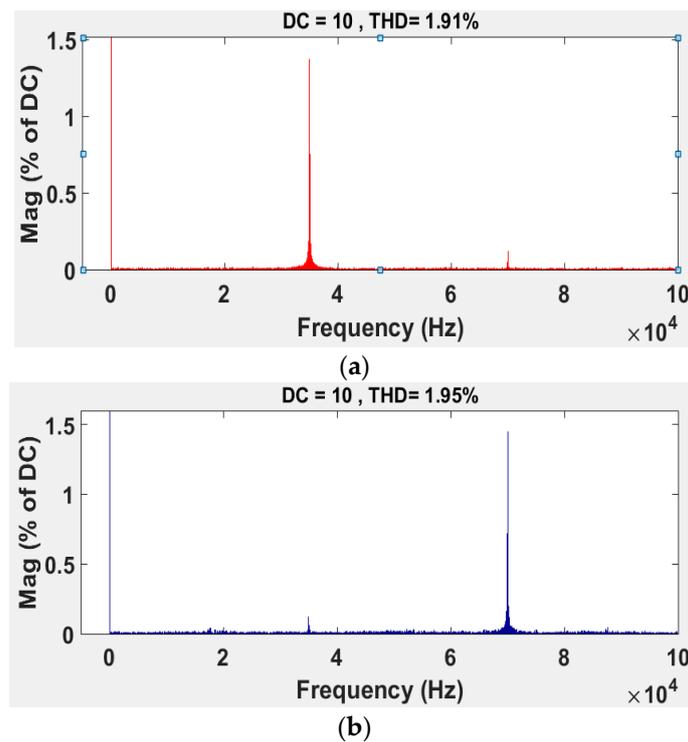
the result of THD for each situation of angle shift and sequence of the conduction–short circuit that is obtained.

The output currents and the THD analysis for the condition of  $f_{svi} = 35$  kHz and  $f_{scsi} = 70$  kHz with an offset angle between the signals carriers of  $90^\circ$  are shown in Figure 18.

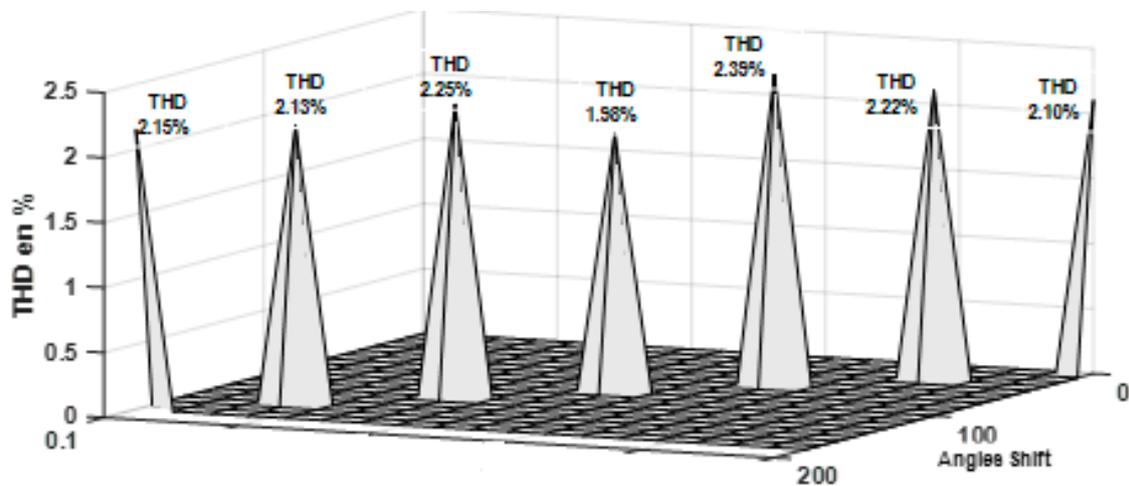
In addition, the same analysis was realized but now with the V-I frequency ratio of 70 kHz, the CSI at 35 kHz and shift-angles of  $0^\circ$ ,  $90^\circ$  and  $120^\circ$ . The results are shown in Figure 19.

The results of these switching patterns indicate that if the frequency of the V-I is double that of the CSI, the short-circuit the time increase. This produces a greater harmonic distortion in the output currents. The THD obtained in these three phase situations are shown in Table 4.

In this way it was determined that situation B is the most optimal, and when the shift angle between the carriers is  $90^\circ$  in this condition, the smallest THD value of the whole analysis is obtained.



**Figure 14.** THD comparison. (a) THD in the DC output current in V-I-CSI to  $f_{svi} = 35$  kHz and  $f_{scsi} = 70$  kHz. (b) THD in the DC output current in V-I-CSI to  $f_{svi} = 70$  kHz and  $f_{scsi} = 35$  kHz.



**Figure 15.** THD results for  $f_{svi} = 35$  kHz and  $f_{scsi} = 70$  kHz when the carrier phase is shifting.

Table 3. THD result with angle-shift and sequence.

Angle of Shift	Values of THD	Sequence ON OFF
0°	2.10%	C*CC*CC   C*CC*CC
30°	2.22%	CC*CC*C   CC*CC*C
60°	2.39%	*CC*C*C   *CC*C*C
90°	1.98%	C*CC*CC   C*CC*CC
120°	2.25%	*CC*CC*   *CC*CC*
150°	2.13%	C*CCC*C   C*CCC*C
180°	2.15%	CC*C*CC   CC*C*CC

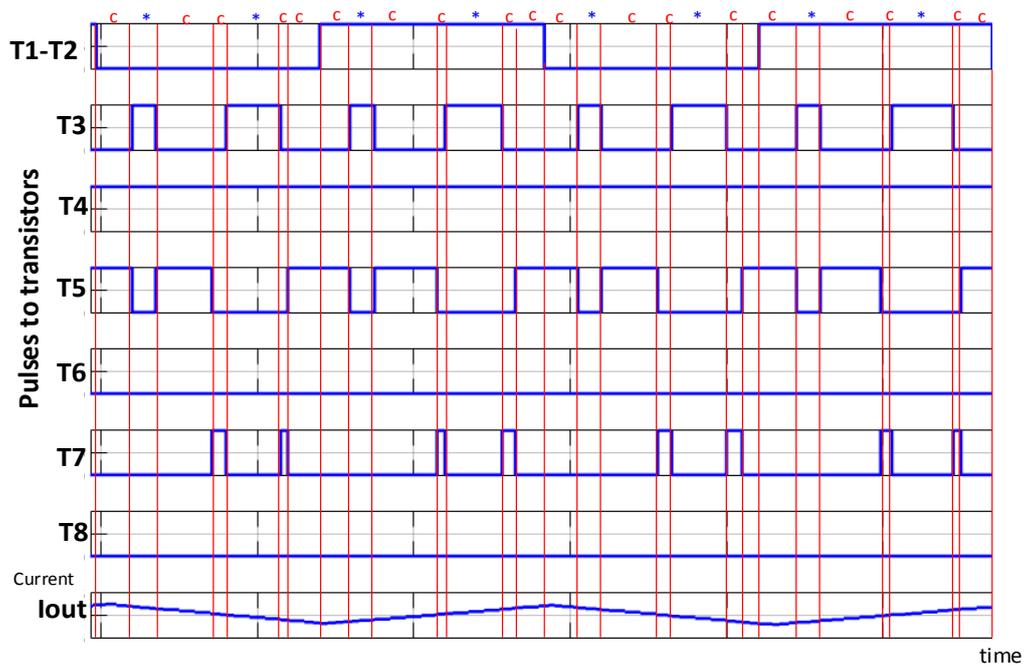
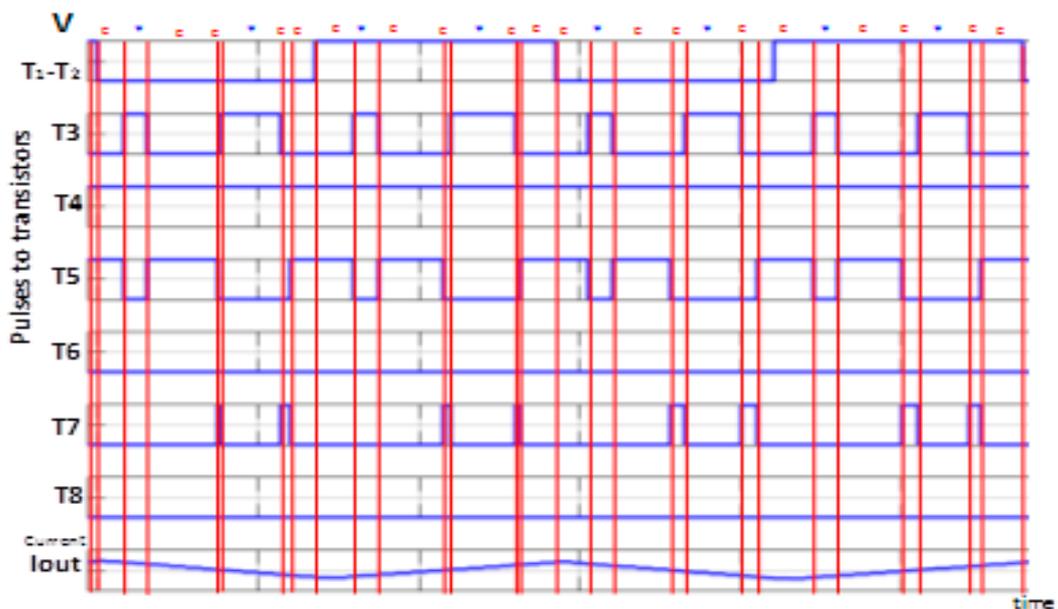


Figure 16. Map signal in CSI and V-I with 0° of phase shift between the signal carrier.



(a)

Figure 17. Cont.

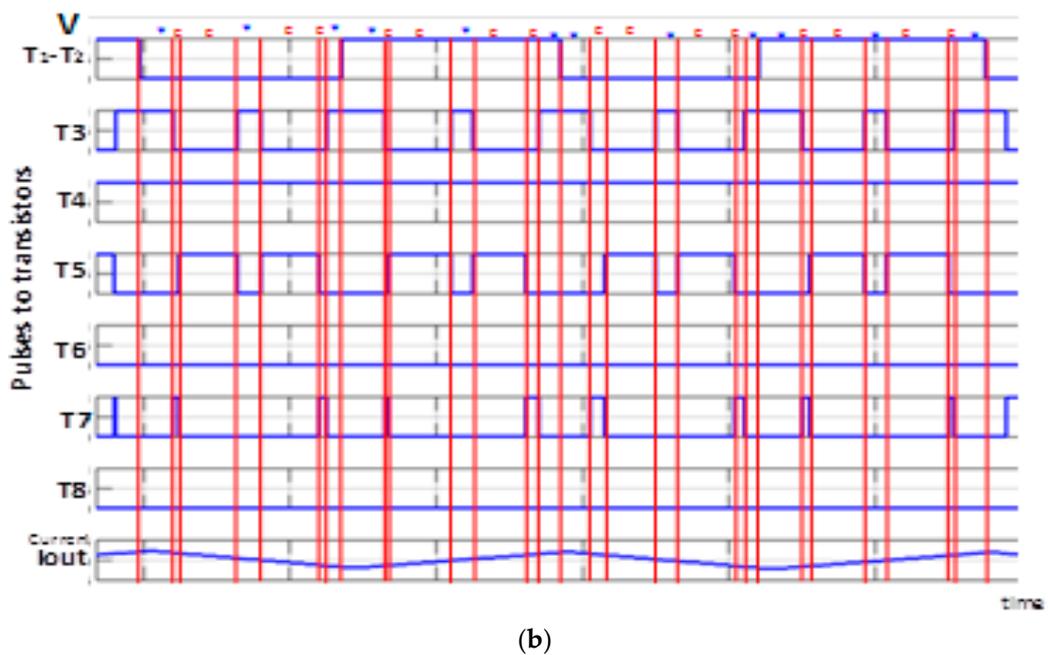


Figure 17. Signal map in CSI and V-I: (a) Situation for 90° of phase shift, (b) situation for 120° of phase shift.

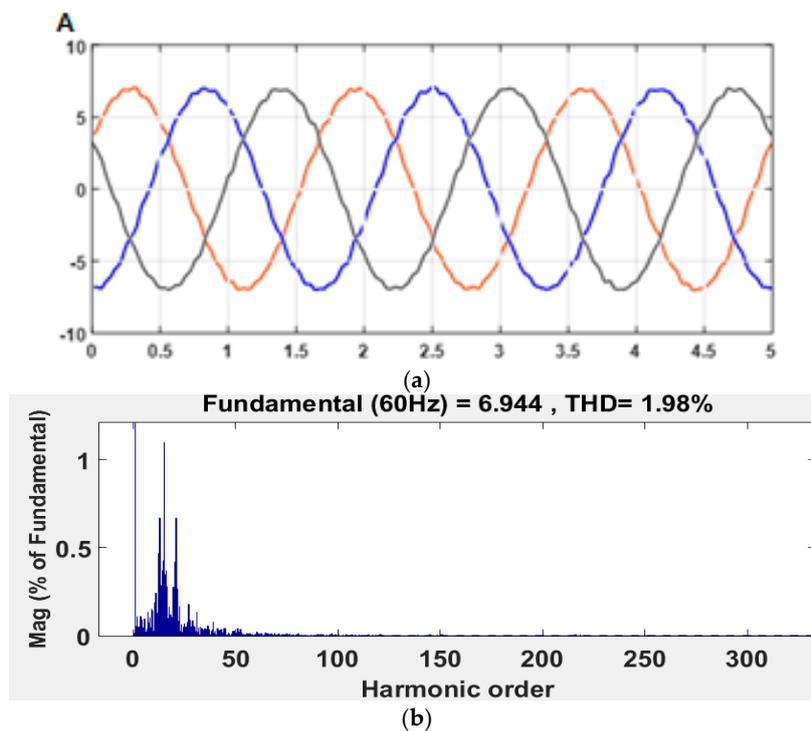
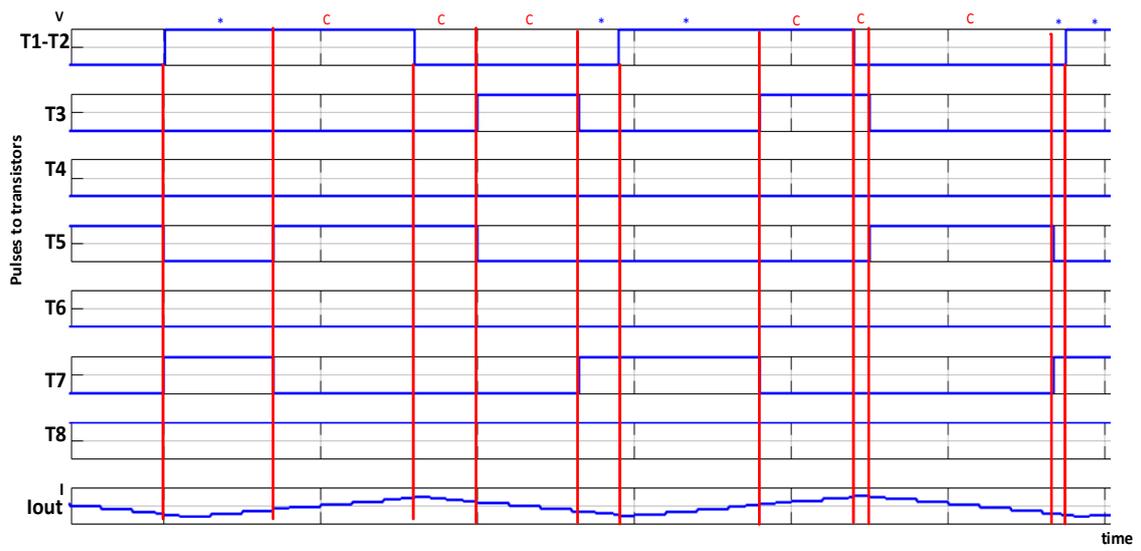


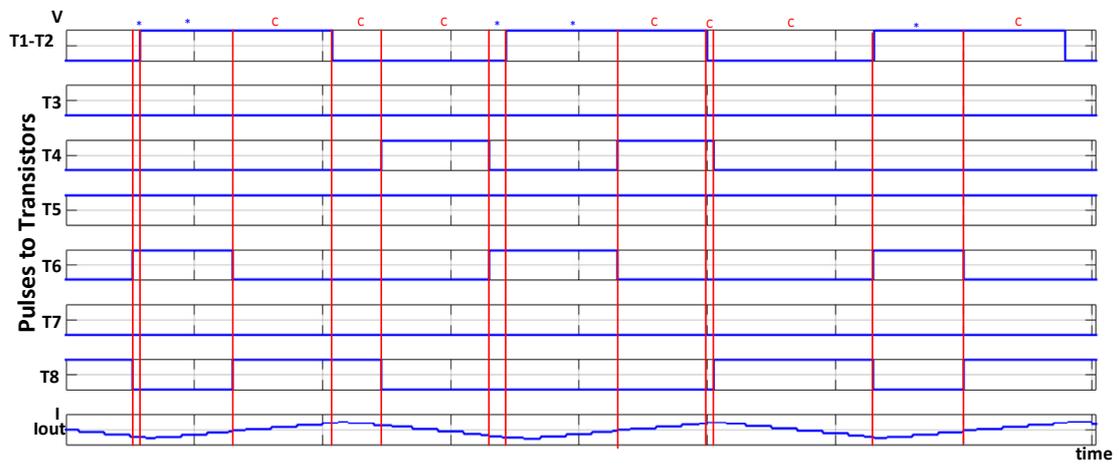
Figure 18. Simulation results of the method for the second part: (a) currents of output in situation B and a 90° shift angle; (b) THD analysis of the output current.

Table 4. Result of THD with an angle shift.

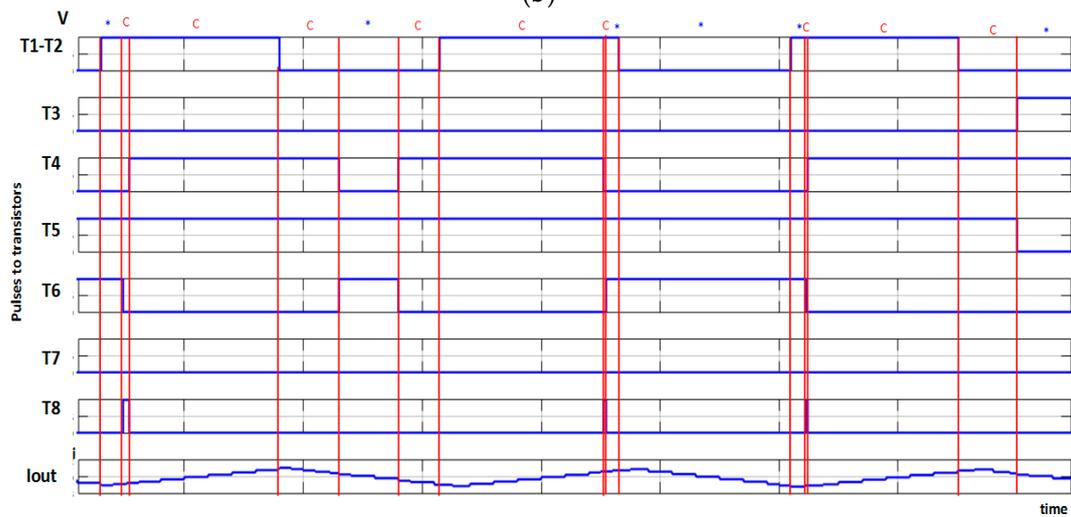
Shift-Angle	Values of THD
0°	2.29%
90°	2.74%
120°	2.45%



(a)



(b)



(c)

**Figure 19.** Simulation results for  $f_{SV-I} = 70$  kHz and  $f_{scsi} = 35$  kHz. (a) Situation at  $0^\circ$  of shift angle. (b) Situation at  $90^\circ$  of shift angle. (c) Situation at  $120^\circ$  of shift-angle.

#### 4. Analysis of Power Losses, Temperature and Efficiency

##### 4.1. Power Losses and Efficiency in the V-I Power Converter

The power losses analyzed were the conduction and switching losses. The parameters of device SiC are shown in Table 5.

**Table 5.** Parameters of simulations.

Parameter	Mosfet SiC	Parameter	Diode SiC
Model	SCT2450KE	Model	C3D10065I
Voltage $V_{DS}$	1200 V	$V_{RRM}$ (V)	650 V
Current	10 A	$Q_C$ (nC)	110 nC
$R_{ds}$	450 m $\Omega$	$I_F$ (A)	10 A
Power Dissipation	85 W		
Operating Junction	175 °C		

The conduction losses in the MOSFET SiC and diode SiC could be expressed for (9) and (10); the switching losses in the Mosfet SiC and SiC diode were expressed in (11) and (12) [4–24]:

$$P_{cond\_MOSFET} = R_{ds(ON)} I_{rms}^2 \quad (9)$$

$$P_{cond\_Diode} = I_{rms}^2 R_D + I_{DC} V_D \quad (10)$$

where  $R_{ds}$  is the drain-source resistor of SiC MOSFET,  $I_{rms}$  were the effective current flowing in the device.  $I_{DC}$  is the value of the current flowing through the diode, respectively:

$$P_{swM} = f_{sw}(E_{on} + E_{off}) \quad (11)$$

$$P_{swD} = f_{sw}(E_{swD}) \quad (12)$$

where  $E_{ON}$  is the turn-on switching energy,  $E_{OFF}$  is the turn-off switching energy in the MOSFET SiC and  $E_{swD}$  is the energy of switching in the SiC Schottky diode [18]. The  $E_{on}$ ,  $E_{off}$ , and  $E_{swD}$  are calculated by (13)–(15):

$$E_{on} = \int_0^{tri + tfv} V_{ds}(t) I_D(t) dt = V_{dc} I_{on\_rms} \left( \frac{tri + tfv}{2} \right) + Q_{rr} V_{dc} \quad (13)$$

$$E_{off} = \int_0^{tri + tfv} V_{ds}(t) I_D(t) dt = V_{dc} I_{off\_rms} \left( \frac{tri + tfv}{2} \right) \quad (14)$$

$$E_{swD} = \int_0^{tri + tfv} V_d(t) I_f(t) dt = \frac{1}{4} Q_{rr} V_{dc} \quad (15)$$

where  $V_{DS}$  is the voltage drain source,  $I_D$  the continuous drain current,  $V_{dc}$  is the voltage Dc link; the  $t_{ri}$ ,  $t_{fv}$ , and  $Q_{rr}$  are the current rise time, voltage fall time, and the reverse recovery charge, respectively [24]. All these parameters are in the datasheet of the devices.

##### 4.2. Inductor Core Losses

The losses in the inductors are from the following sources, hysteresis loss, copper or winding loss and eddy current loss. The hysteresis loss is due to the materials intrinsic properties, due to the energy used to align and re-align the magnetic domains. The general form of the losses for hysteresis  $P_m$  is calculated by the Expression (16):

$$P_m = k \cdot f^a B_{max}^d \quad (16)$$

where  $a$ ,  $d$ , and  $k$  are constants, depending of the type of material, for this case is ferrite. Eddy current loss from the circulating currents within the magnetic materials, due to the differential in flux voltage

inside the cores itself [25]. These losses were highly dependent upon the thickness of the walls of the cores. The eddy current loss per unit of volume could be calculated by Expression (17):

$$P_{ec} = \frac{\eta^2 f^2 B_{max}^2}{6\rho} \tag{17}$$

where  $\eta$  is the Steinmetz hysteresis constant, and  $\rho$  is the density of the material. The copper losses in the inductor are calculated by Expression (18):

$$P_{copper} = i_{dc}^2 R_{coil} \tag{18}$$

The total power losses in the inductor are obtained by the Expression (19) and are shown in Table 6:

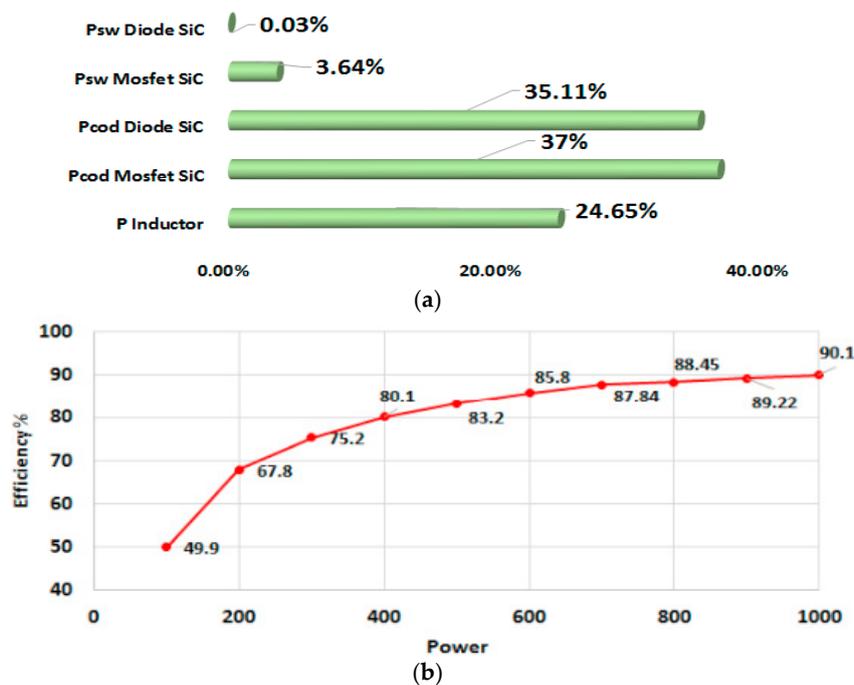
$$P_{inductor} = P_m + P_{sc} + P_{copper} \tag{19}$$

**Table 6.** Inductor core losses.

Parameter	Value
Hysteresis losses	0.0517 W/cm <sup>3</sup>
Eddy current losses	0.2738 W/cm <sup>3</sup>
Copper losses	29.93 W/cm <sup>3</sup>
Total of losses in the inductor	30.255 W/cm <sup>3</sup>

The rated power of the V-I converter is 1 kW. Figure 20 shows the analysis of power losses and efficiency in the V-I power converter switching at 35 kHz, with a phase-shift of 90° in PWM carriers. Efficiency is calculated with Expression (20):

$$\eta = \frac{P_{out}}{P_{out} + \sum P_{Losses}} \tag{20}$$



**Figure 20.** Result of analysis in the V-I power converter. (a) Power losses (b) Efficiency.

#### 4.3. Power Losses and Efficiency in the Current Source Inverter

In the case of the CSI converter, the important rule for the calculation of losses is that there is at least one device turned on in the converter [24]. The expressions that were implemented to calculate the losses for switching and conduction were as in the previous section. However, this time the topology of a Schottky SiC diode connected in series with each SiC MOSFET was considered. The results of power losses in the CSI converter by switching and conduction to 70 kHz, and 90° of phase shift in the PWM carriers are presented in Figure 21. The rated power of the CSI converter was 1.5 kW.

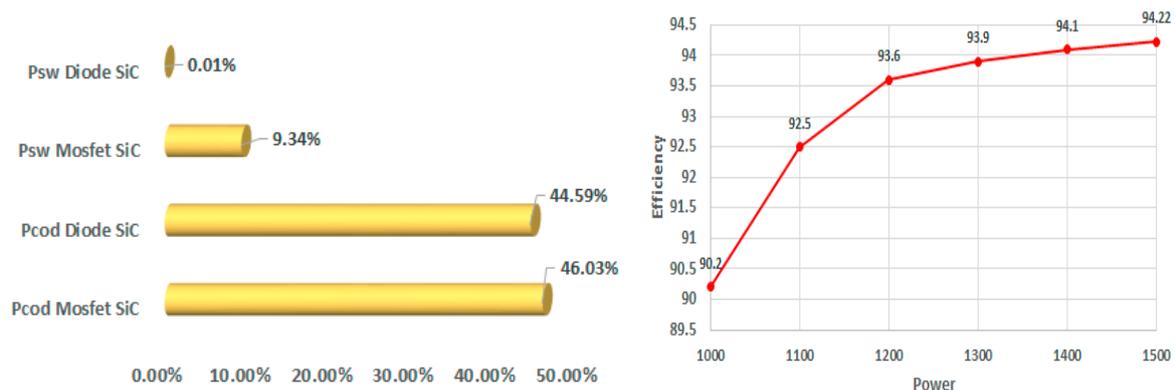


Figure 21. Power losses and efficiency in the CSI power converter.

#### 4.4. Power Losses in the Electric Motor

This section presents the analysis of the power losses in the electric motor, considering four situations of operation previously analyzed, 0 degrees, 60 degrees, 90 degrees (angle with lower THD), 120 degrees of phase shift in PWM carriers for V-I and CSI converters. This analysis aims to perform a comparative study and to show that the reduction of harmonics allows for the improvement of the efficiency of the electric motor.

In the permanent magnet synchronous motor (PMSM), there are two main electrical losses, the core losses in the iron core, and the copper losses in the winding. The fundamental iron loss consisted of hysteresis loss and eddy current loss, and copper losses, which were caused by the stator coil resistance  $R_s$  [26,27]. The copper losses were the losses due to the heat (Joule effect) that produced the current when it was circulated by a conductor, and it could be expressed by (21). In the analysis, the data of a PMSM engine implemented in another previous study was considered [27,28].

$$P_{CU} = mR_s I^2 + \sum_{h=3}^{\infty} I_n^2 R_{n,ac} \quad (21)$$

where  $m$  is the number of phases,  $R_s$  is the resistance, and  $I$  is the DC current,  $I_n$  is the root mean square (RMS) of the  $n$ th current harmonic.  $R_{n,ac}$  is the value of the ohmic for the  $n$ th harmonic that is determined by Expression (22).

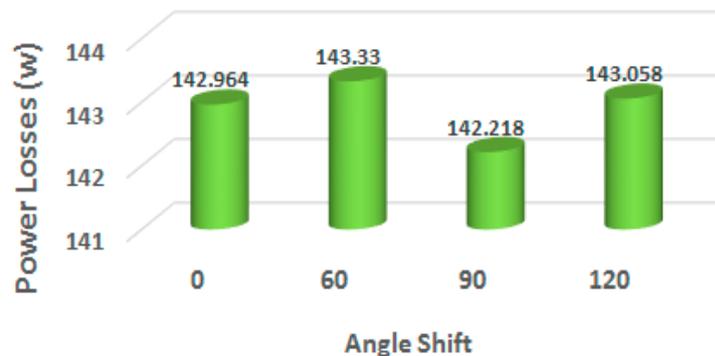
$$R_{n,ac} = R_{dc} (K_{n,se} + K_{n,pe}) \quad (22)$$

where  $K_{n,se}$  is the resistance gain cause for the effect skin, and  $K_{n,pe}$  is the resistance gain caused by the proximity effect. The iron losses are calculated on the basis of Expression (23):

$$P_{iron} = k P_{FEo} \left( \frac{f}{f_o} \right)^{\frac{2}{3}} \left( M_d \left( \frac{B_d}{B_o} \right)^2 + M_{ce} \left( \frac{B_{ce}}{B_o} \right)^2 \right) \quad (23)$$

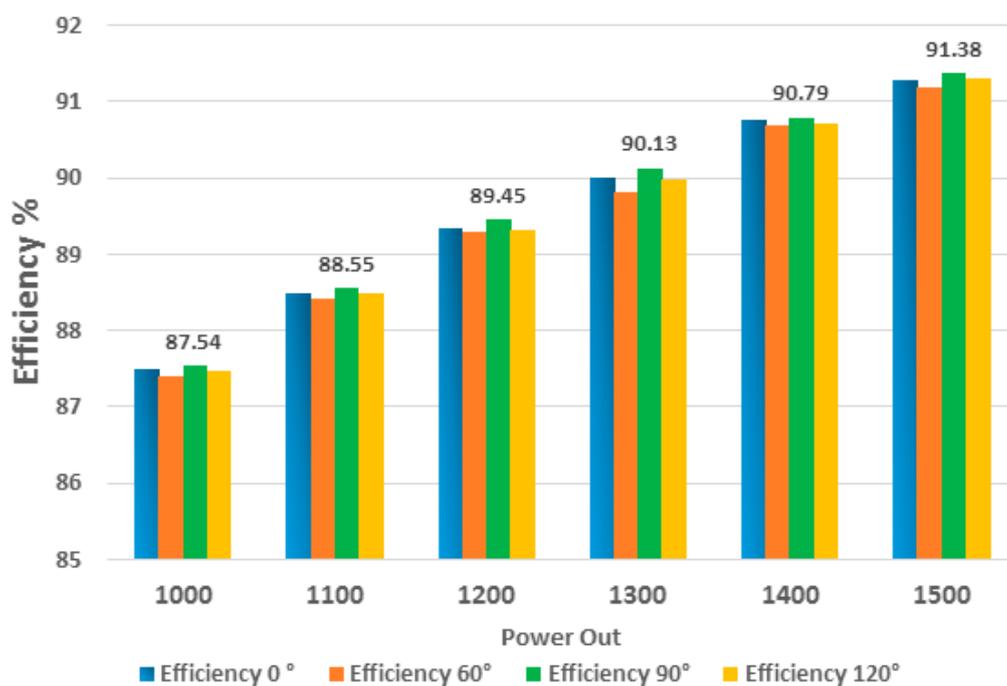
where  $k$  is the coefficient of additional losses in iron,  $P_{FEo}$ , for magnetic sheet M250-50A,  $f_o$  is the frequency,  $B_o$  is the maximum induction value,  $B_d$  is the maximum induction in the teeth,  $B_{ce}$  is the

maximum induction in the stator crown,  $M_d$  is mass of the teeth, and  $M_{ce}$  is the mass of the stator crown. The result of power losses in the PMSM for the four situations are showed in Figure 22.



**Figure 22.** Power losses in permanent magnet synchronous motor (PMSM) with shift angle in 0°, 60°, 90°, and 120° in the power converters.

The representation of the efficiency of the motor for the situations of shift phase angles (0°, 60°, 90°, and 120°) are shown in Figure 23 are compared for different power outputs.



**Figure 23.** Efficiency in an electric motor for shift angles of 0°, 60°, 90°, and 120° in the power converters.

The weighted average efficiency of the whole system (power converters + motor) in the situations of 0° and 90° is shown in Table 7 and Figure 24. The study allows for the demonstration that by using the proposed method, an improvement in the efficiency of the systems analyzed is obtained.

**Table 7.** Parameters of simulations.

System	Efficiency at 0°	Efficiency at 90°	Power Out
V-I	88.25%	90.1%	1 kW
CSI	93.8%	94.22%	1.5 kW
Motor	91.2%	91.38%	1.5 kW
Average	91.08%	92%	1.5 kW

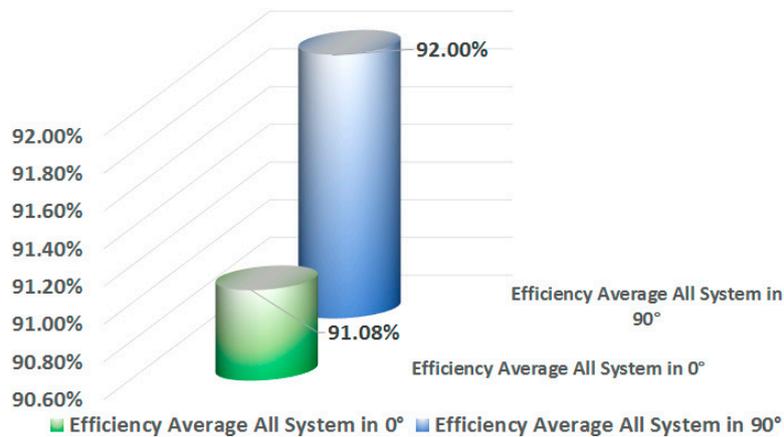


Figure 24. Efficiency in all systems.

Application of the proposed modulation patterns produced a gain in efficiency that was not highly significant (0.91%), but it was good enough to reduce the thermal stress of the power converters, the thermal behavior of the whole system, as well as the improvement of the wave shape of motor currents.

Finally, a comparative study was carried out with a hybrid DC–DC converter and VSI topology with silicon IGBTs and SiC diodes. This was done for the purpose of comparing and validating the efficiency between these topologies with frequency of operation of 5 kHz for DC–DC, and 10 kHz for VSI. The features of devices used for the hybrid DC–DC and VSI topologies are presented in Table 8.

Table 8. Parameters of simulations.

Parameter	Mosfet SiC	Parameter	Diode SiC
Model	HGTG30N60BD3	Model	C3D10065I
Voltage $V_{CE}$	600 V	$V_{RRM}$ (V)	650 V
Current	15 A	$Q_C$ (nC)	110 nC
Power Dissipation	208 W	$I_F$ (A)	10 A
Operating Junction	150 °C		

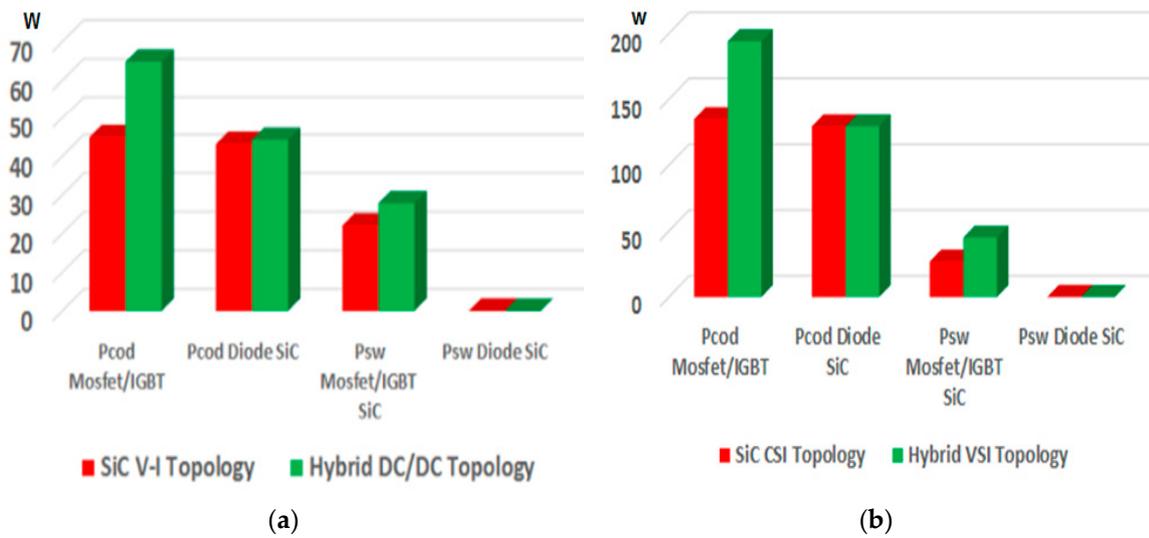
The comparison between the two topologies in terms of power losses are shown in Table 9 and Figure 25.

When obtaining the THD of the currents of the VSI topology (Figure 26) and comparing it with the previous analysis, it can be seen that the harmonic distortion increases to 2.52%. This causes losses throughout the system to increase.

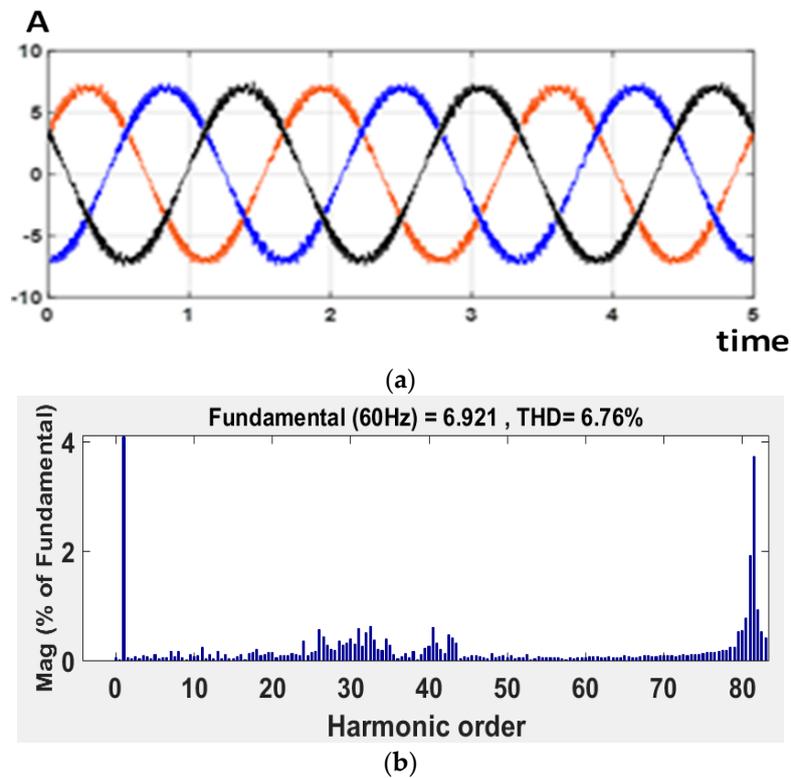
These results justify us that the V-I topology with the CSI inverter of SiC devices presents better responses in losses and in harmonic distortion, with respect to the proposed VSI topology for the comparison.

Table 9. Power losses between SiC topology and Hybrid Topology.

Parameter	All-SiC Topology V-I-CSI		Hybrid Topology DC/DC-VSI	
	$P_{\text{conduction Mosfet SiC/IGBTs}}$	44.98 W	134.94 W	64.9 W
$P_{\text{conduction diodes}}$	43.16 W	129.48 W	44.57 W	129.42 W
$P_{\text{switching SiC/IGBTs}}$	22.87 W	26.88 W	27.88 W	45.08 W
$P_{\text{switching diodes}}$	0.0296 W	0.178 W	0.0006 W	0.036 W
<b>Total</b>	<b>402.51 W</b>		<b>506.29 W</b>	



**Figure 25.** Power losses comparison results. (a) Power losses in V-I SiC vs. DC-DC hybrid topologies. (b) Power losses in CSI SiC vs. VSI hybrid topologies.



**Figure 26.** Results in VSI topology. (a) Current of output in VSI topology. (b) THD spectrum result for 6.76%.

#### 4.5. Heatsink Estimation

The use of a cooling system or heat sink is important for the operation of converter topologies. Using a simple thermal model for SiC devices, containing a junction and a case before the heatsink, and assuming that all devices are placed on the same plate, a maximum thermal resistance for the

heatsink can be estimated following the method described in [29]. The maximum allowable thermal resistance for the heatsink is calculated for Expression (24):

$$R_{\text{thhs}} = \frac{T_h - T_a}{\sum_{i=1}^n P_{d,i}} \quad (24)$$

where the  $R_{\text{thhs}}$  is the heatsink temperature,  $T_a$  is the ambient temperature, and  $P_d$  is the power dissipated by the component. Applying this method gives a heatsink estimate of the heatsink of  $0.68 \text{ }^\circ\text{C/W}$  for the V-I converter, and  $0.22 \text{ }^\circ\text{C/W}$  for the CSI inverter, with an operating temperature of  $142 \text{ }^\circ\text{C}$  and  $25 \text{ }^\circ\text{C}$  of the ambient temperature.

## 5. Conclusions

This paper presents a method for reducing the total harmonic distortion in the output currents of a CSI topology, with a V-I power converter based on SiC. The method consists of adjusting the switching frequency and the phase-shift angle between two carrier signals. The method proposed shows positive results that allow accurate synchronization between converter topologies. Among the results obtained, it is observed that the frequency of operation of the CSI has to be higher (double), that of the V-I, to obtain a reduction of the THD.

In addition, an improvement in the efficiency is observed by varying the phase angle between PWM carriers of both power converters switching modulators, V-I and CSI. According to the comparative analysis, the results show that the efficiency increases from 91.08% to 92% by changing the phase angle from  $0^\circ$  to  $90^\circ$  of shift angle.

Finally, as a general conclusion, the use of SiC devices in the topologies of inverters with current sources (CSI) allows for an increase in the frequency of switching, and improvements in their efficiency. This efficiency could even be increased by a proper adjustment of switching frequencies. These advantages could translate into a substantial reduction of inverter cost and volume, higher reliability, greater power, and improved engine efficiency, allowing for the consolidation of these topologies in electric traction systems.

**Author Contributions:** E.F. performed the design of method and validation in simulations. A.P. performed and assisted with the power losses and state-of-the-art methods. V.S. and L.R. contributed to objective definitions and the revision of the paper's methodology and conclusions. All authors carried out the theoretical analysis and contributed to writing the paper.

**Funding:** This research received no external funding

**Acknowledgments:** This work was supported in part by the Spanish Ministry of Economy and Competitiveness under the TRA2016-80472-R Research Project.

**Conflicts of Interest:** The authors declare no conflict of interest.

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