Voltage Balance Control Analysis of Three-Level Boost DC-DC Converters: Theoretical Analysis and DSP-Based Real Time Implementation

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Abstract: In this paper, a step-by-step description to get a unique three-level boost DC–DC converter (TLBDC) (DC—direct current) small signal model is first presented and validated through simulations and experiments. This model allows for overcoming the usage of two sub-models as in the conventional modeling approach. Based on this model, voltage balance (VB) controllers are designed and VB control analysis is presented. Two VB controllers, namely Proportional Integral (PI) and Fuzzy, were analyzed when the VB control was applied on both TLBDC switches or only one. According to the obtained simulation and experimental results, the proposed model gives an accurate approximation in dynamic, small perturbations around an operating point and steady state modes. Moreover, it has been shown that VB is achieved in a reduced time when VB control is applied on both the TLBDC's switches. Furthermore, the Fuzzy controller performs better than PI controller for VB control.

Keywords: three-level boost DC-DC converter; small signal modeling; voltage balance control

1. Introduction

In recent decades, modeling and control of DC–DC (DC—direct current) converters have gained much attention. This is due to their increased uses in various applications, such as voltage regulation [1–4], renewable energy interfacing [5–7], electric vehicle charging [8–10], etc. The conventional boost and buck converters are the basic topologies that are shown in Figure 1a,b, respectively. Due to their simplicity and high efficiency, they are the most used DC–DC converters. However, because of high voltage stress on their switching components, these conventional converters are not recommended for medium- and high-voltage ratings that require more powerful switching devices, which increase the cost, the volume, and the system complexity.
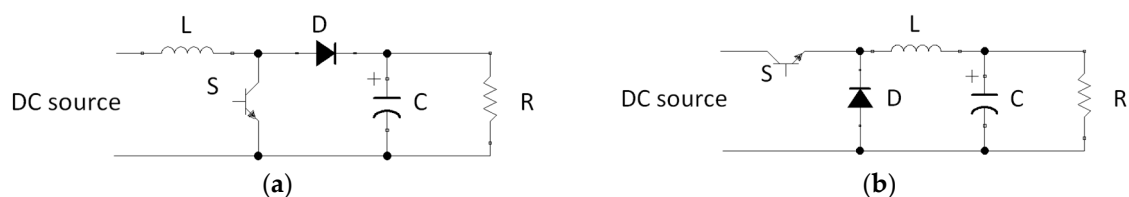
Figure 1. Conventional two-level schemes: (**a**) a boost converter, and (**b**) a buck converter.

Multilevel DC–DC converters are a suitable solution to overcome the aforementioned limitations. This is due to their ability to operate at high power ratings with higher efficiencies compared to

conventional two-level topologies. They also provide other advantages such as low distortion of the output voltage and lower switching losses [2–4,11–14]. The three-level DC-DC boost converter (TLBDC) depicted in Figure 2a, has been widely discussed [14–19]. The converter fundamentals and design considerations were presented in Reference [19], where it has been shown, for instance, that the converter inductance and capacitors can be significantly reduced when compared to the two-level boost DC–DC converter.

Based on the state-space modeling approach, several TLBDC models were presented [17,18,20–22], where two sub-models were used: the first one used for a duty ratio (DR) less than 50%, and the second one is used for a DR greater than 50%. Hence, a selection parameter is required to distinguish between these two sub-models. Using a state space averaged modeling (SSAM) approach and a small signal model (SSM), introduced in Reference [23] and discussed in detail in Reference [3], the transfer functions around a corresponding operating point could be extracted. A discrete-time approach is another way for TLBDC modeling [11,24]. However, it requires long and complex calculations when compared to the previous SSAM method. In Reference [25], a DSP-based implementation of a self-tuning Fuzzy controller for TLBDC has been presented. The converter was modeled using SSAM and three cases based on the DR values were presented: for a DR less than 50%, for a DR higher than 50%, and for any DR. The main objective was the output voltage controller synthesis. However, neither the modeling procedure has been described in detail, nor the simulation and practical model validation were carried out. Moreover, comparison between the single model and the conventional modeling approach was not addressed.

The proper operation of TLBDC needs the balance of the output capacitors' voltages. Different voltage balance (VB) control methods were presented [15,21,26–34]. In References [21,29], and referring to Figure 2, the VB control was achieved by delaying forward or backward SW2 switch control signals of the TLBDC. Another method using an existing energy storage system to ensure the VB was presented in Reference [26]. In References [30–34], the VB control was performed by a PI controller. The controller output was added to the DR of the switch SW1 and subtracted from the DR of switch SW2. A sensor-less VB control method was also proposed in Reference [15] using a PI controller whose output was added to the DR of switch SW2. Finally, in Reference [25], the output capacitors' voltages were sensed, and a PI-controller was used for VB control. The controller output was added to the SW2 switch DR.

Through this literature review, it is clear that the main VB control methods consist in the following: add a small perturbation to one (or both) converter's switch(es) DR(s), or adjust the delay between the switches control signals. However, the method to choose the TLBDC switch(es) on which VB control should be applied was not addressed.

Based on these motivations, and unlike Reference [25], where the main goal was the output voltage controller synthesis, this paper adds further contributions to the state of the art by giving a step-by-step description of the followed method to get a unique model for a TLBDC working in continuous conduction mode (CCM), with a non-zero inductor equivalent series resistor. The unique model allows for avoiding the usage of two sub-models as in the conventional modeling approach, and facilitates synthesizing a convenient VB controller. This model has been validated using simulation and experimental tests, and a comparison with the conventional modeling approach is addressed. On the other hand, a technique is presented to best ensure the VB of the TLBDC. The analysis is carried out using two different VB methods and controllers, namely PI and Fuzzy controllers. This allows for figuring out the convenient controller and the adequate way for the VB control of the TLBDC.

The rest of paper is organized as follows. Section 2 describes the TLBDC operation and the developed small signal model (SSM). The VB control of the TLBDC is analyzed in Section 3, followed by the conclusion. Each of Sections 2 and 3 gives theoretical developments as well as simulation and experimental results.

2. Three-Level Boost DC–DC Converter Small Signal Modeling

The electrical scheme of the TLBDC under study is shown in Figure 2a. It is composed of an inductor L, two power switches SW1 and SW2, two switching diodes D1 and D2, and finally two output capacitors C1 and C2. $u_1(t)$ and $u_2(t)$ are the SW1 and SW2 control signals, respectively. These control signals are phase-shifted by 180°, and two operating modes could be distinguished: a DR less than 50% and a DR higher than 50%. The control signals for these two cases are shown in Figure 2b,c, respectively [15,17–19,25].
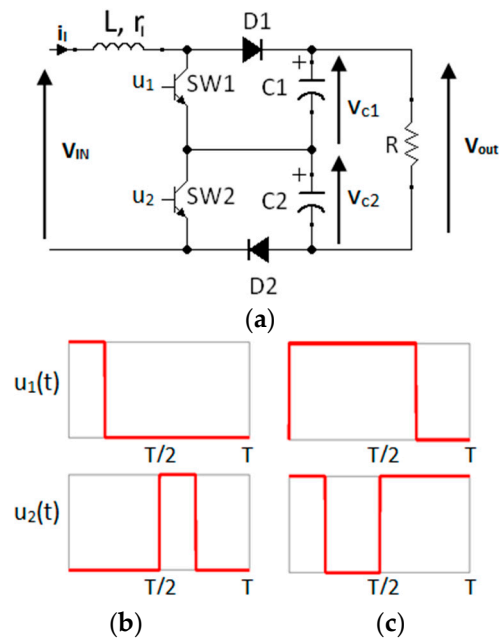
Figure 2. (**a**) The electrical scheme of the TLBDC under study, (**b**) TLBDC control signals for a DR less than 50%, and (**c**) TLBDC control signals for a DR higher than 50%.

Under CCM, the TLBDC is described by a set of equations and equivalent electrical schemes. These are summarized in Table 1 and Figure 3, respectively. i_l, r_l, v_{c1}, v_{c2}, v_{IN}, and v_{out} are the inductor current, inductor equivalent series resistor (ESR) (that equals 0.1 Ω in our case), capacitor C1 voltage, capacitor C2 voltage, and input and output voltages, respectively.
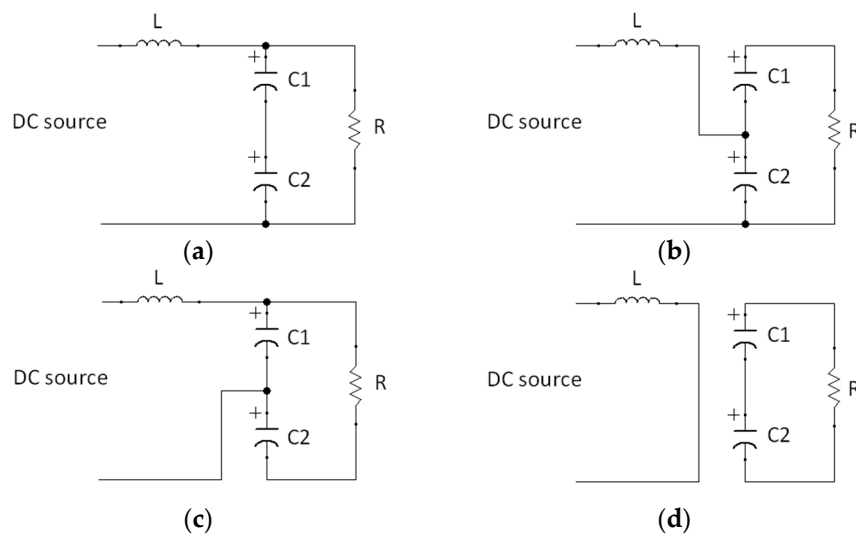
Figure 3. TLBDC equivalent electrical schemes for control signals $u_1(t)$-$u_2(t)$ sequence: (**a**) 0-0, (**b**) 1-0, (**c**) 0-1 and (**d**) 1-1.

Table 1. Differential equations for each control signals sequence of TLBDC working in CCM.

State of the Control Signals ($u_1(t)$-$u_2(t)$)	Differential Equations	
0-0	$\dfrac{d}{dt}i_l = -\dfrac{1}{L}v_{c1} - \dfrac{1}{L}v_{c2} + \dfrac{1}{L}v_{IN} - \dfrac{r_l}{L}i_l,$	(1)
	$\dfrac{d}{dt}v_{c1} = \dfrac{1}{C1}i_l - \dfrac{1}{R\cdot C1}v_{c1} - \dfrac{1}{R\cdot C1}v_{c2},$	(2)
	$\dfrac{d}{dt}v_{c2} = \dfrac{1}{C2}i_l - \dfrac{1}{R\cdot C2}v_{c1} - \dfrac{1}{R\cdot C2}v_{c2},$	(3)
	$v_{out} = v_{c1} + v_{c2},$	(4)
1-0	$\dfrac{d}{dt}i_l = -\dfrac{1}{L}v_{c2} + \dfrac{1}{L}v_{IN} - \dfrac{r_l}{L}i_l,$	(5)
	$\dfrac{d}{dt}v_{c1} = -\dfrac{1}{R\cdot C1}v_{c1} - \dfrac{1}{R\cdot C1}v_{c2},$	(6)
	$\dfrac{d}{dt}v_{c2} = \dfrac{1}{C2}i_l - \dfrac{1}{R\cdot C2}v_{c1} - \dfrac{1}{R\cdot C2}v_{c2},$	(7)
	$v_{out} = v_{c1} + v_{c2},$	(8)
0-1	$\dfrac{d}{dt}i_l = -\dfrac{1}{L}v_{c1} + \dfrac{1}{L}v_{IN} - \dfrac{r_l}{L}i_l,$	(9)
	$\dfrac{d}{dt}v_{c1} = \dfrac{1}{C1}i_l - \dfrac{1}{R\cdot C1}v_{c1} - \dfrac{1}{R\cdot C1}v_{c2},$	(10)
	$\dfrac{d}{dt}v_{c2} = -\dfrac{1}{R\cdot C2}v_{c1} - \dfrac{1}{R\cdot C2}v_{c2},$	(11)
	$v_{out} = v_{c1} + v_{c2},$	(12)
1-1	$\dfrac{d}{dt}i_l = \dfrac{1}{L}v_{IN} - \dfrac{r_l}{L}i_l,$	(13)
	$\dfrac{d}{dt}v_{c1} = -\dfrac{1}{R\cdot C1}v_{c1} - \dfrac{1}{R\cdot C1}v_{c2},$	(14)
	$\dfrac{d}{dt}v_{c2} = -\dfrac{1}{R\cdot C2}v_{c1} - \dfrac{1}{R\cdot C2}v_{c2},$	(15)
	$v_{out} = v_{c1} + v_{c2},$	(16)

Based on the differential Equations (1)–(16), the TLBDC state space equations for the four control signals sequences are given by Equations (17)–(24), where Equations (17) and (18) correspond to the state space equations for 0-0 control signals state, Equations (19) and (20) correspond to the state space equations for 0-1 control signals state, Equations (21) and (22) correspond to the state space equations for 1-0 control signals state, and Equations (23) and (24) correspond to the state space equations for 0-0 control signals state.

$$\frac{d}{dt}\begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} = \begin{vmatrix} -\frac{r_l}{L} & -\frac{1}{L} & -\frac{1}{L} \\ \frac{1}{C1} & -\frac{1}{R\cdot C1} & -\frac{1}{R\cdot C1} \\ \frac{1}{C2} & -\frac{1}{R\cdot C2} & -\frac{1}{R\cdot C2} \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} + \begin{vmatrix} \frac{1}{L} \\ 0 \\ 0 \end{vmatrix} \cdot v_{IN}, \tag{17}$$

$$v_{out} = \begin{vmatrix} 0 & 1 & 1 \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix}, \tag{18}$$

$$\frac{d}{dt}\begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} = \begin{vmatrix} -\frac{r_l}{L} & 0 & -\frac{1}{L} \\ 0 & -\frac{1}{R \cdot C1} & -\frac{1}{R \cdot C1} \\ \frac{1}{C2} & -\frac{1}{R \cdot C2} & -\frac{1}{R \cdot C2} \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} + \begin{vmatrix} \frac{1}{L} \\ 0 \\ 0 \end{vmatrix} \cdot v_{IN},\tag{19}$$

$$v_{out} = \begin{vmatrix} 0 & 1 & 1 \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix},\tag{20}$$

$$\frac{d}{dt}\begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} = \begin{vmatrix} -\frac{r_l}{L} & 0 & -\frac{1}{L} \\ 0 & -\frac{1}{R \cdot C1} & -\frac{1}{R \cdot C1} \\ \frac{1}{C2} & -\frac{1}{R \cdot C2} & -\frac{1}{R \cdot C2} \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} + \begin{vmatrix} \frac{1}{L} \\ 0 \\ 0 \end{vmatrix} \cdot v_{IN},\tag{21}$$

$$v_{out} = \begin{vmatrix} 0 & 1 & 1 \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix},\tag{22}$$

$$\frac{d}{dt}\begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} = \begin{vmatrix} -\frac{r_l}{L} & -\frac{1}{L} & 0 \\ \frac{1}{C1} & -\frac{1}{R \cdot C1} & -\frac{1}{R \cdot C1} \\ 0 & -\frac{1}{R \cdot C2} & -\frac{1}{R \cdot C2} \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} + \begin{vmatrix} \frac{1}{L} \\ 0 \\ 0 \end{vmatrix} \cdot v_{IN},\tag{23}$$

$$v_{out} = \begin{vmatrix} 0 & 1 & 1 \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix},\tag{24}$$

Using discrete variables $u_1(t)$ and $u_2(t)$, Equations (17)–(24) could be assembled into one equation. The obtained TLBDC model is given by Equations (25) and (26).

$$\frac{d}{dt}\begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} = \begin{vmatrix} -\frac{r_l}{L} & -\frac{1-u_1(t)}{L} & -\frac{1-u_2(t)}{L} \\ \frac{1-u_1(t)}{C1} & -\frac{1}{R \cdot C1} & -\frac{1}{R \cdot C1} \\ \frac{1-u_2(t)}{C2} & -\frac{1}{R \cdot C2} & -\frac{1}{R \cdot C2} \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} + \begin{vmatrix} \frac{1}{L} \\ 0 \\ 0 \end{vmatrix} \cdot v_{IN},\tag{25}$$

$$v_{out} = \begin{vmatrix} 0 & 1 & 1 \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix},\tag{26}$$

Equations (25) and (26) could be written as:

$$\frac{d}{dt}\begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} = \left[\begin{vmatrix} -\frac{r_l}{L} & -\frac{1}{L} & -\frac{1}{L} \\ \frac{1}{C1} & -\frac{1}{R \cdot C1} & -\frac{1}{R \cdot C1} \\ \frac{1}{C2} & -\frac{1}{R \cdot C2} & -\frac{1}{R \cdot C2} \end{vmatrix} + u_1(t) \cdot \begin{vmatrix} 0 & \frac{1}{L} & 0 \\ -\frac{1}{C1} & 0 & 0 \\ 0 & 0 & 0 \end{vmatrix} + u_2(t) \cdot \begin{vmatrix} 0 & 0 & \frac{1}{L} \\ 0 & 0 & 0 \\ -\frac{1}{C2} & 0 & 0 \end{vmatrix} \right] \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix} + \begin{vmatrix} \frac{1}{L} \\ 0 \\ 0 \end{vmatrix} \cdot v_{IN},\tag{27}$$

$$v_{out} = \begin{vmatrix} 0 & 1 & 1 \end{vmatrix} \cdot \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix},\tag{28}$$

Let us denote $\overline{x} = \begin{vmatrix} \overline{i_l} \\ \overline{v_{c1}} \\ \overline{v_{c2}} \end{vmatrix}$, $\overline{v_{IN}}$, $\overline{v_{out}}$, $\overline{u_1}$, and $\overline{u_2}$ as the average values of the state vector $x = \begin{vmatrix} i_l \\ v_{c1} \\ v_{c2} \end{vmatrix}$, v_{IN}, v_{out}, u_1, and u_2, respectively. Using this notation, the obtained SSAM is given by Equations (29) and (30):

$$\frac{d}{dt}\begin{vmatrix} \overline{i_l} \\ \overline{v_{c1}} \\ \overline{v_{c2}} \end{vmatrix} = \left[\begin{vmatrix} -\frac{r_l}{L} & -\frac{1}{L} & -\frac{1}{L} \\ \frac{1}{C1} & -\frac{1}{R\cdot C1} & -\frac{1}{R\cdot C1} \\ \frac{1}{C2} & -\frac{1}{R\cdot C2} & -\frac{1}{R\cdot C2} \end{vmatrix} + \overline{u_1}\cdot \begin{vmatrix} 0 & \frac{1}{L} & 0 \\ -\frac{1}{C1} & 0 & 0 \\ 0 & 0 & 0 \end{vmatrix} + \overline{u_2}\cdot \begin{vmatrix} 0 & 0 & \frac{1}{L} \\ 0 & 0 & 0 \\ -\frac{1}{C2} & 0 & 0 \end{vmatrix} \right] \cdot \begin{vmatrix} \overline{i_l} \\ \overline{v_{c1}} \\ \overline{v_{c2}} \end{vmatrix} + \begin{vmatrix} \frac{1}{L} \\ 0 \\ 0 \end{vmatrix} \cdot \overline{v_{IN}}, \quad (29)$$

$$\overline{v_{out}} = \begin{vmatrix} 0 & 1 & 1 \end{vmatrix} \cdot \begin{vmatrix} \overline{i_l} \\ \overline{v_{c1}} \\ \overline{v_{c2}} \end{vmatrix}, \quad (30)$$

Each variable can be written as the sum of small alternating current (AC) variations and DC steady-state quantities as follows:

$$\overline{x} = X + \widetilde{x}, \quad (31)$$

$$\overline{u_1} = U_1 + \widetilde{u_1}, \quad (32)$$

$$\overline{u_2} = U_2 + \widetilde{u_2}, \quad (33)$$

$$\overline{v_{IN}} = V_{IN} + \widetilde{v_{IN}}, \quad (34)$$

$$\overline{v_{out}} = V_{out} + \widetilde{v_{out}}, \quad (35)$$

Using this decomposition, Equations (31)–(35), Equations (29) and (30) become:

$$\dot{\widetilde{x}} = \left[\widetilde{\mathbf{u_1}}\mathbf{A_1} + \widetilde{\mathbf{u_2}}\mathbf{A_2} \right]\cdot\widetilde{\mathbf{x}} + B\widetilde{v_{IN}} + [A_0 + U_1A_1 + U_2A_2]\cdot \widetilde{x} + \widetilde{u_1}A_1X + \widetilde{u_2}A_2X + [A_0 + U_1A_1 + U_2A_2].X + BV_{IN}, \quad (36)$$

$$\overline{v_{out}} = \begin{vmatrix} 0 & 1 & 1 \end{vmatrix} \cdot \begin{vmatrix} \overline{i_l} \\ \overline{v_{c1}} \\ \overline{v_{c2}} \end{vmatrix}, \quad (37)$$

where: $A_0 = \begin{vmatrix} -\frac{r_l}{L} & -\frac{1}{L} & -\frac{1}{L} \\ \frac{1}{c1} & -\frac{1}{R\cdot C1} & -\frac{1}{R\cdot C1} \\ \frac{1}{C2} & -\frac{1}{R\cdot C2} & -\frac{1}{R\cdot C2} \end{vmatrix}$, $A_1 = \begin{vmatrix} 0 & \frac{1}{L} & 0 \\ \frac{-1}{C1} & 0 & 0 \\ 0 & 0 & 0 \end{vmatrix}$, and $A_2 = \begin{vmatrix} 0 & 0 & \frac{1}{L} \\ 0 & 0 & 0 \\ \frac{-1}{C2} & 0 & 0 \end{vmatrix}$.

Neglecting the higher-order terms, steady-state terms are null, and supposing that the supply voltage is constant, terms written in bold, italic, and bold italic in Equation (36), respectively [3]. The SSM of the TLBDC is given by Equations (38) and (39):

$$\dot{\widetilde{x}} = [A_0 + U_1A_1 + U_2A_2]. \widetilde{x} + \widetilde{u_1}A_1X + \widetilde{u_2}A_2X, \quad (38)$$

$$\widetilde{v_{out}} = \begin{vmatrix} 0 & 1 & 1 \end{vmatrix} \cdot \begin{vmatrix} \widetilde{i_l} \\ \widetilde{v_{c1}} \\ \widetilde{v_{c2}} \end{vmatrix}, \quad (39)$$

The proposed model is validated through simulation and experimental results. Simulations were performed on MATLAB software (Matworks, Natick, MA, USA) using the ode23 function, while the experimental tests were carried out on the experimental setup depicted in Section 3. The TLBDC parameters used for these tests are listed in Table 2.

The simulated and experimental output voltage curves for the switched model and the SSM around 30% and 60% DRs are respectively illustrated in Figures 4 and 5, where 4% positive and negative perturbations were introduced around those DR values.

Based on the results reported in Figure 4, it can be seen that the SSM behavior was in accordance with the switched one. In addition, the presented experimental results in Figure 5 were closely matching those obtained from the proposed SSM. By analyzing these results, one can see that the proposed SSM gave an averaged behavior of the TLBDC for both DR cases.
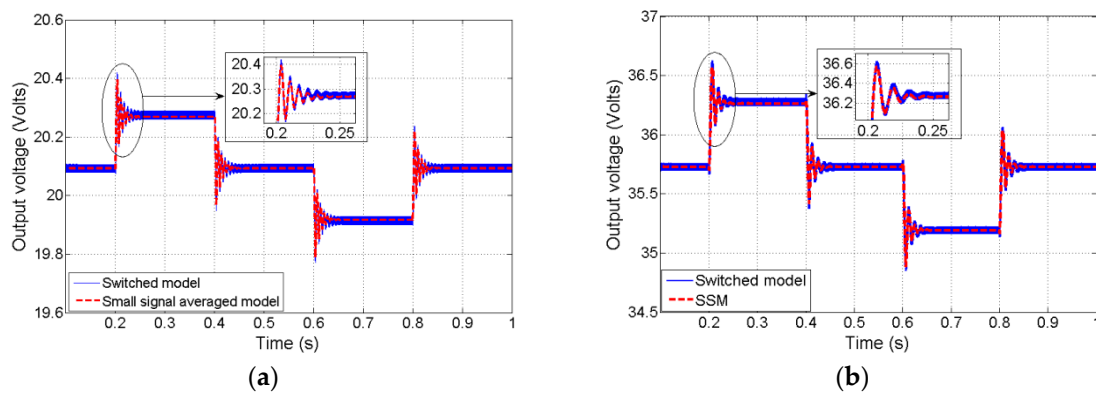
Figure 4. Simulated SSM and switched model output voltage curves in the case of 4% DR perturbation: (**a**) around 30%, and (**b**) around 60% DRs.
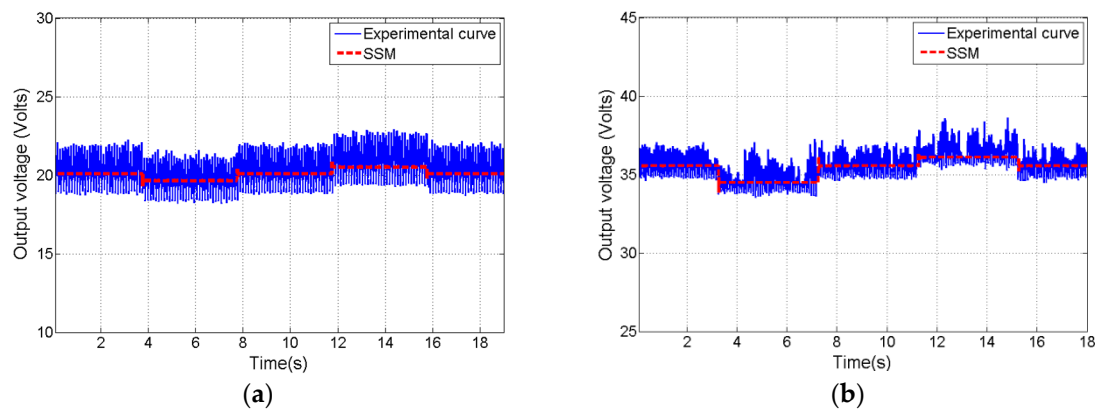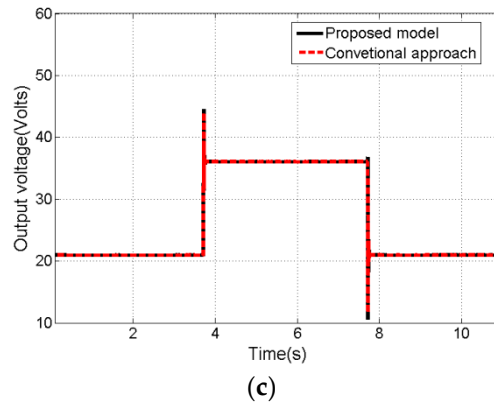

Figure 5. Experimental and SSM output voltages curves with 4% perturbation width: (**a**) around thirty percent and (**b**) around sixty percent DRs.

The results for a DR transition from a value less than 50%, namely 30%, to another one higher than 50%, namely 60%, are shown in Figure 6. The proposed SSAM and experimental output voltage curves are shown in Figure 6a, while Figure 6b illustrates the conventional SSAM and experimental output voltage curves. Finally, Figure 6c presents a comparison between the conventional approach and the proposed one.

Figure 6. *Cont.*

(**c**)
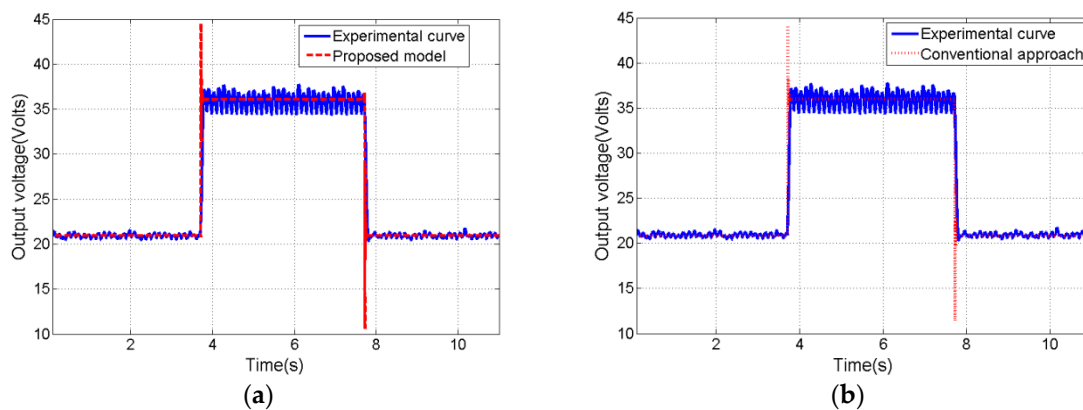
Figure 6. Curves for a DR value change from 30% to 60% to 30%: (**a**) proposed model and experimental output voltages, (**b**) experimental and conventional approach output voltages, and (**c**) proposed and conventional approach output voltages.

By analyzing the results depicted in Figure 6, the model behavior when the DR was changed from a value less than 50% to another one higher than 50% is similar to the conventional one. Both SSAM approaches had identical output voltage curves, but the conventional approach used two different sub-models for the two duty ratio ranges, 0–50% and 50–100%, which required an additional selection parameter that allowed for choosing the convenient model [17,18,20–22]. Additionally, unlike the previous works [17,18,20–22,25], the followed procedure for TLBDC modeling was described in step-by-step detail.

Applying Laplace transforms with zero initial conditions and using the superposition theorem, the small-signal duty-cycles $\widetilde{u_1}$ and $\widetilde{u_2}$ to state vector $\widetilde{x}$ transfer functions are as follows [3,24,35]:

$$\frac{\widetilde{x}(s)}{\widetilde{u_1}(s)} = |sI - [A_0 + U_1A_1 + U_2A_2]|^{-1}.A_1X, . \tag{40}$$

$$\frac{\widetilde{x}(s)}{\widetilde{u_2}(s)} = |sI - [A_0 + U_1A_1 + U_2A_2]|^{-1}.A_2X, \tag{41}$$

The transfer functions $\frac{\widetilde{V_{c1}}(s)}{\widetilde{u_1}(s)}$, $\frac{\widetilde{V_{c1}}(s)}{\widetilde{u_1}(s)}$, $\frac{\widetilde{V_{c2}}(s)}{\widetilde{u_1}(s)}$, $\frac{\widetilde{V_{c2}}(s)}{\widetilde{u_2}(s)}$, and $\frac{\widetilde{V_{c1}}(s)}{\widetilde{V_{c2}}(s)}$ can be deduced, and the required VB controllers are then designed.

3. Three-Level Boost DC–DC Converter Voltage Balance Control (VBC) Analysis

In order to assess the suitable method/controller for the VB control of the TLBDC, a comparison between two different methods using two different controllers, PI and Fuzzy, is carried out. The DR is set by an outer control loop, and the PI/Fuzzy controller ensures the VB control. The VB controllers' parameters are illustrated in Figure 7. The VB control is applied on both switches by subtracting the VB controller output from SW1 DR and adding it to SW2 DR, or on the lower switch only, by adding it to SW2 DR as illustrated in Figure 7. The duty cycles u_1 and u_2 are then used to generate the SW1 and SW2 control signals, respectively. SW1 and SW2 control signals are phase shifted by 180° as previously shown in Figure 2b,c.
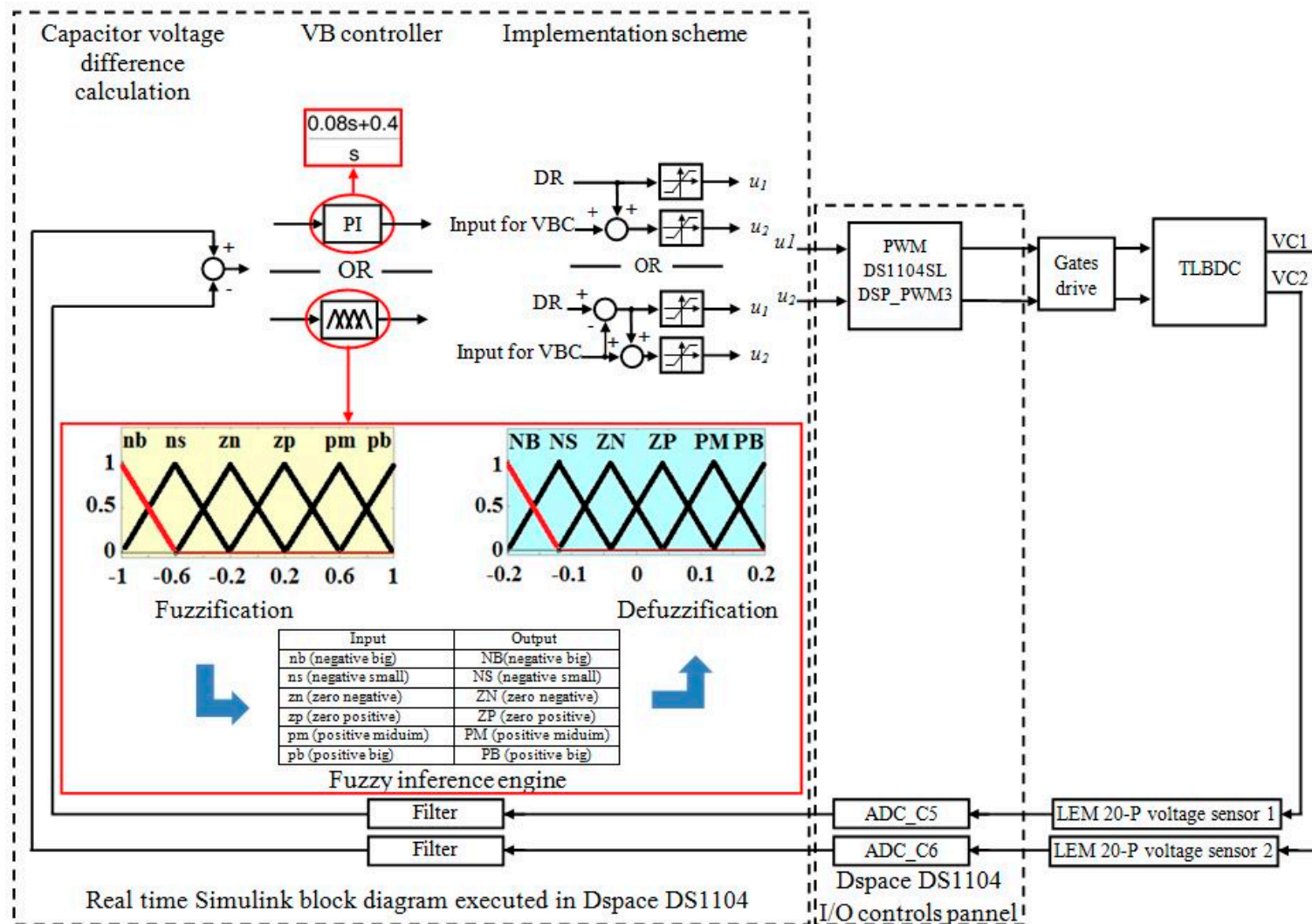
Figure 7. Block diagram of voltage balance control (VBC) schemes.

The aforementioned comparisons were examined via simulations performed in Matlab/Simulink software (Matworks, Natick, MA, USA), while the experimental tests were performed on the TLBDC prototype shown in Figure 8. The simplified scheme of the experimental setup and the TLBDC parameters are shown in Figure 9 and Table 2, respectively.
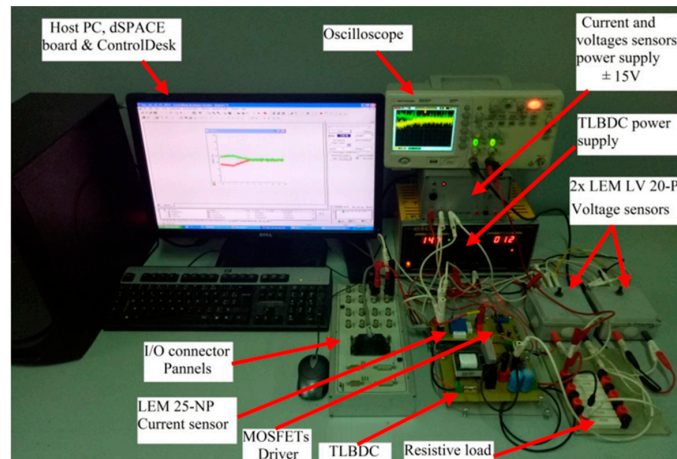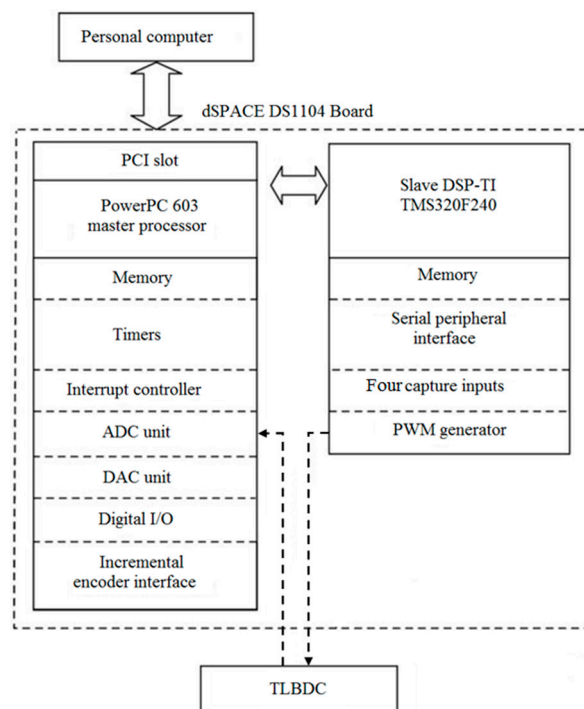

Figure 8. TLBDC Experimental setup.

Figure 9. Block-diagram of the dSPACE DS1104 controller board.

Table 2. TLBDC parameters.

| Parameter	Value
Switching frequency	12.5 kHz
Inductance, ESR	9 mH, 0.1 Ω
Output capacitors	100 uF
Input voltage	15 Volts
Load	82 Ω
Diode's forward voltage	0.5 Volts

VB control was implemented using the dSPACE 1104. After building the TLBDC VBC based on real-time Simulink-blocks, including the dSPACE 1104 slave-PWM generator and analog to digital (A/D) converters, the C code was automatically generated, downloaded and executed on the dSPACE board. The 180° phase-shifted control signals were generated using the dSPACE 1104. The logic signals were provided to an IR2110 gate driver that allowed for controlling the two TLBDC's MOSFETs (Metal–Oxide–Semiconductor Field-Effect Transistors). The dSPACE DS1104 ControlDesk monitor software was used to visualize and save the experimental data. The implemented Matlab/Simulink models on the dSPACE DS1104 board are shown in Figure 10, where Figure 10a illustrates the implemented model when the VB was applied on the lower switch of TLBDC, and Figure 10b shows the implemented model when the VB control was applied on both TLBDC switches. The VB controller, indicated in Figure 10, was either a Fuzzy or PI controller whose parameters are shown in Figure 7.


(**a**)

(**b**)
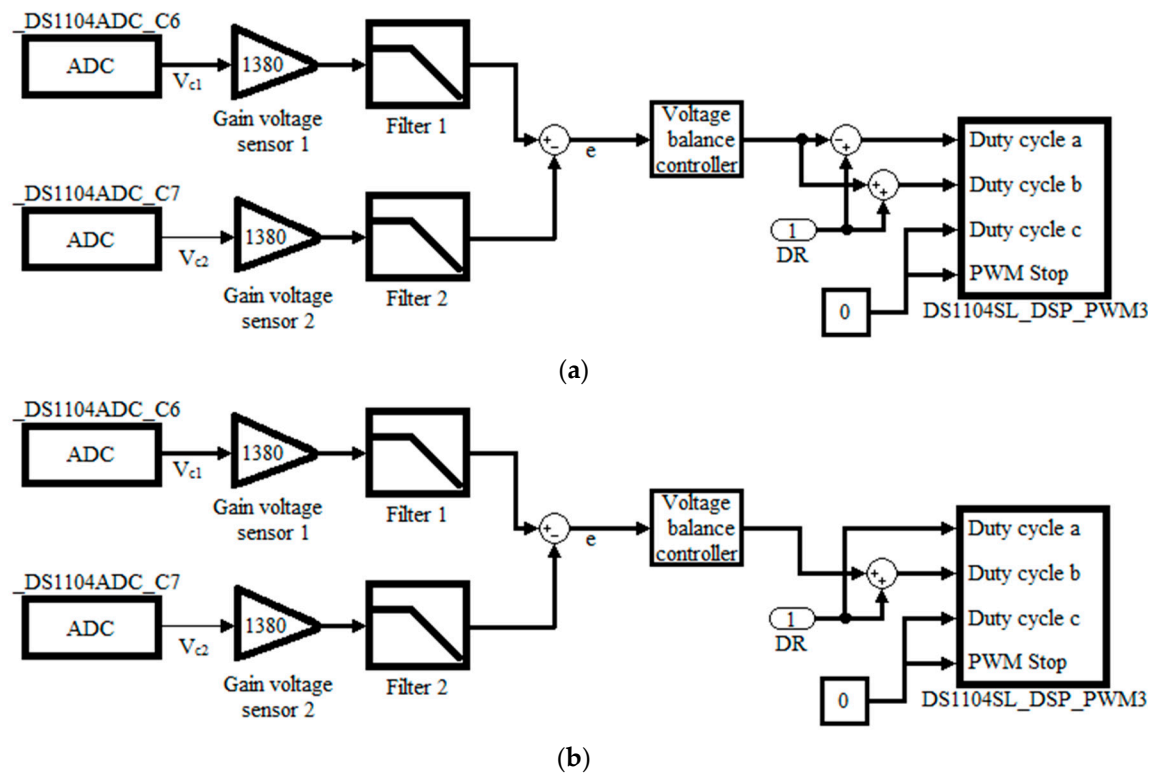
Figure 10. Matlab/Simulink implemented model on the dSPACE DS1104 board: (**a**) VB control applied on the TLBDC lower switch, and (**b**) VB control applied on either switche of the TLBDC.

Simulation and experimental results are depicted in Figures 11 and 12, respectively. Simulated output capacitors' voltages before and after applying the VB control at t = 0.025 s are presented in Figure 11. Using a PI controller, the VB was approximately achieved in 5 ms and 15 ms when the VBC was applied on both TLBDC switches, or only one, respectively. While the Fuzzy controller ensured a VB within 3 ms and 10 ms when the VBC was applied on both switches or on the lower switch, respectively. The same results could be deduced from experimental results presented in Figure 12, where the VB control was applied at t = 0.05 s. The VB, using a PI controller, was achieved in approximately 0.1 s and 0.3 s, when applying the VB control on both switches or one switch, respectively. While it was approximately achieved, using a Fuzzy controller, within 0.08 s and 0.15 s when the VB control was applied on both switches or on the lower switch, respectively.
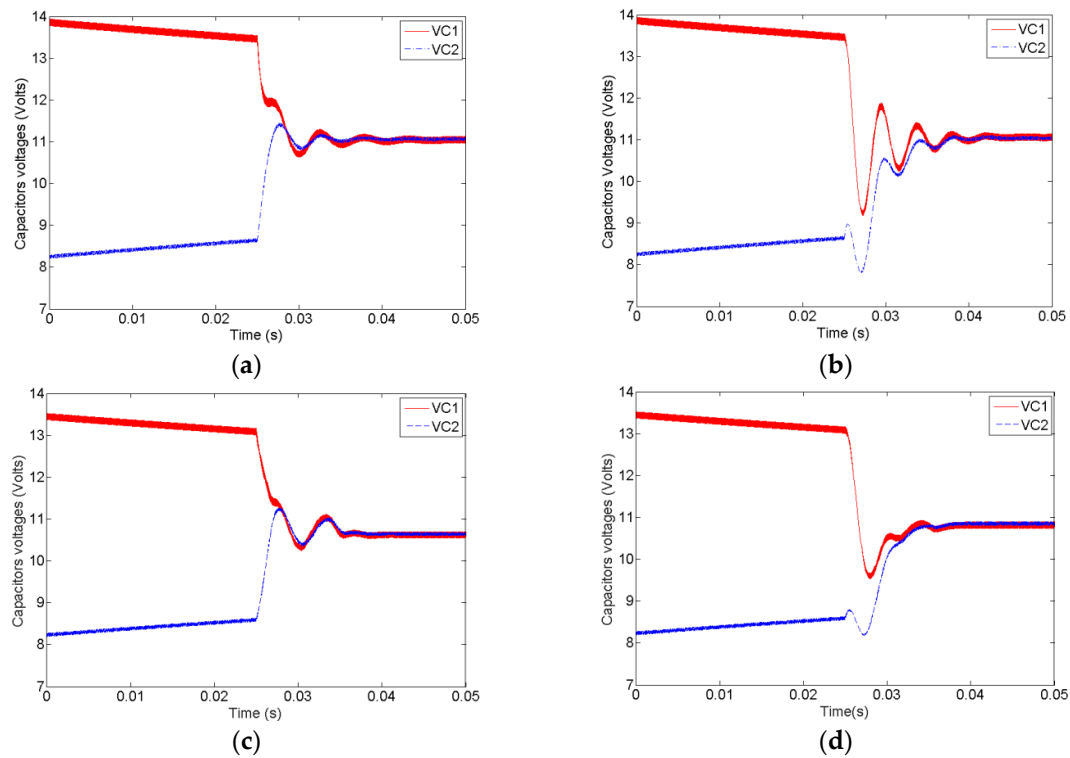
Figure 11. Simulated output capacitors' voltage curves after applying a balancing control at t = 0.025 s: (**a**) on both switches using a PI VB controller, and (**b**) on the lower switch using a PI VB controller, (**c**) on both switches using a Fuzzy VB controller, and (**d**) on the lower switch using a Fuzzy VB controller.
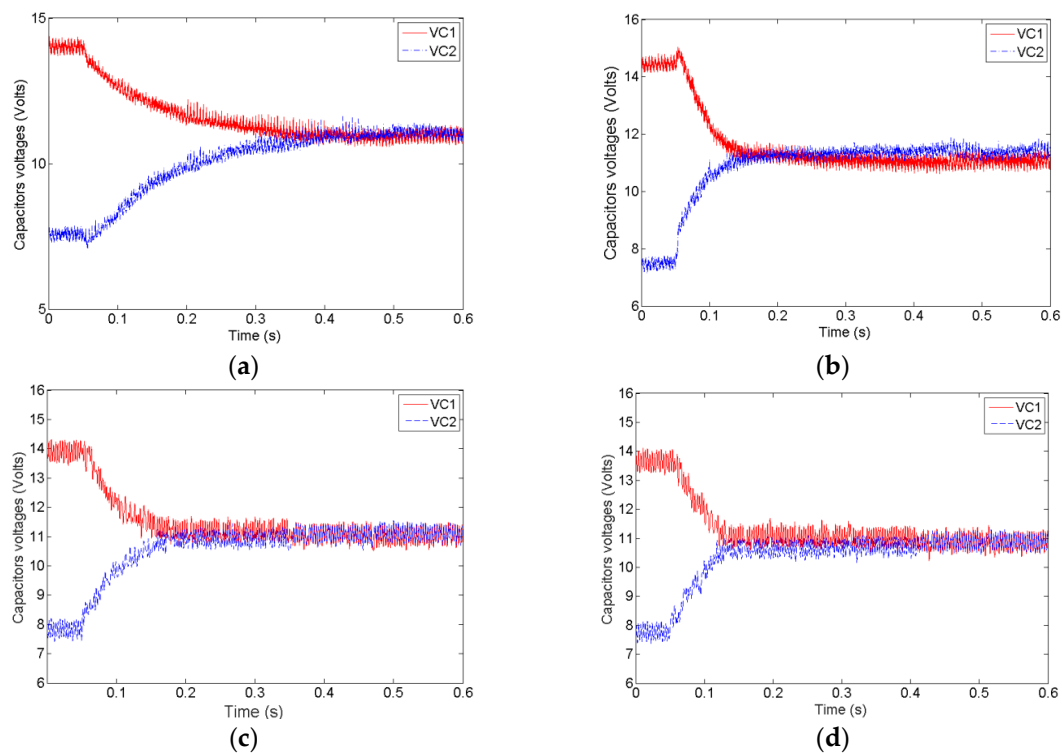
Figure 12. Experimental output capacitors' voltage curves: (**a**) on both switches using a PI VB controller, and (**b**) on the lower switch using a PI VB controller, (**c**) on both switches using a Fuzzy VB controller, and (**d**) on the lower switch using a Fuzzy VB controller.

According to the previous results, static and dynamic behaviors of the proposed model are in agreement with the experiments. The slight observed differences were mainly caused by the simplified assumptions made in the analysis, the slight errors introduced by measuring instruments, etc.

By analyzing the obtained results from the VB control analysis, one can see that the experimental results were in good agreement with the simulated ones. The differences observed in the VB controller's response times, in simulations and experiments, were mainly due to delays included by the digital to analogue (D/A) conversions, the processing time for real time implementation, and the needed time for the voltage average value calculation loop.

The analysis has shown that a VB was ensured in all cases. However, for both controllers, applying the VB control on either of the TLBDC's switches allows achieving the VB within a reduced time compared to applying it on one switch only. This showed that the works presented in References [29–33], where a VB control was applied on both TLBDC switches, have used an efficient way to ensure a VB control. In addition, the Fuzzy VB controller showed better performances compared to the PI controller, in terms of the requested time to ensure a VB for both cases as indicated in Table 3.

Table 3. Time to ensure VBC.

VBC		Requested Time to Ensure VBC Applied on One Switch (ms)	Requested Time to Ensure VBC Applied on Either Switch (ms)
PI	Simulation	15	5
	Experiments	300	100
Fuzzy	Simulation	10	3
	Experiments	150	80

4. Summary and Conclusions

The results of this study present a significant advance in the modeling and control of TLBDCs. This research also fills the gap in the related literature concerning this topic and provides new findings. The TLBDC unique model that describes the converter behavior for all DR values was first described in details. Based on the TLBDC switches' states and their equivalent electrical schemes, the state-space modeling of a non-zero inductor ESR TLBDC was carried out, and its SSM was then derived and validated using a TLBDC prototype. In a second stage, a VB control analysis was presented. Two VB controllers, PI and Fuzzy types, were used and their outputs were applied on both or one TLBDC switch(es), respectively. This allowed for choosing the efficient way and convenient controller for the TLBDC VB control.

The obtained results showed a good agreement between simulations and experiments. They also demonstrated that the developed model gave an accurate estimation of the TLBDC behavior. Generally, the presented results reflected an accurate approximation of the real results in dynamic, small perturbations around a corresponding operating point, and steady-state modes. These results have also shown that VB was achieved in all cases. However, applying the VB control on both switches allowed for achieving a VB in a reduced time compared to applying it on one switch. In addition, the Fuzzy controller presented good results, in terms of required time to ensure a VB control, when compared to the PI VB controller.

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