

Article

A Novel Concept for Three-Phase Cascaded Multilevel Inverter Topologies

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Abstract: One of the key challenges in multilevel inverters (MLIs) design is to reduce the number of components used in the implementation while maximising the number of output voltage levels. This paper proposes a new concept that facilitates a device count reduction technique of existing cascaded MLIs. Moreover, the proposed concept can be utilised to extend existing single phase cascaded MLI topologies to three-phase structure without tripling the number of semiconductor components and input dc-supplies as per the current practice. The new generalized concept involves two stages; namely, cascaded stage and phase generator stage. The phase generator stage is a combination of a conventional three-phase two level inverter and three bi-directional switches while the cascaded stage can employ any existing cascaded topology. A laboratory prototype model is built and extensive experimental analyses are conducted to validate the feasibility of the proposed cascaded MLI concept.

Keywords: multilevel inverters; device counts reduction; cascaded inverter; conventional three-phase inverter

1. Introduction

Multilevel inverters (MLIs) have drawn much attention in renewable, vehicular and industrial applications [1–6]. Also, MLIs have been utilized in flexible AC transmission, heating and air conditions [7]. Conventional MLIs include diode clamped or neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) MLI. Among these types, CHB MLI has been found very reliable in high voltage/high power applications (6.6–13.8 kV, 500 MVA) [8,9]. Several research efforts have been conducted to reduce the number and complexity of DC voltage supplies management [10,11].

Extensive research can be found in the literature to reduce the device count of cascaded MLI (CMLI). Several cascaded MLI topologies comprise two main parts; level generator and polarity generator as shown in Figure 1a can be found in the literature [12–15]. The level generator is a cascaded connection of a number of inverter cells that generates multilevel unipolar voltage while the polarity generator converts this unipolar voltage into bipolar voltage waveform [13]. While level generator structure varies for different topologies, the structure of polarity generator has been always an H-bridge connection involving four semiconductor switches. The number of cascaded cells in the level generator may be increased and/or asymmetric input voltage sources can be used to enhance the number of levels in the output voltage waveform without any change to the polarity generator [12]. The level generator switches may work with high frequency, but the polarity generator switches always function at line voltage frequency [13].

Other CMLI topologies which are able to generate bipolar voltage without using polarity generator as shown in Figure 1b were proposed in the literature [16]. CMLI topologies such as cross-switched and modified H-bridge topologies were also recently proposed in the literature [17–23]. Among the

above mentioned CMLI topologies, some were mainly developed for three-phase multilevel voltage generation and cannot be directly utilized for single phase applications e.g., Figure 1c [24,25].

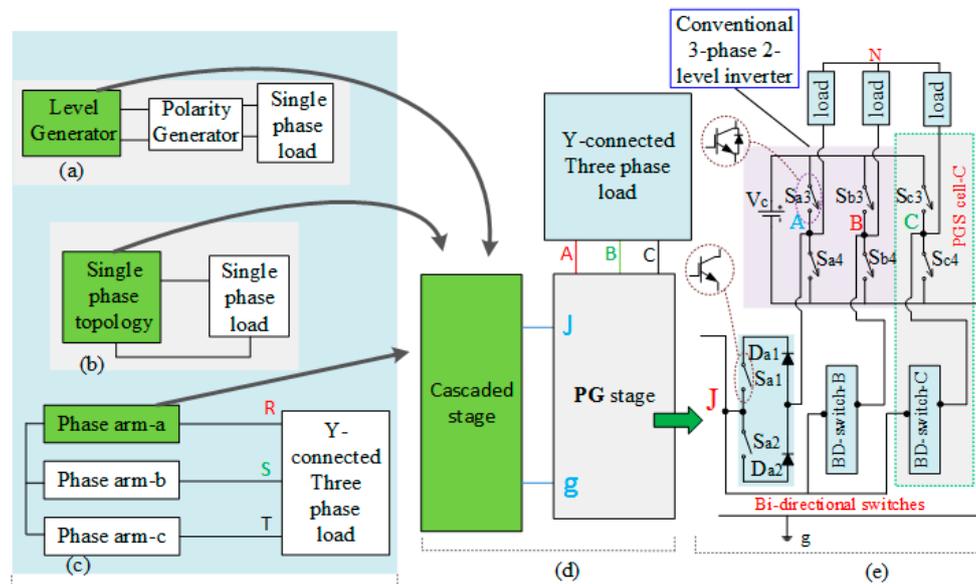


Figure 1. Block diagrams: (a) level and polarity generators-based cascaded multilevel inverter (CMLI) topology; (b) CMLI topology with no polarity generator; (c) 3-phase CMLI topology; (d) proposed 3-phase CMLI; (e) Circuitual model of the PG-stage. Reprint with permission [4261051118814]; 2018, IEEE.

Three-phase CMLI has been widely used in large-scale renewable energy applications to comply with the high-power conversion requirement [1–4]. In order to improve the quality of the output voltage waveform, the number of components required to implement the three-phase CMLI should be significantly increased which increases the implementation cost, inverter physical size and complicates the control system. Although several topologies have been proposed in the literature in order to reduce the device count and increase the number of levels in the output voltage of single phase CMLIs, the majority of these topologies have not been extended to three-phase structure yet. It is a common trend that the number of components of single phase topologies is tripled when they are extended to three-phase structures [13,14,26–28].

Both high frequency and low frequency modulation techniques have been reported as reliable control strategies for CHB MLI [29,30]. The most common high frequency modulation strategy is carrier-based sine pulse width modulation (SPWM) strategy and a wide range of carrier frequency (1–12 kHz) is employed to get the switching pulses [27,28,31,32]. The main problem of SPWM strategy is that it has severe consequences on switching losses [33]. On the other hand, low frequency modulation strategies provide better output voltage waveform with low total harmonic distortions (THD) [25,34].

The main goal of this paper is to introduce a new generalized CMLI topology that could be employed to extend any existing single-phase CMLI topology to a three-phase structure without tripling the devices used within the single-phase structure. The proposed topology can also be employed by existing three-phase CMLI topologies to reduce its device count without compromising its performance. Besides, a low frequency space vector modulation (SVM) technique is applied to generate switching pulses. The proposed topology provides an optimized design solution to CMLI in terms of reducing the implementation cost and physical size while maintaining the quality of the output voltage waveform.

2. Proposed Concept of 3-Phase CMLI

Figure 1d shows the block diagram of the proposed three-phase CMLI, in which a cascaded stage is connected with the polarity generator (PG) stage at junction point 'J'. The structure of the cascaded stage is not fixed as it can be replaced by any existing cascaded MLI topology. The green shaded portions of existing CMLI topologies in Figure 1a–c can be employed as a cascaded stage in the new proposed topology. The PG stage is developed by utilizing three Bi-directional (BD) switches and a conventional three-phase two level inverter (CTPTLI). Each BD switch consists of two insulated gate bipolar transistors (IGBT) and two diodes. Both IGBT switches work simultaneously to turn the BD on or off. Three-phase arms A, B, and C exist in the PG stage. A BD switch and two switches in the CTPTLI can be considered as a PG cell in each phase arm with 120° phase difference among the switching devices of the three cells. The CTPTLI is fed by a dc-voltage supply ' V_C ' of a magnitude greater than the summation of the input voltage supplies in the cascaded stage.

Each pair of the switches, (S_{a3}, S_{a4}), or (S_{b3}, S_{b4}), or (S_{c3}, S_{c4}) within the CTPTLI at different PG cells are responsible for generating V_C and zero voltage levels in the output voltage waveform at the output nodes A, B, C. For any PG cell, the PD-switch is turned off while the two switches within the CTPTLI operate to generate V_C and zero voltage level. The pair switches in the CTPTLI and the BD switch always function in a toggle mode. As mentioned above, any existing CMLI topology can be utilized as a cascaded stage and, hence, no significant change is required in the switching logic for existing CMLI topology when used as a cascaded stage to generate different voltage levels in the proposed topology.

In any PG cell, the PD-switch is only turned on for conducting the voltage levels, which are generated by the cascaded stage to the output points A, B, C. Three BD-switches, which are connected with the cascaded stage at the junction point 'J' as shown in Figure 1e are operated with a 120° phase difference. Figure 2a shows the simplified structure of the PG stage for generating the voltage levels V_C and 0 in the pole voltage V_{Ag} which are achieved by toggle operation of switches S_{a3} and S_{a4} . Figure 2b shows the conduction path of the inverter when it generates intermediate levels between V_C and 0 in the pole voltage. Figure 2c shows the final pole voltage.

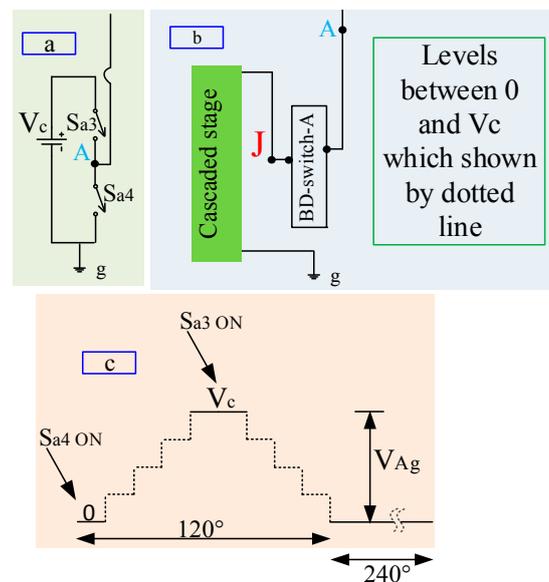


Figure 2. Simplified structure of the proposed CMLI, (a) generation of maximum and zero voltage levels; (b) intermediate level generation; (c) pole voltage waveform. Reprint with permission [4261051118814]; 2018, IEEE.

If V_{Ag} , V_{Bg} , V_{Cg} are the pole voltages, then the line voltage, V_{AB} , V_{BC} , V_{CA} can be derived as below,

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \end{bmatrix} \quad (1)$$

3. Proposed CMLI Using H-Bridge Topology as Cascaded Stage

Cascaded H-Bridge (CHB) MLI topology is a well-established structure for single and three-phase applications [35]. The cascaded stage in the proposed generalized CMLI is facilitated to utilize any single- or three-phase structure as shown in Figure 1.

The conventional CHB MLI topology shown in Figure 3 for n-number of CHB cells is chosen to validate the proposed three-phase inverter concept. The proposed three-phase MLI structure involving three CHB cells in the cascaded stage is shown in Figure 4a.

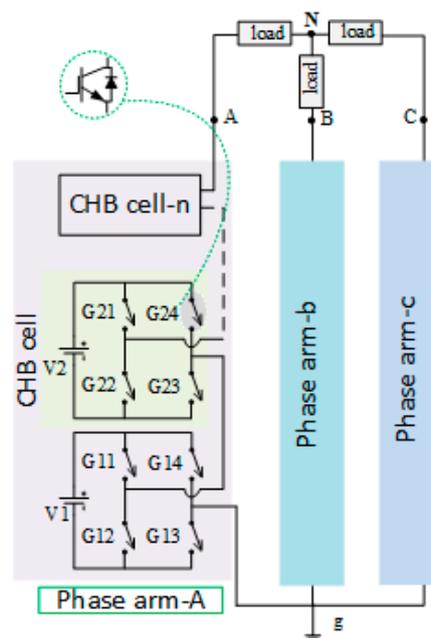


Figure 3. Conventional three-phase CHB-MLI. Reprint with permission [4261051118814]; 2018, IEEE.

The number of CHB cells in the cascaded stage can be increased in order to achieve more levels in the output voltage waveform. Each H-bridge cell (k) comprises four switches (G_{k1} , G_{k2} , G_{k3} , G_{k4}) and a dc-power supply (V_k) as depicted in Figure 4b. Any CHB cell is able to produce three different voltage levels (V_k , 0 , $-V_k$) in the output voltage, V_{out} . Table A1 in the Appendix A shows the switching logic to achieve the aforementioned three output voltages.

Symmetric and asymmetric structures are proposed for conventional CHB MLI topology in [35,36], respectively. Asymmetric methods are found superior than the symmetric in terms of the number of levels in the output voltage as presented in [35]. In [37], an asymmetric CHB MLI is presented, where the dc voltage ratios are kept in binary form ($1:2 \dots 2^n$). The Trinary ratio format ($1:3: \dots :3^n$) has been also proposed for CHB MLI asymmetric structure [38]. The new proposed three-phase CMLI concept in this paper can adopt both symmetric and asymmetric structure of the CHB MLI in the cascaded stage.

As mentioned above, the magnitude of the V_C should be greater than the summation of the connected voltage supplies in the cascaded stage. If V_1, V_2, \dots, V_3 are the input voltages for n-number

of cells in the cascaded stage, then the following respective equations for symmetric, binary-related and trinary-related input supplies can be written,

$$V_1 = v; V_2 = v; \dots; V_n = v \tag{2}$$

$$V_1 = v; V_2 = 2^1v; \dots; V_n = 2^{n-1}v \tag{3}$$

$$V_1 = v; V_2 = 3^1v; \dots; V_n = 3^{n-1}v \tag{4}$$

where 'v' is the per unit voltage value.

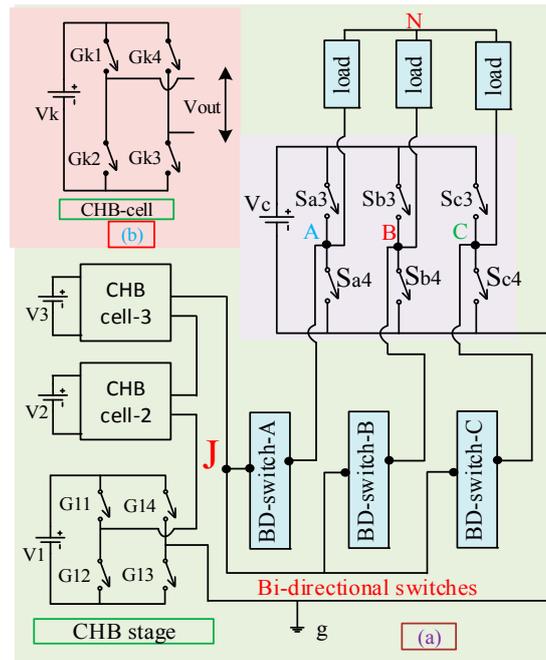


Figure 4. Proposed three-phase CMLI (a) CHB cells are considered as cascaded stage; (b) a standard CHB cell. Reprint with permission [4261051118814]; 2018, IEEE.

The input voltage-supply of the CTPTLI, V_C can be calculated from,

$$V_C = \sum_0^n V_x + V_1 = (V_1 + V_2 + \dots + V_n) + v \tag{5}$$

Figure 5 shows the conduction path for generating the pole voltage. In Figure 5, the magnitudes of the CHB cells input voltage supplies are considered symmetric i.e., $V_1 = V_2 = V_3 = v$; $V_C = 4v$. With the contribution of CTPTLI and CHB cells along with the BD-switches, pole voltages, V_{Ag} , V_{Bg} , V_{Cg} are produced. Only the CTPTLI switches operate to generate the voltage levels, V_C and 0 as shown in Figure 5a,e, respectively. The other voltage levels, $(V_1 + V_2 + V_3)$, $(V_1 + V_2)$, V_1 between 0 and V_C levels are produced using different switching logics among the CHB cells, when the BD-switches are turned on. Figure 5e shows the pole voltage output, V_{Ag} , which can be obtained by the above mentioned switching operation.

While Figure 5 explains the generation of one arm pole voltage, V_{Ag} ; the other two pole voltages follow the same switching logics with 120° phase shift among the PG-cells. The switching function for each phase arm lasts for 120° phase angle.

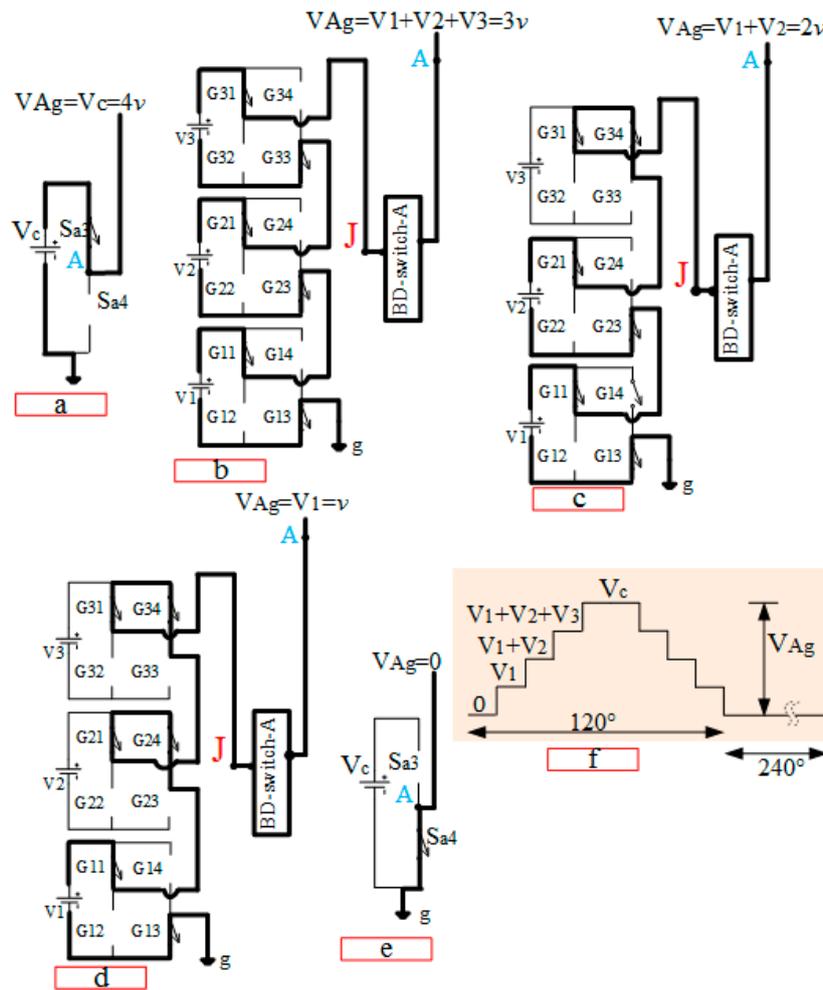


Figure 5. Different switching logics for generating four levels in the pole voltages: (a) level $3v$; (b) Level $2v$; (c) Level v ; (d) Level 0 ; (e) Complete cycle of the pole voltage. Reprint with permission [4261051118814]; 2018, IEEE.

4. Implementation of the Proposed MLI

The proposed MLI topology in Figure 4 is controlled with a low frequency staircase modulation strategy [39,40]. The switching states follow a specific sequence in the d-q plane. The number of switching states, S in the d-q plane is an essential factor to generate the output voltage levels and can be expressed as,

$$S = 6(N_p - 1); N_p > 1 \tag{6}$$

where N_p is the number of levels in the pole voltages.

The number of switching states forms different hexagons as shown in Figure 6 to achieve different number of levels in the pole voltage waveforms.

In Figure 6, the smallest hexagon represents the switching states for $N_p = 2$ and the following hexagons is for $N_p = 3$, $N_p = 4$, and $N_p = 5$; respectively. According to Figure 5, the proposed topology generates $N_p = 5$ in the pole voltages. Hence, the most upper hexagon in Figure 6 is appropriate for getting 24 switching states to generate five voltage levels, $4v$, $3v$, $2v$, v , 0 in the pole voltages.

The 24 switching states are, 044, 043, 042, 041, 040, 140, 240, 340, 400, 430, 420, 410, 400, 401, 402, 403, 404, 304, 204, 104, 004, 014, 024, 034. Each of the switching states has three switching vectors, S_a , S_b , S_c for three-phase voltage generation. The pole voltages, V_{Ag} , V_{Bg} , V_{Cg} are taken as reference

to achieve the three switching vectors in each switching state at any instant of time [39]. In general, the switching angles, φ for each of the switching states are equal and can be calculated from,

$$\varphi = 360^\circ / S \quad (7)$$

Hence, the switching angle of each of the 24 switching state is 15° . This means, a new switching state will come into operation every 15° . In the switching sequence of 24 switching states, the switching vectors 4, 3, 2, 1, 0 are combined in an organised manner to generate three pole voltages and the switching vectors always abide by Table A2 in the Appendix A for different voltage level generation.

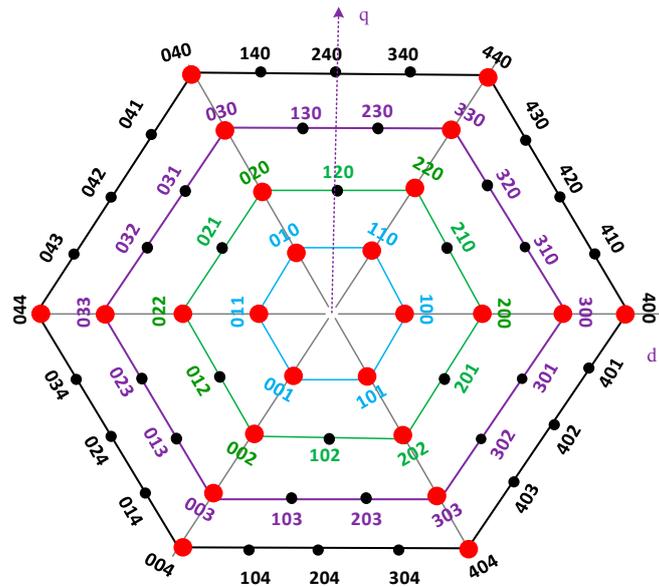


Figure 6. Generalized switching states for generating different number of levels in the pole voltage. Reprint with permission [4261051118814]; 2018, IEEE.

The real time switching signals are obtained using digital signal processor, TMS320F2812 (Texas Instruments, Dallas, TX, USA). The implementation requires 12 IGBTs for three CHB cells in the cascaded stage and 12 IGBTs in the PG cells. A laboratory prototype is developed to validate the feasibility of the proposed inverter.

Figure 7 shows the developed hardware prototype model. A total of 21 general-purpose input/output (GPIO) pins are required in the DSP, TMS320F2812 for achieving all real-time switching signals. Sixteen (GPIOA0-GPIOA15) pins are chosen from GPIO-A while the remaining one pin is chosen from GPIO-B (GPIO B0) pin array. The gate signals of phase B and C within the three PG-cells have similar pattern as in phase-A with a phase shift of 120° and 240° , respectively.

Six IGBTs, IRG4BC40W, 600 V/20 A along with six diodes, RHRP1540, 400 V/15 A are used for the three BD-switches in the PG-stage while 18 IGBTs, HGTG20N60B3D, 600 V/40 A are used to build the CHB cells in the cascaded stage and CTPTLI. A four channel digital storage oscilloscope, Tektronix TPS 2014 (Tektronix Inc., Beaverton, OR, USA) is utilized to capture the experimental output waveforms and analyse total harmonic distortion (THD).

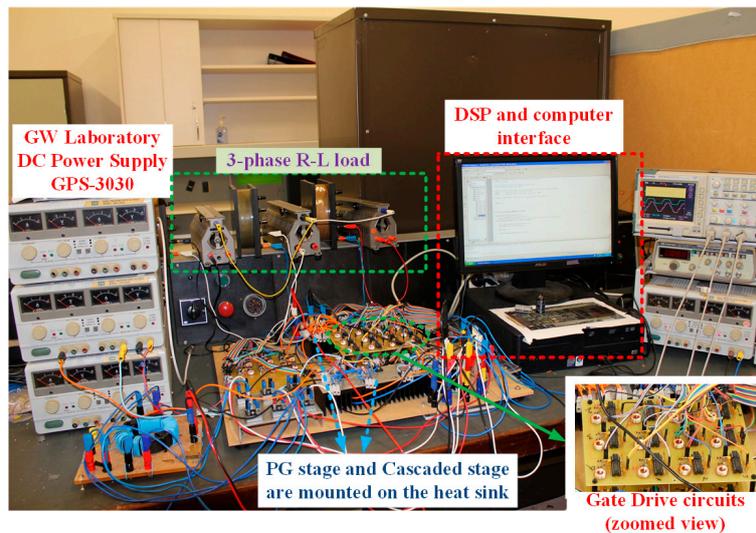


Figure 7. Experimental prototype hardware model. Reprint with permission [4261051118814]; 2018, IEEE.

5. Results and Discussions

Table A3 in the Appendix A shows system specification of the implemented inverter. To validate the feasibility of the proposed topology, its performance in terms of output voltage/current waveforms along with the THD has been compared with the performance of the MLI topology presented in [5,40]. As will be elaborated below, while the proposed topology in this paper can reduce the MLI device count significantly, it almost provides the same performance of the MLI topology presented in [5,40]. Results in various test cases are demonstrated in the following sub-sections.

A. H-bridge cells symmetric input supplies

The input dc-voltage sources are connected such as $V_1 = V_2 = V_3 = v = 70$ V and $V_C = 4v = 280$ V. Inductive 3-phase load ($Z = 55 + j 37.68 \Omega/\text{phase}$) is considered for testing the inverter performance.

Figure 8a shows the junction voltage, V_{Jg} and pole voltages, V_{Ag} , V_{Bg} , V_{Cg} , respectively. As shown in the figure, the pole voltages comprise five levels (280 V, 210 V, 140 V, 70 V, 0) while V_{Jg} comprises three levels (210 V, 140 V, 70 V). Figure 8b,c show the load voltages, V_{AN} , V_{BN} , V_{CN} , and their THD, respectively. The relation between the pole voltages V_{Ag} , V_{Bg} , V_{Cg} , and load voltages can be expressed by,

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \end{bmatrix} \quad (8)$$

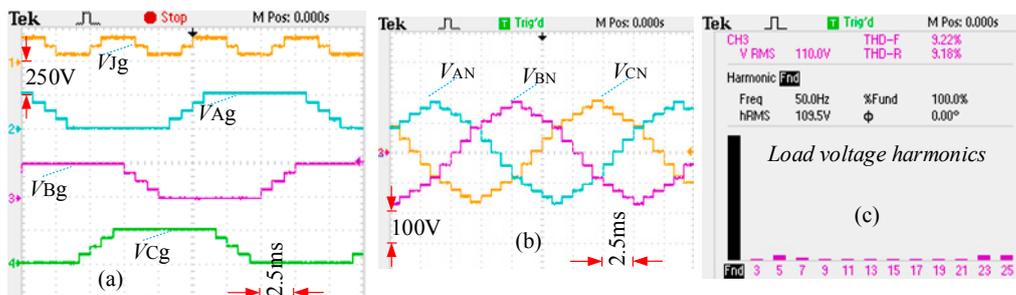


Figure 8. Experimental results of (a) Junction voltage, and Pole voltages when the CHB-cells are fed by symmetric dc-power supplies; (b) load voltage; (c) load voltage harmonics.

On the other hand, the line voltages, V_{AB} , V_{BC} , V_{CA} shown in Figure 9a comprise nine levels (280 V, 210 V, 140 V, 70 V, 0 V, -70 V, -140 V, -210 V, -280 V).

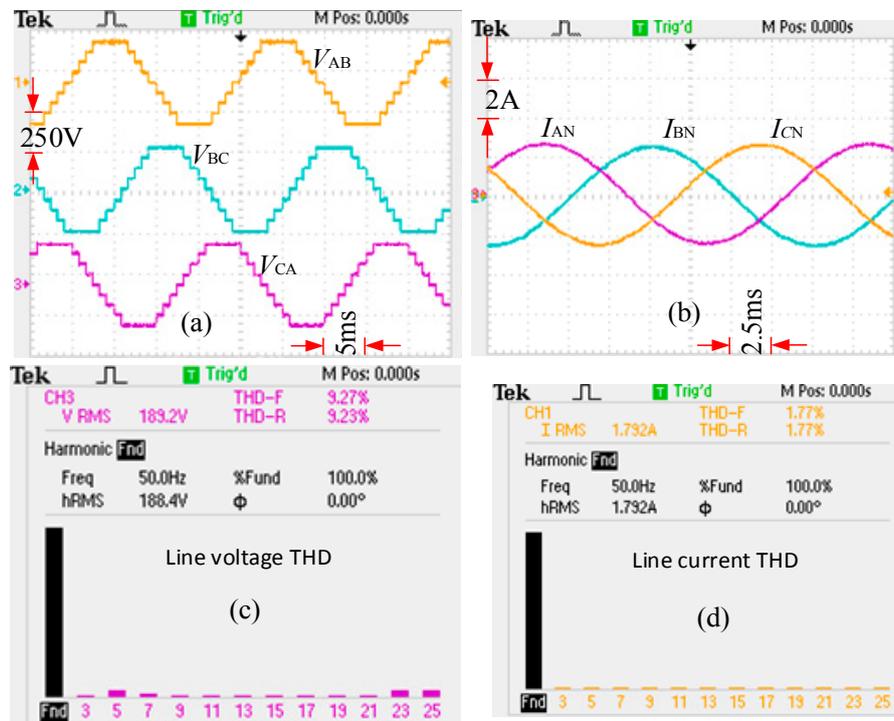


Figure 9. Experimental results, (a) line voltages; (b) line currents; (c) THD of the line voltage; (d) THD of the line current, when CHB cells are fed by Symmetric dc power supplies.

Figure 9b shows the three-phase line currents, I_{AN} , I_{BN} , I_{CN} . It is worth mentioning that no harmonic filter was used in the implemented hardware setup. The total harmonic distortion (THD) of the unfiltered line voltage and line current are 9.27% and 2.09%; respectively as shown in Figure 9c,d, respectively. The THD of the line current and voltage must be less than 5%, to comply with the IEEE standard [41]. While the current THD complies with the mentioned standard, voltage THD is more than 5% in the implemented 9-level CMLI topology. Voltage THD can be reduced by increasing the number of levels in the output voltage.

B. H-bridge cells Trinary-related input supplies

In the proposed topology, the number of levels in the output voltages can be increased by considering asymmetric trinary ratio for the input dc supplies. According to (3) the magnitudes of V_1 , V_2 , V_3 are set to 20 V, 60 V, 180 V; respectively and hence the magnitude of V_C is 280 V.

This configuration is able to generate 15-levels ($N_P = 15$) in the pole voltage and 29-levels in the line voltage. Hence, it needs 84-switching states to generate three-phase output voltages according to (5). Table A4 in the Appendix A shows the switching logics for generating 15 levels in the pole voltage. The junction voltage, and line voltage, V_{AB} are shown in Figure 10a. Figure 10b shows 29-level three-phase line voltages on the same plot. The THD of the unfiltered 29-level line voltages is nearly 5% as shown in Figure 10c.

C. Three-phase conversion of existing single-phase inverter topologies

A number of single phase MLI topologies along with different input voltage algorithms have been recently published [12–15,17–23]. The proposed three-phase inverter concept in this paper permits easy conversion of the existing single phase MLI into three-phase structures without tripling the number of

semiconductor switches and dc-supplies as per the current conventional practice. To do so, only the PG stage in the proposed topology is required to be connected with any existing single phase topology.

To extend any existing single-phase inverter to three-phase structure using the proposed concept, switching logics of the single phase cascaded inverter can be retained. Figure 11a shows a single phase topology published in [12] while Figure 11b shows the extended three-phase structure of this single phase inverter using the proposed concept in this paper. As shown in Figure 11b, the single phase topology acts as a cascaded stage and generates all possible voltage levels by following the same switching logic proposed in [12].

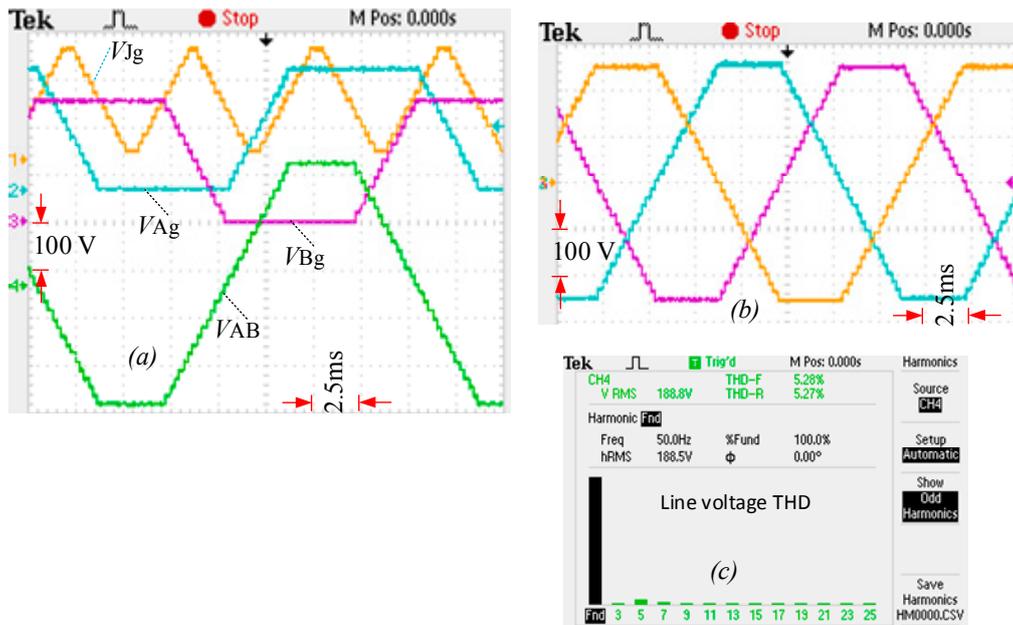


Figure 10. Experimental results, (a) Junction voltage, pole voltages (V_{Ag} , V_{Bg}), line voltage (V_{AB}); (b) 29-level 3-phase line voltages; (c) THD of the line voltage, when CHB cells are fed by trinary related dc power supplies. Reprint with permission [4261051118814]; 2018, IEEE.

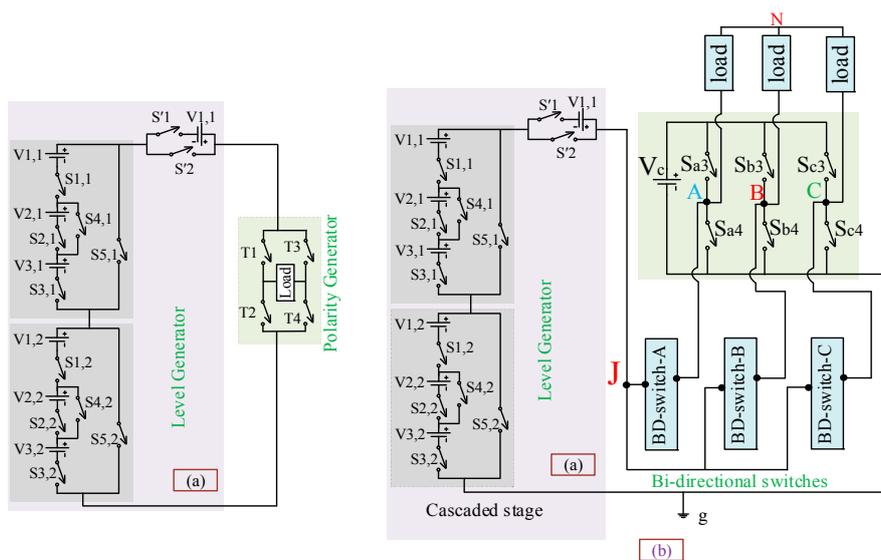


Figure 11. Three-phase conversion of a single phase topology (a) existing single phase topology proposed in [12]; (b) three-phase conversion of existing topology according to the concept proposed in this paper.

The bidirectional and CTPTLI switches operate as shown in Figure 2. In [12], the single phase structure produces 15-levels in the line voltage, when Figure 12a is set with $V_{11} = V_{21} = V_{31} = V_{21} = V_{22} = V_{23} = V'_0 = 40$ V and $V_C = 280$ V. The cascaded stage in Figure 11b is arranged in a similar pattern by imitating the single-phase structure for three-phase conversion.

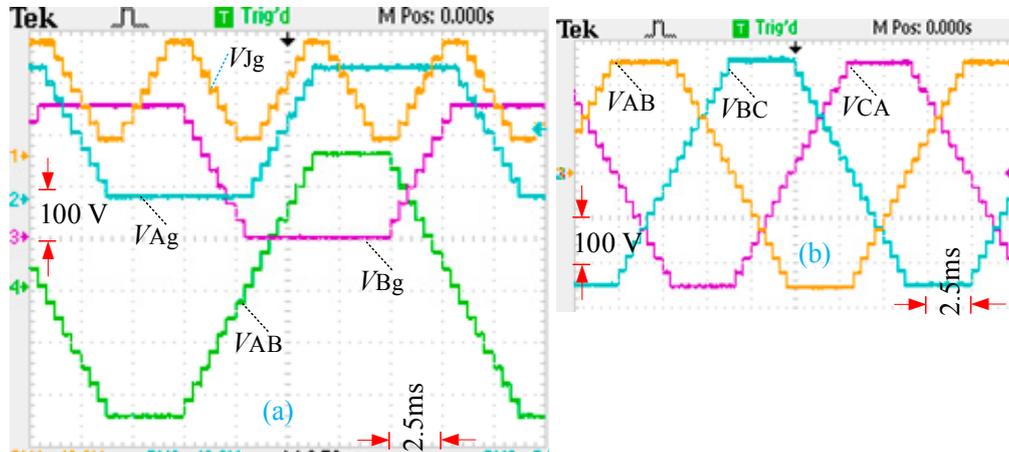


Figure 12. Experimental results, (a) Junction voltage, pole voltages (V_{Ag} , V_{Bg}), line voltages (V_{AB}); (b) 17-level three-phase line voltages.

Figure 11b, the single phase topology acts as a cascaded stage and generates all possible voltage levels by following the same switching logic proposed in [12]. The bidirectional and CTPTLI switches operate as shown in Figure 2. In [12], the single phase structure produces 15-levels in the line voltage, when Figure 12a is set with $V_{11} = V_{21} = V_{31} = V_{21} = V_{22} = V_{23} = V'_0 = 40$ V and $V_C = 280$ V. The cascaded stage in Figure 11b is arranged in a similar pattern by imitating the single-phase structure for three-phase conversion.

Table 1 provides a comparison of using the concept proposed in this paper and conventional methods to transfer single-phase to three-phase structure.

Table 1. Comparison between three-phase conversion of a single-phase structure using conventional methods and proposed concept in this paper.

Topology	Single Phase Structure			Conventional 3 Phase Conversion			This Paper Proposed Concept		
	Line Voltage Levels	Switches	DC-Supplies	Line Voltage Levels	Switches	DC-Supplies	Line Voltage Levels	Switches	DC-Supplies
Non-isolated inverter topology [9]	15	12	7	15	36	21	17	24	8
DC-link half-bridge cascaded inverter [21]	13	12	6	13	36	18	15	24	7

The table reveals the superior advantages of the proposed concept over existing conventional methods in terms of reducing the number of switches and dc-supplies while increasing the levels in the output voltages when a single phase structure is extended to three-phase one.

The three-phase inverter in Figure 11b produces nine levels in the pole voltages and 17-levels in the line voltage. It requires 48-switching states to produce these voltage levels according to (5). Table A5 in the Appendix A shows the switching logic for this inverter. Figure 12a shows the junction

voltage, V_{Jg} , pole voltages and line voltage, V_{AB} of the extended three-phase inverter. Figure 12b shows the three-phase 17-level line voltages on the same plot.

6. Semiconductor Losses and Inverter Efficiency

Semiconductor losses are considered as a crucial design factor for any converter circuit, which influences and defines the required thermal management and contributes to the estimation of overall cost, volume and weight of the inverter. There are two dominant losses in the semiconductor devices; the static and the dynamic losses. The on-state resistance and the forward voltage drop of the semiconductor device are responsible for the static (conduction) losses, while the dynamic losses are produced during the ON-OFF actions dictated by the switching frequency of the device [39].

The overall semiconductor losses of the proposed CMLI can be estimated by the total conduction and switching losses of all used semiconductors as below:

$$P_{total_loss} = P_c(t) + P_{sw} \quad (9)$$

If the output power is P_{out} , the inverter efficiency (η) can be calculated from:

$$\eta\% = \left(\frac{P_{out}}{P_{total_loss} + P_{out}} \right) \times 100\% \quad (10)$$

The output power is calculated from:

$$P_{out} = \sqrt{3} \times \frac{V_C}{\sqrt{2}} \times \frac{I_{line}}{\sqrt{2}} \times PF \quad (11)$$

where V_C and I_{line} are the input voltage to the CTPTLI and output line current, respectively.

The proposed topology (Figure 4b) in this paper utilizes IGBT with anti-parallel diode (HGTG20N60B3D) in the cascaded structure and IGBT (IRG4BC40W) along with diode (RHRP1540) in the PG structure. The following parameters are used to calculate the switching losses; $V_T = 1.8$ V, $R_T = 0.10$, $V_D = 1.2$ V, $R_D = 0.1$, $\beta = 1$, $t_{on} = t_{off} = 1$ μ s. where, the on-state voltage drop of the transistor and diode are expressed by V_T and V_D , respectively. The on-state resistances of the transistor and diode, are given by R_T and R_D , respectively. The transistor amplification factor and ON-OFF time is expressed by ' β ', t_{on} and t_{off} , respectively.

Total switching loss is found to be $P_{total_loss} = 2.9067$ watt with 1.3076 watt losses associated in the cascaded stage and 1.5991 watt in the PG stage. For a connected load of 0.82 lagging power factor (PF) and by using (15), the output power is 98.64 watt which gives an overall efficiency of about 97%.

7. Comparison with Other Topologies

As shown in the results section, the proposed three-phase MLI concept can be adopted to extend any existing single-phase topology to three-phase without tripling the used components as per the current conventional methods. Furthermore, the proposed concept is able to reduce the size of the existing three-phase cascaded MLI topologies in terms of device count without degrading the quality of the output voltage. A comparison is performed in order to show the effectiveness of the proposed three-phase cascaded MLI concept over various existing topologies. Different factors such as number of power semiconductor components, number of gate driver circuits and number of dc-supplies are considered in the comparison.

Table 2 shows a comparison among existing three-phase CHB MLI topologies and the three-phase MLI concept proposed in this paper. The CHB inverter proposed in [35], has two CHB cells and binary relation is maintained between the input dc-supplies in each phase arm.

Table 2. Comparison among conventional three-phase CHB topologies and the proposed three-phase cascaded MLI for different asymmetric input voltage arrangements.

Category	Binary Related Two CHB Cell Topology [35]		Trinary Related Three CHB Cell Topology [42]		Trinary Related Four CHB Cell Topology [38]	
	Existing 3-Phase	Proposed New Concept	Existing 3-Phase	Proposed New Concept	Existing 3-Phase	Proposed New Concept
	No of levels in line voltage	7	9	27	29	81
No of switches	24	20	36	24	48	28
No of diodes	24	20	36	24	48	28
No of gate driver	24	20	36	24	48	28
No of dc supplies	6	3	9	4	12	5

On the other hand, trinary related three and four CHB cells in each phase arm is considered in [38,42], respectively. A significant reduction in the device count can be realized when the new three-phase cascaded MLI concept is applied to these existing topologies as can be seen in Table 2. The percentage of reduction of device count and the input dc supplies is increasing when the number of CHB cells in each phase arm is increasing. For example, 17% reduced power electronic components is achieved in the proposed three-phase cascaded MLI concept for two CHB cell, while 33% and 42% reduction will be achieved when the proposed concept is applied for three and four CHB cells in each phase arm of the existing topologies, respectively.

8. Conclusions

This paper presents a new design for a three-phase CHB MLI. Experimental results validate the practical feasibility of the proposed three-phase MLI concept. Comparison with published three-phase MLI topologies shows the superiority of the proposed concept over existing topologies in terms of reduced device count without compromising the quality of the output voltage. Moreover, the proposed concept can be adopted to extend any single phase MLI to three-phase structures without tripling its components as per the current practice. The new technique can be adopted by existing three-phase topologies to reduce its device count without degrading the overall performance. Since the number of components is directly related to the cost, complexity and the installation area, the new three-phase concept is a cost-effective technique that is expected to have a great potential for renewable power generation systems and smart grid applications.

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Appendix A

Table A1. Generalized switching logic for a cascaded cell.

V_{out}	Turn on Switches
V_k	G_{k1}, G_{k3}
0	G_{k1}, G_{k4}
$-V_k$	G_{k2}, G_{k4}

Table A2. Switching logic for different switching vector.

Switching Vector, $S_a/S_b/S_c$	Switching Logic
4	Figure 5a
3	Figure 5b
2	Figure 5c
1	Figure 5d
0	Figure 5e

Table A3. System specifications of the implemented inverter.

Input DC Source Voltage in CHB Stage (V_1, V_2, V_3)	70 V Each
Input DC source voltage in PGS (V_C)	280 V
Switching frequency	50 Hz
Magnitude of line voltages	280 V (Peak)
Load power factor	0.82
Tested power of the prototype	523 Watt
Number of levels in the peak–peak line voltages	9

Table A4. Switching logic for generating 15 levels in the pole voltage.

Switching Vector, S_a	Pole Voltage		Switching Logic
14	V_C	280 V	Figure 5a
13	$v + 3v + 9v$	260 V	$V_1 + V_2 + V_3$
12	$0 + 3v + 9v$	240 V	$0 + V_2 + V_3$
11	$-v + 3v + 9v$	220 V	$-V_1 + V_2 + V_3$
10	$v + 0 + 9v$	200 V	$V_1 + 0 + V_3$
9	$0 + 0 + 9v$	180 V	$0 + 0 + V_3$
8	$-v + 0 + 9v$	160 V	$-V_1 + 0 + V_3$
7	$v - 3v + 9v$	140 V	$V_1 - V_2 + V_3$
6	$0 - 3v + 9v$	120 V	$0 - V_2 + V_3$
5	$-v - 3v + 9v$	100 V	$-V_1 - V_2 + V_3$
4	$v + 3v + 0$	80 V	$V_1 + V_2 + 0$
3	$0 + 3v + 0$	60 V	$0 + V_2 + 0$
2	$-v + 3v + 0$	40 V	$-V_1 + V_2 + 0$
1	$v + 0 + 0$	20 V	$V_1 + 0 + 0$
0	0	0	Figure 5e

Table A5. Switching logic in the cascaded stage and PG-stage for generating 9 levels in the pole voltage, V_{Ag} .

Switching Vector	Pole Voltage (V)	Switching Logic
0	0	Figure 5a
1	20	S'_1, S_{51}, S_{52}
2	40	$S'_2, S_{11}, S_{31}, S_{41}, S_{52}$
3	60	$S'_1, S_{11}, S_{31}, S_{41}, S_{52}$
4	80	$S'_1, S_{11}, S_{21}, S_{31}, S_{52}$
5	100	$S'_2, S_{11}, S_{21}, S_{31}, S_{12}, S_{32}, S_{42}$
6	120	$S'_2, S_{11}, S_{21}, S_{31}, S_{12}, S_{22}, S_{32}$
7	140	$S'_1, S_{11}, S_{21}, S_{31}, S_{12}, S_{22}, S_{32}$
8	160	Figure 5e

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