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On the Performance Optimization of Two-Level Three-Phase Grid-Feeding Voltage-Source Inverters

Issam A. Smadi *, Saher Albatran and Hamzeh J. Ahmad

Department of Electrical Engineering, Faculty of Engineering, Jordan University of Science and Technology, Irbid 22110, Jordan; saalbatran@just.edu.jo (S.A.); hjahmad13@eng.just.edu.jo (H.J.A.)
* Correspondence: iasmadi@just.edu.jo; Tel.: +962-272-01-000

Received: 11 January 2018; Accepted: 5 February 2018; Published: 9 February 2018

Abstract: The performance optimization of the two-level, three-phase, grid-feeding, voltage-source inverter (VSI) is studied in this paper, which adopts an online adaptive switching frequency algorithm (OASF). A new degree of freedom has been added to the employed OASF algorithm for optimal selection of the weighting factor and overall system optimization design. Toward that end, a full mathematical formulation, including the impact of the coupling inductor and the controller response time, is presented. At first, the weighting factor is selected to favor the switching losses, and the controller gains are optimized by minimizing the integral time-weighted absolute error (ITAE) of the output active and reactive power. Different loading and ambient temperature conditions are considered to validate the optimized controller and its fast response through online field programmable gate array (FPGA)-in-the-loop. Then, the weighting factor is optimally selected to reduce the cost of the L-filter and the heat-sink. An optimization problem to minimize the cost design at the worst case of loading condition for grid-feeding VSI is formulated. The results from this optimization problem are the filter inductance, the thermal resistance of the heat-sink, and the optimal switching frequency with the optimal weighting factor. The VSI test-bed using the optimized parameters is used to verify the proposed work experimentally. Adopting the OASF algorithm that employs the optimal weighting factor for grid-feeding VSI, the percentages of the reductions in the slope of the steady state junction temperature profile compared to fixed frequencies of 10 kHz, 14.434 kHz, and 20 kHz are about 6%, 30%, and 18%, respectively.

Keywords: grid-feeding inverter; multi-objective optimization; switching losses; switching frequency; total demand distortion

1. Introduction

Control of distributed generations (DGs) and AC microgrids becomes crucial, especially with the increased integration of renewable energy generators (REGs) with the grid. Moreover, energy storage systems (ESSs) are now an essential part in any utility-scale or even small-scale REGs. In these systems, voltage source inverter (VSI) is a primary element that interfaces between DC and AC sides. Enhancing the reliability and improving the performance of the VSI are respected aims that have a great reflection on the AC microgrid and generally on the electrical power system [1]. These aims can be achieved by introducing flexible ac transmission systems (FACTs) to utility-scale REGs and improving the utilized control schemes [2].

Based on the VSI mode of operation, DGs can be categorized into three general modes: grid forming, grid feeding, and grid supporting [3]. For grid-connected DGs, grid feeding mode is more commonly used. Therefore, it is considered in this paper. Two important goals shape the scope of this work which are the quality of the output current total demand distortion (TDD) that is ruled by standards and the power losses inside the VSI as a representation of inverters' efficiency. Unfortunately,

the above goals are contradictory objectives and giving more weight or priority to one of them will degrade the other one.

Power losses in insulated-gate bipolar transistors (IGBTs) and their associate antiparallel diodes can be classified into two groups: insignificant and significant power losses. The insignificant power losses include (1) blocking losses, (2) driving losses, and (3) the diode turn-on losses [4]. The significant losses consist of (1) the conduction losses related to the desired output (minimizing this part is not attractive), (2) on-off losses in IGBTs, and (3) turn-off diode losses [5]. In this work, the last two terms—switching and recovery losses—are considered as one objective function.

As a crucial player in the control of VSIs, f_{sw} is considered as the main decision variable of the optimization problem [6]. In the literature [7–11], switching frequency was used either to improve the inverter efficiency [7,9] or the quality of the output power [10,11]. The fixed switching frequency for all conditions was considered in [5] at the maximum possible total harmonic distortion (THD), and in [11] the trajectory of the switching frequency was stated for the single phase inverter based on the calculus of variations. An offline trade-off between electromagnetic torque ripple and losses of the salient-pole permanent magnet synchronous motor was used in [7] to minimize the inverter losses. In [10], the switching frequency was selected to minimize the acoustic noise of the three-phase induction motor. The switching frequency is used in [8] to analyze and design the LCL filter in the grid-connected, cascaded, multilevel inverter to improve harmonic attenuation and reduce the damping power loss.

An online adaptive switching frequency (OASF) algorithm that considers the power quality of the output current and the efficiency of the VSI as a combined objective function is presented recently in [12]. Due to its simplicity and online capability, the variable f_{sw} algorithm in [12] is adopted in this study. The employed OASF depends on the weighting factor to achieve a trade-off between the power quality of the output current and the efficiency of the VSI. The selection of the weighting factor and the overall system optimization design have not been covered or discussed in [12]. A new degree of freedom is added to the employed OASF algorithm for the optimal selection of the weighting factor and the overall system optimization design.

This weighting factor is another degree of freedom that can contribute to the improvement of the performance of the grid-feeding VSI. Selecting the weighting factor can be done in two ways: (1) by giving more priority to one of the two objectives (in this paper, the switching losses are prioritized); or (2) by selecting the optimal weighting factor to minimize a certain cost function.

Toward that end, the design process first selects the weighting factor and optimizes the gains of the controllers to have a fast response time by minimizing the integral time-weighted absolute error (ITAE) of the output active and the reactive power. After that, based on the first stage results, the optimized controller gains are used and an optimal weighting factor is selected based on filter and heat-sink cost minimization. A full mathematical formulation, including the impact of the coupling inductor and the controller response time, is presented in this paper. Under all conditions, the output power signal meets all standards and improves the performance of the grid-feeding VSI, which is proven through FPGA-in-the-loop verification and experimentally. Besides that, the presented algorithm not only improves the performance of the VSI under all loading conditions, including the rated conditions, but also improves the system reliability by considering the importance of the acceptable range of the junction temperature of the IGBT and its antiparallel diode.

The main contributions of this paper are (i) to provide a full mathematical formulation and analysis, including the impact of the coupling inductor and the controller response time on the performance optimization of the two-level three-phase grid-feeding voltage-source inverters; and (ii) to provide a method for the optimal selection of the weighting factor and the overall system optimization design so that the budget for the heat sink and the passive filter is minimized while the performance is improved without any violation to any harmonic standards or the junction temperature limits at any loading condition.

The remainder of this paper is organized as follows. The estimation of power losses, the thermal modeling of IGBT power module, and the time-domain current ripple analysis are presented in

Section 2. The adopted OASF algorithm with an extra degree of freedom is presented in Section 3. FPGA-in-loop verification is done in Section 4. Optimal selection of the weighting factor and the experimental validation are discussed in Section 5. Finally, the paper is concluded in Section 6. The nomenclatures that are used throughout this paper can be found at the end of this paper.

2. Inverter Power Losses and Output Current TDD

To improve the performance of the system shown in Figure 1, different design and control variables can optimally be selected. Besides the proportional-integral (PI) controller's gains (K_P^{PQ}, K_I^{PQ}, K_P^I, K_I^I), the value of the inductance of the L-type filter (L) and the control variables in PQ-controlled DG systems can be optimized as well. Moreover, optimal selection of switching frequency and optimal design of the heat-sink improve the performance of the grid-feeding inverters under different loading and weather conditions. The improvement can be seen by measuring the TDD and the efficiency of the inverter, in which these two contradictory objectives have an important reflection on the junction temperatures of the IGBT and its associated anti-parallel diode. Both the temperature and the variation of the temperature have a significant impact on the life time of any power-electronic device, and the IGBT power module is not an exception [13]. Efficient optimization of these two objectives is necessary and must rely on an accurate mathematical representation of the power-electronic system under study. Both objectives are mathematically linked together in this section, and the detailed derivations can be found in [12,14–20].

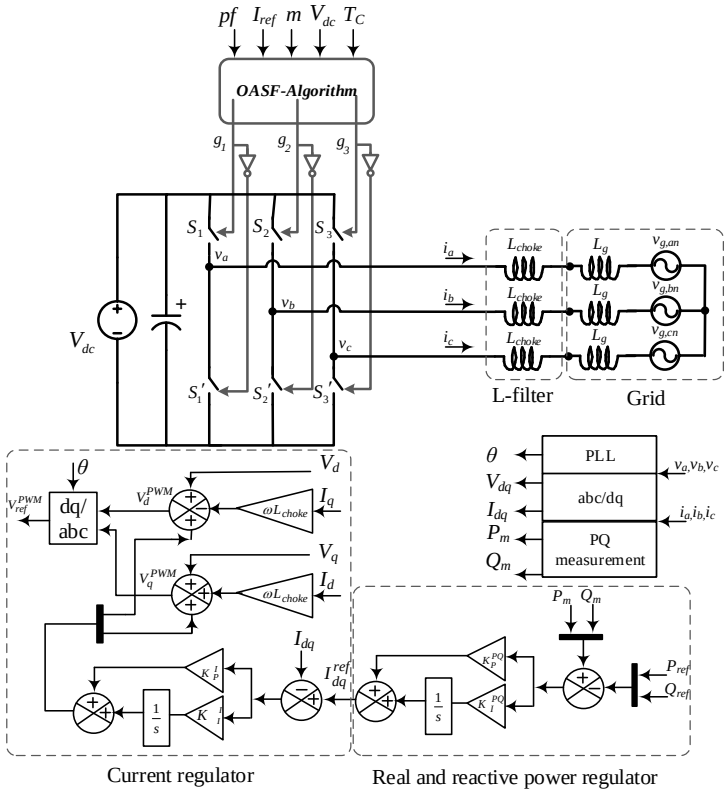


Figure 1. Schematic representation of grid-feeding VSI using the adopted OASF algorithm.

If a sinusoidal current is flowing through a power-electronic module, P_{CQ} and P_{CD} can be formulated as in Equations (1) and (2).

$$P_{CQ} = \frac{V_{CE0}\, i_{pk}}{2\pi} + \frac{R_{CE} i_{pk}^2}{8} + \left(\frac{V_{CE0} i_{pk}}{8} + \frac{R_{CE} i_{pk}^2}{3\pi} \right) m\, \cos(\theta) \tag{1}$$

$$P_{CD} = \frac{V_{f0}\, i_{pk}}{2\pi} + \frac{R_f i_{pk}^2}{8} - \left(\frac{V_{f0} i_{pk}}{8} + \frac{R_f i_{pk}^2}{3\pi}\right) m\, \cos(\theta) \tag{2}$$

Based on manufacturer datasheet parameters and the average behavioural model, E_{on} and E_{off} as a function of the phase-current (i_c) flowing through the IGBT and junction temperature of the IGBT can be expressed by employing surface curve fitting of $E_{on}(i_c, T_{jQ})$ and $E_{off}(i_c, T_{jQ})$ as in Equations (3) and (4), respectively. The subscripts *on,test* and *off,test* in Equations (3) and (4) represent the on and the off test conditions provided by manufacturer datasheet for energy losses measurements and $\alpha_{dc} = \frac{V_{dc}}{V_{dc,test}}$.

$$E_{on} = \frac{E_{on}(R_{g,on})}{E_{on}(R_{g,on,test})}\, \alpha_{dc} E_{on}(i_c, T_{jQ}) \tag{3}$$

$$E_{off} = \frac{E_{off}(R_{g,off})}{E_{off}(R_{g,off,test})}\, \alpha_{dc} E_{off}(i_c, T_{jQ}) \tag{4}$$

Integrating these energy losses over one fundamental period, the IGBT average switching losses per-period can be given as:

$$P_{swQ} = \frac{E_{on} + E_{off}}{\pi} f_{sw} \tag{5}$$

Adopting average behavioural model and surface curve fitting tools E_{rec} can be represented as in Equation (6), and the diode average switching losses per-period are expressed as in Equation (7).

$$E_{rec} = \alpha_{dc} \frac{E_{rec}(R_{g,on})}{E_{rec}(R_{g,on,test})}\, E_{rec}(i_f, T_j) \tag{6}$$

$$P_{swD} = \frac{E_{rec}}{\pi} f_{sw} \tag{7}$$

The total power losses P_T in three-phase module under sinusoidal pulse width modulation (SPWM) are shown in Equation (8).

$$P_T = 6\left(P_{CQ} + P_{CD} + P_{swQ} + P_{swD}\right) \tag{8}$$

Based on the well-known circuit shown in Figure 2 [14], the case, the IGBT, and the diode junction temperatures can be extracted as in Equations (9)–(11). To this end, all significant power losses are formulated and their impact on the junction temperatures is shown without excluding the ambient temperature.

$$T_c = 6\left(P_Q + P_D\right)\left(R_{\mathrm{CS}} + R_{\mathrm{SA}}\right) + T_a \tag{9}$$

$$T_{jQ} = P_Q\, R_{jCQ} + T_c \tag{10}$$

$$T_{jD} = P_D\, R_{jCD} + T_c \tag{11}$$

Another point of interest of this work is the TDD of the output current. As a PQ-controlled inverter, the load of this DG can be represented as an ideal grid voltage source in series with inductive element as shown in Figure 1. This assumption is applicable for motor-drive application as well [14–16]. During any switching period, the inductor current is assumed linear, either in charging or discharging mode, with a constant fundamental component. For star-connected load, the current ripple per fundamental period can be expressed as in Equation (12). The TDD is expressed as in Equation (13).

$$\hat{I}_{h,rms} = \frac{m V_{dc}}{16\sqrt{3} L f_{sw}} \sqrt{2 - \frac{16\sqrt{3}}{3\pi} m + \frac{3}{2} m^2} \tag{12}$$

$$TDD = \frac{\hat{I}_{h,rms}}{\bar{I}_{L,rated}} \tag{13}$$

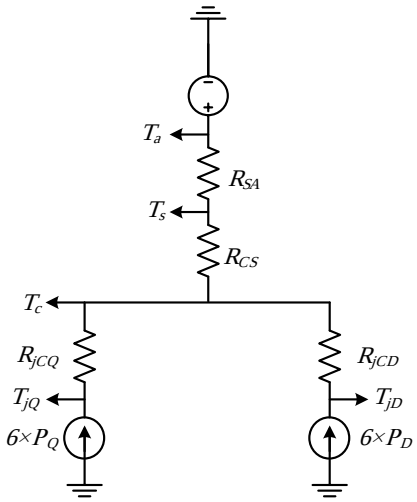


Figure 2. Thermal circuit with common thermal resistance case to heatsink.

3. Online Adaptive Switching Frequency Algorithm

THD standards are related to certain loading conditions, and most of DGs are loaded based on the available or pre-scheduled dispatch energy that does not necessarily match the rated output power. To fulfill the standards at rated conditions, a higher switching frequency can be selected; this increase in switching frequency has mainly two impacts on the power electronics module: (i) the switching losses will increase and (ii) the junction temperature will increase as well. Therefore, linking and adapting the switching frequency with loading conditions is important to improve the overall VSI performance under any circumstance.

Different variable f_{sw} algorithms are presented to improve the performance of the VSI by changing the switching frequency within the power fundamental period [21–24]; in this work, the switching frequency is related to the scheduled power references, and all regulations and performance indices are taken into consideration to ensure optimal operation between the contradictory requirements. In other words, OASF algorithm is adopted to ensure a proper trade-off between TDD and switching losses with firm satisfaction of the operation constraints under any loading condition. This trade-off between the two contradictory objectives is represented by a positive weighting factor w as shown in Equation (14).

$$\text{Minimize } F_u(f_{sw}) = wP_{sw}(f_{sw}) + (1-w)TDD(f_{sw}) \tag{14}$$

Equation (14) is a multi-objective optimization problem, in which the switching frequency is the key player that determines the switching losses and the TDD at the point of common coupling (PCC) based on the previous formulations. The weighting factor can be any fraction between 0 and 1. Selection of the weighting factor depends on the priority of the two objective functions. For large scale VSI, more weight can be given to the switching losses, and w can be selected to be around 60%. Another way to select w is to state a third objective function like the cost of the used filter, and then w will be considered as a new degree of freedom. One possible way of optimizing this weighting factor is presented in Section 5.

The practical values of P_{sw} and TDD cannot be fairly compared in either order of magnitude or units; doing so will lead to the obtaining of a misleading result. To handle this, the objective function in Equation (14) is normalized and updated based on the boundaries of the optimization problem as in Equation (15), in which the superscript ideal notation is related to the minimum possible value.

$$\text{Min } F_u^n(f_{sw}) = w\frac{P_{sw}(f_{sw}) - P_{sw}^{ideal}}{P_{sw}^{nadir} - P_{sw}^{ideal}} + (1-w)\frac{TDD(f_{sw}) - TDD^{ideal}}{TDD^{nadir} - TDD^{ideal}} \tag{15}$$

The TDD^{ideal} solution is linked to f_{sw}^{up}, and P_{sw}^{ideal} is the minimum possible total switching loses at f_{sw}^{low}. On the other hand, P_{sw}^{nadir} and TDD^{nadir} are the maximum possible values on the Pareto curve.

The mathematical formulations in Section 2 need to be updated to comprise the contradictory functions in this optimization problem. These functions and boundaries of the Pareto curve can be rewritten as in Equations (16) and (17). The value of P_{sw}^{nadir} is limited by many constraints, and it is linked with the junction temperature and the derivation of P_{sw}^{nadir} , which will be shown later in this section.

$$P_{sw} = Af_{sw};\ P_{sw}^{ideal} = Af_{sw}^{low};\ P_{sw}^{nadir} = Af_{sw}^{up} \tag{16}$$

$$TDD = \frac{B}{f_{sw}};\ TDD^{nadir} = \frac{B}{f_{sw}^{low}};\ TDD^{Ideal} = \frac{B}{f_{sw}^{up}} \tag{17}$$

in which the constants A and B can be extracted from Equations (13) and (8) as follows

$$A = \frac{6\left(E_{on} + E_{off} + E_{rec}\right)}{\pi} \tag{18}$$

$$B = \frac{mV_{dc}}{16\sqrt{3}LI_{rated}}\sqrt{2 - \frac{16\sqrt{3}}{3\pi}m + \frac{3}{2}m^2} \tag{19}$$

Then, the normalized objective function F_u^n will be

$$F_u^n(f_{sw}) = \frac{1}{f_{sw}^{up} - f_{sw}^{low}}\left(w\left(f_{sw} - f_{sw}^{low}\right) + (1-w)f_{sw}^{low}\left(\frac{f_{sw}^{up}}{f_{sw}} - 1\right)\right) \tag{20}$$

Differentiating Equation (20) yields Equation (21), and solving Equation (21) yields the optimal switching frequency f_{sw}^{opt} as finalized in Equation (22).

$$\left.\frac{dF_u^n}{df_{sw}}\right|_{f_{sw}=f_{sw}^{opt}} = w\frac{1}{f_{sw}^{up} - f_{sw}^{low}} - (1-w)\frac{f_{sw}^{up}f_{sw}^{low}}{f_{sw}^{up} - f_{sw}^{low}}\frac{1}{\left(f_{sw}^{opt}\right)^2} = 0 \tag{21}$$

$$f_{sw}^{opt} = \sqrt{f_{sw}^{up}f_{sw}^{low}\frac{(1-w)}{w}} \tag{22}$$

From the thermal resistance circuit, linking switching power losses with the junction temperature and P_{sw}^{nadir} is related to the maximum junction temperature. It is assumed that $T_{jD}^{\max} = T_{jQ}^{\max} = T_j^{\max}$. Subtracting Equation (11) from Equation (10) yields Equation (23), and making use of Equation (9) at $T_{jD}^{\max}$, the maximum power loss of the diode and IGBT can be related to each other via the thermal resistance as in Equation (24)

$$T_{jQ} - T_{jD} = P_Q\ R_{jCQ} - P_D\ R_{jCD} \tag{23}$$

$$P_Q^{\max} = \frac{R_{jCD}}{R_{jCQ}}P_D^{\max} \tag{24}$$

From Equations (9), (23), and (24), the effect of ambient temperature and the junction temperature on the diode power losses can be expressed as in Equation (25).

$$P_D^{\max} = \frac{T_j^{\max} - T_a}{R_{jCD} + 6(R_{CS} + R_{SA})\left(1 + \frac{R_{jCD}}{R_{jCQ}}\right)} \tag{25}$$

Changing the switching frequency without monitoring the junction temperature may lead to power module failure. As the conduction losses can be estimated, the maximum possible switching

losses are limited to the difference between the maximum power losses and the conduction loss as seen in Equations (26) and (27) for the diode and the IGBT, respectively

$$\begin{array}{l} P_{swD}^{\max} = P_{D}^{\max} - P_{CD} \\ P_{swQ}^{\max} = P_{Q}^{\max} - P_{CQ} \end{array} \tag{26}$$

Finally, P_{sw}^{nadir} can be expressed as:

$$P_{sw}^{nadir} = 6\left(P_{D}^{\max}\left(1 + \frac{R_{JCD}}{R_{JCQ}}\right) - P_{CD} - P_{CQ}\right) \tag{27}$$

Figure 3 shows a summary of the proposed work, in which the proposed algorithm is shown in Figure 3a, while the OASF implementation in the FPGA is shown in Figure 3b. The case temperature is sensed and used as input to the thermal model to estimate T_{jQ}, T_{jD}, and T_a. The loading condition and both T_{jQ} and T_{jD} can be used to estimate the conduction and the energy switching losses based on the behavioral model. Thus, the optimal switching frequency can be readily calculated given the optimal weighting factor w^{opt}.

Two scenarios are considered in the following two sections:

First scenario (S.A): "Weighting factor is selected to favor the switching losses and the controller gains are optimized". The first scenario, presented in Section 4, is used for FPGA-in-loop verification and consists of the following three steps:

Step1.A: Filter inductance is known and weighting factor is selected based on the priority of one objective over the other. The value of the L-filter is important in decoupling the d and q controllers, and this challenge is important in the second scenario.

Step2.A: The PI-controller's gains shown in Figure 1 are optimally selected based on the ITAE of the output PQ response. Step change is applied to the references signals (P_{ref} and Q_{ref}), and teaching-learning-based optimization (TLBO) algorithm is used to select the optimal gains.

Step3.A: The weighting factor is selected with higher priority to switching losses ($w = 60\%$), and the online algorithm is tested and compared with fixed switching frequencies through FPGA-in-the-loop verifications with fast change in the reference power or the ambient temperature. For the first scenario, two tests are carried out:

1. The output power varies from 10% to 100% of 33 kW with 10% step in very brief time (0.5 s) under constant ambient temperature as in Section 4.1.
2. The load is kept constant at the rated load and the ambient temperature varies from 10 °C to 50 °C with 10 °C step at each 0.5 s as in Section 4.2.

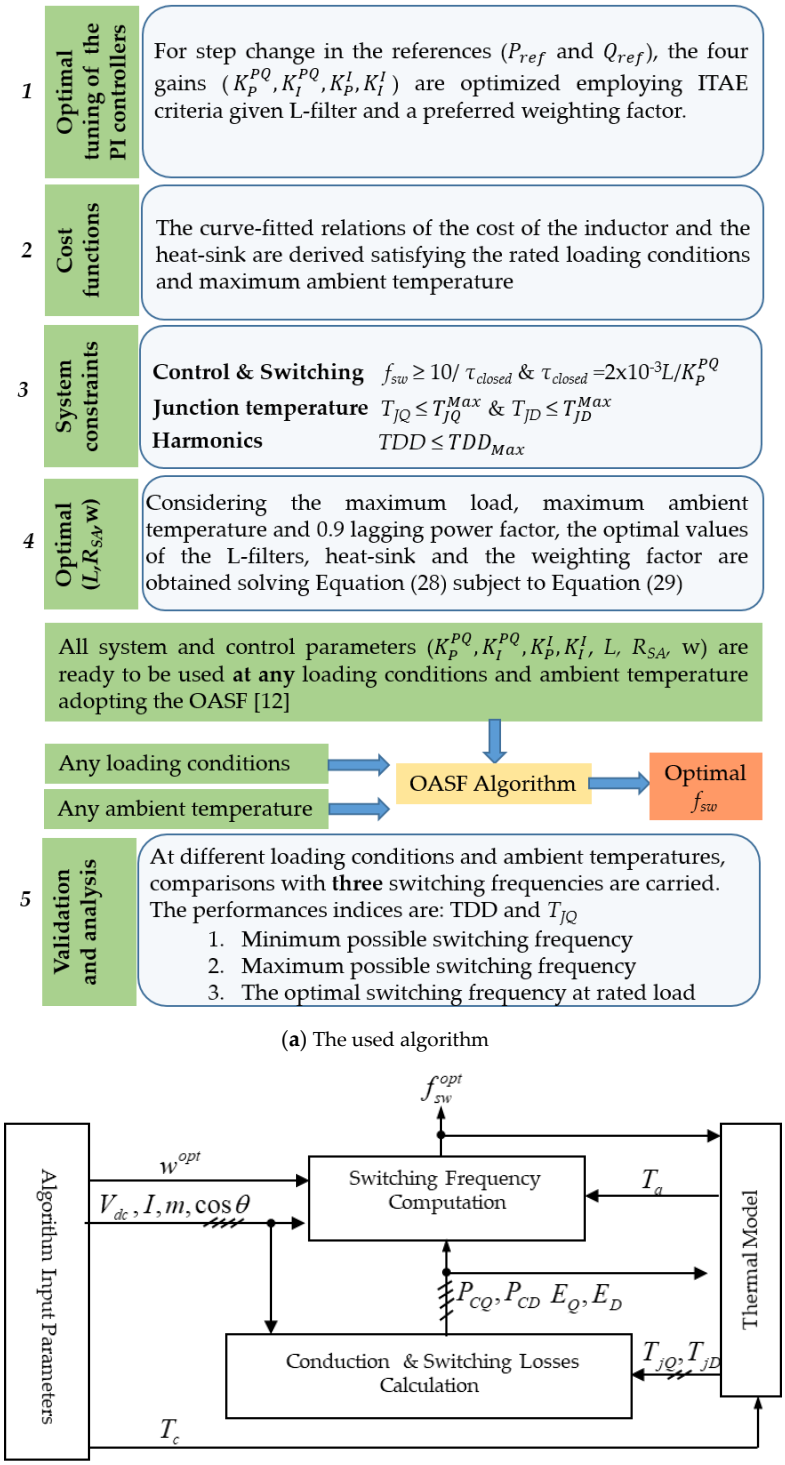
Second scenario (S.B): "The weighting factor is optimally selected as a new degree of freedom to reduce the cost of the L-filter and the heat sink". The second scenario, presented in Section 5, is used to validate the proposed work experimentally and consists of the following two steps:

Step1.B: This scenario is used to verify the work experimentally and analyze the results when there is no significant importance of the switching losses over the quality of the output current as the main objective for the design stage is the cost.

Step2.B: All system, control variable, operational limits, and constraints are considered under the extreme case in which the system is fully loaded (0.9 power factor and 50 °C ambient temperature, to optimally find the weighting factor, switching frequency, filter inductance, and heat sink).

The designed parameters from (SB.Step2.B) are used, and the system is tested while changing load from 10% to 100% of 1.0 kW.

The results are compared with conventional fixed switching frequencies, which are 10 kHz, 20 kHz, and the optimal switching frequency at the extreme case 14.434 kHz in (SB.Step2.B)



(**a**) The used algorithm

(**b**) Online Adaptive Switching Frequency Algorithm

Figure 3. Summary of the proposed work (**a**) the used algorithm; (**b**) OASF implementation in the FPGA.

4. FPGA-In-The-Loop Verification

4.1. Effect of the Load Change

In this section, the relationship between the two objectives and the switching frequency under different loading conditions is discussed, and the benefits of the proposed algorithm with its ability to maintain the TDD standards at the PCC are shown. A 33 kVA, 380 V, 50 Hz VSI is used with different

scheduled power references as shown in Figure 4a. For a weighting factor of 60% and unity power factor, the power reference is changed every 0.5 s starting from 6.6 kW and finishing with 33 kW as in Figure 4a. The proposed algorithm is tested through FPGA in-the-loop to check its computational time. As can be seen from Figure 4b, the corresponding optimal switching frequency of the proposed algorithm is decreasing to attain an optimal trade-off between the switching losses represented by the junction temperatures as in Figure 4c and the TDD as in Figure 4d. The larger the load, the lower the switching frequency, and hence the higher the TDD. The relationship between the switching frequency and the continuous variation of the load from 10% to 100% of the rated capacity is clearly illustrated in Figure 5a. Form results in Figure 5, it can be concluded that the switching frequency decays exponentially as the load increases.

One of the key features of the proposed algorithm is the accurate observation of IGBT and diode junction temperatures while considering the ambient temperature and the conduction losses that are mainly related to loading conditions.

The rate of change of operating temperature is the main cause of failure of most power-electronic switches and electrical devices. From Figure 5b,c, the operating temperature profile under the proposed algorithm is flatter and at lower level compared with the results from middle and upper switching frequencies. Only the minimum switching frequency can result in lower temperatures but with higher TDD as in Figure 6. This coincides with the goals of the proposed algorithm and adds more robustness to the power module when its life time is extended. From Pareto curve, 4.858 kHz is the lower switching frequency and 14.58 kHz is the upper switching frequency. The average of these two frequencies is the middle frequency, which is 9.719 kHz. Comparing the results from OASF algorithm with the results from the optimal two switching frequencies (lower and upper) and its middle value shows the apparent effectiveness of the proposed work.

Alternatively, as the load increases, the TDD resulted from the utilization of the proposed algorithm (Figure 6) will start from its minimum value, which is achieved by selecting the highest switching frequency and then increasing linearly to reach the highest TDD at full loading condition. This shows that the TDD under the OASF algorithm follows the regulation at all loading conditions.

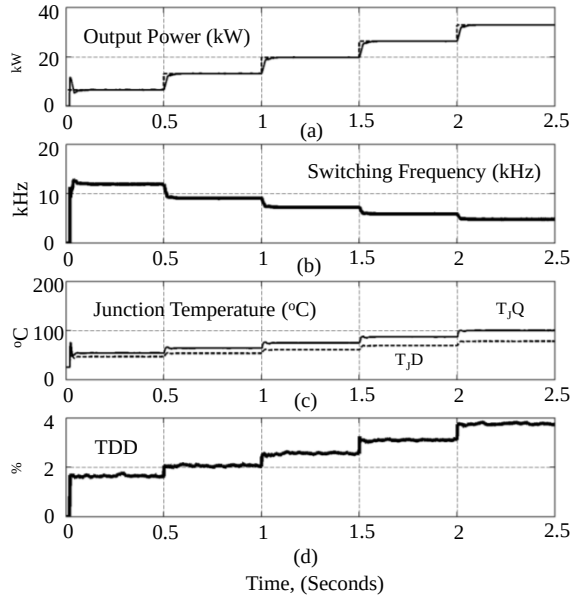


Figure 4. Effect of the load change on the switching frequency, junction temperatures, and TDD, (**a**) the output power in kW; (**b**) the switching frequency in kHz; (**c**) the IGBT and diode junction temperatures in °C; (**d**) the TDD of the output current.

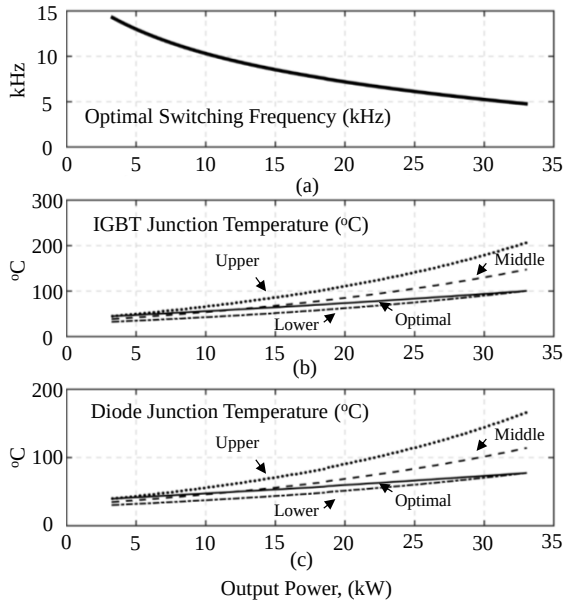


Figure 5. Optimal switching frequency and the junction temperature versus output power for different switching frequencies, (**a**) optimal switching frequency in kHz; (**b**) IGBT junction temperature under different switching frequencies; (**c**) diode junction temperature under different switching frequencies.

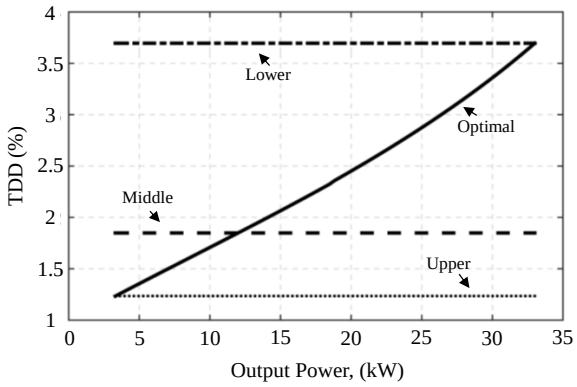


Figure 6. TDD versus output power for different switching frequencies.

4.2. Effect of Variation of Ta under the Rated Loading Condition

To study the impact of T_a, which did not attract a lot of attention in the literature, the load is kept constant at the rated value and unity power factor, while the ambient temperature varies from 5 to 50 °C with 10 degrees-step at each 0.5 s, as shown in Figure 7a. This brief time is selected to be relatively small with respect to the practical rate of change to test the effectiveness of the proposed work as an online algorithm and to summarize the results in smaller figures. The switching frequency decreases as the temperature increases (Figure 7b) to ensure the optimal trade-off between switching losses and TDD (Figure 7d) while keeping the junction temperature within the operational range as indicated in Figure 7c. Moreover, the switching frequency linearly decreases as the ambient temperature increases, as shown in Figure 8a. The temperature profiles shown in (Figure 8b) and (Figure 7c) have smaller range of variation than the other fixed frequencies. At low temperatures, the junction temperatures when OASF algorithm is adopted are close to the junction temperatures obtained from the upper limit of the switching frequency and end with the lower limit of the switching frequency at high ambient temperature.

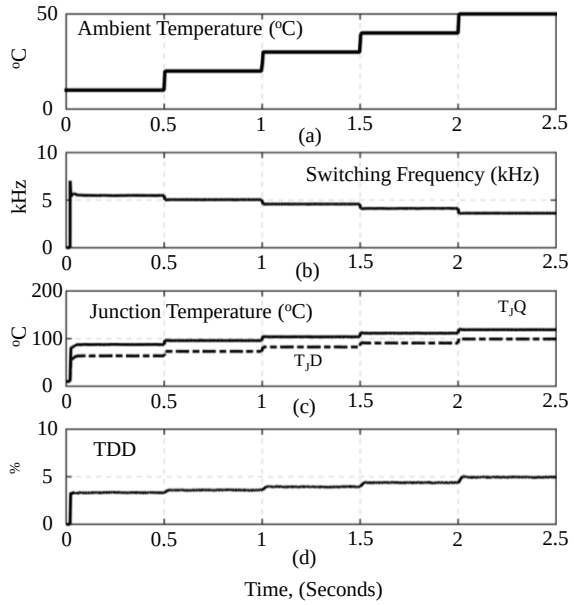


Figure 7. Effect of the ambient temperature on the switching frequency, junction temperatures, and TDD at rated load, (**a**) ambient temperature in °C (**b**) the switching frequency in kHz; (**c**) the IGBT and diode junction temperatures in °C; (**d**) the TDD of the output current.

Figures 8 and 9 illustrate the meaning of the trade-off between the selected objective functions. The OASF algorithm finds the optimal solution when both TDD and power losses are considered. Moreover, the flatter temperature profile (Figure 8b,c) proves the importance of including the ambient temperature and how OASF algorithm is useful to the performance of the VSI. Giving more weight to the switching losses will lead to the touching of the optimization boundaries at lower ambient temperatures.

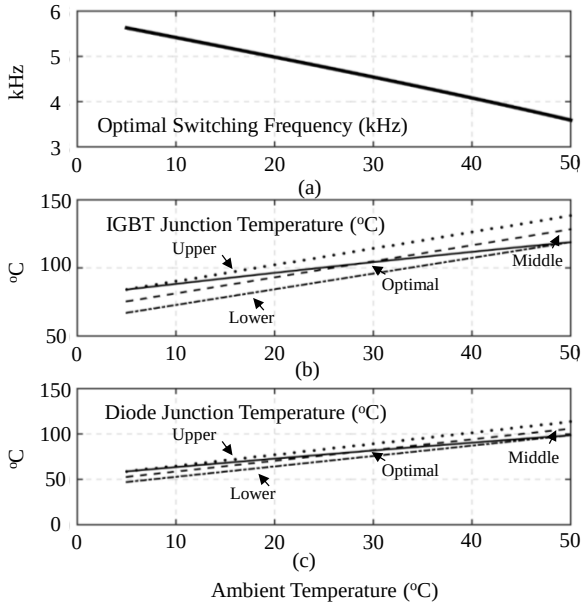


Figure 8. Optimal switching frequency and junction temperatures versus ambient temperature for different switching frequencies, (**a**) optimal switching frequency in kHz; (**b**) IGBT junction temperature under different switching frequencies; (**c**) diode junction temperature under different switching frequencies.

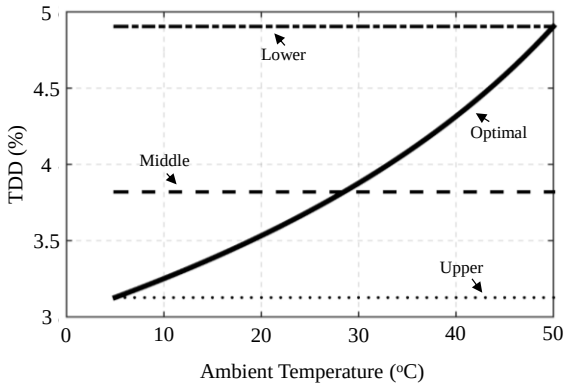


Figure 9. TDD versus the ambient temperature for different switching frequencies.

5. Optimal Selection of Weighting Factor and Experimental Validation

Selecting the weighting factor of the objective function can be considered as an additional degree of freedom of the proposed algorithm. The weighting factor is selected to attain the lowest cost of the heat-sink and the filter. As discussed in the previous part, the minimum switching frequency occurs at maximum output power and maximum ambient temperature. Therefore, the filter should be designed at the minimum optimal switching frequency. Moreover, the cooling system must be designed at this point, because the maximum junction temperature is linked to the same loading condition. The optimization problem formulation that is used to find the minimum cost design at the worst case of loading condition is:

$$\begin{aligned} &\text{Min} \qquad C_{tot} = 3 \times C_L(L) + C_{SA}(R_{SA}) \\ &s.t. \\ &T_{jQ} \leq T_{jQ}^{\max} \\ &T_{jD} \leq T_{jD}^{\max} \\ &TDD \leq TDD_{\max} \\ &f_{sw} \geq 10/\tau_{closed} \end{aligned} \tag{28}$$

where

$$\begin{aligned} &C_L(L) = 10.5 + 0.84\, L \\ &C_{SA}(R_{SA}) = 16.42/(R_{SA} - 0.0105) \\ &\tau_{closed} = 2 \times 10^{-3} L/K_P^{PQ} \end{aligned} \tag{29}$$

In Equation (29), C_L is the curve-fitted cost of a fixed single-phase inductor (mH), which can carry the rated current, and C_{SA} is the cost of the heat sink, which can work at full load condition. Interpolating the price offers from manufacturers' database, as well as the cost functions C_L and C_{SA}, can be determined [18]. The last equation in (29) relates the impact of the coupling inductor to the controller response time.

Based on the datasheet, the first and second constraints of the optimization process $T_{jQ}^{\max}$ and $T_{jD}^{\max}$ are set to be 125 °C, and according to the IEE-519 standards; the third constraint $TDD_{\max}$ is set to be less than 5%. The fourth constraint of the optimization process represents the dependency of the closed-loop controller bandwidth on the value of the inductance. At this point, the bandwidth is selected to be 10 times slower than f_{sw}. The maximum ambient temperature is assumed to be 50 °C. These constraints are used to find the optimal control and design variable in this extreme case. After that, VSI will be tested at different loading and temperature conditions and the performance will be compared against three fixed switching frequencies.

The results from this optimization problem are the desired inductance L, the thermal resistance of the heat sink R_{SA}, and the optimal switching frequency f_{sw}^{opt}. As the boundaries of the switching

frequency are known (f_{sw}^{low}, f_{sw}^{up}) and f_{sw}^{opt} is determined based on Equation (28), then the optimal weighting factor w^{opt} can be extracted from Equation (22). For $V_{dc} = 100$ V, $V_{ac} = 70$ V, $T_a = 50$ °C, and 1.0 kW rated power at 0.9 lagging power factor, the results of the optimization problem of Equation (28) are:

$w^{opt} = 0.4916$, $f_{sw}^{opt} = 14.434$ kHz, $R_{SA} = 4.01$ C/W, $L = 0.786$ mH for optimal cost $C_{tot}^{opt} = 37.586$\$.

Figure 10 shows the experimental setup that is used to verify the proposed work. As the load varies at $T_a = 25$ °C, and unity power factor varies from 10% to 100% of the rated power, f_{sw}^{opt} will decrease exponentially as in Figure 11a. A comparison with three fixed switching frequencies (10 kHz, 20 kHz, and 14.434 kHz) is carried out as shown in Figure 11b,c, in which the estimated junction temperatures and the experimental TDD increase as the load increases. Moreover, since the load is resistive, the TDD will be fixed with fixed switching frequencies, while with OASF algorithm, the switching frequency will decrease as the load increases. Hence, the TDD will increase. From Figure 11a, the full-load optimal f_{sw} is higher than 14.434 kHz (18.9 kHz); this is because of the change in the ambient temperature and the load power factor that relaxes the constraints on the optimal f_{sw}.

It is clear from the IGBT junction temperature (Figure 11c) that the weighting factor does not give any priority to the switching losses, but the rate of change is better (flatter) with OASF algorithm. The experimental TDD (Figure 11b), which is the second objective, gets benefits from this weighting factor, and TDD from OASF is much lower than the other fixed switching frequencies. TDD is more than 5% when the switching frequency is 10 kHz or 14.434 kHz. The last result shows that fixed f_{sw}, which is optimal in the extreme case, is infeasible when the load power factor becomes unity.

Figure 11 shows the importance of adopting the OASF algorithm that employs the optimal weighting factor for grid feeding VSI; the percentages of the reductions in the slope of the steady state junction temperature profile compared to fixed frequencies of 10 kHz, 14.434 kHz, and 20 kHz are about 6%, 30%, and 18%, respectively.

Figure 10. Experimental setup.

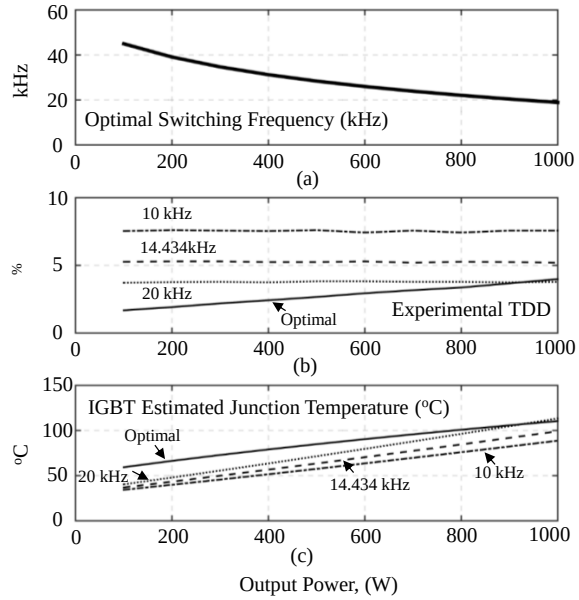


Figure 11. Optimal switching frequency, experimental TDD, and IGBT junction temperature for different switching frequencies, (**a**) optimal switching frequency in kHz; (**b**) the experimental TDD of the output current under different switching frequencies; (**c**) estimated IGBT junction temperature under different switching frequencies.

6. Conclusions

In this paper, full mathematical formulations, including the impact of the coupling inductor and the controller response time on the performance optimization of two-level, three-phase, grid-feeding, voltage-source inverters are considered through the adoption of an online adaptive switching frequency algorithm (OASF) with a new degree of freedom. The adopted OASF algorithm with the extra degree of freedom has been fully analyzed. Based on these analyses, an optimization problem to minimize the cost design in the worst case of the loading condition for the gird-feeding VSI is formulated. The results from this optimization problem are the filter inductance, the thermal resistance of the heat sink, and the optimal switching frequency with the optimal weighting factor. Based on those results, VSI test-bed is designed, and experiments are conducted. From the experimental results, the performance of VSI is improved without any violation of any harmonic standards or the junction temperature limits at any loading condition, while the budget for the heat sink and the passive filter is minimized. Although, as with any variable switching frequency algorithm, changing the switching frequency of the VSI may lead to the oversizing of the output differential mode and the common mode filters, nevertheless the proposed work can be easily implemented in micro-controllers and can be extended to any power converter, which includes multi-level inverters, if the proper models for the power losses and the total demand distortion are constructed. While satisfying the harmonic constraints, the flatness of the junction temperature profile is enhanced even if compared with the minimum switching frequency. At least a 6% reduction in the slope of the junction temperature is achieved by employing the proposed work, which can contribute to the extension of the life time of the gird-feeding VSI, thus, providing a better transient capability while enhancing the overall performance.

Acknowledgments: Besides the open access fees, this research was supported by the deanship of research at Jordan University of Science and Technology (Grant number: 20150010).

Author Contributions: Issam A. Smadi, Saher Albatran and Hamzeh J. Ahmad participated in the research idea formulations and building the experimental setup. Issam A. Smadi and Saher Albatran updated the literature review and improved the quality of presentation. Issam A. Smadi formulated the control design and Saher Albatran and Hamzeh J. Ahmad implemented it. All authors participated in verifying the results and providing answers to all comments from reviewers. All authors read and approved the final manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

The following nomenclature have been used in this paper

Switching and optimization variables

T	Fundamental period [s]
T_{sw}	Switching period [s]
f_{sw}	Switching frequency [Hz]
TDD^{ideal}	TDD at f_{sw}^{up} on the Pareto curve
f_{sw}^{up}	Maximum possible f_{sw} [Hz]
P_{sw}^{ideal}	Minimum possible switching losses on the Pareto curve [Hz]
f_{sw}^{low}	Lowest possible f_{sw} [Hz]
P_{sw}^{nadir}	Maximum possible switching losses on the Pareto curve [W]
TDD^{nadir}	Maximum possible TDD on the Pareto curve
f_{sw}^{opt}	Optimal switching frequency [Hz]
w^{opt}	Optimal value of the trade-off weighting factor

Antiparallel diode variables

V_{f0}	Diode threshold voltage [V]
R_f	Diode forward resistance [Ω]

Module datasheet parameters

E_{on}	IGBT turn-on energy [J]
E_{off}	Diode turn-off energy [J]
R_g	Gate resistance [Ω]
$T_{jD}^{\max}$	Maximum possible diode junction temperature [°C]
$T_{jQ}^{\max}$	Maximum possible IGBT junction temperature [°C]

Load and system variables

L,L_{chocke}	Inductance of the L-filter [mH]
i_{pk}	Peak value of the sinusoidal current [A]
i_c	Phase-current [A]
m	Modulation index
θ	Power factor angle [rad]
V_{dc}	Input dc voltage [V]
$\hat{I}_{h,rms}$	rms current ripple [A]
$\overline{I}_{L,rated}$	rms load (inductor) current [A]
w	Trade-off weighting factor
F_u	Objective function [$]
F_u^n	Normalized objective function

Module and thermal model variables

T_a	Ambient temperature [°C]
T_j	Junction temperature [°C]
T_c	Case temperature [°C]
T_{jD}	Junction temperature of the diode [°C]
T_{jQ}	Junction temperature of the IGBT [°C]
R_{jCD}	Junction to case diode thermal resistance [C/W]
R_{jCQ}	Junction to case IGBT thermal resistance [C/W]
R_{CS}	Case to heat sink thermal resistance [C/W]

IGBT variables

V_{CE0}	IGBT threshold voltage [V]
R_{CE}	IGBT turn-on resistance [Ω]

Module losses

P_{CQ}	Average per-phase conduction losses of the IGBT [W]
P_{CD}	Average per-phase conduction losses of the diode [W]
P_{swQ}	IGBT average switching losses per-period [W]
E_{rec}	Reverse recovery loss of the diode [W]
P_{swD}	Diode average switching losses per-period [W]
P_T	Total power loss [W]
P_Q	Total power loss in the IGBT [W]
P_D	Total power loss in the diode [W]

Controller parameters

K_p^{PQ}	Proportional gain of the PQ regulator
K_I^{PQ}	Integral gain of the PQ regulator
K_p^I	Proportional gain of the current regulator
K_I^I	Integral gain of the current regulator
τ_{closed}	Controller closed loop time constant [s]
P_{ref}	Active power reference
Q_{ref}	Reactive power reference
P_m	Measured active power
Q_m	Measured reactive power
V_d	Direct axis voltage
V_q	Quadrature axis voltage
I_d	Direct axis current
I_q	Quadrature axis current
V_{ref}^{PWM}	Voltage reference to the PWM
PLL	Phase-locked loop

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