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Line-to-Line Fault Analysis and Location in a VSC-Based Low-Voltage DC Distribution Network

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Received: 24 January 2018; Accepted: 26 February 2018; Published: 2 March 2018

Abstract: A DC cable short-circuit fault is the most severe fault type that occurs in DC distribution networks, having a negative impact on transmission equipment and the stability of system operation. When a short-circuit fault occurs in a DC distribution network based on a voltage source converter (VSC), an in-depth analysis and characterization of the fault is of great significance to establish relay protection, devise fault current limiters and realize fault location. However, research on short-circuit faults in VSC-based low-voltage DC (LVDC) systems, which are greatly different from high-voltage DC (HVDC) systems, is currently stagnant. The existing research in this area is not conclusive, with further study required to explain findings in HVDC systems that do not fit with simulated results or lack thorough theoretical analyses. In this paper, faults are divided into transient- and steady-state faults, and detailed formulas are provided. A more thorough and practical theoretical analysis with fewer errors can be used to develop protection schemes and short-circuit fault locations based on transient- and steady-state analytic formulas. Compared to the classical methods, the fault analyses in this paper provide more accurate computed results of fault current. Thus, the fault location method can rapidly evaluate the distance between the fault and converter. The analyses of error increase and an improved handshaking method coordinating with the proposed location method are presented.

Keywords: fault analysis; DC distribution network; voltage source converter; fault location

1. Introduction

In recent years, distributed generation has been promoted on a large scale, primarily for DC current systems. For this reason, hybrid AC/DC power systems have developed considerably. Voltage source converters (VSCs) attracted widespread attention because of their excellent control and operation characteristics in low-voltage DC distribution networks [1,2]. Hence, technology to protect VSC-based DC distribution networks has become a heavily researched topic. However, the relevant research is limited, especially in the area of fault analysis and location. Some papers have been published in the last two years, with the relevant results summarized below.

For DC relay protection, Baran et al. [3] proposed a protection method based on early overcurrent. Yang et al. [4] considered that freewheel diodes were very easy to damage because of the severe overcurrent resulting from a capacitance discharge. Next, Baran et al. [3] proposed replacing the diodes with emitter turn-off devices (ETOs) to provide diodes with the capacity to block the current. Moreover, Baran et al. [3] adopted an ETO-based capacitance DC circuit breaker to cut off the capacitance branches and block the discharge current. However, this method increased the power loss to some extent. Deng et al. [5] developed an expression establishing the relationship between the peak value of the discharge current and the current-limiting inductance with the result that a simple inductance was effectively used to protect the diodes. Several papers have investigated the superconducting fault current limiter [6–9].

As the theoretical basis for fault location and current-limiting technology, papers examining short-circuit faults or ground fault analyses in VSC-based DC networks are still inadequate. Most of these papers' results are based on numerical simulation tests, lacking theoretical analysis. These studies' conclusions are made based on qualitative relationships or curves derived from simulated data. Yang et al. [4] first divided the fault into 3 stages ((a) capacitor discharge, (b) diodes freewheel and (c) grid current feeding) and provided in-depth theoretical analyses of the transient discharge process in a 2nd-order circuit model, eventually proposing formulas for fault current and voltage. Deng et al. [5] performed similar work to determine the relationship between the transient fault current and parameters of capacitance and inductance, providing a theoretical basis for current limiting by inductance on the DC side. Consequently, almost all later theories, both in high-voltage DC (HVDC) and low-voltage DC (LVDC) systems, regarding fault analyses were developed based on the above results, which may mislead the current limiter designs and fault location principles to some extent. Furthermore, few papers present research on steady-state fault analysis. A whole fault process includes both a transient-state fault and a steady-state fault. Steady-state fault analysis is of great significance for efforts to limit current.

However, almost all study about fault analyses are based on an HVDC-VSC transmission system [4,5,10–15], which presents several problems in a LVDC distribution network. The main problem is that stage 1, capacitor discharge, does not arise in a 2nd-order circuit model because the DC voltage is not considerably higher than that of the AC side. Under this circumstance, the diodes freewheel throughout the whole fault process, and the fault is better represented by a 3rd-order circuit model. Thus, the theoretical formulas in [4] have omitted the forced response and resulted in larger errors in fault current computing or location of an LVDC system. Alwash et al. [16] initially considers the diodes conduction stage and the current feeding from AC side in fault analyses. However, it omits the capacitance branch which is unsuitable for some fault cases.

In the study of fault locations, a prevalent method is injecting signals into a faulty cable with a probe power unit (PPU) [17,18]; a handshaking method is proposed in [19] to locate a fault without any communication models. These methods must disconnect all the sources from the system, which greatly reduces the speed of power recovery. In addition, the handshaking method may lose selectivity in some cases. Yang et al. [20] determined the fault distance by analyzing the fault information sampled by two mutual inductances separated by a known distance, but the expense of measuring the equipment is double. Tang et al. [21] located the fault by comparing the derivative, time interval or oscillation mode of the fault current in different places. It is a communication-based method which is unfit for a distribution network. Other studies have attempted to develop an accurate fault location technology, with research still focusing on the method based on a traveling wave [22–25]. However, the traveling wave location method is difficult to adopt in a distribution network with short cables because the demanded sampling frequency is too high. Additionally, some papers, such as [4,26], previously referred to the fault analysis results and determined the fault distance by solving for the parameters of resistance and inductance. However, the method in [26] has lower accuracy than that in [4] with fault resistance because its fault distance is calculated from measured resistance and unit resistance of a cable (R/km).

However, because the fault stages differ from the HVDC system, the theoretical formulas in [4] are not appropriated for fault location in the LVDC distribution system. In addition, steady-state fault analysis is indispensable because the DC-linked capacitors are cut in some protection scheme [3]. However, relevant works are deficient.

Thus, in accordance with the low-voltage distribution network itself, this paper compares the whole fault process in the HVDC transmission and LVDC distribution systems, giving a reasonable explanation for their differences. Then, we divide short-circuit fault into two stages: the transient- and steady-state stages. The primary focus of the paper is fault analysis during the steady-state stage. Next, a 3rd-order circuit was adopted for transient-state short-circuit fault analyses to correct the shortcomings of the 2nd-order circuit model analysis results in a low-voltage network. A fault location

method adopting both transient and steady fault components was proposed based on the theoretical analyses. The computed results of fault current base on theoretical formulas in [4] and this paper are compared to verify the improvement in the computed accuracy. In addition, the reasons for the increase in errors in high fault resistance short-circuit faults is explained in brief. Finally, an improved location method is proposed by coordinating with the classical handshaking method, by which the performance of the handshaking method is enhanced.

This paper is organized as follows: Section 2 presents the comparison of fault processes, detailed fault analyses, and a theoretical solution for transient and steady-state short-circuit faults is developed. Specific parameters and simulations in PSCAD/EMTDC are provided in Section 3. The fault location method, data on the location results, error analysis and coordination with other methods are presented in Section 4.

2. LVDC Cable Short-Circuit Fault Analysis

2.1. Fault Stages Comparison

When a short-circuit fault occurs, all DC-linked capacitances in the system will discharge to the fault location. This discharge leads the system voltage to collapse and the fault current to surge. As the classical theory proposed in [4], a whole fault progresses in three stages: (i) Capacitor discharges stage (Natural Response); (ii) Diode freewheel stage (Natural Response under the circumstance of $u_{dc} = 0$); and (iii) Grid-side current feeding stage (Forced Response). The classical equivalent circuits and electrical waveforms of different stages are shown as Figures 1 and 2a, respectively. The fact that stage 2 is the most challenging for freewheel diodes is generally accepted. However, stage 2 merely arise under the specified condition. Classically, the DC voltage will oscillate under the condition $R_2 < 2\sqrt{L_2/C}$ and drop to zero at $t_1 = t_0 + (\pi - \beta)/\omega$, where t_0 is fault occurring moment, $\beta = \arctan(\omega/\delta)$, $\delta = R/2L$ and $\omega = \sqrt{1/LC - \delta^2}$.

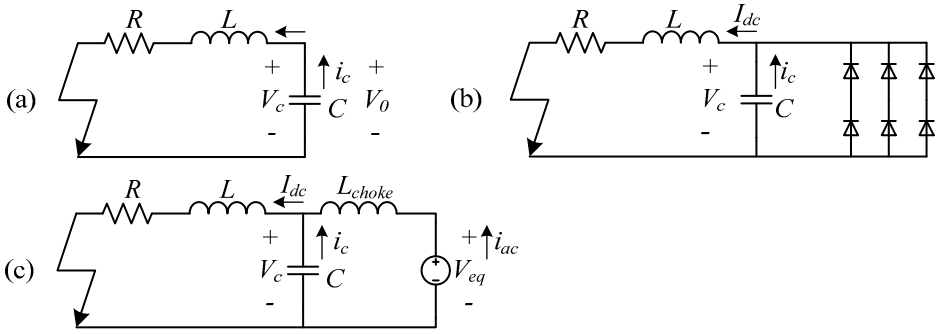

Figure 1. The equivalent circuits of different stages: (**a**) Stage 1: Capacitor discharge; (**b**) Stage 2: Diodes freewheel; and (**c**) Stage 3: Grid current feeding.

However, a fault progresses differently in the LVDC distribution system, and the main differences are reflected in stage 1. Note that the derivatives of grid-side current are as follows:

$$\frac{di_{g\ a.b.c}}{dt} = \frac{1}{L_{choke}}\Delta u = \frac{1}{L_{choke}}(U_{dc} - u_{ab,ac,bc}) \quad (1)$$

where Δu is the difference in DC voltage U_{dc} and AC line voltage u_{l_l}. In the HVDC transmission system, U_{dc} is much higher u_{l_l}. This means that $i'_{g\ a.b.c}$ is high enough and that time is sufficient for the freewheel diodes to be blocked swiftly before U_{dc} gets lower than u_{l_l} in stage 1. Just the natural response arises in a 2nd-order circuit in this stage (Figure 2a). In the LVDC distribution system, U_{dc} is not so high. This means that $i'_{g\ a.b.c}$ and Δu are low; therefore, time is insufficient for the freewheel diodes to be blocked before U_{dc} gets lower than u_{l_l} in stage 1. Once inequality $U_{dc} < u_{l\_l}$ is established,

freewheel diodes will not be blocked. Both the natural and forced responses arise in a 3rd-order circuit in this stage (Figure 2b). Thus, considerable errors arise in fault current computation and fault location if analyzed results in [4] continue to be adopted. Moreover, the criterion for DC voltage oscillation and estimated time when voltage reaches zero in HVDC system is unsuitable for LVDC system as the whole forced response feeding from AC-side is omitted. Whether DC voltage oscillates and when it drops to zero are depend on the actual expression of transient-state fault current. Fault analysis in a 3rd-order circuit must be proposed.

In this paper, the fault process is divided into two stages: the transient- and the steady-state stages. According to the simulated results, the transient duration is generally approximately 2 ms, and the surge current is more than ten times the normal current. The steady-state develops as the DC-side power steadies. Until all breakers trip, this stage lasts approximately 100 ms [21]. The fault current is a steady DC current with 6 waves, where the amplitude is influenced by the AC-side resistance, inductance and DC-side resistance. The amplitude of the steady fault current is much lower than that of the surge current, but it has a long duration. Therefore, the freewheel diodes will be damaged without appropriate current-limiting measures.

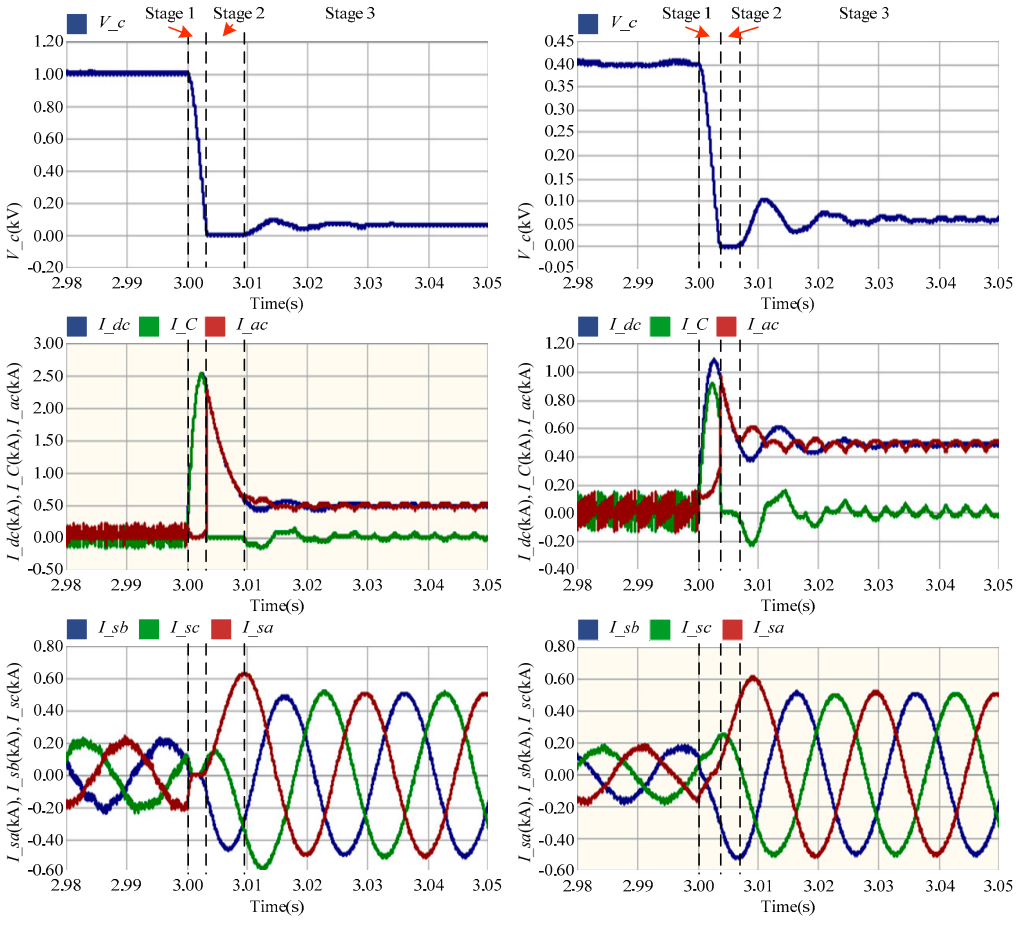

Figure 2. The electrical waveforms of different stages: (**a**) The waveforms in the HVDC system: DC-side voltage *V_c* (in kV), DC-side current *I_dc* (in kA), capacitor current *I_C* (in kA), AC-side feeding current *I_ac* (in kA), and AC-side three-phase current *I_sa,b,c* (in kA); (**b**) The waveforms in the LVDC system: DC-side voltage *V_c* (in kV), DC-side current *I_dc* (in kA), capacitor current *I_C* (in kA), AC-side feeding current *I_ac* (in kA), and AC-side three-phase current *I_sa,b,c* (in kA).

Thus, the peak value of the surge current and the amplitude of the steady current are the most significant parameters in fault analyses.

2.2. Fault Stages Comparison

DC-linked capacitance and inductance have no influence on the amplitude of the steady fault current. Therefore, a simplified circuit model is adopted as depicted in Figure 3a. The actual waveforms of the model in Figure 3a are presented as Figure 4. R_1, L and R_2 are the total AC resistance, AC inductance and DC resistance, respectively.

During the steady-state process, all freewheel diodes conduct for half of a primitive period, which is different from the situation observed in a three-phase rectification circuit (freewheel diodes conduct for one third of a primitive period). This finding is attributable to the freewheel effect of the AC-side inductance when the AC voltage U_{abc} is lower than the DC voltage U_{dc}. However, when the current of the AC-side inductance decreases to 0 (point A in Figure 4), the freewheel diodes prevent the current from decreasing further. Therefore, the rate of change in the current of the AC-side inductance $\mathrm{d}i_1/\mathrm{d}t$ abruptly changes to 0, which results in $U_{abl} = U_{abs} < U_{dc}$, with the result that diode 1 is blocking and diode 4 is conducting. Note that each diode conducts for less than half of a primitive period when $R_2/wL > 3\sqrt{3}$.

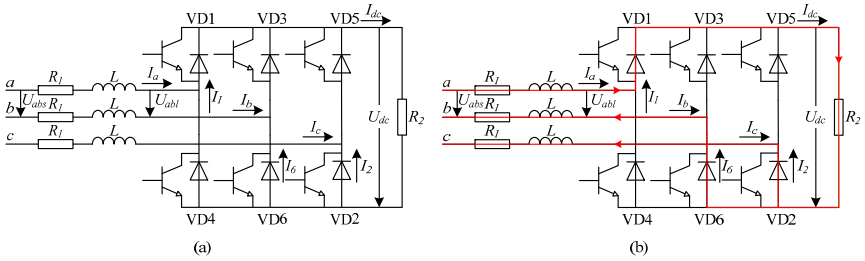

Figure 3. The equivalent circuit for analysis: (**a**)The simplified circuit model of VSC; (**b**) The current path and direction.

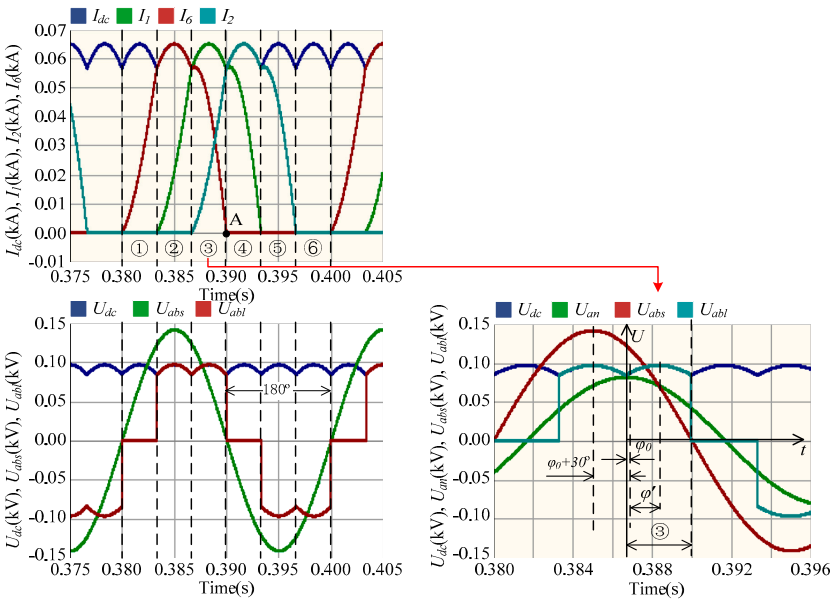

Figure 4. The waveform of steady-state quantities in Figure 3: I_{dc}, I_1, I_2, and I_6 (in kA); U_{dc}, U_{abl}, U_{abs} and U_{an} (in kV).

A primitive period can be divided into 6 equivalent periods based on the conducting status of the freewheel diodes, where each period corresponds to three different conducting freewheel diodes. Because all periods are the same, any one period can be chosen for analysis. In this paper, period ③, in which diodes 1, 2 and 6 are conducting, is analyzed in detail. The current path and direction are shown in Figure 3b. Assume that the starting time of period ③ is 0 and the coordinate system is established as shown in Figure 4.

The differential equations of the circuit in Figure 3b are listed as follows:

$$u_{abs} - u_{dc} = R_1 i_a + L\frac{di_a}{dt} - R_1 i_b - L\frac{di_b}{dt} \tag{2}$$

$$u_{acs} - u_{dc} = R_1 i_a + L\frac{di_a}{dt} - R_1 i_c - L\frac{di_c}{dt} \tag{3}$$

$$u_{dc} = i_{dc} R_2 = i_a R_2 \tag{4}$$

Because of the equivalence relations—$u_{abs} + u_{acs} = 3u_a$, $i_a + i_b + i_c = 0$ and $\mathrm{d}i_a/\mathrm{d}t + \mathrm{d}i_b/\mathrm{d}t + \mathrm{d}i_c/\mathrm{d}t = 0$—we obtain a 1-order differential equation after plugging the above relationships into Equations (2) + (3):

$$u_a = \left(\frac{R_1}{R_2} + \frac{2}{3}\right) u_{dc} + \frac{L}{R_2}\frac{\mathrm{d}u_{dc}}{\mathrm{d}t} \tag{5}$$

where $u_a = U_{an}\cos(\omega t + \varphi_0)$. The solution of the above equation is

$$u_{dc} = Ce^{-\tau} + U'\cos(\omega t + \varphi_0 - \varphi') \tag{6}$$

where

$$\tau = (2R_2 + 3R_1)/3L$$

$$U' = (R_2/\sqrt{X_L^2 + (R_1 + 2R_2/3)^2})U_{an}$$

$$\varphi' = \arctan(3X_L/(2R_2 + 3R_1))$$

Note that $C = 0$ and $\varphi_0 - \varphi' = -\pi/6$ in the steady-state process. Thus, the amplitude of the steady-state voltage can be estimated as

$$U_{dc} = \frac{R_2}{\sqrt{X_L^2 + \left(R_1 + \frac{2}{3}R_2\right)^2}} U_{an} \tag{7}$$

In a similar way, the amplitude of the steady-state current can be estimated as

$$I_{dc} = \frac{U_{an}}{\sqrt{X_L^2 + \left(R_1 + \frac{2}{3}R_2\right)^2}} \tag{8}$$

2.3. Transient-State Fault

The transient-state fault is more difficult to analyze than the steady-state fault. Based on the boost effect of the VSC, the voltage at the DC side is always higher than that of the AC side. Especially in the HVDC transmission system, the voltage of the DC side is much higher (like AC/DC is 0.392 kV/1.0 kV in [4]). Thus, all freewheel diodes will be blocked in stage 1 and each side will be isolated. Therefore, it is simple and reasonable to analyze this system in the 2nd-order circuit model. However, in the LVDC distribution system, the voltage of the DC side is not sufficiently high. As the analysis in Section 2.1, the fault should be analyzed using the 3rd-order circuit model.

In this paper, the transient-state fault process is divided into the natural response process and the forced response process. Compared to the transient fault current, the normal current is very small and

can be omitted. To simplify the analysis, the DC-side circuit is regarded as open. Thus, the transient fault corresponding circuits are shown in Figure 5.

Figure 5a is the circuit representing the natural response process. $R_1{}'$ and $L_1{}'$ are the equivalent parameters of the AC-side components. Two of the three-phase branches are always in parallel connection, connected with the remaining branch in series (circuit structure in Figure 4a). Thus, consider$R_1{}'$ and $L_1{}'$ to be equal to $1.5R_{ac}$ and $1.5L_{ac}$, respectively. R_2 and L_2 are the total parameters of the DC-side components. C is the parameter of DC-linked capacitance. The DC-linked capacitance discharges to each branch at the voltage of the operating value, $U_c(0)$. Figure 5b depicts the circuit representing the forced response process. Considering that the DC source is connected to the circuit at the moment of fault occurrence, the magnitude of the source can be equal to the step signal, the amplitude of which is derived from the output voltage of three-phase full-wave bridge circuit $2.34U_{p-p}$.

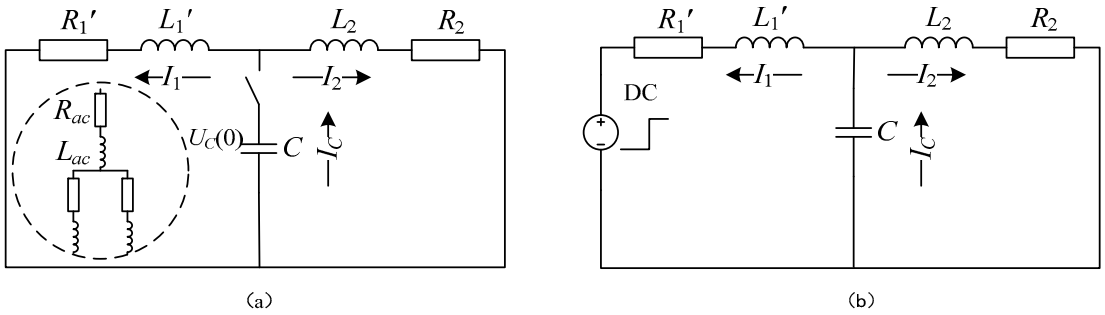

Figure 5. The equivalent transient-state circuit model of VSC: (**a**) the natural response process equivalent circuit; and (**b**) the forced response process equivalent circuit.

(1) Forced response of the transient-state fault:

The differential equations describing the circuit in Figure 5a are

$$U_{dc} = R_1{}'i_1 + L_1{}'\frac{\mathrm{d}i_1}{\mathrm{d}t} + u_c \tag{9}$$

$$u_c = R_2 i_2 + L_2\frac{\mathrm{d}i_2}{\mathrm{d}t} \tag{10}$$

$$-C\frac{\mathrm{d}u_c}{\mathrm{d}t} = i_1 - i_2 \tag{11}$$

According to Equations (9)–(11), the state equations are

$$\begin{bmatrix} u_c{}' \\ i_1{}' \\ i_2{}' \end{bmatrix} = Ax + Bu = \begin{bmatrix} 0 & -\frac{1}{C} & \frac{1}{C} \\ -\frac{1}{L_1{}'} & -\frac{R_1}{L_1{}'} & 0 \\ \frac{1}{L_2} & 0 & -\frac{R_2}{L_2} \end{bmatrix} \begin{bmatrix} u_c \\ i_1 \\ i_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L_1{}'} \\ 0 \end{bmatrix} U_{dc} \tag{12}$$

Applying Formula $|sI - A| = 0$, the characteristic equation can be obtained as follows:

$$CL_1L_2s^3 + C(L_1R_2 + L_2R_1)s^2 + (L_1 + L_2 + CR_1R_2)s + (R_1 + R_2) = 0 \tag{13}$$

where

$$k_1 = \frac{(L_1R_2 + L_2R_1)}{L_1L_2}$$

$$k_2 = \frac{(L_1 + L_2 + CR_1R_2)}{CL_1L_2}$$

$$k_2 = \frac{(L_1 + L_2 + CR_1R_2)}{CL_1L_2}$$

Thus, applying the radical formula for a cubic equation, a real root $s_1 = -\alpha_1$ and dual conjugate complex roots $s_{2,3} = -\alpha_2 \pm i \cdot \omega_2$ can be obtained as follows:

$$\alpha_1 = \sqrt[3]{\Delta} - \frac{3k_2 - k_1^2}{9\sqrt[3]{\Delta}} - \frac{k_1}{3} \tag{14}$$

$$\alpha_2 = -\frac{1}{2}(\sqrt[3]{\Delta} - \frac{3k_2 - k_1^2}{9\sqrt[3]{\Delta}}) - \frac{k_1}{3} \tag{15}$$

$$\omega_2 = \frac{\sqrt{3}}{2}(\sqrt[3]{\Delta} + \frac{3k_2 - k_1^2}{9\sqrt[3]{\Delta}}) \tag{16}$$

$$\Delta = \frac{k_1k_2}{6} - \frac{k_3}{2} - \left(\frac{k_1}{3}\right)^3 + \sqrt{[\frac{k_1k_2}{6} - \frac{k_3}{2} + \left(\frac{k_1}{3}\right)^3]^2 - [\frac{k_2}{3} + \left(\frac{k_1}{3}\right)^2]^3} \tag{17}$$

Hence, the analytic expression of the forced response surge current in Figure 4a is

$$I_2' = C_1\left(1 - e^{-\alpha_1 t}\right) + C_2 e^{-\alpha_2 t}\sin(\omega_2 t) + C_3 e^{-\alpha_2 t}\cos(\omega_2 t) \tag{18}$$

Under the initial conditions of $u_c = R_2 i_2 + L_2 i_2' = 0$, $I_2'(0) = 0$ and $dI_2'(0)/dt = 0$. Note that $I_2'(\infty) = U_{dc}/(R_1 + R_2)$. Thus, the constant terms $C_1 = U_{dc}/(R_1 + R_2)$, $C_2 = \alpha_1 U_{dc}/\omega_2(R_1 + R_2)$, $C_3 = 0$, and the final analytical expression of the forced response surge current is

$$I_2' = \frac{U_{dc}}{(R_1 + R_2)}(1 - e^{-\alpha_1 t} + \frac{\alpha_1}{\omega_2}e^{-\alpha_2 t}\sin(\omega_2 t)) \tag{19}$$

(2) Natural response of the transient-state fault:

The DC-linked capacitance discharges to two resistance-inductance (*R*-*L*) branches in the natural response circuit. An equivalent branch is adopted to replace the two RL branches as shown in Figure 6. Hence, the *RLC* circuit shown in Figure 6 simplifies the analysis.

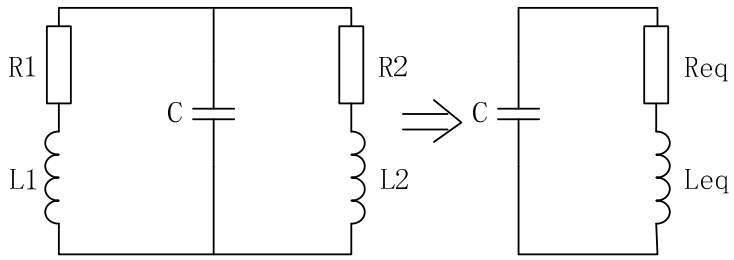

Figure 6. The equivalent convert of the RLC circuit.

Assuming that $Z_1 = R_1 + j\omega_2 L_1$ and $Z_2 = R_2 + j\omega_2 L_2$, the following equations can be obtained:

$$Z_{eq} = \frac{Z_1 Z_2}{(Z_1 + Z_2)} = R_{eq} + j\omega_2 L_{eq} \tag{20}$$

where

$$R_{eq} = (R_1R_2^2 + R_2R_1^2 + R_1(\omega_2 L_2)^2 + R_2(\omega_2 L_1)^2)/K$$

$$L_{eq} = (L_1{R_2}^2 + L_2{R_1}^2 + L_1(\omega_2 L_2)^2 + L_2(\omega_2 L_1)^2)/K$$

$$K = (\omega_2 L_1 + \omega_2 L_2)^2 + (R_1 + R_2)^2$$

Hence, the inherent frequency, attenuation coefficient and natural oscillation frequency of the above *RLC* circuit are $\omega_0 = \sqrt{1/L_{eq}C}$, $\alpha_0 = R_{eq}/2L_{eq}$ and $\omega_1 = \sqrt{\omega_0^2 - \alpha_0^2}$, respectively. Thus, the analytical expression of the natural response surge current in the capacitance branch is

$$I_C = \frac{U_{c0}}{\omega_1 L_{eq}} e^{-\alpha_0 t} \sin(\omega_1 t) \tag{21}$$

The current content is inversely proportional to the impedance of each *RL* branch. Thus, the analytical expression of the natural response surge current in the DC branch is

$$I_2{}'' = \frac{|Z_1| U_{c0}}{|Z_1 + Z_2| \omega_1 L_{eq}} e^{-\alpha_0 t} \sin(\omega_1 t) \tag{22}$$

Note that the above analytical results are reasonable under the circumstance of

$$\frac{R_2}{2L_2} \to \frac{R_1}{2L_1} \to \frac{R_{eq}}{2L_{eq}} \tag{23}$$

and error increases considerably if Equation (23) is unsatisfied.

(3) Computation of the complete response and the surge current:

The analysis presented above shows that the complete response of the short-circuit fault surge current equals the sum of the forced response surge current and the natural response surge current in an equivalent linear circuit

$$I_2 = \frac{U_{dc}}{(R_1 + R_2)}(1 - e^{-\alpha_1 t} + \frac{\alpha_1}{\omega_2} e^{-\alpha_2 t} \sin(\omega_2 t)) + \frac{|Z_1| U_{c0}}{|Z_1 + Z_2| \omega_1 L_{eq}} e^{-\alpha_0 t} \sin(\omega_1 t) \tag{24}$$

Theoretically, applying Equation (24), the peak value of the surge current can be calculated. Because the derivative of the current equals 0 at the time of the peak, the peak time can be obtained by

$$\frac{dI_2}{dt} = \frac{U_{dc}}{(R_1+R_2)}(\alpha_1 e^{-\alpha_1 t_p} + \frac{\alpha_1}{\omega_2}\sqrt{\alpha_2^2 + \omega_2^2} e^{-\alpha_2 t_p} \sin(\omega_2 t_p + \varphi_1)) + \frac{|Z_1| U_{c0} \sqrt{\alpha_0^2 + \omega_1^2}}{|Z_1 + Z_2| \omega_1 L_{eq}} e^{-\alpha_0 t_p} \sin(\omega_1 t_p + \varphi_1) = 0 \tag{25}$$

Thus, the peak value of the current can be obtained as $I_2(t_p)$.

3. Case Studies

Simulations were completed in PSCAD/EMTDC 4.5 (Manitoba HVDC Research Centre, Manitoba, Canada). The parameters of the low-voltage distribution network are shown in Table 1. The RMS of the AC side line voltage $U_{l-l} = 380$ V and phase voltage $U_{p-p} = 220$ V. Therefore, the DC voltage source in the equivalent circuit $U_{dc} = 513$ V. The cables adopt π-model parameters, and grounding capacitances are omitted.

Table 1. Simulation parameters and computed initial values.

System Components	Value	System Voltage	Value
AC-side Inductance L_{ac}	1.5 mH	Phase Voltage U_{p_p}	220 V
AC-side Resistance R_{ac}	0.3 Ω	Line Voltage U_{l_l}	380 V
DC-linked Capacitance C	6 mF	Equivalent DC Source U_{dc}	513 V
DC-side Inductance L_{dc}	0.56 mH/km	Initial DC voltage V_0	400 V
DC-side Resistance R_{dc}	0.12 Ω/km		

Figure 7 shows the comparison between the theoretical waveform1 obtained by Equation (24), theoretical waveform2 obtained by formulas in [4] and the simulated waveform of the surge current,

with a metal short-circuit fault occurring on 2 km of the whole cable. As the figure shows, nearly no errors are observed between the theoretical waveform1 and simulated waveform when the fault occurs with no resistance. However, considerable errors appear between the theoretical waveform2 and simulated waveform. The theoretical value is much lower than the simulated value, as the forced response from AC-side is omitted.

Table 2 shows the theoretical value, simulated value and the error when a metal short-circuit fault occurs over a different distance. Moreover, the theoretical value of the surge current includes a theoretical value obtained by Equation (24) (theoretical transient-state peak current1) and a theoretical value obtained by formulas in [4] (theoretical transient-state peak current2). As Table 2 shows, in the metal short-circuit fault case, current1 has little error, which is slightly higher than the simulated results. The simulated results demonstrate that the error is approximately 2%, and not more than 4%. Meanwhile, current2 is much lower than simulated results, and the error increases up to 15%. Note that the error increases with increasing fault distance. The error in the steady-state fault current decreases with increasing fault distance. The error is more than 5% within a fault distance of 3 km and less than 5% at a fault distance of 4 km or more. Moreover, the error of the steady-state fault current stabilized approximately 5%.

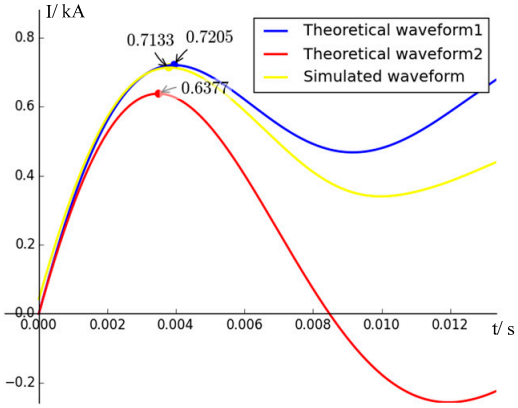

Figure 7. The waveform of the surge current of simulated values; theoretical values in [4] and this paper.

Table 2. Simulation parameters and computed initial values.

Fault Distance (km)	1	2	3	4	5
Simulation steady-state current (kA)	0.480	0.445	0.411	0.380	0.351
Theoretical steady-state current (kA)	0.513	0.471	0.433	0.398	0.368
Error (%)	6.78	5.88	5.33	4.85	4.75
Simulation transient-state peak current (kA)	1.078	0.713	0.556	0.464	0.402
Theoretical transient-state peak current1 (kA)	1.087	0.721	0.564	0.475	0.416
Error (%)	0.91	1.06	1.51	2.32	3.52
Theoretical transient-state peak current2 (kA)	0.994	0.638	0.486	0.398	0.339
Error (%)	7.75	10.56	12.67	12.62	15.59

4. Fault Location and Protection Coordination

4.1. Short-Circuit Fault Location and Analysis

Because the location method based on stage 1 in [4] is inaccurate, this paper proposed a fault location method adopting the amplitude of the steady-state fault current and the transient-state surge peak current based on the fault analyses presented above.

Referring to the simulation result and Equation (8), the value of the resistance on the DC side can be obtained. Due to the 5% computational error, 1.05-fold of the steady-state fault current should be plugged into Equation (8). The DC-side resistance R_x can be obtained as follows:

$$R_x = 1.5(\sqrt{\left(\frac{U_{am}}{1.05I_{dc}}\right)^2 - X_L^2} - R_1) \tag{26}$$

Based on the transient-state fault analysis, a function establishing a relationship among the DC-side resistance R_x, DC-side inductance L_x and transient-state surge peak current I_{peak} can be obtained as follows:

$$I_{\text{peak}} = f(R_x, L_x) \tag{27}$$

Obviously, L_x can be obtained when R_x and I_2 are given. Based on the linear relationship between L_x and fault distance d, a location result can be obtained.

The location results and errors of the proposed location method for different fault distances are shown in Table 3 at fault resistances of 0 and 0.05 Ω. The error increases with increasing fault distance and resistance. The method has high accuracy with an error less than 5% in the metal short-circuit fault case.

Table 3. Results for the proposed location method.

Fault Distance/m	**500**	**1000**	**1500**	**2000**	**2500**	**3000**
d/m ($R_f = 0$)	519	1015	1539	2054	2589	3130
Error (%)	0.63	0.50	1.30	1.80	2.97	4.33
d/m ($R_f = 0.5\ \Omega$)	579	1114	1653	2190	2769	3366
Error (%)	2.63	3.80	5.13	6.33	8.97	12.20

However, the error increases significantly in the non-metal short-circuit case due to the following causes: (i) dissatisfying the circumstance Equation (23) or (ii) the impedance of the DC side is much higher than that of the AC side. This can be explained as follows:

Note that I_{peak} is mainly supplied by natural response current I_2''. According to Equation (22), I_{peak} can be approximatively expressed as follows:

$$I_{\text{peak}} = K\frac{|Z_1|}{|Z_1 + Z_2|} \tag{28}$$

where K is regarded as constant.

Taking Equation (28)'s partial derivative respect to Z_2, the derivative function can be obtained as follows:

$$\frac{dI_{\text{peak}}}{dZ_2} = -K\frac{|Z_1|}{(Z_1 + Z_2)^2} \tag{29}$$

$$dZ_2 = -\frac{(Z_1 + Z_2)^2}{K|Z_1|}dI_{\text{peak}} \tag{30}$$

Equation (30) means that a small measured or computed error of I_{peak} will result in high deviation of Z_2 under the circumstance of $Z_2 \gg Z_1$. Therefore, the fault distance determined by Z_2 is inaccurate.

Moreover, according to Equation (30), the location error can be reduced by enlarging the value of Z_1. Thus, a limiter is installed at AC-side to reduce the error in Table 3. The limiter's parameters are $R_{limit} = 0.15\ \Omega$ and $L_{limit} = 0.75$ mH. The location results and errors are shown in Table 4. Obviously, the location error declines dramatically with the limiter installed. In addition, reliable measurement, monitoring and sensor devices are required for error elimination.

Table 4. Results for the improved proposed location method.

Fault Distance/m	500	1000	1500	2000	2500	3000
d/m ($R_f = 0$)	519	1012	1507	2016	2520	3032
Error (%)	0.63	0.40	0.23	0.53	0.67	1.07
d/m ($R_f = 0.5\ \Omega$)	536	1049	1564	2089	2620	3160
Error (%)	1.20	1.63	2.13	2.97	4.00	5.33

4.2. Coordination with the Handshaking Method

As analyzed above, the location method proposed has a higher error in a remote fault condition with high resistance. Thus, it has limited advantage when adopted as an independent location method. However, the biggest advantage of this method is easy to realize. The faults are rapidly located without any control and with small quantities of computation. Hence, it is more suitable for fast fault estimation and coordinate with other locations.

In [19], Tang and Ooi proposed a handshaking method for a location fault without any communications in the multi-terminal loop-type DC system. In this method, faults are located according to the following principles:

1. Disconnect all the sources;
2. Open the switches that carry the fault current from the bus to the line;
3. Reconnect all the sources; and
4. Re-close the switches with both of their poles connected to an energized bus.

This method can effectively locate and isolate the fault extent. However, too many switch operation times and limited selectivity are its disadvantages. For instance, a multi-terminal loop-type DC distribution network is operating as Figure 8 shows. The system parameters are the same as those shown in Table 1, and the length of each cable is 1 km. To ensure safety, the system is open-loop so S1 and S5 are opened. If a fault occurs as Figure 8 shows, according to principle 2 above, S3, S6, S8, S9 and S11 will be opened (Figure 9a). However, according to principle 4 above, only S1 is re-closed after all the sources are reconnected (Figure 9b). Obviously, the fault is located and isolated, but the power supply of load1 and load2 are interrupted.

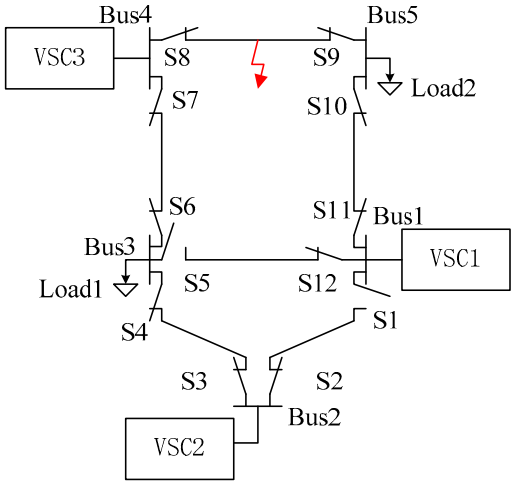

Figure 8. The structure of a multi-terminal loop-type DC distribution network.

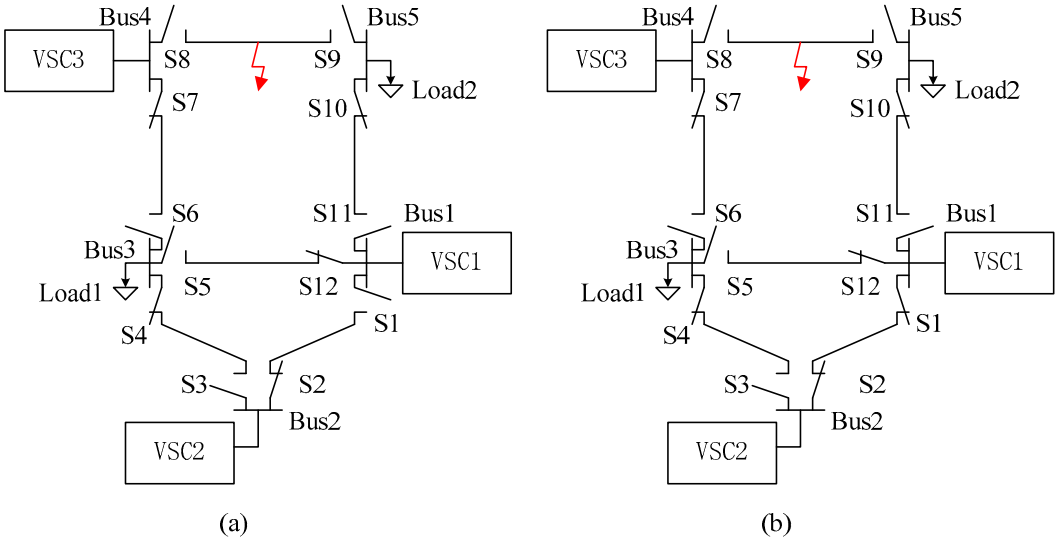

Figure 9. Switch operations of the classical handshaking method: (**a**) Switches state after step 2; (**b**) Switches state after step 4.

The handshaking method loses its selectivity because not all the buses are connected to a source. However, the location method proposed in Section 4.1 can be adopted to coordinate with the handshaking method to reduce switch operation times and ensure selectivity under this circumstance. The improved principles are as follows:

p1. Estimate the fault distance according to the current of each VSC branch;

p2. Determine if the operation instructions of switches connected to the same active bus with VSC should be blocked according to the estimated fault distance;

Then, the remaining switches operate as steps 1–4 of the original principles.

The criterion to block the switch operation instructions is $L_m < 1.2L_{min}$, where L_{min} is the minimal length of cables connected to active bus, and L_m is the fault distance calculated by the method proposed in Section 4.1. For instance, the same fault occurs in the DC system, and the peak currents of VSC are $I_{p1} = 0.850$ kA, $I_{p2} = 0.720$ kA and $I_{p3} = 1.470$ kA, respectively. According to Equations (26) and (27), the distances of the fault to VSC1, VSC2 and VSC3 are 1.45 km, 2.01 km and 0.63 km, respectively (Data in detail are given in appendices). According to step p2, the operation instructions of switches connected to Bus1 and Bus2 should be blocked. Thus, S1, S2, S3, S11 and S12 will not be opened or re-closed until the last step. The remaining switches S6, S8 and S9 will be opened according to step 2 (Figure 10a), and only S6 will be reclosed according to step 4 (Figure 10b).

Hence, switch operation times are reduced and selectivity is ensured after the handshaking method is improved by coordinating with the fault distance estimation.

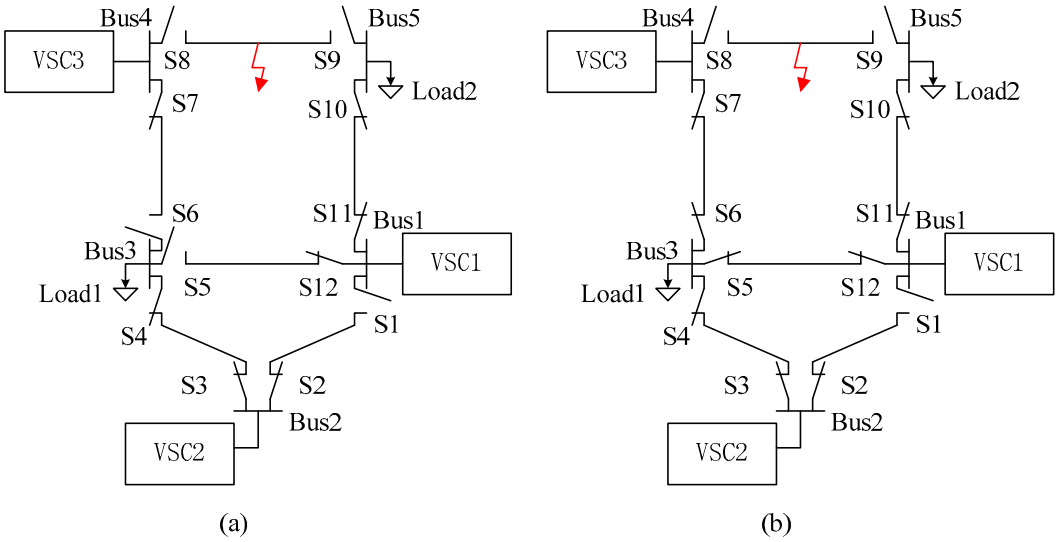

Figure 10. Switch operations of the improved handshaking method: (**a**) Switches state after step 2; (**b**) Switches state after step 4.

5. Conclusions

This paper identified the difference in fault analyses between the HVDC-VSC and LVDC-VSC systems. The steady-state fault analyses and the transient-state fault analyses considering forced response and adopting the 3rd-order circuit model are proposed. The new theories are in accordance with the line-to-line short-circuit fault characteristics in a LVDC distribution network based on a VSC. Simulation results demonstrate that the steady-state fault current and transient-state surge peak current can be computed through analytical expressions derived to describe the fault. Compared to the classical theories neglecting the forced response in [4], the analytical expressions in this paper have fewer errors and more significant implications for current limiter designs and fault locations. The proposed fault location method adopting steady-state and transient-state components is effective and meaningful in the case of line-to-line short-circuit faults. The reason for the increase in location error with increased fault distance and resistance is analyzed at the end of the paper, and the corresponding measure is proposed to improve the location accuracy effectively. For implementation in practice, the location method is adopted to coordinate with the handshaking method. Obviously, the improved method has decreased switch operation times and higher selectivity. Further research may lead to further method improvements to reduce location error.

Acknowledgments: This work was supported in part by the National Natural Science Foundation of China under Grant 51207103 and 51577129, by the Tianjin Municipal Natural Science Foundation under Grant 14JCYBJC21000 and by National High Technology Research and Development (863 program) under Grant 2015AA050102.

Author Contributions: Shi-Min Xue researched the fault analysis theories, fault location principle and drafted the article. Chong Liu provided the results of the simulation. Valuable comments on the first draft were received from Chong Liu. All the authors were involved in revising the paper.

Conflicts of Interest: The authors declare no conflicts of interest.

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