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Adaptive and Nonlinear Control Techniques Applied to SEPIC Converter in DC-DC, PFC, CCM and DCM Modes Using HIL Simulation

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Abstract: In this paper, we propose adaptive nonlinear controllers for the Single-Ended Primary Inductance Converter (SEPIC). We also consider four distinct situations: AC-DC, DC-DC, Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). A comparative analysis between classic linear and nonlinear approaches to regulate the control loop is made. Three adaptive nonlinear control laws are designed: Feedback Linearization Control (FLC), Passivity-Based Control (PBC) and Interconnection and Damping Assignment Passivity-Based Control (IDAPBC). In order to compare the performance of these control techniques, numerical simulations were made in Software and Hardware in the Loop (HIL) for nominal conditions and operation disturbances. We recommend adaptive controllers for the two different situations: Adaptive Passivity-Based Feedback Linearization Control (APBFLC) for the PFC (Power Factor Correction) AC-DC system and IDAPBC-BB (IDAPBC Based on Boost converter) for the regulator DC-DC system.

Keywords: SEPIC; PFC; CCM; DCM; FLC; PBC; IDAPBC; HIL; APBFLC; IDAPBC-BB

1. Introduction

Conventional power supplies usually only have one full-bridge diode rectifier and one large capacitive filter in the input stage. This front-end circuit operates with a high Total Harmonic Distortion (THDi) in the grid current, a low power factor (0.5–0.7) and normally does not meet regulatory standards, such as the important international standard IEC 61000-3-2 [1]. Among the possible alternatives to improve the performance of switched sources, a highlight is the use of a DC-DC converter to creation a Power Factor Correction (PFC) system. As shown in Figure 1, this solution makes it possible to build nearly ideal rectifiers (emulates a resistor) and still achieve voltage, current or power regulation.

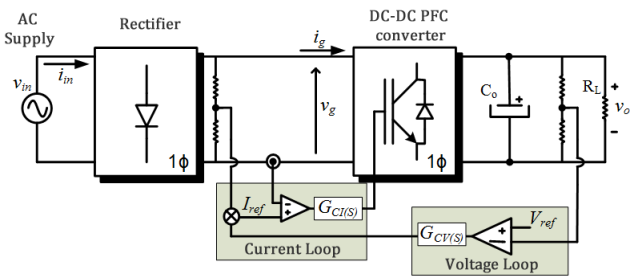

Figure 1. Schematic diagram of the DC-rectification system with the power factor correction stage.

Several topologies of converters used in power factor correction are present in the literature [2,3]. Among them, the most popular topology is the boost converter [4,5]. However, this converter has some disadvantages:

- Relatively high output voltage (at least equal to the AC source voltage), which can generate over-voltage stress in the switches;
- Difficulty in implementing insulation between input and output;
- Lack of overload and over-current control due to the absence of a serial switch between the input and the output;
- Inability to start-up.

However, the CUK and SEPIC topologies overcome these drawbacks presented by the boost converter, which becomes a good choice in PFC applications. In time, SEPIC converters have attracted much attention from modern applications, especially those involving renewable energy [6] such as LED (Light Emitting Diode) [7,8], fuel cells [9], battery chargers [10], photovoltaics [11] and eolic systems [12,13].

In this work, the operation characteristics, the modeling and control system of the SEPIC PFC converter in CCM and DCM are presented. Initially, a comparative analysis between two control techniques will be performed for this converter. The first one deals with the Classical Linear Control (CLC) based on the small-signal model, and the other is based on the Feedback Linearization Control (FLC) approach. Next, we suggest a new nonlinear controller, which works around the drawbacks of the CLC and FLC methods. The proposed control law, explained in the dedicated section, we call Adaptive Passivity-Based Feedback Linearization Control (APBFLC).

In order to analyze the operation of the SEPIC PFC converter, numerical simulations were performed in software for both the nominal condition and disturbances in the operation of this converter, by analyzing the Power Factor (PF) on the AC side, the harmonic distortion (THDi) of the input current and the DC side voltage regulation.

We list the main contributions of this paper:

- a comparative analysis between linear and nonlinear control;
- the proposal of an adaptive nonlinear control without current measurement in the intermediate inductor and with low harmonic distortion: APBFLC;
- recent IDAPBC methods adapted from the boost converter adjusted to the SEPIC converter with very low overshoot in view of load disturbances: IDAPBC-BB;
- HIL simulation of nonlinear control techniques applied to DC-DC SEPIC in CCM mode.

This work is organized as follows. Section 2 introduces the modeling and analysis of the converters in CCM and DCM. The description of the design and the control techniques implemented for the PFC system, as well as the control law for DC-DC are shown in Section 3. Section 4 presents the proposed APBFLC controller. Section 5 includes the adaptation of new and efficient boost control laws to SEPIC converters. Section 6 demonstrates and discusses the main simulations and the HIL experimental results. Finally, in Section 7, the final comments and conclusions are presented.

2. Modeling

The PFC and DC-DC SEPIC converter circuits are illustrated in Figure 2. Based on [14,15], the average State-Space Model (SSM) and Euler–Lagrange Model (ELM) are presented in Table 1. Note that i_{L1} and i_{L2} are the average currents in the inductors L_1 and L_2, v_{C1} is the capacitor voltage C_1, v_o is the output voltage across the capacitor C_o, d is duty cycle, G is the load conductance and v_g is the input voltage. Note in Table 1 that the differences between the two conduction modes basically consist of the residual term presented in the states representing the inductors currents ($I_{sig} = 0$ for CCM and $I_{sig} \neq 0$ for DCM).

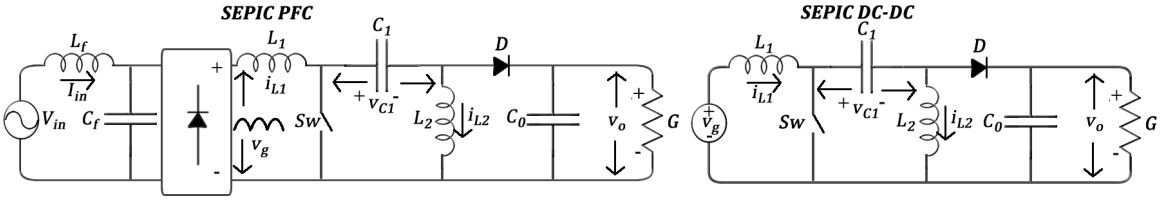

Figure 2. SEPIC PFC and SEPIC DC-DC.

Table 1. Converter models.

	SEPIC CCM	**SEPIC DCM**
SSM	$L_1\dot{i_{L1}} = v_g - (1-d)(v_o + v_{C1})$ $C_o\dot{v_o} = (1-d)(i_{L1} + i_{L2}) - Gv_o$ $L_2\dot{i_{L2}} = dv_{C1} - (1-d)v_o$ $C_1\dot{v_{C1}} = (1-d)i_{L1} - di_{L2}$	$L_1\dot{i_{L1}} = v_g - (1-d)(v_o + v_{C1}) + (1-d).\frac{L_1}{L_1+L_2}(v_g - v_{c1})$ $C_o\dot{v_o} = (1-d)(i_{L1} + i_{L2}) - Gv_o$ $L_2\dot{i_{L2}} = dv_{C1} - (1-d)v_o - (1-d)\frac{L_2}{L_1+L_2}(v_g - v_{c1})$ $C_1\dot{v_{C1}} = (1-d)i_{L1} - di_{L2}$
ELM	$D_B\dot{x} + [(1-d)J_{B1} + dJ_{B2}]x + R_Bx = F$ $z = \begin{bmatrix} i_{L1} \\ v_o \\ i_{L2} \\ v_{C1} \end{bmatrix}$; $D_B = \begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & C_o & 0 & 0 \\ 0 & 0 & L_2 & 0 \\ 0 & 0 & 0 & C_1 \end{bmatrix}$; $R_B = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$; $F = \begin{bmatrix} v_g \\ 0 \\ 0 \\ 0 \end{bmatrix}$; $I_{sig} = \begin{bmatrix} 1 \\ 0 \\ -1 \\ 0 \end{bmatrix}$ $J_{B1} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ -1 & 0 & -1 & 0 \\ 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix}$; $J_{B2} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & 0 \end{bmatrix}$	$D_B\dot{x} + [(1-d)J_{B1} + dJ_{B2}]x + R_Bx = F + \frac{(1-d)}{L_1+L_2}(v_g - v_{c1})D_BI_{sig}$

2.1. CCM and DCM Analysis

The operation details of the SEPIC converter in DCM, illustrated in Figure 3, outline three mode configurations, which depend on the states of the semiconductor switch S and the diode D. The third configuration (c) represents the discontinuous operation mode, which is characterized by the annulment of the current drained through the diode. This is due to the inversion in one of the inductor currents of the converter, which will also equal in intensity the current of the other inductor; so the sum of these currents $(i_{L1} + i_{L2})$ will become zero during a short time interval. If the sum of these currents is always greater than zero $(i_{L1} + i_{L2}) > 0$ over the entire span where the switch remains open, there will be a current across the diode, and only the configurations (a) and (b) will be observed, which will represent the operation of the converter in continuous mode.

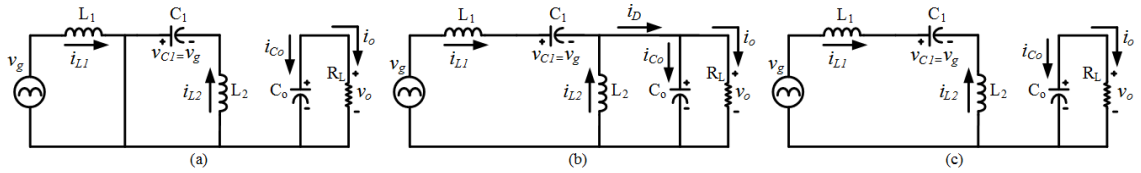

Figure 3. Electrical configuration of the SEPIC DCM converter operation: (**a**) closed switch; (**b**) open switch and diode conduction; and (**c**) open switch and blocked diode.

According to [14], the operation of the SEPIC converter in DCM can be analytically represented by (1), where S_Q and $\theta_{L_1+L_2}$ are the switching and the threshold functions, respectively. These functions of the switch model are presented in (2) and (3), where $z = i_{L1} + i_{L2}$. In addition, $\overline{S}_Q$ and are their respective complements.

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = S_Q \cdot v_g + \overline{S}_Q \cdot \theta_{(z)} \cdot (v_g - v_{c1} - v_o) + \overline{S}_Q \cdot \overline{\theta}_{(z)} \cdot \frac{L_1}{L_1+L_2} \cdot (v_g - v_{c1}) \\ L_2 \frac{di_{L2}}{dt} = S_Q \cdot v_{c1} - \overline{S}_Q \cdot \theta_{(z)} \cdot v_o - \overline{S}_Q \cdot \overline{\theta}_{(Q)} \cdot \frac{L_2}{L_1+L_2} \cdot (v_g - v_{c1}) \\ C_1 \frac{dv_{C1}}{dt} = \overline{S}_Q \cdot i_{L1} - S_Q \cdot i_{L2} \\ C_o \frac{dv_o}{dt} = \overline{S_Q} \cdot \theta_{(z)} \cdot (i_{L1} + i_{L2}) - i_o \end{cases} \quad (1)$$

$$S_Q = \begin{cases} 0, close\ switch \\ 1, open\ switch \end{cases} \quad (2)$$

$$\theta(z) = \begin{cases} 0, se\ z \leq 0 \\ 1, se\ z > 0 \end{cases} \quad (3)$$

Let us derive the state-space averaging approach of (1), considering the DCM SEPIC converter operation, to obtain:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = v_g - (1-d) \cdot (v_{c1} + v_o) + (1-d) \cdot \frac{L_1}{L_1+L_2}(v_g - v_{c1}) \\ C_o \frac{dv_o}{dt} = (1-d) \cdot (i_{L1} + i_{L2}) - i_o \\ L_2 \frac{di_{L2}}{dt} = d \cdot v_{c1} - (1-d).v_o - (1-d) \cdot \frac{L_2}{L_1+L_2} \cdot (v_g - v_{c1}) \\ C_1 \frac{dv_{C1}}{dt} = (1-d) \cdot i_{L1} - d \cdot i_{L2} \end{cases} \quad (4)$$

where d is the duty cycle of the semiconductor switch. According to [16], the average output current of the SEPIC converter in DCM for a half cycle of the AC line and the AC current grid can be written, respectively, as follows:

$$I_o = \frac{V_{in}^2 D^2 T_S}{4 L_{eq} v_o} \quad (5)$$

$$i_{in} = I_{in} sin(wt) \quad (6)$$

where L_{eq} is the equivalent inductance derived from the parallel association of the inductors and I_{in} is given by:

$$I_{in} = \frac{V_{in} D^2 T_S}{2 L_{eq}} \quad (7)$$

2.2. PFC Converter Characteristics

In power factor correction applications (AC-DC), as shown in Figure 4, the input voltage and current can be described by:

$$v_g = V_{in} |sin(wt)| \quad (8)$$

$$i_{L1} = I_{in} |sin(wt)| \quad (9)$$

where V_{in} and I_{in} are the amplitude values of these input quantities and w is the angular frequency. Note that for a DC-DC system, the input v_g is constant.

On the other hand, the output voltage v_o remains practically constant throughout each half cycle due to the presence of the large output capacitor C_o. Hence, this voltage can be approximated by a constant value $v_o \simeq V_o$.

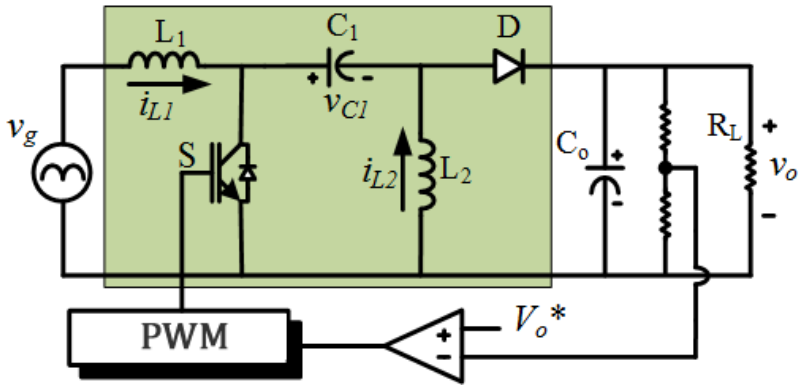

Figure 4. Schematic of the SEPIC PFC converter.

In addition, the PFC converter operates under very special conditions where the nominal DC voltage transformation m_{wt} and the load r_{wt} "seen" by the converter, at each period, are given by:

$$m(wt) = \frac{v_o}{v_g} \simeq \frac{V_o}{V_{in}|sin(wt)|} = \frac{M}{|sin(wt)|} \tag{10}$$

$$r(wt) = \frac{R}{2sin^2(wt)} \tag{11}$$

where these quantities periodically vary from a minimum value M and $R/2$ ($wt = \pi/2$) to infinity ($wt = k\pi$, with $k = 0, 1, 2, 3, ...$) in each half cycle of the grid frequency. Such features extend to any type of DC-DC converter used as PFC.

2.3. CIECA Modeling

The CIECA approach (Current Injected Equivalent Circuit Approach), proposed by [17], works to simplify the DCM SEPIC modeling taking into account some desired characteristics:

- Simple, clear, works in both continuous and discontinuous conduction mode (CCM or DCM);
- Can produce a well-suited approximated version of a real converter;
- The equivalent circuit can be used directly in digital software simulators (SPICE, MATLAB, PSIM and others).

In the CIECA design procedure, the first step is to identify the nonlinear part of the converter circuit (containing the switch). The second is the linearization, which is done through the average current. This fact makes simple the application of this approach, and the final result of the modeling becomes a set of small-signal equations. Therefore, a linear equivalent circuit model for the nonlinear converter is sketched in Figure 5, representing the transfer ratios of the converter. The CIECA modeling can be applied to CLC control.

The dynamic properties of the converter are determined from an introduction of an AC small-signal variation on the steady-state operating point, where the small signal values are considered to be much smaller than the quiescent values: $d = \overline{D} + \tilde{d}$, $V_{in} = \overline{V}_{in} + \tilde{v}_{in}$, $v_o = \overline{V}_o + \tilde{v}_o$, $I_{in} = \overline{I}_{in} + \tilde{i}_{in}$ and $i_o = \overline{I}_o + \tilde{i}_o$, where "$-$" indicates the steady-state value and "$\sim$" represents the small-signal disturbance introduced.

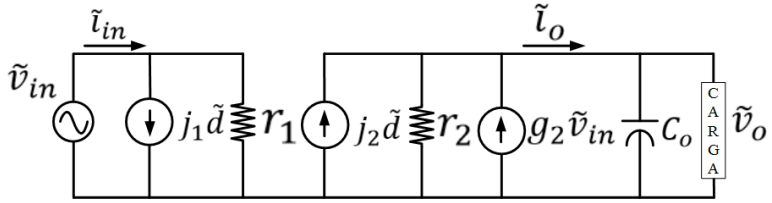

Figure 5. Equivalent small-signal circuit of the SEPIC PFC.

Applying these disturbances in (5), which shows the value of the output current, and upon eliminating nonlinear second-order terms, this leads to:

$$\tilde{i}_o = j_2\tilde{d} + g_2\tilde{v}_{in} - \frac{1}{r_2}\tilde{v}_o \tag{12}$$

where: $j_2 = \frac{\overline{V}_{in}^2}{\overline{V}_o}\frac{\overline{D}T_S}{2L_{eq}}$, $g_2 = \frac{\overline{V}_{in}}{\overline{V}_o}\frac{\overline{D}^2T_S}{2L_{eq}}$ and $r_2 = \frac{\overline{V}_o}{\overline{I}_o}$.

Using these same perturbations in (7), we have:

$$\tilde{i}_{in} = j_1\tilde{d} + \frac{1}{r_1}\tilde{v}_{in} \tag{13}$$

where: $j_1 = \frac{\overline{V}_{in}\overline{D}T_S}{L_{eq}}$ and $r_1 = \frac{2L_{eq}}{\overline{D}^2T_S}$.

The expressions (12) and (13) represent the model of small low-frequency signals of the SEPIC converter. They are also used to obtain the equivalent small-signal circuit, illustrated in Figure 5. From this equivalent circuit, the desired transfer functions of the SEPIC converter can be obtained. In addition, it should be noted that the equivalent small signal impedance of the load (Z_{load}) directly depends on the load to which the PFC converter is connected. In this case, making use of a purely resistive load (R_L), the equivalent small signal impedance shall be considered equal to the load itself, i.e., $Z_{load} = R_L$.

3. Control System

Several control techniques for switched converters are presented in the literature. In this work, an initial comparison is made between two of them: the traditional approach, using a Proportional-Integral (PI) controller and the nonlinear technique based on FLC (Feedback Linearization Control). A generalized procedure for both linear and non-linear control is shown in Figure 6. The complementary flowchart, sketched in Figure 7, outlines important observations:

- CLC needs CIECA modeling (Section 3.1);
- FLC and PBC employ SSM and ELM models, respectively;
- The APBFLC control (Section 4) incorporates the advantages of FLC and PBC. The integral action used in the classical control can also be added.
- The IDAPBC-BB control (Section 5) is obtained through the simplified modeling based on the boost converter and the IDABPBC control, which utilizes the Port-Controlled Hamiltonian (PCH) model (Appendix B);

When considering the classic control system of the PFC converters, there are two main methods: the multiplicative and the follower voltage, portrayed in [16]. In the case of SEPIC PFC in DCM mode operation, there is an inherent characteristic that simplifies and establishes the control system, explained in the following subsection.

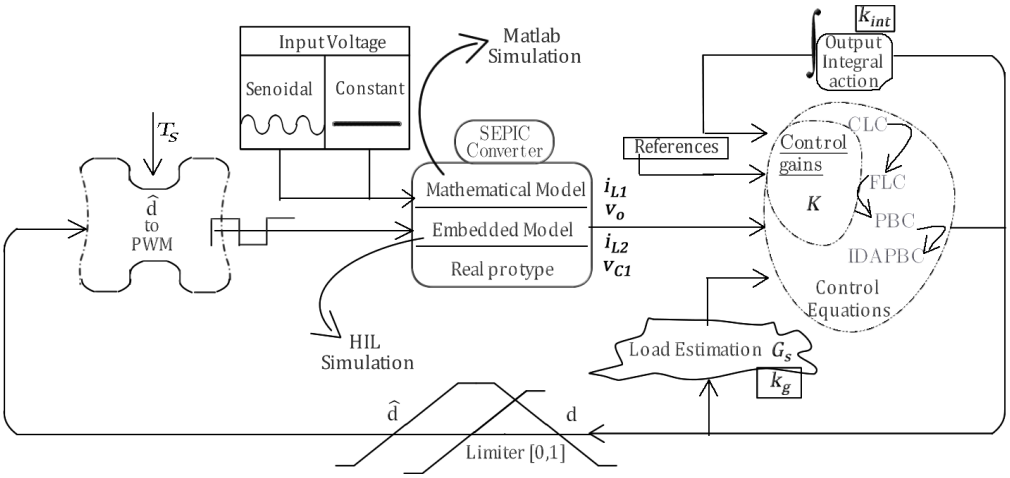

Figure 6. Standard control procedure. The control goal is to get the equation for d. With the signal of the duty cycle synthesized, it is necessary to limit it between zero and one, and then, the corresponding PWM (Pulse Width Modulation) signal is produced for input to the converter. Therefore, it is necessary to estimate the value of the load represented by G_s and add an integral action.

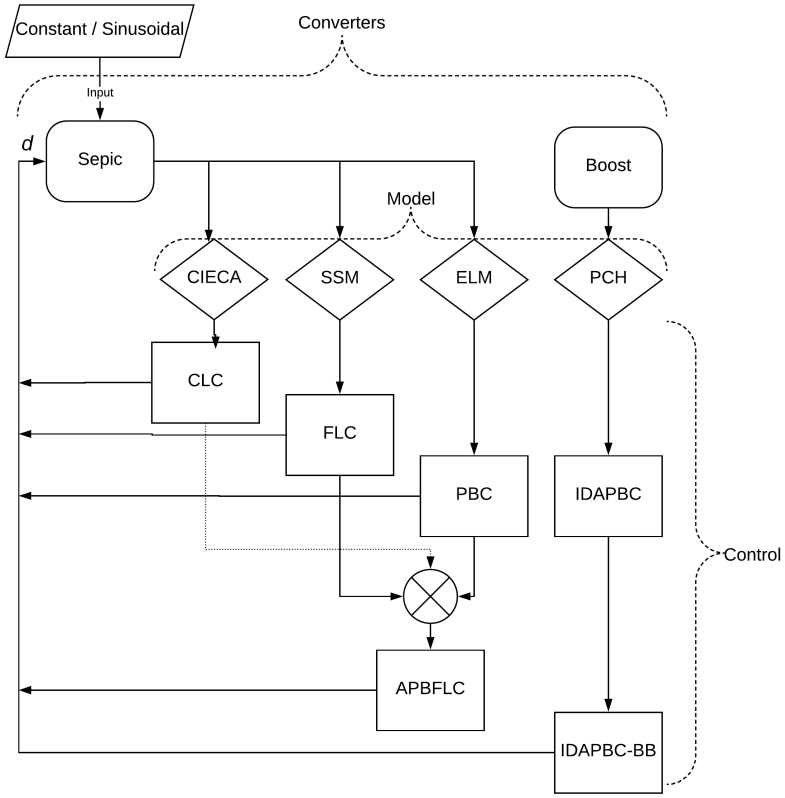

Figure 7. Flowchart of the methods used in this work.

3.1. Classic Control

In the traditional linear approach, the control system is reduced to a single voltage loop, which is sketched in Figure 4. This control system can also be represented in the form of block diagrams of Figure 8, where the SEPIC converter and the PWM controller (Pulse-Width Modulation) are replaced by their respective transfer functions: $G_{vd(s)}$ and $G_{C(s)}$. The other elements correspond to the amplitude of the triangular wave V_M and voltage sensor gain $H_{(s)}$.

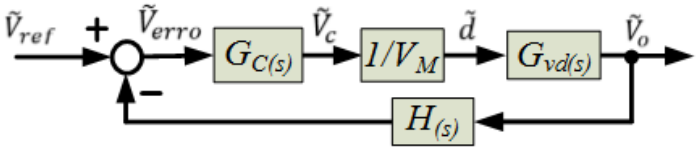

Figure 8. Block diagram of the control system in voltage mode.

The voltage-proportional-integral PWM controller is designed using the classical frequency domain technique presented in [18]. The transfer function $G_{vd(s)}$ relates the output voltage to the duty cycle, obtained from the small-signal equivalent circuit of the Figure 5, as follows:

$$G_{vd(s)} = \frac{j_2}{C_o s + \left(\frac{1}{r_2} + \frac{1}{R_L}\right)} \tag{14}$$

In addition, this classical PI controller adjustment is based on the definition of the transfer function $T_{(s)}$, which is given by:

$$T_{(s)} = H_{(s)} G_{C(s)} G_{vd(s)} / V_M \tag{15}$$

3.2. Feedback Linearization Control

In the case of the FLC technique, there is a linearization of the nonlinear dynamics of the system by state feedback, which is applied to the entire domain of the state space except for some singular points, so, it is global. Thus, this approach differs from linearization in the neighborhood of an equilibrium point, which was used to construct the equivalent model of Figure 5.

The design of the control system in the FLC approach is performed including a variable change, which shows the structure of the designed controller [14]. In addition, the control law is based on the knowledge of the average converter model, which was presented in (4). In relation to this model, it is observed that the system presents a unity relative degree. This fact makes possible the derivation of the current control law from the first equation of this average model:

$$d = \frac{(L_1 v_i - v_g)(L_1 + L_2)}{(L_1 + L_2)(v_{c1} + V_o) + L_1(v_{c1} - v_g)} + 1 \tag{16}$$

which:

$$d = \frac{1}{2}\left(1 + \frac{u_i}{V_M}\right) \tag{17}$$

where u_i is the output of the FLC controller, V_M corresponds to the amplitude of the triangular wave and v_i is the new variable, given by:

$$v_i = \frac{i_{L1}^*}{dt} - \frac{K}{L_1}(i_{L1} - i_{L1}^*) \tag{18}$$

In turn, the reference current i_{L1}^*, whose amplitude was defined in (7), is represented by:

$$i_{L1}^* = I_{in}|sin(wt)| \tag{19}$$

In addition, due to possible regime errors caused by the parametric uncertainties and in order to regulate the output voltage at the desired value V_o^*, it is necessary to introduce an integral action, which is represented as follows:

$$V_o = -K_{int} \int_0^t (v_o - V_o^*)\, dt \tag{20}$$

Finally, Figure 9 shows the control system in the FLC approach, where the function T represents the relation between the auxiliary variable v_i and the controller output u_i. Such a function can be obtained by solving the expressions (16)–(18). FLC and PBC control equations for CCM and DCM SEPIC are summarized in Table 3. Note that PBC has the same first Equation (16) and three morestate equations.

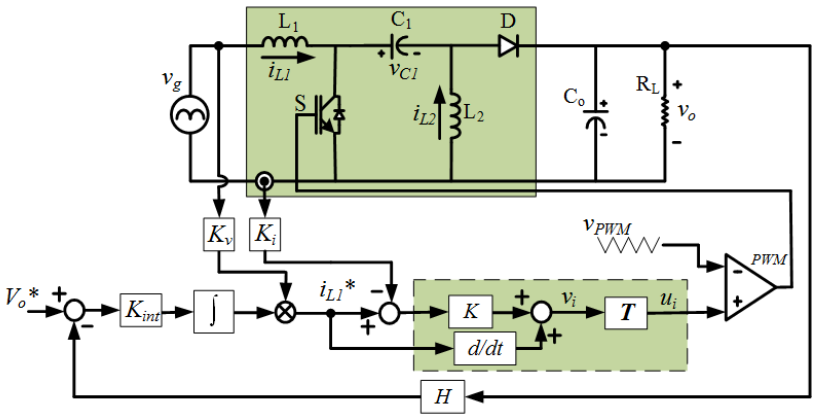

Figure 9. FLC control in block diagrams.

3.3. Numerical and Initial Implementations for SEPIC DCM PFC

The reactive power elements of SEPIC is presented in Appendix A. An important quantity to be calculated is the transfer function $G_{vd(s)}$ shown in (14), which is given numerically by:

$$G_{vd(s)} = \frac{400}{0.016S + 1} \tag{21}$$

where: $j_2 = 8.06$ and $r_2 = 99.20$.

This transfer function has great importance for the control loop adjustment in the classical approach, which must be sufficiently slow in order to avoid the injection of the second harmonic of the output in the input current. In this case, an expressive third order harmonic component can appear. As suggested in [19,20], it is necessary to allocate the crossover frequency of the control at least three times less than the AC input frequency, which makes the control system naturally slow.

Again, the PI controller was tuned using the classical frequency domain technique. The characteristics of this control system are shown in Table 2 together with the FLC control parameters. The next step is to analyze the AC side Power Factor (PF), the Total Harmonic Distortion of the input current (THDi) and the DC side voltage regulation in the simulated system for both the nominal condition and operation disturbances.

Table 2. Control system specifications.

Parameters	Value	Unity
Triangular wave ampl.(V_M)	1	V
Voltage sensor gain (H)	0.05	–
Proportional gain ($K_{p,PI}$)	0.2	–
Integral gain ($K_{i,PI}$)	10	–
Scalar (K_v) gain	1/180	–
Scalar (K_i) gain	1	–
FLC control gain (K)	40,000	–
Integral FLC gain (K_{int})	40	–

The first analysis considers the operation of the full load converter (100 W), as shown in Figure 10a. In this figure, it is possible to observe the power factor correction characteristic of the SEPIC PFC

converter, which has a high power factor (*Linear*—0.9975, *FLC*—0.9971), low harmonic content (*Linear*—6.33%; *FLC*—7.60%) and is still able to maintain the output voltage at the reference of 100 V within the limits imposed by the design. The low harmonic content of the input current is evidenced in the spectral analysis shown in Figure 11, where it is noted that the values obtained in the two control approaches are far below the limits imposed by the IEC 61000-3-2, Standard Class C.

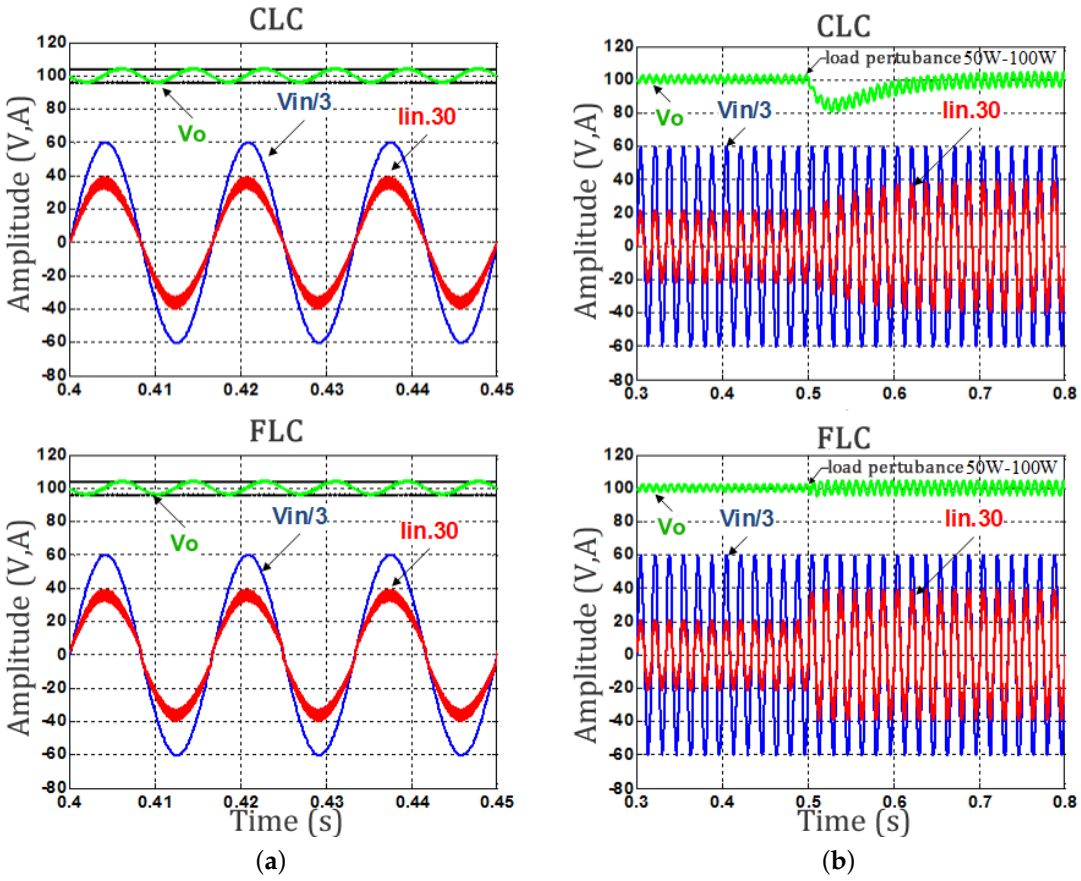

Figure 10. (**a**) Steady-state. Full-load operation (100 W) and (**b**) transient. Transient response to a load variation (50–100 W).

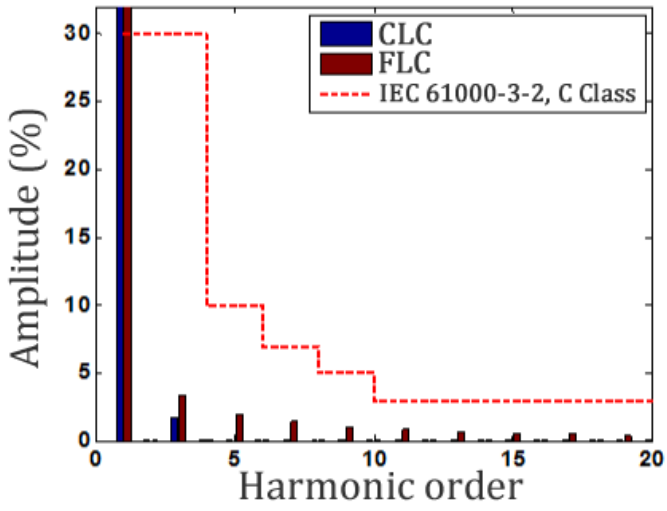

Figure 11. Comparison of the harmonic current with the limits imposed by IEC 61000-3-2.

It can be seen from Figure 10b that the dynamic behavior of the SEPIC converter is able to regulate the output voltage in both control strategies, although it takes different times to achieve this regulation, for a load variation of 50 W–100 W. In the case of the linear approach, the SEPIC converter spends approximately 120 ms to perform the voltage regulation, allowing that voltage to decrease by approximately 20 V. On the other hand, the converter has been able to regulate this output voltage in less than one grid cycle in the FLC approach. In addition, in the nonlinear technique, an overvoltage or current signal is not verified in the voltage regulation, surpassing the linear approach in this discussion point.

Finally, an analysis of the power factor and harmonic distortion of the AC input current is performed for both the universal input voltage values (90–265 V peak) at full load (100 W) and for different values of the load connected to the SEPIC converter. The first one is presented in Figure 12a and shows that the converter has a high power factor and low harmonic content in the AC current along the entire voltage range of the universal input in both methods. However, it is noted that the linear technique presents a slight superiority in this test.

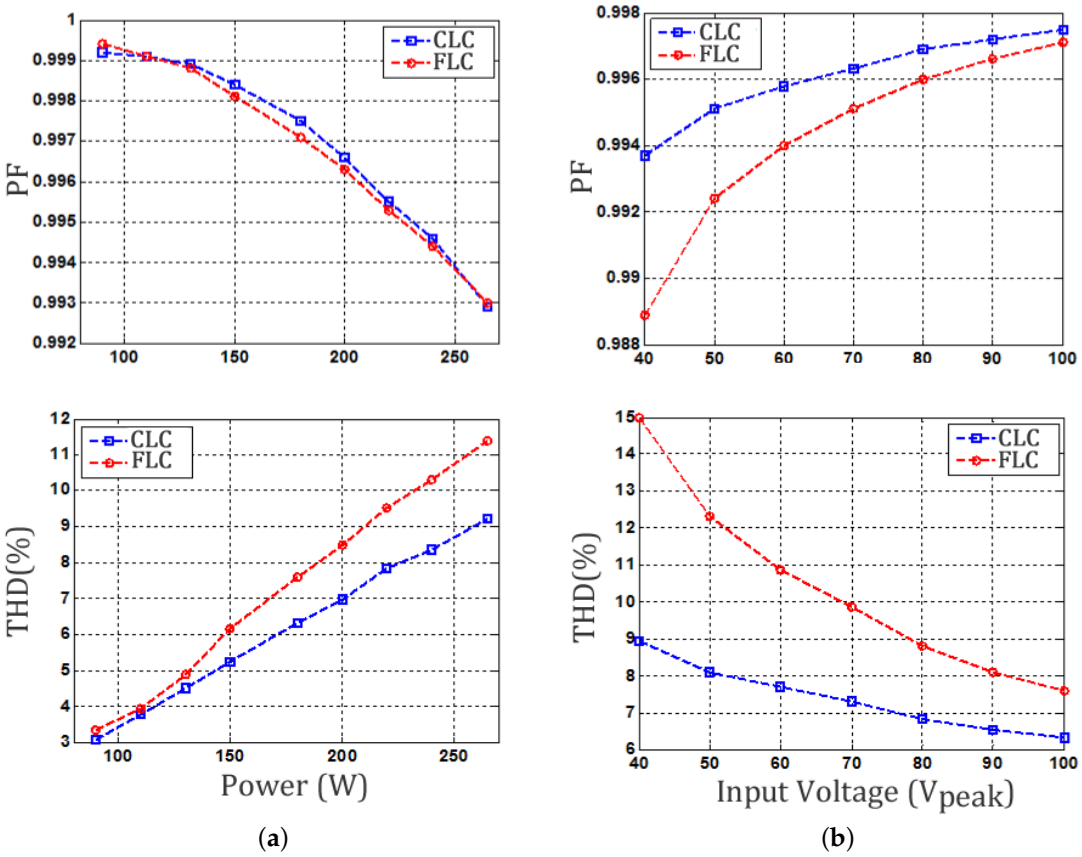

Figure 12. Power factor and Total Harmonic Distortion (THD) for: (**a**) universal input voltage. Universal input voltage (90–265 V) and (**b**) load variation. Different load values.

The other analysis is presented in Figure 12b, and again, the converter is able to maintain a high power factor and low harmonic content in both control approaches, now for different load values. In addition, it is observed that there is a more evident superiority of the linear approach in this last analysis to the different values of the load, which can be explained by the distortion in the waveform of the current in the passage through zero due to the presence of a derivative action in the FLC methodology.

4. Proposed Adaptive Non Linear Control Law

The two control laws discussed above, both linear and non-linear, have some drawbacks, which will be discussed below. First, for the classic controller shown in Figure 7, the control structure directly depends on the output signal of a voltage error amplifier (which contains a second harmonic component) and the input rectified sine wave voltage. As explained in [20], the linear controller ends up leading to higher levels in the third harmonic of the input current. To minimize this aggravating factor, the control loop is intentionally slow. The other disadvantage is the restriction at the operation point of the system since linearization is local around the equilibrium point. It should also be added that linear control works for DCM mode; the same performance does not occur in CCM mode.

The FLC control presents a major practical implementation problem: it needs the known value of the load G. Note that (7) depends on the desired current value in the primary inductor, which in turn depends on the value of G. Figure 11 shows this deficiency in the FLC control. In view of these two major disadvantages, we propose the following adaptive control law based on the passivity-based control and feedback linearization control Table 3, which we call APBFLC.

Table 3. FLC and PBC control equations in CCM and DCM SEPIC.

	SEPIC CCM	**SEPIC DCM**
FLC	$d = \frac{\left[L\dot{i}^*_{L1} - k_1(i_{L1} - i^*_{L1}) + V_o + V_{c1} - v_g\right]}{V_o + V_{c1}}$	$d = \frac{(L_1 v_i - v_g)(L_1 + L_2)}{(L_1 + L_2)(v_{c1} + V_o) + L_1(v_{c1} - v_g)} + 1$
PBC	$d = \frac{\left[L_1\dot{i}^*_{L1} - k_1(i_{L1} - i^*_{L1}) + V^*_o + v^*_{c1} - v_g\right]}{v^*_o + v^*_{c1}}$ $\dot{v}^*_o = \frac{1}{C_o}\left((1-d)(i^*_{L1} + i^*_{L2}) - Gv^*_o + k_2(v_o - v^*_o)\right)$ $\dot{i}^*_{L2} = \frac{1}{L_2}\left(d\left(v^*_o + v^*_{c1}\right) - v^*_o + k_3\left(i_{L2} - i^*_{L2}\right)\right)$ $\dot{v}^*_{c1} = -\frac{1}{C_1}\left(d\left(i^*_{L1} + i^*_{L2}\right) - i^*_{L1} - k_4\left(v_{C1} - v^*_{c1}\right)\right)$	$d = \frac{(L_1 v_i - v_g)(L_1 + L_2)}{(L_1 + L_2)(v^*_{c1} + v^*_o) + L_1(v_{c1} - v_g)} + 1$ $\dot{v}^*_o = \frac{1}{C_o}\left((1-d)(i^*_{L1} + i^*_{L2}) - Gv^*_o + k_2(v_o - v^*_o)\right)$ $\dot{i}^*_{L2} = \frac{1}{L_2}\left(d\left(v^*_o + v^*_{c1}\right) - v^*_o + k_3(i_{L2} - i^*_{L2}) - \left((1-d).\frac{L_2}{L_1+L_2}.(v_g - v^*_{c1})\right)\right)$ $\dot{v}^*_{c1} = -\frac{1}{C_1}\left(d\left(i^*_{L1} + i^*_{L2}\right) - i^*_{L1} - k_4\left(v_{C1} - v^*_{c1}\right)\right)$
AC-DC	$v_g = v_{g_{max}}\left\|sin\left(wt + \phi\right)\right\|$, $i^*_{L1} = I_d\left\|sin\left(wt + \phi\right)\right\|$, $\dot{i}^*_{L1} = I_d w cos\left(wt + \phi\right) sgn\left(sin\left(wt + \phi\right)\right)$	
DC-DC	$\dot{i}^*_{L1} = 0$ and $i^*_{L1} = I_d$	
Load estimation	$\dot{\hat{G}}_s = -k_g v^*_o\left(v_o - v^*_o\right)$ or $\widehat{G_s} = \frac{i_o}{v_o}$	
Integral action	$G_{Int} = -k_{int}\int_0^t \left(v_o\left(s\right) - V^*_o\right) ds$	

$$v_i = \frac{i^*_{L1}}{dt} - \frac{K_1}{L_1}(i_{L1} - i^*_{L1}),$$

$$DCM : d = \frac{(L_1 v_i - v_g)(L_1 + L_2)}{(L_1 + L_2)(v_{c1} + v^*_o) + L_1(v_{c1} - v_g)} + 1,$$

$$CCM : d = \frac{L_1 v_i + v^*_o + v_{c1} - v_g}{v^*_o + v_{c1}}, \tag{22}$$

$$\dot{v^*_o} = \frac{1}{C_o}\left[(1-d)(i^*_{L1} + i^*_{L2}) - Gv^*_o + k_2(v_o - v^*_o)\right], \tag{23}$$

$$i^*_{L1} = I_{in}|sin(wt)|,$$

$$i^*_{L2} = \frac{v_g}{V^*_o} I_{in}|sin(wt)|, \tag{24}$$

$$G = G_s. \tag{25}$$

When the load is unknown, although constant, an adaptive control strategy, as presented in [21], can be applied, where the unknown load conductance is adapted as follows:

$$G_s = -k_g v^*_o \int_0^t [v_o(s) - v^*_o(s)]ds. \tag{26}$$

For a DC-DC system:

$$\frac{i_{L1}^*}{dt} = 0, i_{L1}^* = \frac{G}{v_g} V_o^{*2},$$

$$i_{L2}^* = G V_o^*. \tag{27}$$

Note that it is necessary to estimate an additional state: the output voltage v_o given by (23). The integral action, given by (20), can also be included in the control law. We list the following advantages of the proposed law:

- In contrast to the classical control, it gives an indirect and less dependent control of the 120-Hz ripple output voltage, which, therefore, allows for lower THDi levels; a higher phase margin due to non-restriction operating point. The integral gain can be stipulated for a faster response.
- Complements the FLC control and allows load estimation given by (26), being more robust to load disturbances;
- Given the caveats imposed by (22), the adaptive control law works for both conduction current modes (DCM and CCM);
- Neglecting the current measurement of the intermediate inductor L_2; this characteristic is motivated by the analysis discussed in the following section.

5. Revised SEPIC as a Boost Converter and Derived Equations

The SEPIC converter has two inductors and two capacitors (a fourth order system), so it is necessary to reduce the number of states and measurements, for cost and error propagation reasons. In view of this concern, Ref. [15,22] use observers and immersion techniques. In [23], the fourth order transfer function of SEPIC is reduced to second order using the Pade approximation method, where the designed compensator closely follows the original system's response. Furthermore, Ref. [24] employ a simplified second order state-averaged model, using the sliding surface-regulated current-mode PWM controller. In addition, the CIECA modeling discussed in Section 2.3 motivates an interesting question: Is it possible to reduce the states of the SEPIC converter, for example, considering only the output voltage and the input current?

In Figure 13, the boost and SEPIC converters are placed side by side for comparison. It is observed that when removing the intermediate elements (L_2, C_1) highlighted by the dotted line, the SEPIC converter becomes similar to the boost converter, having similar equilibrium points as shown in Table 4. This is the reason that these converters are recommended to work in PFC systems. What is the advantage of this adaptation?

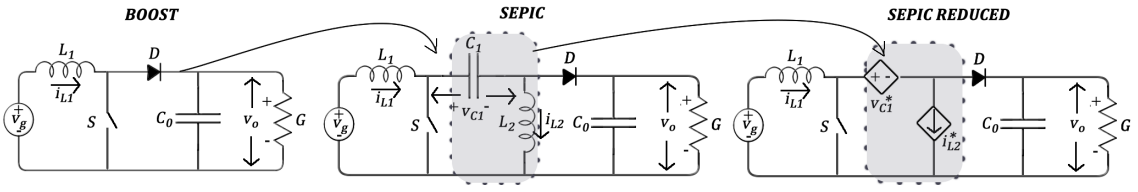

Figure 13. PFC SEPIC and DC-DC SEPIC.

Table 4. Equilibrium points of the converters.

Converter	i_{L1}^*	v_o^*	i_{L2}^*	v_{C1}^*
Boost	$\frac{G}{v_g} V_o^{*2}$	V_o^*	-	-
SEPIC	$\frac{G}{v_g} V_o^{*2}$	V_o^*	$G V_o^*$	v_g

Therefore, we can use the boost equations and apply them to control the SEPIC converter replacing the state variables eliminated (i_{L2} and v_{c1}) by the equilibrium points, provided in Table 4, represented by dependent sources in the model. If we substitute, for example, v_{c1} by v_g and i_{L2} by GV_o^* in the SEPIC converter, it saves two sensors. Figure 13 summarizes this process. The other option is to replace the desired state reference by the measurement of the state itself, as seen in (23).

To illustrate an example application, we consider two control laws based on IDAPBC. In [22], IDAPBC control is applied to boost converters achieving an effortless and open loop control equation:

IDAPBC-1:

$$\begin{aligned} \bar{d} &= 1 - \frac{v_g}{V_o^*}, \\ d &= 1 - \left(1 - \bar{d}\right) \left(\frac{v_o}{V_o^*}\right)^{k_\alpha} \end{aligned} \tag{28}$$

Yet, Ref. [25] proposed an evolution of (28) given by:

IDAPBC-2:

$$d = 1 - \frac{k_z v_g}{2 v_g v_o + (k_z - 2 v_o) V_o^*} \tag{29}$$

Equations (28) and (29) can be applied to SEPIC converters, which we denominate as IDAPBC-BB control equations. Again, the integral action, given by (20), can also be added. In order to illustrate how to insert this term in the control law, just replace the desired variable in the output voltage (V_o^*) by the integral of the error between the measured variable (v_o) and the reference constant value (V_o^*). Thus, the new control law becomes:

$$\begin{aligned} d &= 1 - \frac{k_z v_g}{2 v_g v_o + (k_z - 2 v_o) V_{o(int)}^*}, \\ V_{o(int)}^* &= -k_{int} \int_0^t [v_o(s) - V_o^*] ds \end{aligned} \tag{30}$$

The boost IDAPBC control equations are presented in Appendix B.

6. Main Results

In order to verify the performance of the control systems applied to the SEPIC DC-DC CCM and SEPIC PFC DCM, software and HIL simulations were performed using the specifications presented in Table 5.

Table 5. Initial and converters parameters.

Parameters	DC-DC CCM SEPIC	PFC DCM SEPIC
$V_o{}^*$	12 V	100 V
v_g	50 V	127 Vrms
R_{load}	10 Ω	100 Ω
L_1,L_2	146 µH, 35 µH	146 µH, 35 µH
C	470 µF	470 µF
f_{sw}	60 kHz	50 kHz
k_1	100	15
k_2	20	10
k	14	14
k_{int}	200	−5000
k_z	−150	-
k_α	0.8	0.8

6.1. SEPIC DC-DC CCM and HIL Simulation Results

This section presents the digital simulation results using MATLAB and Hardware in the Loop (HIL) procedure described in [26]. The converter is implemented according to the design specifications of Table 5 and the three control laws: FLC, APBFLC and IDAPBC-BB.

Figure 14 shows the capacitor voltage and inductor current response for load perturbation, respectively, in the SEPIC converter simulated in software. In the same way, Figure 15 presents the voltage and current response to an input voltage variation. In both input and load variation, consecutive steps of 50–100% are applied in the simulated systems. Figure 16 shows the out capacitor voltage of SEPIC converter, respectively, for the HIL application.

As seen in Figures 14–16, both software simulations and HIL results converged to the steady state value after the consecutive step applications. It is notable that the behavior of the systems are compatible, since the same transient dynamics is seen, even for the IDA-PBC's oscillatory dynamics. None of the implemented systems in software or in HIL converged to instability. This means that the embedded models and control equations are capable of controlling the systems, so validating the control techniques.

The processing time for the DSP to compute the control law and therefore to run a real-time simulation is 1.2 µs. Using a switching frequency of 50 kHz (20 µs), the processing time of all control equations (1.2 µs) demands 6% of the bandwidth.

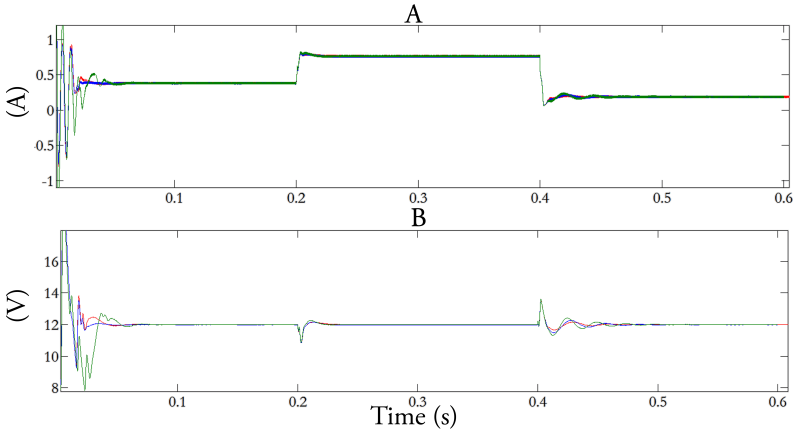

Figure 14. Input current i_{L1} (**A**) and output voltage v_o (**B**) in the MATLAB simulation with load change (20 – 10 – 40 Ω). FLC (blue), APBFLC (green) and IDAPBC-BB-1 (red).

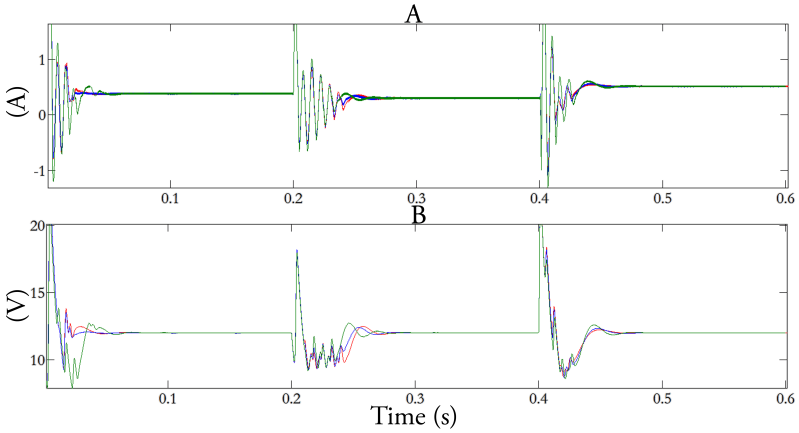

Figure 15. Input current i_{L1} (**A**) and output voltage v_o (**B**) in the MATLAB simulation with input voltage variation (20 – 15 – 25 V). FLC (blue), APBFLC (green) and IDAPBC-BB-1 (red).

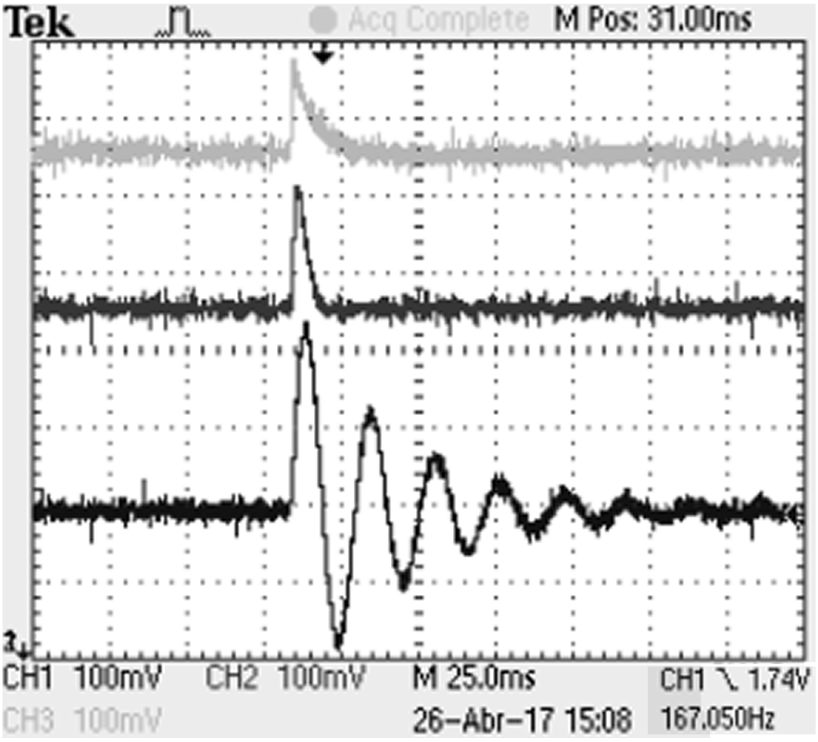

Figure 16. HIL experimental result for SEPIC converter. Normalized output voltage v_o in view of load perturbation (50–100%). FLC (top), APBFLC (middle) and IDAPBC-BB-1 (bottom).

6.2. APBFLC Results

As sketched in Figure 17, the output voltage can asymptotically track the set-point even if the load perturbation is present. The APBFLC controller features low THDi (<2%), low overshoot (<10%) and fast response speed (<0.05 s). The power factor achieved for the nominal condition is PF = 0.99.

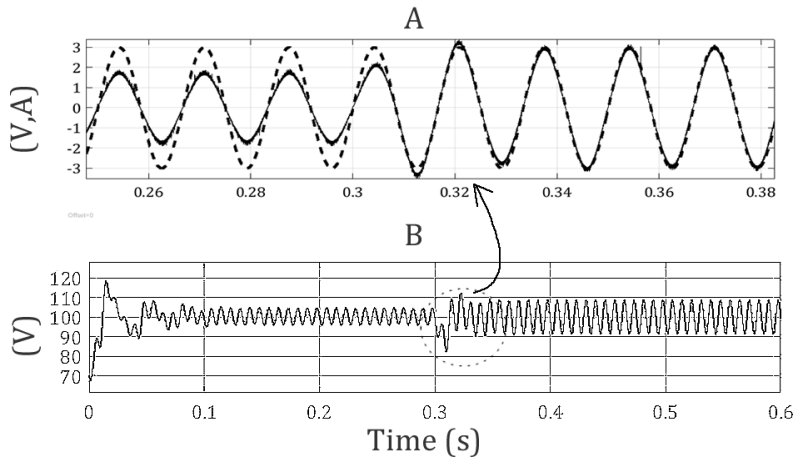

Figure 17. Detail of the input current (**A** continue) and normalized grid voltage (**A** dashed) and the output voltage transient (**B**) with a load change from R = 100 Ω to R = 50 Ω for APBFLC control.

6.3. IDAPBC-BB Results

Next, the two control laws (28) and (29) are validated in simulation. We can again observe the stability of the adapted nonlinear controllers by analyzing the change in perturbation of the output voltage waveform over a load step (note the insignificant overshoot of IDAPBC-BB-2 response). Hence, this variable is controlled at the desired value $V_o{}^*$. The steady-state and perturbed waveforms are

sketched in Figure 18 showing that the two methods have low overshoot and fast response, even considering a control law adapted from the boost converter, taking into account only the measurement of the output voltage.

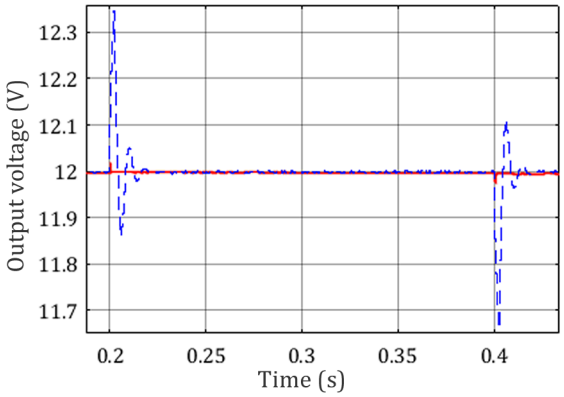

Figure 18. IDAPBC-BB-1 (dashed blue) and IDAPBC-BB-2 (continue red) simulations. Output voltage v_o for load perturbation (70–100%).

7. Conclusions

The intrinsic power factor correction includes SEPIC in a particular group of converters. Hence, the design of the control system derived from the model based on CIECA and the boost converter is satisfactory, revealing that it is possible to obtain high performance controllers using a simplified modeling. In addition, the effectiveness of the nonlinear approaches was verified, whose control laws proved to be efficient, especially for the voltage regulation and transient dynamics.

The performance of the proposed nonlinear controllers was analyzed under variations in load and input voltage. The software and HIL simulations demonstrated the feasibility of the nonlinear algorithms that can be used in embedded systems and practical applications, with simplicity and high accuracy.

Thus, we recommend:

- For DC-DC SEPIC: the IDAPBC-BB-2 controller, because it presents ultra-low overshoot and ultra-fast response speed; all these benefits are sufficiently attained using only one measure (output voltage v_o);
- For PFC SEPIC: the APBFLC control method, which offers high robustness, low THDi, low overshoot, load estimation possibility and fast response; all these advantages were achieved regardless of mode operation (CCM or DCM).

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
DC	Direct Current
CCM	Continuous Conduction Mode
CIECA	Current Injected Equivalent Circuit Approach
DCM	Discontinuous Conduction Mode

ELM	Euler–Lagrange Model
FLC	Feedback Linearization Control
PBC	Passivity-Based Control
IDAPBC	Interconnection and Damping Assignment Passivity-Based Control
IDAPBC-BB	Interconnection and Damping Assignment Passivity-Based Control—Based on the Boost Converter
PCH	Port-Controlled Hamiltonian
SSM	State-Space Model

Nomenclature

v_g	Input voltage
d	Duty cycle
i_{L1}	Inductor L_1 current
i_{L2}	Inductor L_2 current
v_o	Capacitor voltage
i_o	Output load current
L_1	Primary-side inductance
L_2	Secondary-side inductance
C_o	Output capacitance
G	Load conductance
R_L	Load resistance

Appendix A. Reactive Elements of Power Circuits

The choice of the power circuit reactive elements of the SEPIC PFC converter in DCM, discussed in this work, is directly influenced by the operation mode of this converter. Based on the work of [16], these design specification are calculated, as seen in Table A1.

Table A1. Design specifications.

Parameters	Value	Unity
Input voltage (v_{in})	127	V_{RMS}
Frequency (f)	60	Hz
Nominal power (P_{nom})	100	W
Output voltage (V_o)	100	V
Resistive load (R_L)	100	Ω
Switch frequency (f_s)	50	kHz
Inductors (L_1/L_2)	4/100	mH/µH
Capacitors (C_1/C_o)	470/330	nF/µF

Thus, the DCM operation requires:

$$D < \frac{M}{M+1} \tag{A1}$$

Note that in Figure 3, the average current in the load can be represented by the ratio of the output voltage v_o and the load impedance R_L. However, the amplitude of this current was previously defined in (5). Therefore, the nominal duty cycle can now be calculated as:

$$D = \sqrt{2}M\sqrt{K_a} \tag{A2}$$

where K_a is the parameter given by:

$$K_a = \frac{2L_{eq}}{R_L T_S} \tag{A3}$$

At this discussion point, from the results presented in (A1) and (A2), it is necessary to establish a critical parameter, which will define the operating modes of the PFC SEPIC, in terms of the ratio M. Hence, we have:

$$K_{crit} = \frac{1}{2(M+1)^2} \tag{A4}$$

Note that the DCM operation requires $K_a < K_{crit}$.

Next, the inductor parameters L_1 and L_2 are calculated in view of the L_1 current ripple term:

$$i_{rip} = \frac{v_g D T_S}{L_1} \tag{A5}$$

Therefore, considering the worst case i_{rip} ($wt = 90°$), the L_1 value is defined by evaluation of (A5) and the specification of the maximum admissible ripple I_{rip}:

$$L_1 = \frac{V_{in} D T_S}{I_{rip}} \tag{A6}$$

Use of Equations (A6) and (7) leads to:

$$L_2 = \frac{L_1 L_{eq}}{L_1 - L_{eq}} \tag{A7}$$

Finally, the value of the intermediate capacitor C_1, which strongly influences the input current waveform of the SEPIC PFC converter, will be calculated. According to [16], a good choice is:

$$C_1 = \frac{1}{w_r^2 (L_1 + L_2)} \tag{A8}$$

where w_r is the angular frequency of C_1, L_1 and L_2, generally allocated between the angular frequency of the ac w and switching frequency w_s, that is $w << w_r << w_s$.

Appendix B. IDA-PBC Control for Boost Converter

The average boost converter circuit can be written by Euler–Lagrange equations, as:

$$D_B \dot{x} + (1 - d) J_B x + R_B x = F, \tag{A9}$$

with:

$$x = \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{co} \end{bmatrix}, D_B = \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix},$$
$$R_B = \begin{bmatrix} 0 & 0 \\ 0 & G \end{bmatrix}, F = \begin{bmatrix} v_g \\ 0 \end{bmatrix}, J_B = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}. \tag{A10}$$

The equivalent state space equations are:

$$\dot{x}_1 = -(1 - d)\frac{1}{L} x_2 + \frac{v_g}{L}, \tag{A11}$$

$$\dot{x}_2 = (1 - d)\frac{1}{C} x_1 - \frac{G}{C} x_2, \tag{A12}$$

The modeling and IDA-PBC control of the boost converter are presented in [22]. Consecutively, the Port-Controlled Hamiltonian model (PCH) can be rearranged by the ELM to obtain:

$$x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}, H(x) = \frac{1}{2} L x_1^2 + \frac{1}{2} C x_2^2,$$

$$J_H = \begin{bmatrix} 0 & \frac{-1-d}{LC} \\ \frac{1-d}{LC} & 0 \end{bmatrix}, R_H = \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{RC^2} \end{bmatrix}, g_H = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix},$$

$$\dot{x} = [J_H(d) - R_H] \frac{\partial H}{\partial z}(z) + g_H v_g \tag{A13}$$

The equilibrium points obtained when $\dot{x}_1 = 0$ and $\dot{x}_2 = 0$ in Equations (A11) and (A12) are:

$$\bar{x}_1 = \frac{v_g G}{(1-d)^2} \tag{A14}$$

$$\bar{x}_2 = \frac{v_g}{(1-d)} \tag{A15}$$

By the equation, d as a constant value in (A14), (A15) and $\bar{d}$, as an equilibrium value, this leads to:

$$\bar{x}_1 = \frac{G}{v_g} \bar{x}_2^2 \tag{A16}$$

Let us now consider the desired output capacitor voltage as $x_{2d} = \bar{x}_2 = V_o^*$, the equilibrium point to stabilize $\bar{x}$ and the constant input control $\bar{d}$ given by:

$$\bar{d} = 1 - \frac{E}{V_o^*}, \bar{x} = [\bar{x_1}, \bar{x_2}]^T = \left[G V_o^* \left(\frac{V_o^*}{E} \right), V_o^* \right]^T. \tag{A17}$$

The main objective of IDA-PCB control is to find a static function through space state feedback, $d = \nu(x)$. Thus, the closed loop dynamics becomes a Port-Controlled Hamiltonian (PCH), given by:

$$\dot{x} = [J_d(x,d) - R_d] \frac{\partial H_d}{\partial x}(x) \tag{A18}$$

where the new function H_d has a local minimum at the desired equilibrium point, $\bar{x}$. The terms $J_d(x, \nu(x)) = -J_d^T(x, \nu(x))$ and $R_d(x) = R_d^T(x) 0$ are the desired interconnection and damping matrices, respectively. Now, given the system:

$$\dot{x} = [J_H(x,d) - R_H] \frac{\delta H}{\delta x}(x) + g_H(x,d) \tag{A19}$$

Taking into account the damping term R_{aH}, given by:

$$R_{aH} = \begin{bmatrix} R_{aH} & 0 \\ 0 & G \end{bmatrix} \tag{A20}$$

this leads to the following matrix:

$$R_d = \begin{bmatrix} R_{aH} & 0 \\ 0 & 0 \end{bmatrix}. \tag{A21}$$

Substituting R_{aH} in (A18), (A19) and assuming $d = \nu(x_2)$ and $J_H(\nu(x)) - R_d$ invertible, the gain control vector K is obtained:

$$K = \begin{bmatrix} K_1 \\ K_2 \end{bmatrix} = \begin{bmatrix} -\frac{GLx_2}{(1-\nu(x_2))} \\ \frac{CG\left(GR_{aH}L^2x_1 + v_g\right)}{(1-\nu(x_2))} - \frac{GR_{aH}L^2Cx_2}{(1-\nu(x_2))^2} \end{bmatrix} \tag{A22}$$

The sufficient and necessary condition for making the K vector a gradient of a scalar function is:

$$\frac{\partial K_2}{\partial x_1}(x) = \frac{\partial K_1}{\partial x_2}(x). \tag{A23}$$

Then, this condition is reduced to a simple Ordinary Differential Equation (ODE):

$$\frac{x_2}{(1-\nu(x_2))}\frac{\partial \nu(x_2)}{\partial x_2} = -(1 - LCR_{aH}R) \tag{A24}$$

which can be easily solved through the variable separation method, leading to:

$$d = 1 - c_1 z_2^{\alpha}, \alpha = 1 - LCR_{aH}R. \tag{A25}$$

The constant c_1 is chosen in such a way so as to ensure the equilibrium form:

$$\frac{\partial H_d}{\partial x}(\bar{x}) = \frac{\partial H}{\partial x}(\bar{x}) = \frac{\partial H_a}{\partial x}(\bar{x}) = 0 \tag{A26}$$

which implies:

$$c_1 = \frac{(1-\bar{d})}{V_o^{*\alpha}} \tag{A27}$$

and the IDA-PBC control equation:

$$d = 1 - (1-\bar{d})\left(\frac{x_2}{V_o^*}\right)^{\alpha}. \tag{A28}$$

Substituting (A17) in (A28) derives:

$$d = 1 - \left(\frac{v_g}{V_o^*}\right)\left(\frac{x_2}{V_o^*}\right)^{\alpha}. \tag{A29}$$

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