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Review

Dynamic Modeling and Analysis of PCM-Controlled DCM-Operating Buck Converters—A Reexamination

Teuvo Suntio

Laboratory of Electrical Energy Engineering, Tampere University of Technology, 33720 Tampere, Finland; teuvo.suntio@tut.fi; Tel.: +358-400-828-431

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Abstract: Peak-current-mode (PCM) control was proposed in 1978. The observed peculiar behavior caused by the application of PCM-control in the behavior of a switched-mode converter, which operates in continuous conduction mode (CCM), has led to a multitude of attempts to capture the dynamics associated to it. Only a few similar models have been published for a PCM-controlled converter, which operates in discontinuous conduction mode (DCM). PCM modeling is actually an extension of the modeling of direct-duty-ratio (DDR) or voltage-mode (VM) control, where the perturbed duty ratio is replaced by proper duty-ratio constraints. The modeling technique, which produces accurate PCM models in DCM, is developed in early 2000s. The given small-signal models are, however, load-resistor affected, which hides the real dynamic behavior of the associated converter. The objectives of this paper are as follows: (i) proving the accuracy of the modeling method published in 2001, (ii) performing a comprehensive dynamic analysis in order to reveal the real dynamics of the buck converter under PCM control in DCM, (iii) providing a method to improve the high-frequency accuracy of the small-signal models, and (iv) developing control-engineering-type block diagrams to facilitate the development of generalized transfer functions, which are applicable for PCM-controlled DCM-operated buck, boost, and buck-boost converters.

Keywords: peak-current-mode control; dynamic modeling; duty-ratio constraints; discontinuous conduction mode

1. Introduction

Peak-current-mode (PCM) control of switched-mode converters was publically introduced in 1978 [1,2], and it quickly became a very popular control method because of the beneficial features that it provides in converter operation and protection, as discussed in [3]. A huge number of modeling approaches has been proposed since the introduction of the PCM control in continuous conduction mode (CCM), as discussed and referenced in [4]. It has been recently shown in [4] that the accurate dynamic models of PCM-controlled converters, which operates in CCM, can be obtained by developing such duty-ratio constraints that include the duty-ratio gain (F_m), which becomes infinite at the mode-limit duty ratio (i.e., the maximum duty ratio after which the converter enters into harmonic mode of operation). Such models can be found, for example, from [4–8]. Only a few similar analytical models applicable for discontinuous conduction (DCM) are published [9–14].

The models in [9] are derived assuming that the inductor current does not exist as a state variable (i.e., no feedback from the inductor current is considered), because all the energy in the inductor is dissipated within the cycle, as assumed in [15]. This assumption is not valid, because the time-averaged inductor current does exist and it is a continuous state variable as discussed explicitly in [16]. A modeling technique is introduced in [10], which produces duty-ratio constraints with infinite duty-ratio gain (F_m) at the mode limit between the DCM and CCM operation but the models are load-resistor affected, which modifies the dynamics of the converter significantly, as discussed

in [4,17]. The models presented in [11] are given in an implicit form including the load-resistor effect, which makes the model validation a challenging task, because the unterminated small-signal transfer functions cannot be recovered based on the given equivalent circuits. A discrete-time-modeling approach is presented in [12] for a buck converter including also PCM control in DCM, but it does not give any explicit transfer functions for comparison. The average and small-signal behavior of PCM-controlled boost converter based on numerical analysis methods is provided in [18] but no explicit analytic transfer functions are presented either. The unterminated PCM state spaces are given in [13] (pp. 139–144) and in [14] (pp. 222–224) for a buck converter based on the method introduced in [10], but the transfer functions are not solved for comparison.

As discussed in [4], the experimental verifications do not usually prove the validity of the models especially at the high frequencies due to the existence of un-modeled circuit elements at the input and/or output terminals, which affect the measurements either through the source or load-effect phenomena [14] (pp. 38–40). A good example of such a phenomenon can be found, for example, from [19] (cf. Figure 16 in [19]). Figure 1 shows the experimentally measured (red line), the analytically predicted (black line), and the simulation-based (blue line) frequency responses of the control-to-output-voltage transfer functions of a direct-duty-ratio (DDR) controlled buck converter analyzed in this paper [20]. The effect of the external circuit elements is explicitly visible, especially, in the behavior of the phase at the higher frequencies (cf. red line, >10 kHz). The predicted (black line) and simulation-based (blue line) frequency responses have very good match with each other. The ability to predict correctly the high frequency phase behavior (i.e., $\geq$1/10th of switching frequency) is a quite important feature of the small-signal models from the control-design point of view. Therefore, it is well justified to perform the model validation by using Matlab^{TM} Simulink environment, where all the circuit elements are perfectly known.

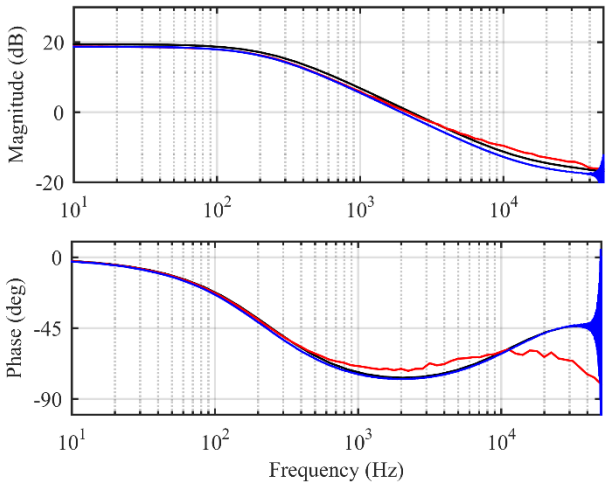

Figure 1. Measured (red line), analytically predicted (black line), and simulation-based (blue line) control-to-output-voltage frequency responses of direct-duty-ratio (DDR)-controlled buck converter operating in discontinuous conduction mode (DCM) at the input voltage of 20 V.

The investigations of this paper show that the modeling method in [10] will produce highly accurate unterminated small-signal models, when the parasitic circuit elements are taken into account. If the parasitic elements are omitted then the accuracy of the simplified models is not acceptable, especially, at the low input-voltage levels. The investigations show clearly also that an unterminated buck converter will become unstable in open loop at $M \approx 1/2$, where M denotes V_0/V_{in}. The load-resistor-affected instability will take place at $M \approx 2/3$ as predicted earlier in [10,11] as well as demonstrated explicitly in [21]. The existence of the right-half-plane (RHP) pole requires to designing the output-voltage feedback-control loop to have the crossover frequency higher than the RHP pole

for stability to exist. The RHP pole will move into higher frequencies along the increase in M and D (i.e., duty ratio) requiring careful selection of the feedback-loop crossover frequency for ensuring the stability of the converter. Therefore, the new findings concerning the location of the RHP pole have real scientific as well as practical values.

The rest of the paper is organized as follows: Section 2 introduces briefly the PCM-modeling method developed in [10] in a generalized unterminated form, and provides the corresponding explicit transfer functions for a buck converter. Section 3 presents the validation of the developed small-signal models by utilizing Matlab^{TM} Simulink-based switching models, and the pseudo-random binary-sequence-based frequency-response measurement technique introduced in [22,23]. The conclusions are provided finally in Section 4.

2. PCM-Control Modeling

The accurate small-signal modeling method of DCM-operated direct-duty-ratio (DDR) or voltage-mode (VM) controlled converters was establish in the late 1990s in [24,25] and later elaborated in a more convenient form in [16]. It is claimed in [26] that the small-signal models in [25] are not accurate enough, but the paper does not explicitly provide the required correction elements to improve the model accuracy. The small-signal models in [24,25] are load-resistor affected, which will hide the unterminated dynamic behavior of the converter, especially, at the low frequencies as well as which affects also the location of the low-frequency system poles [17]. Therefore, we will apply the methods presented in [16] for obtaining the small-signal DDR state space with the parasitic circuit elements included, which is utilized also in the corresponding PCM modeling. Figure 1, in Section 1, proves explicitly that the method described in [16] produces highly accurate unterminated small-signal models, when all the parasitic elements are included in the model. The duty ratio is generated in a DRR-controlled converter by means of a fixed pulse-width-modulator (PWM) ramp signal. In a PCM-controlled converter, the duty ratio is generated by means of the up slope of the instantaneous inductor current. As a consequence of this, the small-signal state space of a PCM-controlled converter can be found by developing proper duty-ratio constraints of the form [4,10,14]:

$$\hat{d} = F_{\mathrm{m}}(\hat{x}_{\mathrm{c}} - \sum_{i=1}^{n} q_i \hat{x}_i) \tag{1}$$

where F_{m} denotes duty-ratio gain,x_{c} the control variable (i.e., control current (i_{co})), and q_i the feedback or feedforward gain related to variable x_i, which can be either a state, or input variable of the converter as well as n the number of input and state variables [4]. The modeling is finalized by replacing the perturbed duty ratio ($\hat{d}$) by (1) in the linearized state space of the corresponding DDR-controlled converter [4,10,14]. The hat over the variables in (1) indicates that the corresponding variables are small-signal variables. This notation method is applied in rest of the paper.

2.1. Generalized Duty-Ratio Constrains in DCM

Figure 2 shows the inductor-current waveforms, the control current (i_{co}), and the inductor-current compensating ramp (m_{c}) during one switching cycle in DCM under dynamic conditions. According to [16], the real state variables, which will produce the dynamic behavior of the converter up to half the switching frequency, are the time-averaged values of the instantaneous variables (i.e., inductor currents and capacitor voltages), where the averaging is performed within one cycle. The time-averaged variables are denoted in this paper by $\langle x_i \rangle$. Figure 2 shows that at the time instant $t = (k + d)T_{\mathrm{s}}$) the variables in Figure 2 are linked together by:

$$i_{\mathrm{co}} - m_{\mathrm{c}} d T_{\mathrm{s}} = \sum_{i=1}^{n} \langle i_{\mathrm{L}} \rangle + \Delta i_{\mathrm{L}} \tag{2}$$

which is known as the comparator equation, because the associated PWM comparator will change state, when the condition determined by (2) is valid [13]. The only unspecified variable in (2) is Δi_L (cf. Figure 2), which can be solved by applying the definition of the time-averaged inductor current (i.e.,$\langle i_L \rangle$) at $t = (k + d)T_s$:

$$\langle i_L \rangle = \frac{m_1 d(d + d_1)T_s}{2} \tag{3}$$

where d_1 can be solved based on the inductor-current waveforms in Figure 2 as $d_1 = m_1 d/m_2$ [10]. Thus Δi_L can be given by:

$$\Delta i_L = m_1 dT_s - \langle i_L \rangle = m_1 dT_s - \frac{m_1(m_1 + m_2)d^2 T_s}{2m_2} \tag{4}$$

and the corresponding comparator equation in (2) by:

$$i_{co} - m_c dT_s = \langle i_L \rangle + m_1 dT_s(1 - \frac{d(m_1 + m_2)}{2m_2}) \tag{5}$$

where m_1 and m_2 denote the absolute values of the up and down slopes of the inductor current as denoted in Figure 2.

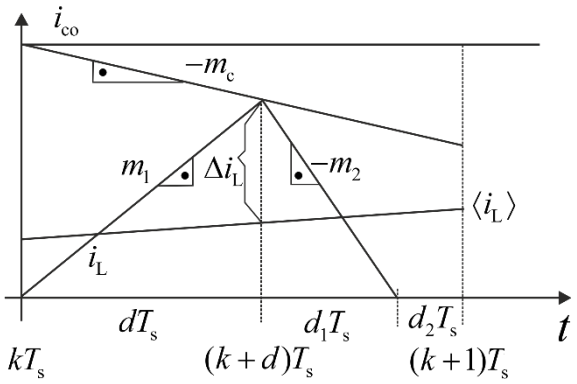

Figure 2. Inductor-current waveforms in DCM including the control current (i_{co}) and compensation ramp (m_c).

The coefficients in the small-signal duty ratio constraints in (1) can be found by substituting the up and down slope of the inductor current with their topology-based values in (5) as well as linearizing (5) at a certain operating point. The linearization requires to applying the partial-derivative-based method due to the highly nonlinear nature of the comparator equation in (5) for obtaining the required coefficients in (1) (cf. pp. 60, 61, [14]). Thus the duty-ratio gain (F_m) can be given in a generalized form (Note: In this case, only the duty ratio (d) is a variable, and all the other variables are constant) by:

$$F_m = \frac{1}{T_s\left(M_c + \frac{M_1(M_2 - D(M_1+M_2))}{M_2}\right)} \tag{6}$$

which indicates that F_m becomes infinite, when the duty ratio (D) equals:

$$D = \frac{M_2}{M_1 + M_2} + \frac{M_2}{M_1(M_1 + M_2)} \cdot M_c \tag{7}$$

Equation (7) defines the mode limit for the converter operation at the switching frequency, where the first term denotes actually the mode limit between the DCM and CCM operation [14], because the only operational condition in DCM, where $DM_1 - D'M_2$ equals zero, is the boundary between

DCM and CCM (i.e., the boundary conduction mode (BCM) [11]). It equals symbolically the same value, which defines the mode limit at $D = 0.5$ in the PCM-controlled converter in CCM, when $M_c = 0$ [4]. Figure 3 shows the inductor-current waveforms, when the converter is driven into the harmonic modes of operation. The figure shows definitively that the buck converter can adopt both even and odd harmonic modes as discussed also in [10]. The reason for the existence of the odd harmonics is actually the existence of an RHP pole in the converter open-loop dynamics. In case of CCM operation, only the even harmonic modes are possible as explained in detail in [4]. In DCM operation, the mode-limit duty ratio does not either equal the average duty ratio of the harmonic operation as it does in CCM operation [4].

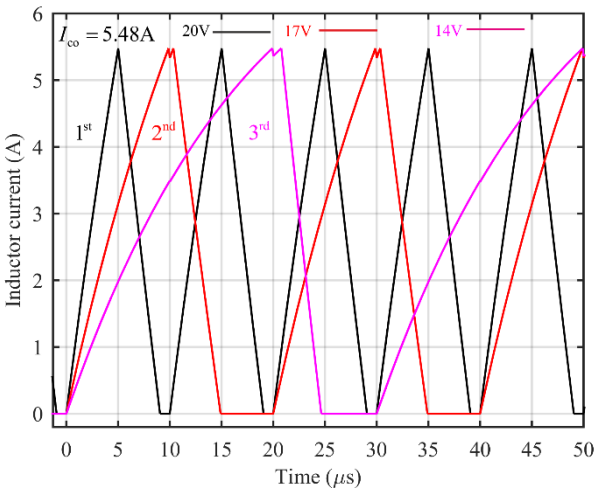

Figure 3. Simulation-based inductor-current behavior in harmonic modes in a peak-current-mode (PCM)-controlled buck converter.

Equation (5) can be developed in terms of duty ratio (D) for a second-order converter with $M_c = 0$ as [13]:

$$\frac{M_1(M_1 + M_2)T_s}{2M_2} \cdot D^2 - M_1 T_s \cdot D - \Delta I_L = 0 \tag{8}$$

where $\Delta I_L = I_{co} - I_L$. According to (8), we can compute that ΔI_{L-min} will be limited to:

$$\Delta I_{L-min} = \frac{M_1 M_2 T_s}{2(M_1 + M_2)} \tag{9}$$

at the duty ratio of:

$$D_{max} = \frac{M_2}{M_1 + M_2} \tag{10}$$

which equals D in (7) (i.e., the first term). At the higher duty ratios, Equation (8) does not have any more real-valued solutions indicating that the converter enters into harmonic operation mode as shown in Figure 3.

The steady-state comparator equation in (8) can be developed further in terms of the input-to-output gain (M) (i.e., $M = V_o/V_{in}$), and K (i.e., $K = 2L/T_s/R_{eq}$ and $R_{eq} = V_o/I_o$). It should be observed that M_1 and M_2 denote the inductor current up and down slopes as absolute values, and they have to be expressed as a function of M according to the behavior of the corresponding converter. In addition, the duty ratio (D) has to be replaced by the converter specific formula, which can be given for the buck converter as $D = M\sqrt{K/(1-M)}$ [11]. These procedures yield for the buck converter as:

$$M^3 - M^2 + K\left(\frac{I_{co}R_L}{2V_{in}}\right)^2 = 0 \tag{11}$$

Equation (11) can be further developed as:

$$\left(M-\frac{2}{3}\right)^2\left(M-\left(\frac{3I_{\mathrm{co}}R_{\mathrm{L}}}{4V_{\mathrm{in}}}\right)^2\right)=0 \tag{12}$$

which indicates that there exists a double root at $M = 2/3$ in (11), which means that there are no real-valued solutions for $M > 2/3$ in open loop, as discussed also in [11,12] as well as explicitly demonstrated in [21]. It is explicitly proved in [10] that the mode limit at $M = 2/3$ does not exist, when the output-voltage feedback loop is closed. The dynamic analysis will reveal that the mode limit at $M = 2/3$ produces an RHP pole (i.e., the converter is unstable), which does not take place in the CCM converter. Therefore, the output-voltage feedback can remove the RHP pole when its control bandwidth is higher than the RHP pole. The boost and buck-boost converters do not have similar anomalies as the buck converter has in the open-loop behavior as discussed also in [11]. Equation (11) is actually load-resistor affected, and therefore, it does not correctly predict the location of the actual RHP pole in a buck converter as will be shown later in Section 2.3.

2.2. Small-Signal Model of DDR-Controlled Buck Converter in DCM

The averaged complete (i.e., including all parasitic elements) state space of a DDR-controlled buck converter shown in Figure 4, which operates in DCM, can be given according to [14,16] by:

$$\begin{aligned}
\frac{d\langle i_{\mathrm{L}}\rangle}{dt} &= \frac{d(\langle v_{\mathrm{in}}\rangle+(R_1-R_2)\langle i_{\mathrm{L}}\rangle+V_{\mathrm{D}})}{L}-\frac{2\langle i_{\mathrm{L}}\rangle}{dT_{\mathrm{s}}}\cdot\frac{R_1\langle i_{\mathrm{L}}\rangle+\langle v_{\mathrm{C}}\rangle-r_{\mathrm{C}}\langle i_{\mathrm{o}}\rangle+V_{\mathrm{D}}}{\langle v_{\mathrm{in}}\rangle-R_2\langle i_{\mathrm{L}}\rangle-\langle v_{\mathrm{C}}\rangle+r_{\mathrm{C}}\langle i_{\mathrm{o}}\rangle}\\
\frac{d\langle v_{\mathrm{C}}\rangle}{dt} &= \frac{\langle i_{\mathrm{L}}\rangle}{C}-\frac{\langle i_{\mathrm{o}}\rangle}{C}\\
\langle i_{\mathrm{in}}\rangle &= \frac{d^2T_{\mathrm{s}}}{2L}(\langle v_{\mathrm{in}}\rangle-R_2\langle i_{\mathrm{L}}\rangle-\langle v_{\mathrm{C}}\rangle+r_{\mathrm{C}}\langle i_{\mathrm{o}}\rangle)\\
\langle v_{\mathrm{o}}\rangle &= \langle v_{\mathrm{C}}\rangle+r_{\mathrm{C}}C\frac{d\langle v_{\mathrm{C}}\rangle}{dt}\\
R_1 &= r_{\mathrm{L}}+r_{\mathrm{d}}+r_{\mathrm{C}}R_2 = r_{\mathrm{L}}+r_{\mathrm{ds}}+r_{\mathrm{C}}
\end{aligned} \tag{13}$$

from which the operating point can be derived by setting the derivatives to zero and denoting the circuit variables (i.e., voltages and currents) by capital letters yielding:

$$\begin{aligned}
I_{\mathrm{L}} &= I_{\mathrm{o}}I_{\mathrm{in}} = \frac{((r_{\mathrm{L}}+r_{\mathrm{d}})I_{\mathrm{o}}+V_{\mathrm{o}}+V_{\mathrm{D}})}{(V_{\mathrm{in}}+(r_{\mathrm{d}}-r_{\mathrm{ds}})I_{\mathrm{o}}+V_{\mathrm{D}})}\cdot I_{\mathrm{o}}\\
V_{\mathrm{o}} &= V_{\mathrm{C}}\\
D &= \sqrt{\frac{2LI_{\mathrm{o}}}{T_{\mathrm{s}}}\cdot\frac{V_{\mathrm{o}}+V_{\mathrm{D}}+(r_{\mathrm{L}}+r_{\mathrm{d}})I_{\mathrm{o}}}{(V_{\mathrm{in}}-V_{\mathrm{o}}-(r_{\mathrm{L}}+r_{\mathrm{ds}})I_{\mathrm{o}})(V_{\mathrm{in}}+V_{\mathrm{D}}+(r_{\mathrm{d}}-r_{\mathrm{ds1}})I_{\mathrm{o}})}}
\end{aligned} \tag{14}$$

The small-signal state space can be derived by linearizing the averaged state space in (13) by applying the partial-derivatives-based method (cf. pp. 60, 61, [14]) at a certain operating point (14) yielding (15):

$$\begin{aligned}
\frac{d\hat{i}_{\mathrm{L}}}{dt} &= -\frac{A_1}{L}\hat{i}_{\mathrm{L}}-\frac{A_2}{L}\hat{v}_{\mathrm{C}}+\frac{A_3}{L}\hat{v}_{\mathrm{in}}+\frac{A_4}{L}\hat{i}_{\mathrm{o}}+\frac{V_{\mathrm{e}}}{L}\hat{d}\\
\frac{d\hat{v}_{\mathrm{C}}}{dt} &= \frac{\hat{i}_{\mathrm{L}}}{C}-\frac{\hat{i}_{\mathrm{o}}}{C}\\
\hat{i}_{\mathrm{in}} &= -B_1R_2\hat{i}_{\mathrm{L}}-B_1\hat{v}_{\mathrm{C}}+B_1\hat{v}_{\mathrm{in}}+B_1r_{\mathrm{C}}\hat{i}_{\mathrm{o}}+I_{\mathrm{e}}\hat{d}\\
\hat{v}_{\mathrm{o}} &= \hat{v}_{\mathrm{C}}+r_{\mathrm{C}}C\frac{d\hat{v}_{\mathrm{C}}}{dt}
\end{aligned} \tag{15}$$

where:

$$\begin{aligned} A_1 &= D(R_2 - R_1) + \frac{2L}{DT_s}\left(\frac{V_o+V_D+(2R_1-r_C)I_o}{V_{in}-V_o-(R_2-r_C)I_o} - \frac{R_2 I_o(V_o+V_D+(R_1-r_C)I_o)}{(V_{in}-V_o-(R_2-r_C)I_o)^2}\right) \\ A_2 &= \frac{2LI_o}{DT_s}\frac{V_{in}+V_D+(R_1-R_2)I_o}{(V_{in}-V_o-(R_2-r_C)I_o)^2} \\ A_3 &= D + \frac{2LI_o}{DT_s}\left(\frac{V_o+V_D+(R_1-r_C)I_o}{(V_{in}-V_o-(R_2-r_C)I_o)^2}\right) \\ A_4 &= \frac{2LI_o r_C}{DT_s}\frac{V_{in}+V_D+(R_1-R_2)I_o}{(V_{in}-V_o-(R_2-r_C)I_o)^2} \\ B_1 &= \frac{D^2T_s}{2L} \end{aligned} \tag{16}$$

and:

$$\begin{aligned} V_e &= V_{in} + V_D + (R_1 - R_2)I_o + \frac{2LI_o}{D^2T_s}\left(\frac{V_o+V_D+(R_1-r_C)I_o}{V_{in}-V_o-(R_2-r_C)I_o}\right) \\ I_e &= \frac{DT_s}{L}(V_{in} - V_o - (R_2 - r_C)I_o) \\ R_1 &= r_L + r_d + r_C \\ R_2 &= r_L + r_{ds} + r_C \end{aligned} \tag{17}$$

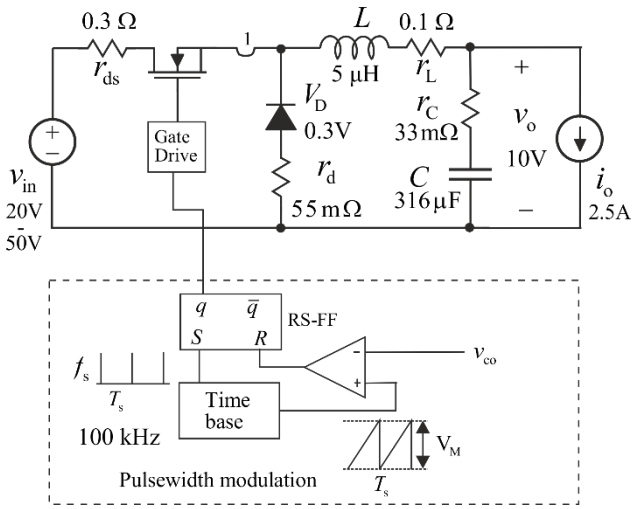

Figure 4. The power stage of the DDR-controlled buck converter in DCM.

2.3. Small-Signal Models of PCM-Controlled Buck Converter in DCM

The power stage of the PCM-controlled buck converter including the resistive load and the values of components are given in Figure 5, where the power stage equals the power stage in Figure 4. The generalized comparator equation for the second-order converters has been given earlier in (5), and the inductor-current up and down slopes, which are valid for a buck converter, are given explicitly in (18). According to (5) and (18), the corresponding unterminated duty-ratio constraints can be computed to be as given in (19) and in (20), respectively:

$$\begin{aligned} m_1 &= \frac{\langle v_{in}\rangle - R_2\langle i_L\rangle - \langle v_C\rangle + r_C\langle i_o\rangle}{L} \\ m_2 &= \frac{R_1\langle i_L\rangle + \langle v_C\rangle - r_C\langle i_o\rangle + V_D}{L} \end{aligned} \tag{18}$$

$$\hat{d} = F_m(\hat{i}_{co} - q_L\hat{i}_L - q_C\hat{v}_C - q_{in}\hat{v}_{in} - q_o\hat{i}_o) \tag{19}$$

where:

$$
\begin{aligned}
F_{\mathrm{m}} &= \frac{1}{T_{\mathrm{s}}\left(M_{\mathrm{c}}+\frac{(V_{\mathrm{in}}-V_{\mathrm{o}}-(R_2-r_{\mathrm{C}})I_{\mathrm{o}})(V_{\mathrm{o}}+V_{\mathrm{D}}-DV_{\mathrm{in}}+(D'R_1+DR_2-r_{\mathrm{C}})I_{\mathrm{o}})}{L(V_{\mathrm{o}}+V_{\mathrm{D}}+(R_1-r_{\mathrm{C}})I_{\mathrm{o}})}\right)} \\
q_{\mathrm{L}} &= 1-\frac{DT_{\mathrm{s}}}{L}R_2+\frac{D^2T_{\mathrm{s}}}{2L(V_{\mathrm{o}}+V_{\mathrm{D}}+(R_1-r_{\mathrm{C}})I_{\mathrm{o}})}\left(\begin{array}{c}(R_1-R_2)V_{\mathrm{o}}-(R_1-R_2)(2R_2-r_{\mathrm{C}})I_{\mathrm{o}} \\ +\frac{R_1(V_{\mathrm{in}}+(R_1-R_2)I_{\mathrm{o}})(V_{\mathrm{in}}-V_{\mathrm{o}}-(R_2-r_{\mathrm{C}})I_{\mathrm{o}})}{V_{\mathrm{o}}+V_{\mathrm{D}}+(R_1-r_{\mathrm{C}})I_{\mathrm{o}}}\end{array}\right) \\
q_{\mathrm{C}} &= -\frac{DT_{\mathrm{s}}}{L}\left(1-\frac{D}{2}\frac{(V_{\mathrm{in}}+V_{\mathrm{D}}+(R_1-R_2)I_{\mathrm{o}})(V_{\mathrm{in}}+(R_1-R_2)I_{\mathrm{o}})}{(V_{\mathrm{o}}+V_{\mathrm{D}}+(R_1-r_{\mathrm{C}})I_{\mathrm{o}})^2}\right) \\
q_{\mathrm{in}} &= \frac{DT_{\mathrm{s}}}{L}\left(1-\frac{D}{2}\cdot\frac{2V_{\mathrm{in}}-V_0+(R_1-2R_2+r_{\mathrm{C}})I_{\mathrm{o}}}{V_{\mathrm{o}}+V_{\mathrm{D}}+(R_1-r_{\mathrm{C}})I_{\mathrm{o}}}\right) \\
q_{\mathrm{o}} &= \frac{DT_{\mathrm{s}}r_{\mathrm{C}}}{L}\left(1-\frac{D}{2}\cdot\frac{(V_{\mathrm{in}}+(R_1-R_2)I_{\mathrm{o}})(V_{\mathrm{in}}+V_{\mathrm{D}}+(R_1-R_2)I_{\mathrm{o}})}{(V_{\mathrm{o}}+V_{\mathrm{D}}+(R_1-r_{\mathrm{C}})I_{\mathrm{o}})^2}\right)
\end{aligned}
\tag{20}
$$

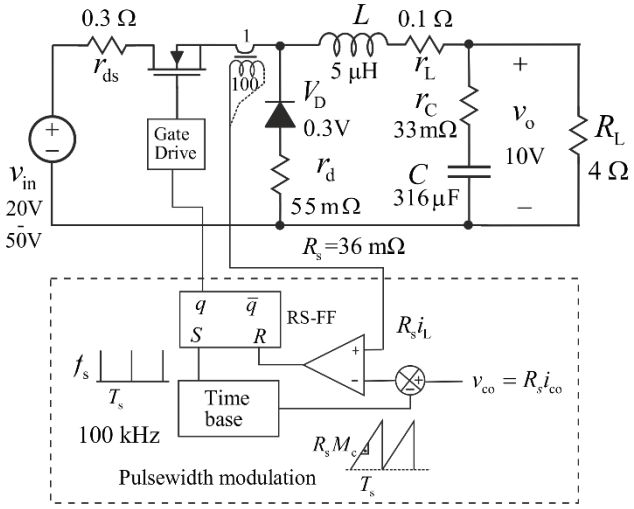

Figure 5. The power stage of the PCM-controlled buck converter in DCM.

In Equation (20), R_1 and R_2 are defined in (17), and M_{c} denotes the inductor-current compensation ramp in A/s. As discussed in the beginning of this section, the PCM state space can be obtained from the DDR state space in (15) by replacing the perturbed duty ratio by (19). As an outcome of this process, the small-signal state space valid for a PCM-controlled buck converter operating in DCM can be given by:

$$
\begin{aligned}
\frac{d\hat{i}_{\mathrm{L}}}{dt} &= -\frac{A_1+F_{\mathrm{m}}q_{\mathrm{L}}V_{\mathrm{e}}}{L}\hat{i}_{\mathrm{L}}-\frac{A_2+F_{\mathrm{m}}q_{\mathrm{C}}V_{\mathrm{e}}}{L}\hat{v}_{\mathrm{C}}+\frac{A_3-F_{\mathrm{m}}q_{\mathrm{in}}V_{\mathrm{e}}}{L}\hat{v}_{\mathrm{in}}+\frac{A_4-F_{\mathrm{m}}q_{\mathrm{o}}V_{\mathrm{e}}}{L}\hat{i}_{\mathrm{o}}+\frac{F_{\mathrm{m}}V_{\mathrm{e}}}{L}\hat{i}_{\mathrm{co}} \\
\frac{d\hat{v}_{\mathrm{C}}}{dt} &= \frac{\hat{i}_{\mathrm{L}}}{C}-\frac{\hat{i}_{\mathrm{o}}}{C} \\
\hat{i}_{\mathrm{in}} &= -(B_1R_2+F_{\mathrm{m}}q_{\mathrm{L}}I_{\mathrm{e}})\hat{i}_{\mathrm{L}}-(B_1+F_{\mathrm{m}}q_{\mathrm{C}}I_{\mathrm{e}})\hat{v}_{\mathrm{C}}+(B_1-F_{\mathrm{m}}q_{\mathrm{in}}I_{\mathrm{e}})\hat{v}_{\mathrm{in}}+(B_1r_{\mathrm{C}}-F_{\mathrm{m}}q_{\mathrm{o}}I_{\mathrm{e}})\hat{i}_{\mathrm{o}}+F_{\mathrm{m}}I_{\mathrm{e}}\hat{i}_{\mathrm{co}} \\
\hat{v}_{\mathrm{o}} &= \hat{v}_{\mathrm{C}}+r_{\mathrm{C}}C\frac{d\hat{v}_{\mathrm{C}}}{dt}
\end{aligned}
\tag{21}
$$

where A_{1-4} and B_1 are defined explicitly in (16) and V_{e}, and I_{e} in (17) as well as F_{m}, q_1, q_{c}, q_{in} and q_0 in (20), respectively.

The transfer functions representing the dynamics of the converter can be solved by applying proper software packages such as, for example, Matlab™ Symbolic Toolbox. The symbolic-form transfer functions representing the input-side dynamics (i.e., the control-to-input-current transfer function, the output-current-to-input-current transfer function, and the input impedance) are very long, and thus only the transfer functions representing the output-side dynamics (i.e., the control-to-output-voltage transfer function ($G_{\mathrm{co-o}}=\hat{v}_{\mathrm{o}}/\hat{i}_{\mathrm{co}}$), audiosusceptibility ($G_{\mathrm{io-o}}=\hat{v}_{\mathrm{o}}/\hat{v}_{\mathrm{in}}$), and output impedance ($Z_{\mathrm{o-o}}=\hat{v}_{\mathrm{o}}/\hat{i}_{\mathrm{o}}$)) are given explicitly in this paper in (22).

Usually, the DCM state spaces are given omitting all the parasitic circuit elements as a function of M and K (cf. pp. 222–224, [14]). We will show later in Section 3 that the simplified transfer functions do not represent correctly the dynamic behavior of the buck converter analyzed in this paper, and therefore, they are not given here. We will use the simplified transfer functions, however, in certain cases for providing better physical insight into the converter dynamics, when performing approximate analyses.

The three transfer functions comprising the output dynamics of the PCM-controlled buck converter in DCM are given in (22). The unterminated denominator (Δ) of the transfer functions is given in (23). The load-resistor-affected denominator is given in (24):

$$\begin{aligned} \Delta Z_{\mathrm{o-o}}^{\mathrm{PCM}} &= \tfrac{sL+\mathrm{A}_1-\mathrm{A}_4+F_\mathrm{m}V_\mathrm{e}(q_\mathrm{L}+q_\mathrm{o})}{LC}(1+sr_\mathrm{C}C) \\ \Delta G_{\mathrm{io-o}}^{\mathrm{PCM}} &= \tfrac{\mathrm{A}_3-F_\mathrm{m}q_\mathrm{in}V_\mathrm{e}}{LC}(1+sr_\mathrm{C}C) \\ \Delta G_{\mathrm{co-o}}^{\mathrm{PCM}} &= \tfrac{F_\mathrm{m}V_\mathrm{e}}{LC}(1+sr_\mathrm{C}C) \end{aligned} \tag{22}$$

where the unterminated denominator Δ equals:

$$s^2+s\frac{A_1+F_\mathrm{m}q_\mathrm{L}V_\mathrm{e}}{L}+\frac{A_2+F_\mathrm{m}q_\mathrm{C}V_\mathrm{e}}{LC} \tag{23}$$

As discussed in [11], the PCM-controlled converters are highly damped converters, which means that the poles of the system are highly separated (i.e., the low-frequency pole ($\omega_{\text{p-LF}}$) lies close to origin, and the high-frequency pole ($\omega_{\text{p-HF}}$) lies close to infinity). Thus the poles can be approximated from (22) with quite high accuracy by utilizing the properties of a second-order polynomial, and the high separation of the poles, which yield (Note: the last simplified terms in (24) are computed assuming $M_\mathrm{c}=0$):

$$\begin{aligned} \omega_{\text{p-LF}} &\approx -\tfrac{A_2+F_\mathrm{m}q_\mathrm{C}V_\mathrm{e}}{(A_1+F_\mathrm{m}q_\mathrm{L}V_\mathrm{e})C} \approx -\tfrac{1-2M}{1-M}\cdot\tfrac{1}{R_\mathrm{eq}C} \\ \omega_{\text{p-HF}} &\approx -\tfrac{A_1+F_\mathrm{m}q_\mathrm{L}V_\mathrm{e}}{L} \approx -\tfrac{D}{M-D}\cdot\tfrac{R_\mathrm{eq}}{L} \end{aligned} \tag{24}$$

where $M=V_\mathrm{o}/V_\mathrm{in}$ and $R_\mathrm{eq}=V_\mathrm{o}/I_\mathrm{o}$ as well as $D=M\sqrt{K/(1-M)}$ and $K=2L/T_\mathrm{s}/R_\mathrm{eq}$ (cf. p. 164, [14]).

Equation (24) shows explicitly that $\omega_{\text{p-LF}}$ becomes an RHP pole, when $M>0.5$ (i.e., the minus sign becomes a plus sign), and it moves into higher frequencies in RHP, when M and D increases. $\omega_{\text{p-HF}}$ stays always as a left-half-plane (LHP) pole, because $M\geq D$, and it moves towards infinity, when M and D increases.

The full-order load-resistor-affected denominator can be given according to (25) but it does not give enough information to understand the effect of the load resistor on the system poles:

$$\begin{aligned} &s^2(1+\tfrac{r_\mathrm{C}}{R_\mathrm{L}})+s(\tfrac{1}{R_\mathrm{L}C}+\tfrac{A_1+F_\mathrm{m}q_\mathrm{L}V_\mathrm{e}}{L}+\tfrac{(A_1-A_4+F_\mathrm{m}V_\mathrm{e}(q_\mathrm{L}+q_\mathrm{o}))r_\mathrm{C}}{R_\mathrm{L}L})+ \\ &\tfrac{A_2+F_\mathrm{m}q_\mathrm{C}V_\mathrm{e}}{LC}+\tfrac{A_1-A_4+F_\mathrm{m}V_\mathrm{e}(q_\mathrm{L}+q_\mathrm{o})}{LCR_\mathrm{L}} \end{aligned} \tag{25}$$

Equation (26) is derived from (25) by omitting the parasitic circuit elements as well as by transforming it into a more customary form according to [10]:

$$s^2+s\left(\frac{1}{R_\mathrm{L}C}+\frac{R_\mathrm{eq}\sqrt{\frac{K}{1-M}}+2F_\mathrm{m}V_\mathrm{in}}{L}\right)+\frac{1}{LC}\left(\frac{R_\mathrm{eq}}{R_\mathrm{L}}+\frac{1}{1-M}\right)\sqrt{\frac{K}{1-M}}+2F_\mathrm{m}V_\mathrm{in}\left(\frac{1}{R_\mathrm{L}}+q_\mathrm{C}\right)) \tag{26}$$

from which the simplified system poles can be solved at fully resistive load (i.e., $R_L = R_{eq}$) as:

$$\begin{aligned}\omega_{\text{p-LF}} &\approx -\frac{\frac{1}{LC}\left(\frac{2-M}{1-M}\right)\sqrt{\frac{K}{1-M}}+2F_m V_{in}\left(\frac{1}{R_{eq}}+q_C\right)}{\frac{1}{R_{eq}C}+\frac{R_{eq}\sqrt{\frac{K}{1-M}}+2F_m V_{in}}{L}} \approx -\frac{\frac{(2-3M)D}{(M-D)(1-M)}}{\frac{L}{R_{eq}}+\frac{D}{M-D}\cdot R_{eq}C} \approx -\frac{(2-3M)}{R_{eq}C(1-M)} \\ \omega_{\text{p-HF}} &\approx -\left(\frac{1}{R_{eq}C}+\frac{R_{eq}\sqrt{\frac{K}{1-M}}+2F_m V_{in}}{L}\right) \approx -\left(\frac{1}{R_{eq}C}+\frac{D}{M-D}\cdot\frac{R_{eq}}{L}\right) \approx -\frac{D}{M-D}\cdot\frac{R_{eq}}{L}\end{aligned} \tag{27}$$

Equation (27) shows that the load-resistor-affected low-frequency pole moves into RHP, when $M > 2/3$, which complies with the instability condition predicted by Equation (12) in Section 2.1. The high-frequency pole equals the high-frequency pole in (24) and stays an LHP pole.

The load-resistor-affected denominator of transfer functions derived from the equivalent circuit representing the dynamics of the buck converter in [11] is explicitly given in [10] as:

$$s^2 + s\left(\frac{1}{R_{eq}C}+\frac{R_{eq}(1-M)}{L(1-2M)}\right)+\frac{1}{LC}\cdot\frac{2-3M}{1-2M} \tag{28}$$

from which the system poles can be approximated to be as:

$$\begin{aligned}\omega_{\text{p-LF}} &\approx -\frac{2-3M}{R_{eq}C(1-M)} \\ \omega_{\text{p-HF}} &\approx -\left(\frac{1}{R_{eq}C}+\frac{R_{eq}(1-M)}{L(1-2M)}\right) \approx -\frac{R_{eq}(1-M)}{L(1-2M)}\end{aligned} \tag{29}$$

When studying carefully the system poles in (29) then it is obvious that the high-frequency pole becomes an RHP pole when $M > 0.5$, and the low-frequency pole becomes an RHP pole when $M > 2/3$. In practice, this means that the converter should be unstable under resistive load already when $M > 0.5$ but the converter has not been observed to behave like that. This means that the modeling method introduced in [11] does not provide correct second-order transfer functions.

The behavior of the system poles is presented in Table 1 in case of the converter in Figure 5, where the high separation of the poles is clearly visible. In addition, the table shows that the instability will take place already at the input voltage of 21.6 V, where $M < 0.5$ due to the contribution of the power-stage losses. The determining factor in the appearing of the open-loop instability is that the zeroth-order coefficients in (23) and (25) become negative, which indicates that one of the roots of (23) and (25) lies in RHP. This happens, because the feedback gain q_C (i.e., the output-capacitor-voltage feedback gain) (cf. Equation (20)) is negative. Actually, the missing of the negative sign of the first-order term indicates that the low-frequency pole is an RHP pole. It is obvious that the appearance of the instability can be controlled by the inductor-loop compensation (M_c), which will reduce F_m (cf. Equation (20)). This form of instability has not been reported earlier even if comprehensive analyses have been performed, for example, in [12]. The reason for this is that the load resistor affects the location of the poles as is visible in the load-resistor-affected poles given in (27) as well as in Table 1 (i.e., two right most columns) [17]. The investigations of this paper show that the load-resistor-affected RHP pole appears in vicinity of $M = 2/3$ as discussed in [10–14] and derived explicitly in Section 2.1 (Equation (12)) and in (27). The power-stage losses will shift the appearance of the instability into an operating point, where $M < 2/3$ as clearly visible in Table 1. The instability in vicinity of $V_{in} \approx 17$ V is also clearly visible in Figure 3 as the second-harmonic mode of operation.

The entries in Table 1 are computed by using the complete models. The coarsely approximated load-resistor-affected system poles in (27) (i.e., the last terms) yield $\omega_{\text{p-LF}} = -126$ Hz and $\omega_{\text{p-HF}} = -307$ kHz at the input voltage of 20 V. The coarsely approximated unterminated system poles in (24) (i.e., the last terms) yield $\omega_{\text{p-LF}} \approx 0$ Hz and $\omega_{\text{p-HF}} = -307$ kHz. These figures indicate that the simplified models will not predict accurately the location of the system poles.

The input-to-output transfer function ($G_{\mathrm{io-o}}^{\mathrm{PCM}}$) (known also as audiosusceptibility in [11]) in (22) can be nullified by providing M_{c} such that $\mathrm{A}_3 - F_{\mathrm{m}} q_{\mathrm{in}} V_{\mathrm{e}} = 0$. The approximate value of M_{c} can be computed to be:

$$M_{\mathrm{c}} = \frac{M(1-M)}{2-M} \frac{V_{\mathrm{in}}}{L} \tag{30}$$

which complies with the value given in [12] (note: the definition of M_{c} in [12] differs from the definition of M_{c} in this paper; when the difference is taken into account, the values are equal).

Table 1. Behavior of the system poles ($\omega_{\text{p-LF}}$ & $\omega_{\text{p-HF}}$) as a function of M and D with $M_{\mathrm{c}} = 0$, $V_{\mathrm{o}} = 10$ V, and $I_{\mathrm{o}} = 2.5$ A.

V_{in}	M	D	$\omega_{\text{p-LF}}$	$\omega_{\text{p-HF}}$	$\omega_{\text{p-LH}}^{R_L}$	$\omega_{\text{p-HF}}^{R_L}$
50 V	0.2	0.117	−87 Hz	−160 kHz	−210 Hz	−160 kHz
30 V	0.333	0.218	−56 Hz	−188 kHz	−180 Hz	−188 kHz
21.6 V	0.463	0.344	1.2 Hz	−233 kHz	−123 Hz	−233 kHz
20 V	0.5	0.388	10 Hz	−253 kHz	−67 Hz	−253 kHz
17.5 V	0.57	0.489	114 Hz	−311 kHz	−12 Hz	−311 kHz
17.2 V	0.58	0.505	133 Hz	−323 kHz	5.7 Hz	−323 kHz

2.4. Generalized Small-Signal Transfer Functions Applicable for Buck, Boost, and Buck-Boost Conveters

The set of PCM transfer functions, which are valid for the buck, boost, and buck-boost converters, can be developed in a generalized form from the block diagrams presented in Figure 6 based on the generalized duty-ratio constraints in (31). In Figure 5, the transfer functions denoted by the superscript 'DDR' corresponds to the set of transfer functions of the corresponding DDR-controlled converter. The coefficients of (31) do not equal exactly the coefficients given in (20), because the output voltage is used as such in computing the inductor-current slopes as Figure 6 explicitly implies. The coefficient H_{sr} denotes a series resonant circuit, which is placed in the inductor-current feedback loop, for correcting the high-frequency phase behavior of the transfer functions (cf. [4]). H_{sr} is given in (32), where $\omega_{\mathrm{sr}} = 2\pi f_{\mathrm{s}}$ and $\zeta = 0.5$ in case of buck converter. The series-resonant circuit in (32) differs significantly from the series-resonant circuit utilized in [4], where $\omega_{\mathrm{sr}} = \pi f_{\mathrm{s}}$ and $\zeta = 0$. The validity of the proposed H_{sr} in case of PCM-controlled DCM buck converter is discussed in more detail in Section 3.

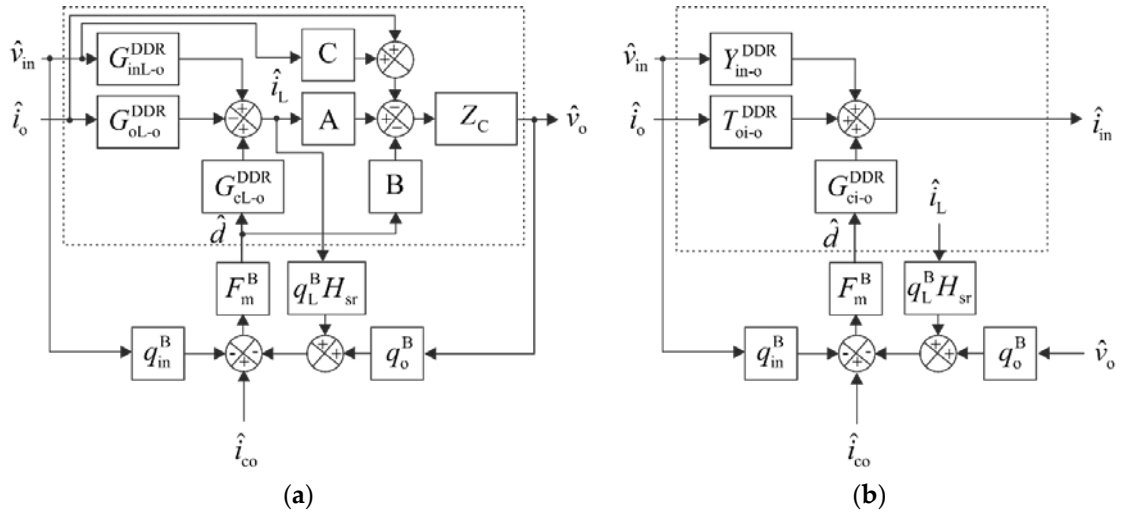

Figure 6. The control-engineering-type block diagrams for computing the general transfer functions representing (**a**) the output dynamics, and (**b**) the input dynamics of the basic second-order converters in DCM.

$$\hat{d} = F_{\mathrm{m}}^{\mathrm{B}}(\hat{i}_{\mathrm{co}} - q_{\mathrm{L}}^{\mathrm{B}} H_{\mathrm{sr}} \hat{i}_{\mathrm{L}} - q_{\mathrm{in}}^{\mathrm{B}} \hat{v}_{\mathrm{in}} - q_{\mathrm{o}}^{\mathrm{B}} \hat{v}_{\mathrm{o}}) \tag{31}$$

$$H_{\mathrm{sr}} = 1 + s\frac{2\zeta}{\omega_{\mathrm{sr}}} + \frac{s^2}{\omega_{\mathrm{sr}}^2} \tag{32}$$

The general set of transfer functions, which is valid for the buck, boost, and buck-boost converters, can be given as shown in (33) (the output dynamics) and (34) (the input dynamics), respectively:

$$\begin{aligned} G_{\mathrm{io-o}}^{\mathrm{PCM}} &= \frac{\hat{v}_{\mathrm{o}}}{\hat{v}_{\mathrm{in}}} = \frac{(1+\frac{F_{\mathrm{m}} q_{\mathrm{L}}^{\mathrm{B}} H_{\mathrm{sr}} \mathrm{B}}{\mathrm{A}}) G_{\mathrm{io-o}}^{\mathrm{DDR}} - F_{\mathrm{m}}(q_{\mathrm{in}}^{\mathrm{B}} + \frac{q_{\mathrm{L}}^{\mathrm{B}} H_{\mathrm{sr}} \mathrm{C}}{\mathrm{A}}) G_{\mathrm{co-o}}^{\mathrm{DDR}}}{1+L_{\mathrm{c}}+L_{\mathrm{v}}} \\ Z_{\mathrm{o-o}}^{\mathrm{PCM}} &= \frac{\hat{v}_{\mathrm{o}}}{\hat{i}_{\mathrm{o}}} = \frac{(1+\frac{F_{\mathrm{m}} q_{\mathrm{L}}^{\mathrm{B}} H_{\mathrm{sr}} \mathrm{B}}{\mathrm{A}}) Z_{\mathrm{o-o}}^{\mathrm{DDR}} + \frac{F_{\mathrm{m}} q_{\mathrm{L}}^{\mathrm{B}} H_{\mathrm{sr}}}{\mathrm{A}} G_{\mathrm{co-o}}^{\mathrm{DDR}}}{1+L_{\mathrm{c}}+L_{\mathrm{v}}} \\ G_{\mathrm{co-o}}^{\mathrm{PCM}} &= \frac{\hat{v}_{\mathrm{o}}}{\hat{i}_{\mathrm{co}}} = \frac{F_{\mathrm{m}}^{\mathrm{B}} G_{\mathrm{co-o}}^{\mathrm{DDR}}}{1+L_{\mathrm{c}}+L_{\mathrm{v}}} \end{aligned} \tag{33}$$

$$\begin{aligned} Y_{\mathrm{in-o}}^{\mathrm{PCM}} &= \frac{\hat{i}_{\mathrm{in}}}{\hat{v}_{\mathrm{in}}} = Y_{\mathrm{in-o}}^{\mathrm{DDR}} - \frac{F_{\mathrm{m}}^{\mathrm{B}} G_{\mathrm{ci-o}}^{\mathrm{DDR}}}{1+L_{\mathrm{c}}+L_{\mathrm{v}}}(q_{\mathrm{in}}^{\mathrm{B}} + \frac{q_{\mathrm{L}}^{\mathrm{B}} H_{\mathrm{sr}} \mathrm{C}}{\mathrm{A}} + (q_{\mathrm{o}}^{\mathrm{B}} + \frac{q_{\mathrm{L}}^{\mathrm{B}} H_{\mathrm{sr}}}{\mathrm{A} Z_{\mathrm{C}}}) G_{\mathrm{io-o}}^{\mathrm{DDR}}) \\ T_{\mathrm{oi-o}}^{\mathrm{PCM}} &= \frac{\hat{i}_{\mathrm{in}}}{\hat{i}_{\mathrm{o}}} = T_{\mathrm{oi-o}}^{\mathrm{DDR}} + \frac{F_{\mathrm{m}} G_{\mathrm{ci-o}}^{\mathrm{DDR}}}{1+L_{\mathrm{c}}+L_{\mathrm{v}}}((q_{\mathrm{o}}^{\mathrm{B}} + \frac{q_{\mathrm{L}}^{\mathrm{B}} H_{\mathrm{sr}}}{\mathrm{A} Z_{\mathrm{C}}}) Z_{\mathrm{o-o}}^{\mathrm{DDR}} - \frac{q_{\mathrm{L}}^{\mathrm{B}} H_{\mathrm{sr}}}{\mathrm{A}}) \\ G_{\mathrm{ci-o}}^{\mathrm{PCM}} &= \frac{\hat{i}_{\mathrm{in}}}{\hat{i}_{\mathrm{co}}} = \frac{F_{\mathrm{m}} G_{\mathrm{ci-o}}^{\mathrm{DDR}}}{1+L_{\mathrm{c}}+L_{\mathrm{v}}} \end{aligned} \tag{34}$$

where L_{c} and L_{v} denote the inductor-current and output-voltage loop gains (i.e., $G_{\mathrm{cL-o}}^{\mathrm{DDR}}$ and $G_{\mathrm{co-o}}^{\mathrm{DDR}}$ denote the control-to-inductor-current and control-to-output-voltage transfer functions of the DDR-controlled converter) given in (35):

$$\begin{aligned} L_{\mathrm{c}} &= F_{\mathrm{m}} q_{\mathrm{L}}^{\mathrm{B}} H_{\mathrm{sr}} G_{\mathrm{cL-o}}^{\mathrm{DDR}} \\ L_{\mathrm{v}} &= F_{\mathrm{m}} q_{\mathrm{o}}^{\mathrm{B}} G_{\mathrm{co-o}}^{\mathrm{DDR}} \end{aligned} \tag{35}$$

and Z_{C} denotes the impedance of the output capacitor, as well as A = 1, B = 0, and C = 0 for a buck converter, and A, B, and C are defined in (36) for boost and buck-boost converters, respectively:

$$\mathrm{A} = 1 - \frac{D^2 T_{\mathrm{s}}}{2L}(r_{\mathrm{L}} + r_{\mathrm{ds}})\ \mathrm{B} = \frac{D T_{\mathrm{s}}}{L} V_{\mathrm{in}}\ \mathrm{C} = \frac{D^2 T_{\mathrm{s}}}{2L} \tag{36}$$

The duty-ratio constrains applicable for (32) and (33) can be obtained from (19) by setting $r_{\mathrm{C}} = 0$ as:

$$\begin{aligned} F_{\mathrm{m}}^{\mathrm{B}} &\approx F_{\mathrm{m}} \\ q_{\mathrm{L}}^{\mathrm{B}} &\approx q_{\mathrm{L}} \\ q_{\mathrm{in}}^{\mathrm{B}} &\approx q_{\mathrm{in}} \\ q_{\mathrm{o}}^{\mathrm{B}} &\approx q_{\mathrm{C}} \end{aligned} \tag{37}$$

as well as $G_{\mathrm{cL-o}}^{\mathrm{DDR}}$ and $G_{\mathrm{co-o}}^{\mathrm{DDR}}$ for computing $G_{\mathrm{co-o}}^{\mathrm{PCM}}$ in (33) can be given for a buck converter as:

$$G_{\mathrm{cL-o}}^{\mathrm{DDR}} = \frac{\hat{i}_{\mathrm{L}}}{\hat{i}_{\mathrm{co}}} = \frac{V_{\mathrm{e}} s}{L(s^2 + s\frac{\mathrm{A}_1}{L} + \frac{\mathrm{A}_2}{LC})} G_{\mathrm{co-o}}^{\mathrm{DDR}} = \frac{\hat{v}_{\mathrm{o}}}{\hat{i}_{\mathrm{co}}} = \frac{V_{\mathrm{e}}(1 + s r_{\mathrm{C}} C)}{LC(s^2 + s\frac{\mathrm{A}_1}{L} + \frac{\mathrm{A}_2}{LC})} \tag{38}$$

where the coefficients $A_{1,2}$ are given in (16) and V_{e} in (17), respectively.

3. Simulink-Based Model Validation

As stated earlier, the applied Simulink models for a buck converter are explicitly given in [27]. The principles of the frequency-response-measuring method is described in [22,23]. The method is realized as a Simulink m-file for measuring the frequency responses from the switching models based on Simulink. The pseudo-random binary-sequence technique [22,23], which is utilized in measuring

the frequency responses, will produce increased distribution in the data points, when the injection frequency approaches half the switching frequency [4]. The used component values are defined in Figure 5 (Section 2.3). In the presented frequency responses, the inductor-current sensing resistor (R_s) is assumed to be 1 Ω instead of 36 mΩ (cf. Figure 5) (note: R_s affects the gain of the control-related transfer functions by multiplying the corresponding transfer functions with $1/R_s$ [4]), and the inductor-current compensation $M_c = 0$. As stated in [10,12], the inductor-current-loop compensation is not required in a DCM-operated converter similarly as it is a necessity in CCM-operated converter, because the absolute mode limit will take place in the boundary between the DCM and CCM operation, and the DCM converter has to be designed accordingly. The converter in Figures 4 and 5 is designed to operate in DCM up to $D = 0.75$ (i.e., $K_{crit} = D' = 2Lf_s/R_{eq} = 0.25$; cf. [11]).

3.1. Open-Loop Validation

Figure 7 shows the set of control-to-output-voltage transfer functions, where the simulated transfer functions are denoted by dashed lines (i.e., unterminated: red and load-resistor affected: blue). The solid black lines denote the predicted transfer functions, respectively. The operating point of the converter corresponds to M = 0.5. The red responses in Figure 7 indicate that the unterminated converter would be unstable in open loop due to the existence of an RHP pole (i.e., the zeroth-order term in the denominator has become negative, which has caused a change of 180 degrees in the phase behavior at the low frequencies). The dashed blue line (i.e., the load-resistor-affected response) indicate that the load resistor has shifted the appearance of the RHP pole to the higher values of M compared to the unterminated case. Figure 7 shows also that the simulated phase behavior deviates from the averaged-model-based prediction as it does in PCM-controlled CCM converter as well [4]. The phase deviation starts already in vicinity of 10 kHz (i.e., at 1/10th of switching frequency). In CCM, the phase deviation is observed to start at 1/5th of the switching frequency [4]. This kind of phase deviation has not been reported earlier to take place in a PCM-controlled DCM-operated converter. As Figure 7 indicates, the predicted and simulated responses match very well. The unterminated G_{co-o} is solved computationally according to $G_{co-o} = (1 + Z_{o-o}/R_L) \cdot G^{R_L}_{co-o}$ by means of the corresponding simulated responses (i.e., Z_{o-o} and $G^{R_L}_{co-o}$) [4].

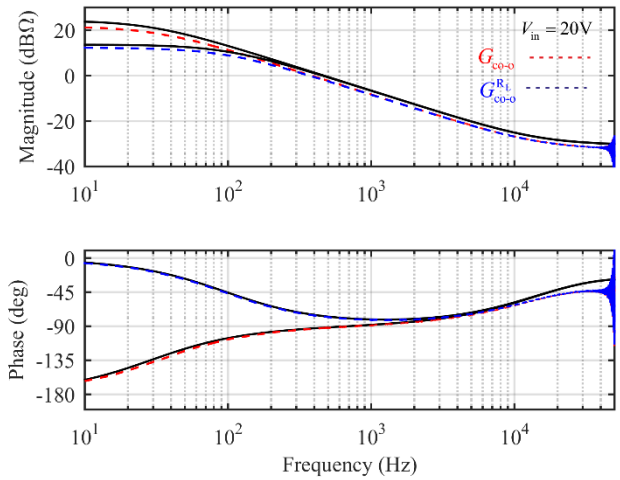

Figure 7. The control-to-output-voltage transfer function as unterminated (G_{co-o}) (red dashed line) and as resistor-load-affected ($G^{R_L}_{co-o}$) (blue dashed line) at the input voltage of 20 V. The predicted responses are denoted by solid black line and the simulated by dashed line, respectively.

Figure 8 shows the simulated (dashed red line) and predicted (solid black line) control-to-output-voltage transfer functions, when the high-frequency extension (H_{sr}) in Equation (32) with

$\omega_{sr} = 2\pi f_s$ (i.e., f_s denotes the switching frequency) and $\zeta = 0.5$ (i.e., ζ denotes the damping factor) have been taken into account in the prediction.

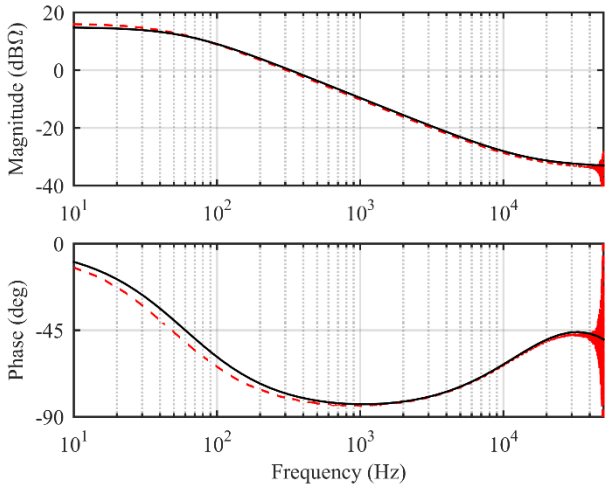

Figure 8. The unterminated control-to-output-voltage transfer function (G_{co-o}) (measured: dashed read line, predicted: solid black line) at the input voltage of 30 V. The high-frequency extension (H_{sr}) (Equation (32)) is added into the prediction.

The match between the simulated and predicted responses is very good. In case of PCM control in CCM, the $\omega_{sr} = \pi f_s$ and $\zeta = 0$, respectively, for obtaining similar match between the simulated and predicted responses as in [4].

Figure 9 shows the simulated (dashed lines) and predicted (solid black lines) output impedances of the converter at the input voltages of 20 V (read color) and 30 V (blue color). The figure shows that the average-model-based prediction matches well also at the high frequencies. The same phenomenon takes place also in PCM-controlled CCM converter as shown in [4]. The absence of the excess phase shift is caused by the output-terminal capacitor, which removes the internal high-frequency behavior from the output impedance (cf. [4]). The open-loop instability at $M = 0.5$ is also clearly visible in the output impedance. The output impedance can be measured directly even if the converter is loaded with a resistor or whatever load impedance.

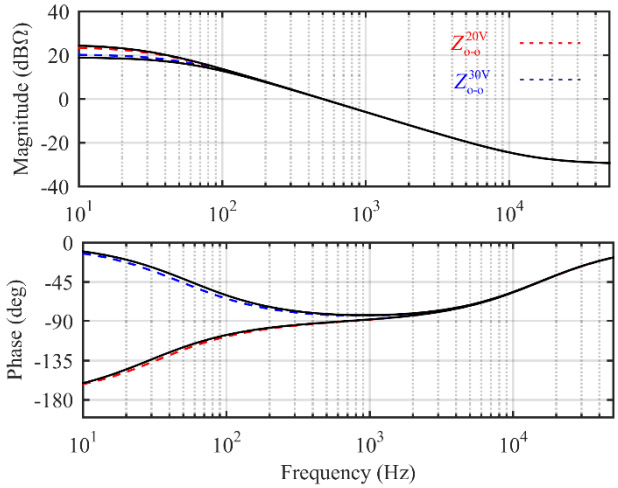

Figure 9. The output impedance (Z_{o-o}) (measured: dashed lines, predicted: solid black line) at the input voltage of 20 V (red color) and 30 V (blue color). The high-frequency extension (H_{sr}) (Equation (32)) is added into the predictions.

Figure 10 shows the comparison of the predicted frequency responses of the control-to-output-voltage transfer functions when the predictions are based on the simplified models (solid lines: 20 V (red) and 50 V (blue)) and on the complete models (dashed lines: 20 V (red) and 50 V (blue)). The responses show that both the models predict the responses with equal accuracy at high input voltage but the prediction accuracy of the simplified model is quite poor at the low input voltages.

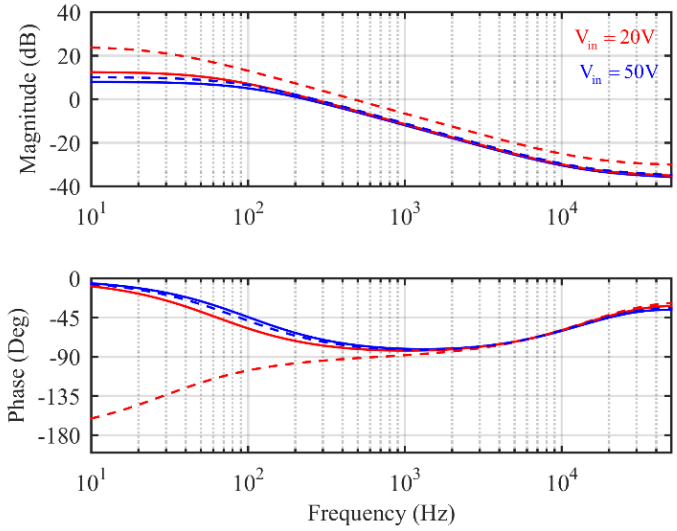

Figure 10. The predicted frequency responses of the control-to-output transfer functions at the input voltage of 20 V (red lines) and 50 V (blue lines). The solid lines denote the responses predicted by means of the simplified models and the dashed lines the responses predicted by the complete models.

3.2. Closed-Loop Validation

The output-voltage loop was designed to have the crossover frequency of 10 kHz and the phase margin (PM) of 60 degrees by using Type-2 controller shown in (39). The controller design was performed at the input voltage of 50 V. The controller zero (ω_z) was placed at $1/\sqrt{LC}$, and the high-frequency pole (ω_p) at $\pi f_s/4$, which require to use the controller gain (K_{cc}) of 851,138 to obtain the crossover frequency of 10 kHz, respectively:

$$G_{cc} = \frac{K_{cc}(1 + s/\omega_z)}{s(1 + s/\omega_p)} \tag{39}$$

Figure 11 shows the simulated (dashed lines) and predicted (solid black lines) output-voltage loop gains at the input voltage of 20 V (magenta color), 30 V (blue color), and 50 V (red color). The figure shows also that the converter is stable at 20 V, because the crossover frequency is much higher than the frequency of the RHP pole (cf. Table 1 for the low-frequency-pole locations). The figure shows clearly that the crossover frequency and PM does not change along the changes in the input voltage. This behavior is characteristic to the PCM control as discussed in [4]. Figure 7 indicates that the control design can be performed by using the load-resistor-affected $G_{co-o}^{R_L}$, when the output-voltage feedback-loop crossover frequency is placed at the frequencies of 1/10th of switching frequency or higher. In case of output-current-feedback control, it is required to use unterminated models, because the load resistor affects, especially, the high-frequency part of the transfer function as discussed and demonstrated in [4,17].

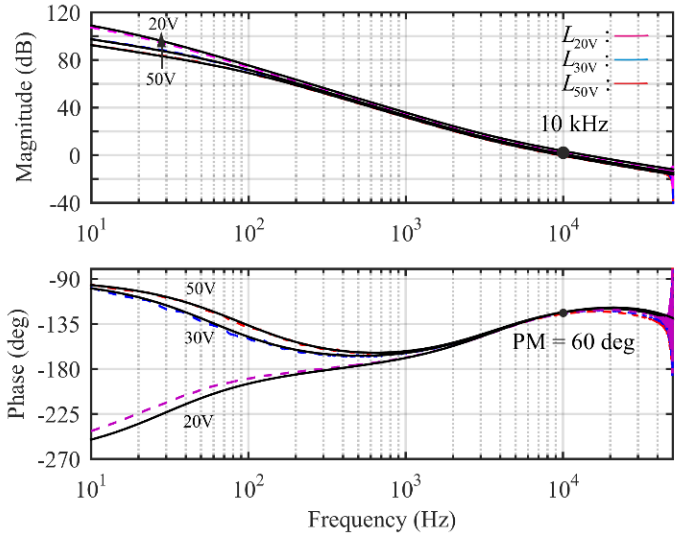

Figure 11. The simulated (dashed lines) and predicted (solid black lines) output-voltage loop gains at the input voltage of 20 V (magenta color), 30 V (blue color), and 50 V (red color), respectively. The high-frequency extension (H_{sr}) (Equation (32)) is added into the prediction.

4. Conclusions

The investigations of this paper show evidently that the method to model the dynamic behavior of a PCM-controlled converter in DCM, which was published in 2001 [10], yields very accurate predictions, when the parasitic circuit elements and the high-frequency extension proposed in this paper are included. In addition, the investigations show that the phase behavior of the DCM-operated PCM-controlled converter exhibits also excess phase shift at the high frequencies but the phase-shift behavior differs from that of the CCM-operated converter [4]. In addition, the buck converter will be unstable in open loop (i.e., an RHP pole appears), when $M > 0.5$, which differs from the earlier predicted instability condition at $M > 2/3$. The stability can be ensured in closed loop by designing the crossover frequency of the feedback control loop to be higher than the RHP pole. The PCM-controlled DCM-operated converter does not need to be compensated either, because the mode limit between the basic switching frequency and the second-harmonic modes of operation will take place at the boundary between the DCM and CCM mode of operation. The mode limit will take place, because the duty-ratio gain becomes infinite at the DCM-CCM-mode boundary similarly as the CCM converter at $D = 0.5$ without the inductor-current-loop compensation. This paper proposes also useful control-engineering-type block diagrams for solving the generalized transfer functions, which are applicable for buck, boost, and buck-boost converters in DCM similarly as presented in [4,13,14] for the PCM-controlled converters operating in CCM.

Conflicts of Interest: The author declares no conflict of interest.

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