

Article

# A Single-Stage Asymmetrical Half-Bridge Flyback Converter with Resonant Operation

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**Abstract:** This paper proposes a single-stage asymmetrical half-bridge fly-back (AHBF) converter with resonant mode using dual-mode control. The presented converter has an integrated boost converter and asymmetrical half-bridge fly-back converter and operates in resonant mode. The boost-cell always operates in discontinuous conduction mode (DCM) to achieve high power factor. The presented converter operates simultaneously using a variable-frequency-controller (VFC) and pulse-width-modulation (PWM) controller. Unlike the conventional single-stage design, the intermediate bus voltage of this controller can be regulated depending on the main power switch duty ratio. The asymmetrical half-bridge fly-back converter utilizes a variable switching frequency controller to achieve the output voltage regulation. The asymmetrical half-bridge fly-back converter can achieve zero-voltage-switching (ZVS) operation and significantly reduce the switching losses. Detailed analysis and design of this single-stage asymmetrical half-bridge fly-back converter with resonant mode is described. A wide AC input voltage ranging from 90 to 264  $V_{rms}$  and output 19 V/120 W prototype converter was built to verify the theoretical analysis and performance of the presented converter.

**Keywords:** fly-back converter; zero-voltage-switching (ZVS); variable-frequency-controller (VFC); single-stage

## 1. Introduction

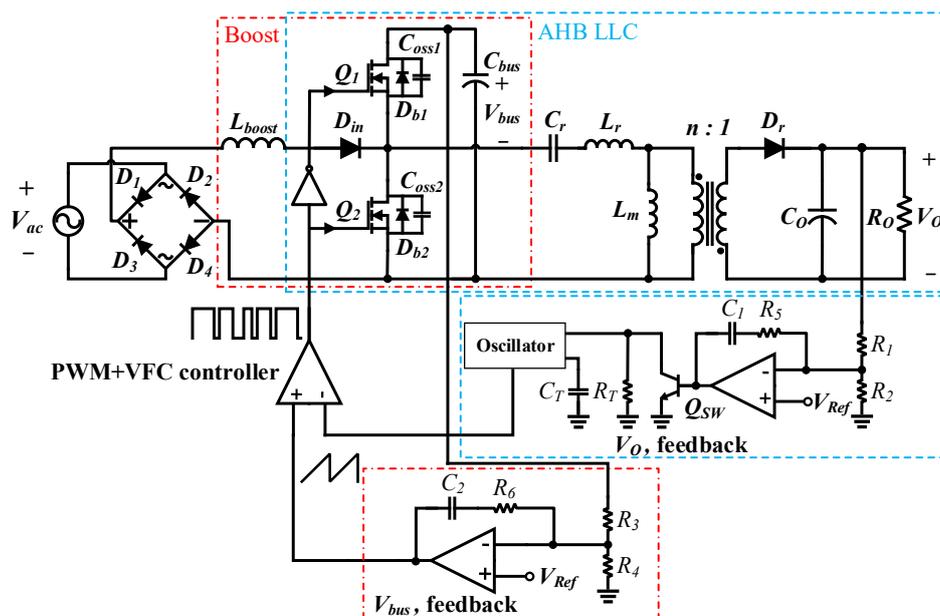
A conventional power supply was designed with a two-stage scheme that can be divided into two parts. The first stage achieves power-factor-correction (PFC) to reduce the input current harmonics. The second stage is a DC/DC converter that regulates the output voltage. However, the two-stage scheme has several defects, such as high cost and power supply system complexity. In recent years, a single-stage scheme was proposed [1–5] that integrates a boost stage and a DC/DC stage to share a common switch. The boost-cell stage operates in discontinuous conduction mode (DCM) to provide high power factor while the DC/DC stage can be responsible for output voltage regulation. Unfortunately, the single-stage scheme presents major problems in which the intermediate bus voltage cannot be regulated, such as the boost integrated flyback rectifier energy DC/DC (BIFRED) converter, single-stage fly-back converter and single-stage LLC resonant converter [6–10]. When voltage is input for universal applications, the intermediate bus voltage could be as high as 1000 V, causing difficulty in selecting converter components, with voltage stress issues throughout the capacitors and switches. The wide intermediate bus voltage variation will cause output voltage regulation design difficulty and also cause lower conversion efficiency through the DC/DC stage. The single-stage scheme intermediate bus voltage cannot be regulated at light loads and universal input voltage. The zero-voltage-switching

(ZVS) fly-back converters have been used widely in industry and are suitable for low-to-medium power applications, such as LED-driver and desktop computer power supplies. Various kinds of ZVS schemes have been proposed, such as the active-clamp network and asymmetrical half-bridge circuit [11,12]. The active-clamp fly-back converter [13] employs the active clamp network to achieve ZVS operation; however, the voltage stresses on the switches are greater than input voltage which will cause high conduction losses in the power switches. The asymmetrical half-bridge fly-back converter (AHBF) with resonant mode [14–20] was developed to achieve ZVS and reduce the voltage stresses on the switches to less than that of the active-clamp fly-back converter, so the power density and conversion efficiency can be effectively increased. Furthermore, it can operate under changed duty cycles or variable switching frequencies for regulated output voltage.

This paper proposes a new single-stage asymmetrical half-bridge fly-back converter with resonant mode. The proposed converter integrates a boost converter and an asymmetrical half-bridge fly-back converter with resonant mode using dual-mode control. The converter intermediate bus voltage can be regulated by the pulse-width-modulation control (PWM). The variable-frequency-controller (VFC) can regulate the converter output voltage. Therefore, this proposed converter can operate in universal input voltage and solves the voltage stress issues throughout the capacitors and switches. The proposed converter utilizes the ZVS technique to decrease the switching losses, resulting in high conversion efficiency. The operational principle for the proposed converter is analyzed, a prototype converter with AC input voltage of 90–264  $V_{rms}$  and output voltage/current of 19 V/8 A is built to verify the analytical results.

## 2. Circuit Description and Principle Operation of Proposed Converter

Figure 1 shows the circuit configuration for the single-stage asymmetrical half-bridge fly-back converter with resonant mode. The primary switches  $Q_1$  and  $Q_2$  operate at asymmetrical duty ratio.  $D_{b1}$  and  $D_{b2}$  are the anti-parallelled power MOSFETs. The primary side diode  $D_{in}$  is a braking diode. The  $L_{boost}$  is a boost-cell inductor. The resonant inductor  $L_r$ , resonant capacitor  $C_r$  and magnetizing inductor  $L_m$  for are the resonant tank for the asymmetrical half-bridge fly-back converter. The secondary diode  $D_r$  is a rectifier diode, the  $C_{bus}$  is boost cell output capacitor and  $C_o$  is the asymmetrical half-bridge fly-back converter output capacitor.



**Figure 1.** Schematic of the proposed single-stage asymmetrical half-bridge fly-back converter with resonant mode.

The following assumptions were made to analyze the proposed single-stage asymmetrical half-bridge fly-back converter:

- These conduction losses of all switches, diodes and layout traces, and the copper losses of the transformer are neglected.
- The turn ratio of the transformer windings is  $n = N_1/N_2$ .
- The resonant inductor  $L_r$  is composed of a leakage inductor and external inductor, where  $L_r = L_{leakage} + L_{ex}$ .
- The conduction times for  $Q_1$  are  $(1 - D)T_s$  and  $Q_2$  is  $DT_s$ , respectively, where  $D$  is the duty cycle for  $Q_2$ , and  $T_s$  denotes the switching period. In addition, the dead time is much smaller than that other of conduction times.
- In the steady state the bus capacitance  $C_{bus}$  and output capacitance  $C_O$  are large enough so that the bus voltage  $V_{bus}$  and output voltage  $V_O$  are a constant value.

Both the boost-cell stage and asymmetrical half-bridge fly-back converter stage share the common switches  $Q_1$  and  $Q_2$ , and furthermore there is bus capacitor  $C_{bus}$  between the two stages. The boost-cell stage was presented in [21]. When the switch  $Q_2$  is turned on and the switch  $Q_1$  is turned off, this results in a positive voltage  $V_{Lboost} = V_{IN}$  across the inductor  $L_{boost}$  causing a linear increase in the inductor current  $i_{Lboost}$ . Conversely, when the switch  $Q_1$  is turned on and the switch  $Q_2$  is turned off, the inductor  $L_{boost}$  releases energy to the bus capacitor  $C_{bus}$ . Therefore, from the flux-balance of  $L_{boost}$  under the steady-state,  $V_{bus}$  can be determined as:

$$\frac{V_{bus}}{V_{IN}} = \frac{1}{2} + \frac{\sqrt{1 + 2 \cdot \frac{D^2 \cdot R_{Lbus}}{L \cdot f_s}}}{2} \quad (1)$$

In the DC/DC stage, when the switch  $Q_1$  is turned on, the intermediate bus voltage  $V_{bus}$  will charge  $C_r$ ,  $L_r$  and  $L_m$ . Conversely, when the switch  $Q_2$  is turned on, the secondary diode  $D_r$  conducts and  $L_m$  releases energy to the output load. When the asymmetrical half-bridge fly-back converter operates in resonant mode, the voltage transfer ratio can be expressed as:

$$M = \frac{nV_O}{V_{bus}} = \frac{(1 - D) \cdot \frac{1 - \cos\left[\omega_r \cdot \left(\frac{D}{f_s}\right)\right]}{Z_r \cdot \omega_r}}{\frac{1 - D}{\omega_r} \left[ \frac{1}{n^2 R_o} + \frac{D}{2L_m f_s} \right] \cdot \sin\left[\omega_r \cdot \left(\frac{D}{f_s}\right)\right] + \frac{(1 - D)^2}{n^2 R_o f_s} + \frac{1 - \cos\left[\omega_r \cdot \left(\frac{D}{f_s}\right)\right]}{Z_r \cdot \omega_r}} \quad (2)$$

where:

$$\omega_r = \frac{1}{\sqrt{C_r \cdot L_r}} \quad (3)$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \quad (4)$$

From Equation (2), the voltage transfer ratio of the asymmetrical half-bridge fly-back converter includes relation between the duty ratio  $D$  and switching frequency  $f_s$  simultaneously. Figure 2 shows the relation between the duty ratio  $D$ , switching frequency  $f_s$  and voltage transfer ratio. It shows that when the duty-ratio  $D$  is decreased from 0.35 to 0.65, to maintain fixed voltage gain, the switching frequency can shift from  $f_c$  to  $f_a$  correspondingly. However, Figure 2 also shows that when the switching frequency  $f_s$  or duty ratio  $D$  decreases the voltage gain will be increased. In contrast, when the switching frequency  $f_s$  or duty ratio  $D$  increase, the voltage gain will be decreased.

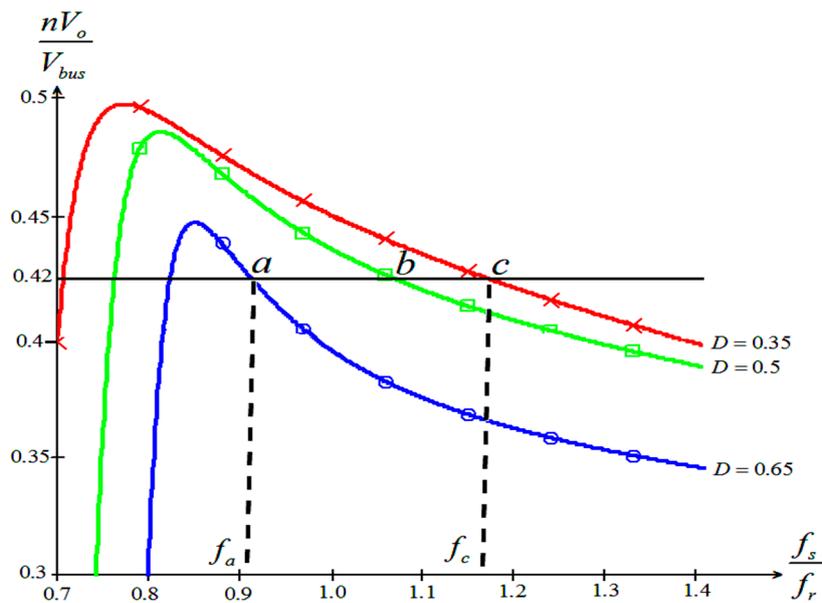
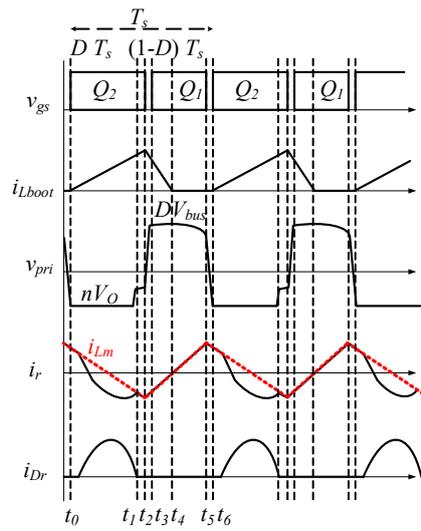


Figure 2. Voltage transfer ratio versus normalized switching frequency.

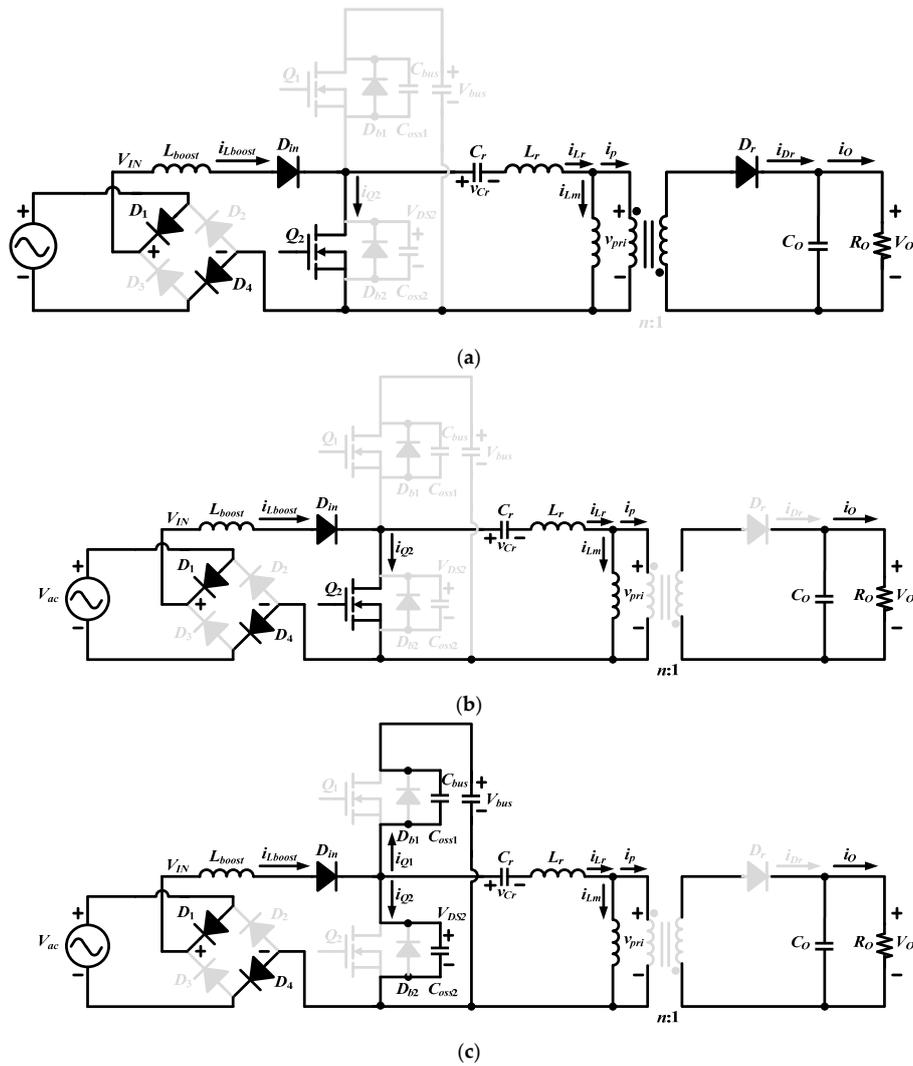
From Figure 1, the resistors  $R_3$  and  $R_4$  can measure output voltage  $V_{bus}$  and it can be to through the compensator, which is composed of  $C_2$ ,  $R_6$  and operational amplifier (OPA). The output voltage of compensator can provide a DC level for PWM + VFC controller, so that the duty ratio can be changed according to  $V_{bus}$ . On the other hand, the  $Q_2$  is the boost-cell stage main switch, therefore the intermediate bus voltage  $V_{bus}$  is regulated by the  $D$  to  $Q_2$  duty ratio. Unfortunately, changing the  $D$  to  $Q_2$  duty ratio will affect the asymmetrical half-bridge fly-back converter output voltage. For example, when the  $D$  to  $Q_2$  duty ratio is increased, the asymmetrical half-bridge fly-back converter output voltage will decrease. Conversely, when the  $D$  to  $Q_2$  duty ratio is decreased, the asymmetrical half-bridge fly-back converter output voltage will increase. To overcome the change in  $D$  to  $Q_2$  duty ratio causing unstable asymmetrical half-bridge fly-back converter output voltage, a VFC has been added to the feedback control loop.

From the section of  $V_O$ -feedback of Figure 1, the resistors  $R_1$  and  $R_2$  can measure output voltage  $V_O$ , and the feedback-voltage can be to through the compensator, which is composed of  $C_1$ ,  $R_5$  and OPA. Therefore, the output of OPA will adjust  $Q_{SW}$  at basis-terminal voltage, so that the oscillator can be changed the frequency of saw-tooth wave in output-terminal. When the asymmetrical half-bridge fly-back converter output voltage is decreased, the switching frequency  $f_s$  will decrease to provide larger voltage gain for regulated output voltage. Conversely, when the output voltage is increased, the switching frequency  $f_s$  will be increased to provide lower voltage gain. According to the above analysis, the intermediate bus voltage  $V_{bus}$  and output voltage  $V_O$  of the proposed converter can be regulated simultaneously from the PWM control and VFC.

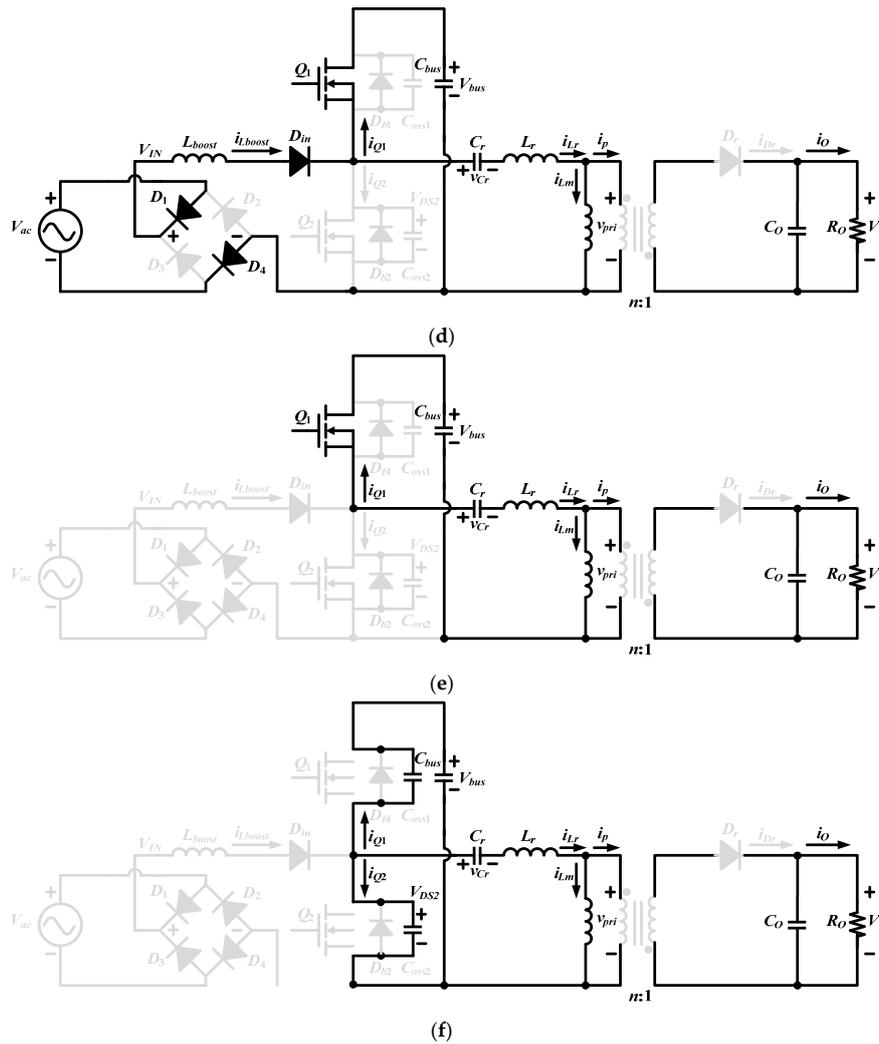
Figure 3 depicts the key waveforms of the proposed single-stage asymmetrical half-bridge fly-back converter with resonant mode. Six states are required to complete a switching cycle. The conduction paths for each operating state are illustrated in Figure 4.



**Figure 3.** Key waveforms of the proposed single-stage asymmetrical half-bridge fly-back converter with resonant mode.



**Figure 4.** Cont.



**Figure 4.** Operation Modes of the proposed single-stage asymmetrical half-bridge fly-back converter during one switching period: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5; (f) Mode 6.

**Mode 1** [ $t_0, t_1$ ]:

As shown in Figure 4,  $Q_2$  is turned on with the ZVS operating condition. In the meantime the rectifier diode  $D_r$  is conducted and the energies stored in the transformer magnetizing inductors are transferred to the output load. The output voltage is reflected to the primary side, therefore, the primary transformer is clamped to  $-nV_o$ , and  $i_{Lm}$  decreases linearly. During this period, the resonant inductor  $L_r$  and resonant capacitor  $C_r$  begin to resonate. On the other hand, the diode  $D_{in}$  is conducted and the voltage across the input inductor  $L_{boost}$  is equal to the input voltage  $V_{IN}$  so the input inductor current  $i_{Lboost}$  increases linearly. The input current  $i_{Lboost}$  can be expressed as:

$$i_{Lboost}(t) = \frac{V_{bus}}{L_{boost}}(t - t_0) \tag{5}$$

The resonant inductor current  $i_{Lr}$  and the resonant capacitor voltage  $v_{Cr}$  are given as:

$$i_{Lr}(t) = i_{Lr}(t_0) \cdot \cos[\omega_r(t - t_0)] - \frac{v_{Cr}(t_0) + nV_o}{Z_r} \cdot \sin[\omega_r(t - t_0)] \tag{6}$$

$$v_{Cr}(t) = nV_o + [v_{Cr}(t_0) + nV_o] \cdot \cos[\omega_r(t - t_0)] + Z_r i_{Lr}(t_0) \cdot \sin[\omega_r(t - t_0)] \tag{7}$$

The magnetizing current  $i_{Lm}$  of transformer can be expressed as

$$i_{Lm}(t) = i_{Lm}(t_0) - \frac{nV_O(t - t_0)}{L_m} \quad (8)$$

This interval is ended when  $i_{Lr}$  equals  $i_{Lm}$  at  $t_1$ .

### Mode 2 [ $t_1, t_2$ ]:

At time  $t_1$  the input inductor current  $i_{L_{boost}}$  increases linearly. The resonant inductor current  $i_{Lr}$  is the same as the magnetizing current  $i_{Lm}$  therefore, no current is transferred to the secondary side so the rectifier diode  $D_r$  is turned off. During this mode, the resonant circuit is composed of  $C_r, L_r$  and  $L_m$ . Moreover,  $L_m$  is equal to series with  $L_r$  and  $L_m$  is much larger than  $L_r$ , so that the resonant cycle is much longer than the previous state. The  $i_{Lm}, i_{Lr}$  and  $v_{Cr}$  are expressed as:

$$i_{Lr}(t) = i_{Lr}(t_1) \cdot \cos[\omega_{r2}(t - t_1)] - \omega_{r2}C_r v_{cr}(t_1) \cdot \sin[\omega_{r2}(t - t_1)] \quad (9)$$

$$v_{Cr}(t) = v_{Cr}(t_1) \cdot \cos[\omega_{r2}(t - t_1)] + L_m i_{Lr}(t_1) \omega_{r2} \cdot \sin[\omega_{r2}(t - t_1)] \\ + L_r i_{Lr}(t_1) \omega_{r2} \cdot \sin[\omega_{r2}(t - t_1)] \quad (10)$$

$$i_{Lm}(t) = i_{Lr}(t) \quad (11)$$

here:

$$\omega_{r2} = \frac{1}{\sqrt{C_r \cdot (L_m + L_r)}} \quad (12)$$

When  $Q_2$  is turned off this interval is ended.

### Mode 3 [ $t_2, t_3$ ]:

The mode begins when  $Q_2$  is turned off at  $t = t_2$ . The magnetizing current  $i_{Lm}$  charges the  $Q_2$  junction capacitors and discharges the  $Q_1$  junction capacitors until the  $Q_2$  junction capacitors equal  $V_{bus}$  and the  $Q_1$  body diode conducts. Therefore, at time  $t_3$ ,  $Q_1$  can be turned on to achieve ZVS. During this period, which is used to allow enough time to achieve ZVS, as well as prevent shoot through in the two switches, the  $i_{Lr}$  and  $v_{Cr}$  are expressed as

$$i_{Lr}(t) = i_{Lr}(t_2) \cdot \cos[\omega_{r1}(t - t_2)] - \omega_{r2}C_r v_{cr}(t_1) \cdot \sin[\omega_{r1}(t - t_2)] \quad (13)$$

$$v_{Cr}(t) = \frac{i_{Lr}(t_2)}{\omega_{r1}C_r} \cdot \sin[\omega_{r1}(t - t_2)] + v_{cr}(t_2) \cdot \cos[\omega_{r1}(t - t_2)] \quad (14)$$

where:

$$\omega_{r1} = \frac{1}{\sqrt{(L_m + L_r) \cdot (C_{eq} || C_r)}} C_{oss1} = C_{oss2}; C_{eq} = C_{oss1} = C_{oss2} \quad (15)$$

The input current  $i_{L_{boost}}$  can be expressed as:

$$i_{L_{boost}}(t) = -\frac{V_{IN} - V_{bus}}{L_{boost}}(t - t_2) \quad (16)$$

### Mode 4 [ $t_3, t_4$ ]:

In this state,  $Q_1$  is turned on which carries the resonant inductor current  $i_{Lr}$  and input inductor current  $i_{L_{boost}}$ . The voltage across the input inductor  $L_{boost}$  is about  $(V_{IN} - V_{bus})$  so the input inductor current  $i_{L_{boost}}$  linearly decreasing. Referring to Figure 4d, the rectifier diode  $D_r$  is reverse-biased and in the meantime the input energy is stored in the primary magnetizing inductance  $L_m$ , while the output capacitors  $C_O$  provide energy to the output load. The resonant inductor current  $i_{Lr}$ , magnetizing inductance current  $i_{Lm}$  and resonant capacitors voltage  $v_{Cr}$  can be expressed as:

$$i_{Lr}(t) = i_{Lr}(t_3) \cdot \cos[\omega_{r2}(t - t_3)] + \omega_{r2}C_r v_{bus} \cdot \sin[\omega_{r2}(t - t_3)] \\ - \omega_{r2}C_r v_{cr}(t_3) \cdot \sin[\omega_{r2}(t - t_3)] \quad (17)$$

$$v_{Cr}(t) = v_{cr}(t_3) + i_{Lr}(t_3) \cdot \cos[\omega_{r2}(t - t_3)] + \omega_{r2}C_r v_{bus} \cdot \sin[\omega_{r2}(t - t_3)] \\ - \omega_{r2}C_r v_{cr}(t_3) \cdot \sin[\omega_{r2}(t - t_3)] \quad (18)$$

$$i_{Lm}(t) = i_{Lr}(t) \quad (19)$$

The input current  $i_{Lboost}$  are given as:

$$i_{Lboost}(t) = -\frac{V_{IN} - V_{bus}}{L_{boost}}(t - t_3) \quad (20)$$

When input current  $i_{Lboost}$  reach zero level, this interval is ended.

**Mode 5** [ $t_4, t_5$ ]:

During this stage,  $Q_1$  remains turned on so that the direction of  $i_{Lr}$  is reversed. As with Stage 4 the primary magnetizing inductance  $L_m$  stores energy and the output capacitors  $C_O$  continue to provide energy through the output load. The current in  $L_{boost}$  stays at zero (DCM operation) so the PFC feature can be achieved. In the meantime, diode  $D_{in}$  is in reverse bias. The resonant inductor current  $i_{Lr}$ , magnetizing inductance current  $i_{Lm}$  and the resonant capacitor voltage  $v_{Cr}$  are given as:

$$i_{Lr}(t) = i_{Lr}(t_4) \cdot \cos[\omega_{r2}(t - t_4)] + \omega_{r2}C_r v_{bus} \cdot \sin[\omega_{r2}(t - t_4)] - \omega_{r2}C_r v_{cr}(t_4) \cdot \sin[\omega_{r2}(t - t_4)] \quad (21)$$

$$v_{Cr}(t) = v_{cr}(t_4) + i_{Lr}(t_4) \cdot \cos[\omega_{r2}(t - t_4)] + \omega_{r2}C_r v_{bus} \cdot \sin[\omega_{r2}(t - t_4)] - \omega_{r2}C_r v_{cr}(t_4) \cdot \sin[\omega_{r2}(t - t_4)] \quad (22)$$

$$i_{Lm}(t) = i_{Lr}(t) \quad (23)$$

where:

$$\omega_{r2} = \frac{1}{\sqrt{C_r \cdot (L_m + L_r)}} \quad (24)$$

When  $Q_1$  turned off, this interval is ended.

**Mode 6** [ $t_5, t_6$ ]:

In this stage,  $Q_1$  and  $Q_2$  are turned off and the input current  $i_{Lboost}$  remains at zero, while the output capacitors continue to provide energy through the output load. At this interval, the resonant current  $i_{Lr}$  charges the  $Q_1$  junction capacitors and discharges the  $Q_2$  junction capacitors. When  $Q_1$  equals  $V_{bus}$  and the body diode across  $Q_2$  conducts, this interval is ended and the operating state returns to Stage 1 to begin the next switching cycle. The resonant inductor current  $i_{Lr}$ , magnetizing inductance current  $i_{Lm}$  and resonant capacitor voltage  $v_{Cr}$  can be expressed as:

$$i_{Lr}(t) = i_{Lr}(t_5) \cdot \cos[\omega_{r1}(t - t_5)] + \omega_{r1}C_r v_{Cr}(t_5) \cdot \sin[\omega_{r1}(t - t_5)] \quad (25)$$

$$v_{Cr}(t) = \frac{I_{Lr}(t_5)}{\omega_{r1}C_r} \cdot \sin[\omega_{r1}(t - t_5)] + v_{Cr}(t_5) \cdot \cos[\omega_{r1}(t - t_5)] \quad (26)$$

$$i_{Lm}(t) = i_{Lr}(t) \quad (27)$$

When Stage 6 ends the operating state returns to Stage 1 and the next switching cycle begins.

### 3. Circuit Design for the Proposed Converter

$D_{max}$  is the maximum duty cycle for the proposed converter. For to achieve high power-factor the input inductor current must be operated in DCM so the input inductor  $L_{boost}$  can be expressed as:

$$L_{boos} < \frac{V_{bus}T_s}{2 \cdot i_{INpeak}f_{smin}} \cdot (D_{max}) \cdot (1 - D_{max})^2 \quad (28)$$

where  $i_{IN peak}$  is the maximum peak-current of the input inductor  $L_{boost}$ , and  $f_{smin}$  is the lowest switching frequency for the proposed converter. From Equation (25), when  $L_m$  is greater than the resonant inductor  $L_r$ , the voltage gain can be approximated as:

$$V_O = \frac{1}{n} V_{bus} \cdot (1 - D) \quad (29)$$

Therefore, the turn ratio of the transformer primary winding to secondary winding can be equal to:

$$n = \frac{V_{bus}}{V_O} \cdot (1 - D) \quad (30)$$

At  $t = t_3$ , to ensure the ZVS operation for  $Q_1$ , the magnetizing inductance current  $i_{L_m}$  must discharge the  $C_{oss1}$  until the voltage is equal to zero so the minimum  $i_{L_m}$  at  $t_3$  can be given as

$$i_{L_m(t_3)\min} = \frac{nV_O}{2L_m} \cdot D_{\min} T_s \quad (31)$$

According to Equation (28), the maximum magnetizing inductance  $L_m$  can be expressed as:

$$L_{m(t_3)\max} = \frac{nV_O \cdot t_{dead}}{2 \cdot V_{bus} (C_{oss1} + C_{oss2}) \cdot f_s} \cdot D_{\min} \quad (32)$$

On the other hand, at  $t = t_6$ , to ensure ZVS operation for  $Q_2$ , the magnetizing inductance current  $i_{L_m}$  must discharge  $C_{oss2}$  until the voltage is equal to zero so the minimum  $i_{L_m}$  at  $t_6$  can be given as:

$$i_{L_m(t_6)\min} = \frac{nV_O}{2 \cdot L_m \cdot f_s} \cdot (1 - D_{\max}) \quad (33)$$

According to Equation (30), the maximum magnetizing inductance  $L_m$  can be expressed as:

$$L_{m(t_6)\max} = \frac{nV_O \cdot t_{dead}}{2 \cdot V_{bus} (C_{oss1} + C_{oss2}) \cdot f_s} \cdot (1 - D_{\max}) \quad (34)$$

From Figure 4a, the resonant capacitor  $C_r$  and the resonant inductor  $L_r$  are resonating from  $t_0$  to  $t_1$ , this time interval is during the  $Q_2$  turn-on time, which is about half the resonant period and can be approximately expressed as:

$$C_r \leq \frac{\left(\frac{2 \cdot D_{\max}}{\omega_r}\right)^2}{L_r} \quad (35)$$

The output filter capacitance  $C_O$  can be calculated as:

$$C_O \geq \frac{P_O \cdot (1 - D_{\max})}{\Delta V_O \cdot f_s} \quad (36)$$

where  $f_s$  is the switching frequency and  $\Delta V_O$  is the output voltage ripple. The voltage stresses of  $Q_1$  and  $Q_2$  are equal to  $V_{bus}$ . The voltage stresses of the secondary diode  $D_r$  is:

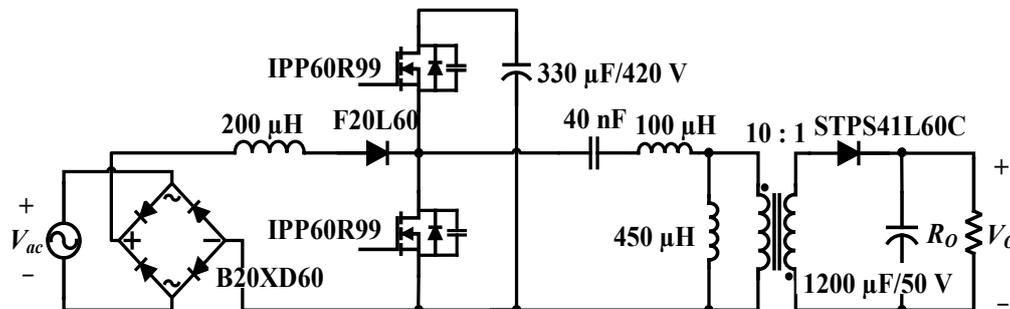
$$D_r = \frac{D_{\max} \cdot V_{bus}}{n} + V_O \quad (37)$$

The peak secondary diode current is expressed as:

$$I_{D_r,\max} = \frac{\pi}{2 \cdot (1 - D_{\max})} \cdot I_O \quad (38)$$

#### 4. Experimental Results

In order to verify the feasibility of the proposed converter, a 120 W prototype converter is built in the laboratory. Figure 5 shows the proposed converter and the experimental parameters are designed in Table 1.



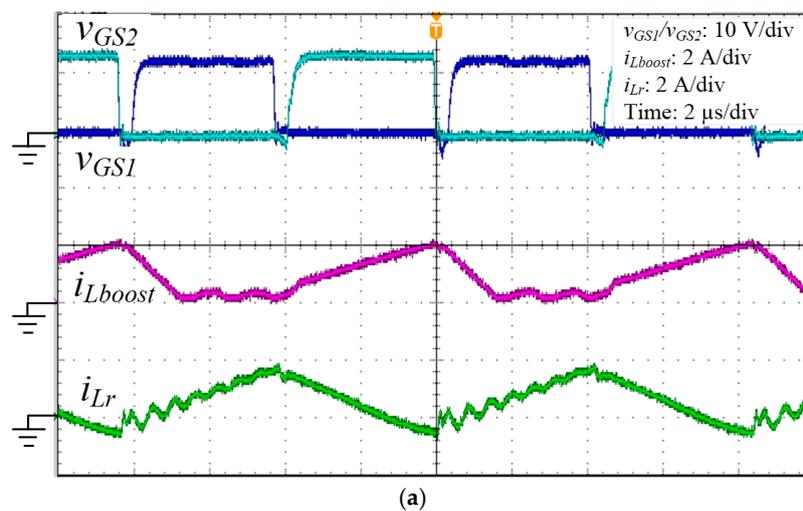
**Figure 5.** Implementation of the proposed single-stage asymmetrical half-bridge fly-back converter with resonant mode.

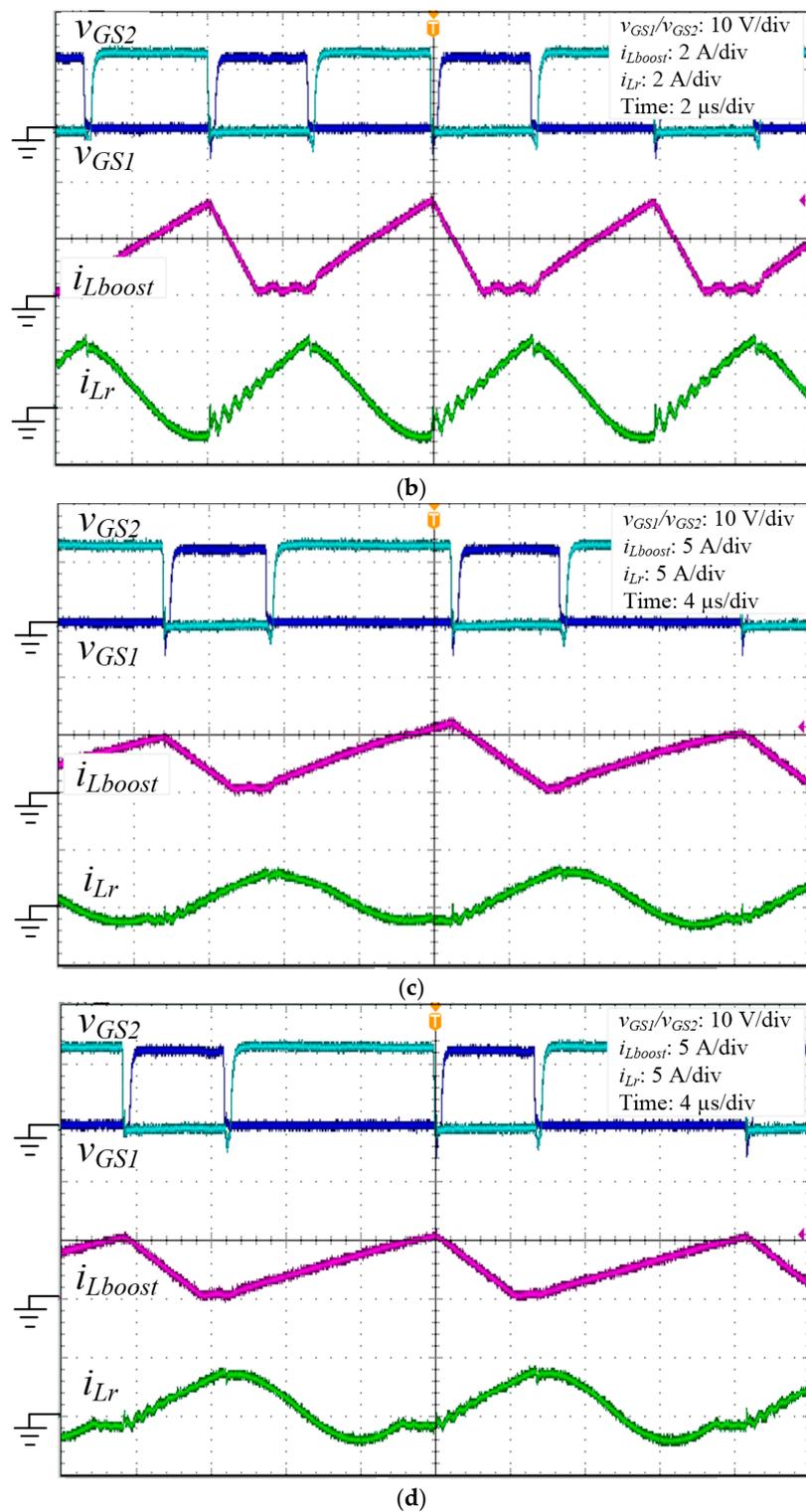
**Table 1.** Experimental parameters of the proposed converter.

Parameters	Value
Input ac voltage range:	85–264 $V_{rms}$
Output voltage:	$V_O = 19$ V
Output voltage ripple:	$\Delta V_O = 0.95$ V
Intermediate bus voltage:	$V_{bus} = 420$ V
Maximum output current:	$I_O = 6.32$ A
Input inductor:	$L_{boost} = 200$ $\mu$ H
Magnetizing inductance:	$L_m = 450$ $\mu$ H
Turns ratio:	$n = N_p/N_s = 3$ T
Resonant inductor:	$L_r = 100$ $\mu$ H
Maximum duty cycle:	$D_{max} = 0.75$
Resonant capacitors:	$C_r = 40$ nF
Switching frequency:	$f_s = 60$ – $150$ kHz
Output capacitor:	$C_O = 1200$ $\mu$ F

A PQ26/20 TDK core is used for the input inductor. The PQ32/30 core is used for the isolation transformer and the transformer turn ratio is calculated from Equation (26). The magnetizing inductance  $L_m$  is designed from Equation (29) at approximately 450  $\mu$ H. The IPP60R99 MOSFET is used producing output capacitance  $C_{OSS}$  of about 130 pF at a 430 V drain-to-source voltage, including the output capacitances of  $Q_1$  and  $Q_2$  it is about 260 pF. Therefore, to ensure ZVS operations, 330 ns dead time was inserted between the  $Q_1$  and  $Q_2$  gate signals. The resonant frequency  $f_r$  is placed at about 80 kHz so the resonant capacitor  $C_r$  and resonant inductor  $L_r$  can be calculated from Equation (32). The output voltage ripple  $\Delta V_O$  is required to be smaller than 0.95 V. The output capacitor  $C_O$  is calculated to be greater than 474  $\mu$ F from Equation (33). Therefore, a 1200  $\mu$ F output capacitor is used.

Figure 6 shows the experimental results for  $v_{GS1}$ ,  $v_{GS2}$ ,  $i_{Lboost}$  and  $i_{Lr}$  at different output currents and at  $V_{In,main}$ . Referring to Figure 3, six operation states can be observed in Figure 6. When  $Q_1$  is turned on and  $Q_2$  is turned off, the  $i_{Lboost}$  linearly decreases and  $i_{Lr}$  linearly increases. When  $Q_1$  and  $Q_2$  are turned off, ZVS operation can be achieved. During the  $Q_1$  turned off and  $Q_2$  turned on period, the  $i_{Lboost}$  increases linearly and the resonant inductor  $L_r$  and resonant capacitor begin to resonate. On the other hand, Figure 6 also shows that when the output load increases from light load to full load, the duty ratio of  $Q_2$  increases from 0.5 to 0.75 for regulated bus voltage  $V_{bus}$ , and the switching frequency decreases from about 125 kHz to 62 kHz for regulated output voltage  $V_O$ . Figure 7 shows the measured input voltage  $v_{ac}$ , input current  $i_{ac}$  and input inductor current  $i_{Lboost}$  under full load conditions. The input current near sinusoidal waveform and input inductor current are shown operated in DCM so that high power factor can be achieved.

**Figure 6.** Cont.



**Figure 6.** Waveforms for  $v_{GS1}$ ,  $v_{GS2}$ ,  $i_{Lboost}$  and  $i_{Lr}$  at different load current: (a) 1.6 A; (b) 3.2 A; (c) 4.7 A; (d) 6.3 A.

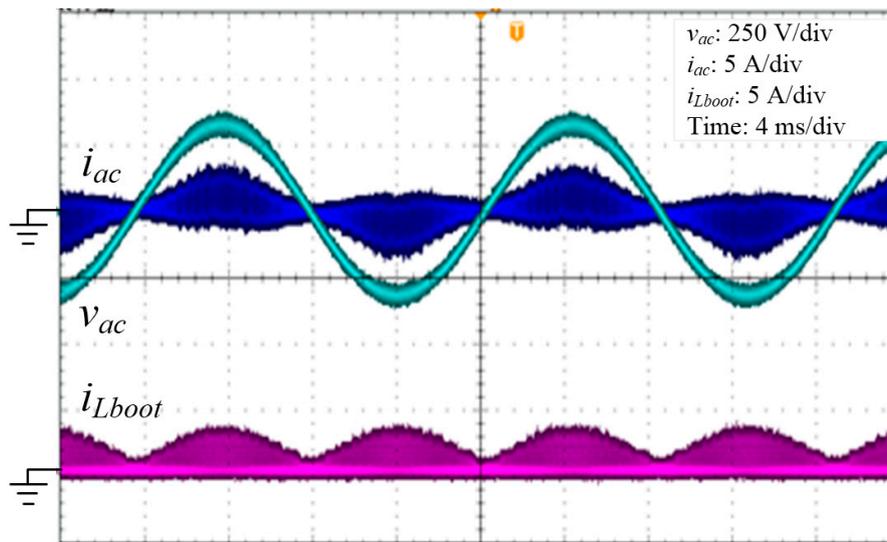


Figure 7. Waveforms for  $v_{ac}$ ,  $i_{ac}$  and  $i_{Lboot}$  at  $v_{ac} = 230 V_{rms}$ .

Figure 8 shows the gate-to-source waveforms and drain-to-source voltages for primary switches  $Q_1$  and  $Q_2$  at the full-load. The waveform shows that  $V_{DS1}$  and  $V_{DS2}$  reach zero levels after  $Q_1$  and  $Q_2$  are turned on. Therefore, ZVS conduction is achieved so that overall conversion efficiency is increased. The transient output voltage  $V_O$  during a step load current from 1.6 to 6.3 A and from 6.3 to 1.6 A are shown in Figure 9 when input voltage of 230  $V_{rms}$ , which shows that  $V_O$  can still be regulated. Figure 10 depicts the bus voltage variation under 25%, 50%, 75% and 100% load condition and the bus voltage is regulated around 430 V. Figure 11 also depicts the input current power factor. It indicates that the power factor is greater than 0.9 at different load conditions. Figure 12 shows the measured efficiencies of the proposed single stage asymmetrical half-bridge fly-back converter through different outputs. The average efficiency is around 86% above which the rated full load efficiency is about 90%.

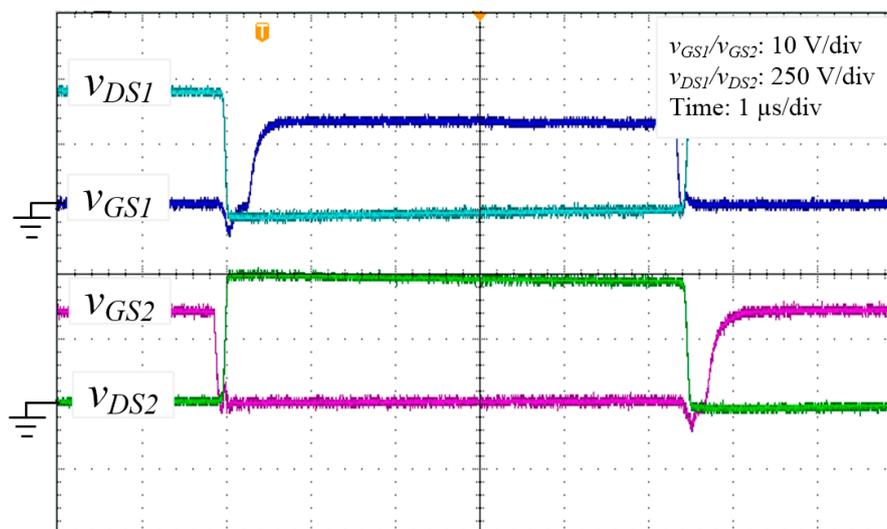


Figure 8. Zero-voltage turn-on switching for  $Q_1$  and  $Q_2$ .

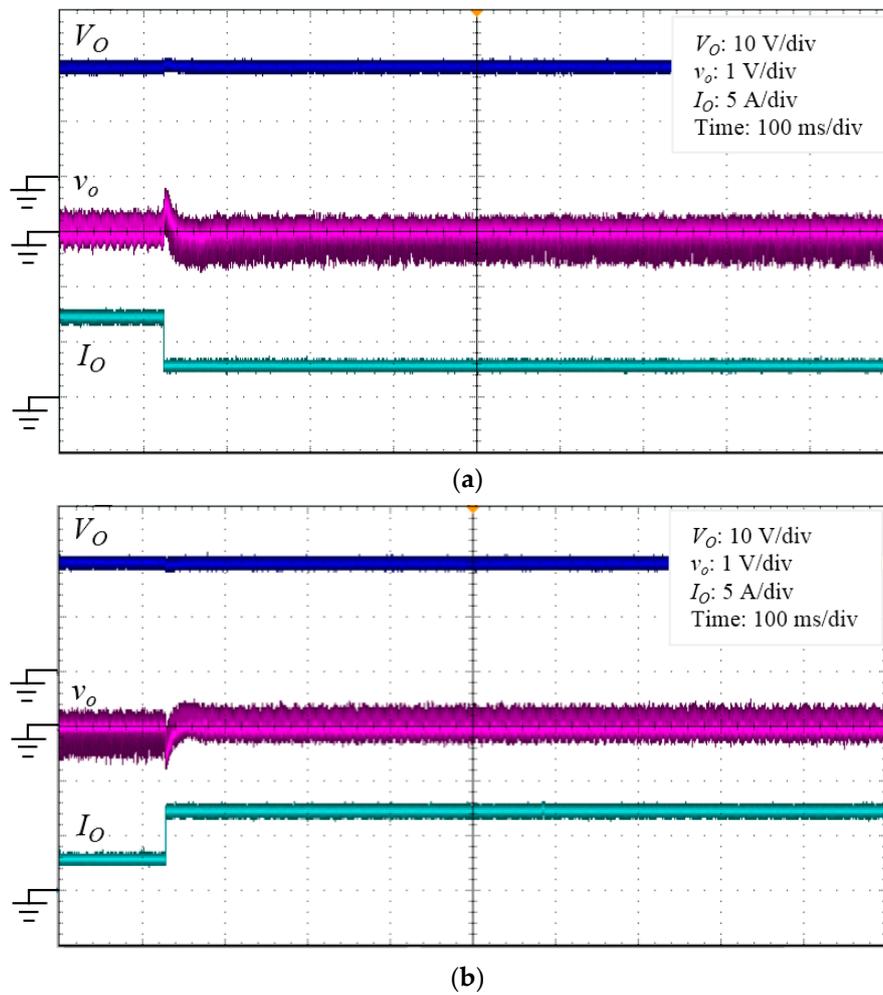


Figure 9. Load transient response under different loads: (a) 20% to 100%; (b) 100% to 20%.

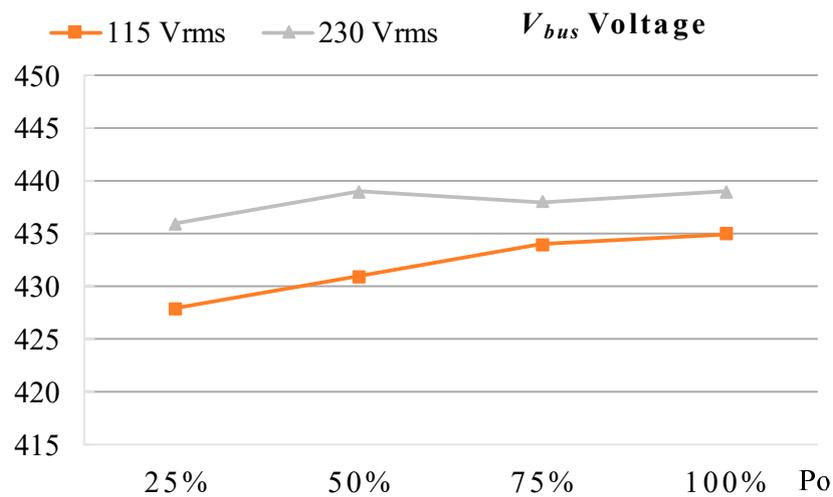


Figure 10.  $V_{bus}$  voltage variation curve for 115  $V_{rms}$  and 230  $V_{rms}$ .

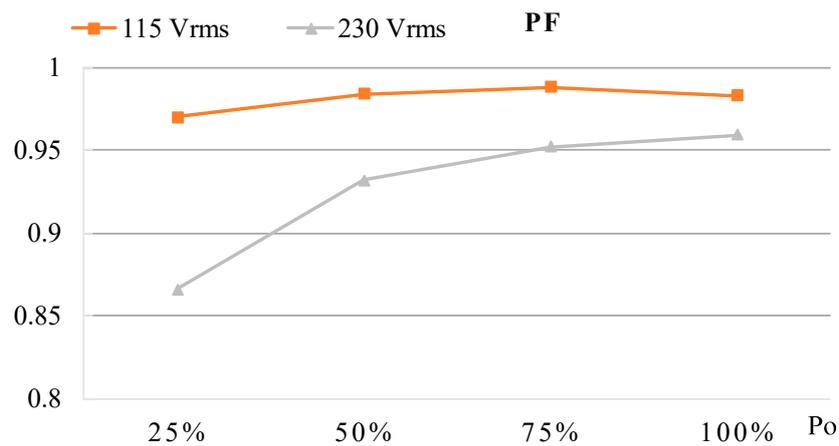


Figure 11. PF curve for 115  $V_{rms}$  and 230  $V_{rms}$ .

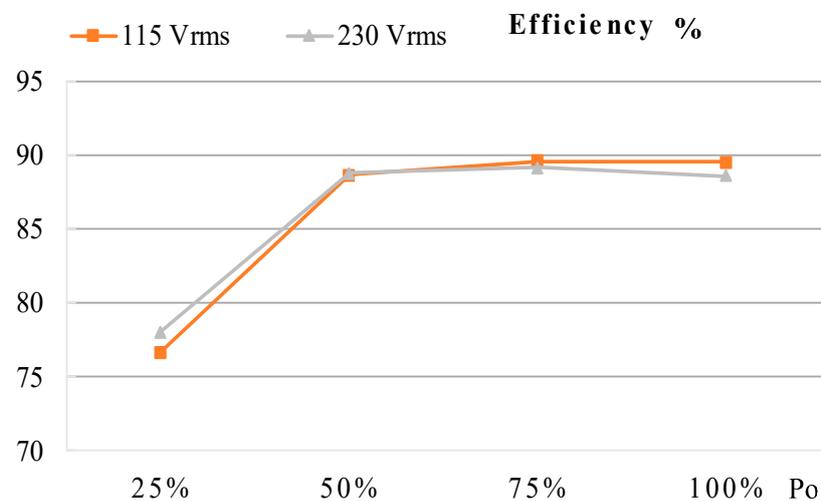


Figure 12. Efficiency curve for 115  $V_{rms}$  and 230  $V_{rms}$ .

Table 2 shows the comparison among the converters proposed in [14,15,17]. Compared with the input voltage range, this presented converter can be operated in universal-voltage, and other converter just can operate in high-line voltage situations. Moreover, this proposed converter has the lowest component cost because it does not need an additional power-device or inductor for a high PF. Figure 13 shows the prototype of the proposed converter.

Table 2. Comparison to the other published methods.

	Proposed Converter	2005 [14]	2012 [15]	2014 [17]
Input Voltage	90–264 $V_{rms}$	180–265 $V_{rms}$	180–270 $V_{rms}$	180–265 $V_{rms}$
Output Voltage	19 V	24 V	24 V	24 V
Switching Frequency	60–150 kHz	100 kHz	99–119 kHz	100 kHz
Efficiency	90%	91%	91.5%	92%
Power Factor	98%	99%	None	99%
ZVS/ZCS	Yes	Yes	Yes	Yes
Control Techniques for power factor	VCF and PWM	Coupled Inductor	Frequency Compensator	PWM
Cost	Low	High	Middle	High

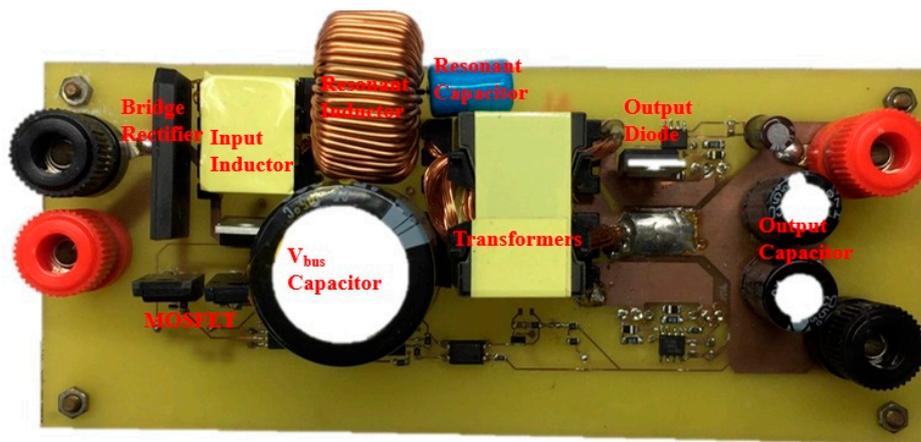


Figure 13. The prototype of the proposed converter.

## 5. Conclusions

This paper presented a single stage asymmetrical half-bridge fly-back converter with resonant mode. The switches operate simultaneously in the variable-frequency-controller (VFC) and pulse-width-modulation (PWM) control to regulate the bus voltage and output voltage. The operating modes in a complete switching cycle were analyzed and discussed in detail. The key equations were derived and the design procedures formulated. The experimental results on an AC input voltage 90 to 264  $V_{rms}$  with output 120 W prototype were recorded to verify the theoretical scheme. The measured results show that the power factor is above 0.9, the average efficiency is around 86% and the highest conversion efficiency is about 90%. The proposed single stage asymmetrical half-bridge fly-back converter is especially suitable for low-to-medium power level applications.

**Author Contributions:** C.-Y.T. designed, simulated the work, and wrote the paper; Y.-C.H. implemented the work and performed the experiment; J.-Y.L. provided all material for implementing the work, supervised the design, circuit simulation, analysis, experiment, and correct the paper.

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