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# Modeling and Parameter Design of Voltage-Controlled Inverters Based on Discrete Control

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**Abstract:** Grid-connected inverters are widely used to interface renewable energy and energy storage resources into the grid. Voltage-controlled inverters have attracted more and more attention due to their grid-friendly characteristics. The mathematical models of the voltage and current loops are developed in this paper, considering especially the discrete control delay caused by calculation and modulation. In order to suppress the resonance peak in the current loop, the frequency characteristics of the current loop are analyzed in detail. The optimum design flow of the current controller and voltage controller parameters are presented based on numerical analysis, and the stability, dynamic performance and the resonance peak suppression in voltage loop are also considered. Finally, the validity of the mathematical model and the effectiveness of the controller parameters design method are verified by simulation and experimental results.

**Keywords:** voltage-controlled inverter; discrete control; parameter design; optimal design

## 1. Introduction

In order to address the issues of the energy crisis and environmental pollution, solar [1,2], wind [3,4] and other renewable energy sources are attracting more and more attention. However, the output of renewable energy sources is stochastic and intermittent. As the vital interface between renewable energy sources and the utility grid, grid-connected inverters [5] have always been a research priority.

Grid-connected inverters can be divided into current-controlled inverters and voltage-controlled inverters according to the control target [6]. Current-controlled inverters take the grid-connected current as the control target, and thus can provide high quality current for the utility grid, but they cannot support the grid voltage, especially when the grid experiences disturbances. There are many control strategies used in current-controlled inverters, such as proportional-integral (PI) control, proportional-resonant (PR) control [7], hysteresis control [8], repetitive control [9] and so on. Voltage-controlled inverters take the output voltage or the capacitor voltage as the control target, so they can support the grid voltage and provide active power for sudden load changes, which benefits the grid voltage and frequency stability. Voltage-controlled inverters include the V-f controlled inverter, droop-controlled inverter [10] and virtual synchronous generator (VSG) [11]. In microgrids, the V-f controlled inverter operates in grid-forming mode as the main voltage source, so it can provide voltage and frequency support to an islanded microgrid [12]. In [13], a power-voltage controlled inverter based on the capacitor voltage feedback control of inductance-capacitor-inductance (LCL) filter is proposed. According to impedance analysis, this inverter is more adaptive under weak grid conditions.

Droop-controlled inverters are used to share the load automatically without communication lines, which can enhance the reliability of the system. In [14], in order to realize power sharing between parallel multi-inverters, an improved robust droop control strategy is proposed. In [15], by modifying the droop coefficients, the impact of line impedance on paralleling current sharing is reduced and the system performance of parallel inverters is improved. The virtual synchronous generator (VSG) can emulate the behavior of a real synchronous generator by controlling the inverter's output frequency. Therefore, VSGs can reduce the frequency fluctuation by providing more active power when the power system frequency drops, which is beneficial for the power system stability. In [16], a VSG named Synchronverter is proposed to emulate the electromagnetic transient process of a synchronous generator, but due to the lack of inner voltage and current loops, overcurrents easily occur in the Synchronverter. In order to protect the switching devices and improve the power quality, voltage and current loops are introduced into VSGs [17].

As most inverters use digital controllers for sampling, calculation and modulation, the delay is inevitable. This will cause a phase lag in the phase-frequency curve of the open-loop transfer function compared with a continuous control system, which complicates the stability analysis and parameter design of the system. Current-controlled inverters based on discrete control have been researched in many papers. In [18], new small-signal z-domain models are deduced for digital current-controlled grid-connected inverters, which allows direct design for controllers in the z-domain. Reference [19] analyzes the stability problem of the grid-connected inverter with an LCL filter adopting a digital controller. According to the stability analysis based on a Nyquist diagram, the inherent damping characteristics due to delay are revealed, and the stability region of the LCL filter and control parameters are obtained. In [20], a real-time computation method with dual sampling mode is proposed to reduce the calculation delay, by which the system robustness and the control performance are greatly improved. There are however few studies on voltage-controlled inverters based on discrete control. Therefore, it is necessary to model the voltage-controlled inverter based on discrete control and investigate the control parameter design flow.

In this paper, a virtual synchronous generator (VSG) is taken as an example to analyze the model of the voltage-controlled inverter and the design of control parameters. The rest of this paper is organized as follows: in Section 2, the VSG schematic and the mathematical models of the voltage and current loops in the VSG are discussed. In Section 3, the parameter design of the current controller is analyzed in detail for the resonance peak suppression. In Section 4, optimum parameter design of the voltage controller is proposed. To verify the correctness of the mathematical model and the validity of parameter design method, simulation results are shown in Section 5. The experiment results are presented to further confirm the validity of the proposed approach in Section 6. Finally, Section 7 concludes this paper.

## 2. Modeling of the Voltage and Current Loops in VSG

The schematic of a VSG with voltage and current loops is shown in Figure 1. The outer loop is the VSG control scheme, and the inner loops are the voltage control and current control, respectively.

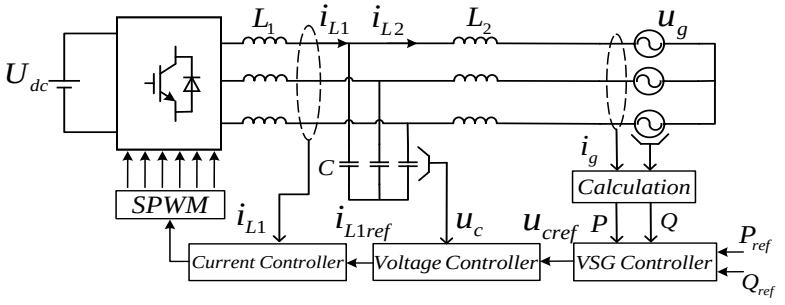


**Figure 1.** Schematic diagram of a virtual synchronous generator (VSG).

The VSG controller provides the references for the cascaded voltage and current controllers in a synchronously rotating reference frame (*dq* reference frame). The voltage controller is utilized to control the capacitor voltage, and the current controller is utilized to control the inductance current. Both the voltage controller and current controller are PI controllers. $U_{dc}$ is the DC voltage source, which is used to represent the renewable energy source. A LCL filter is used to suppress the high-order harmonic currents.

The schematic diagram of the voltage and current controllers is depicted in Figure 2a. The control block diagram of the voltage and current loops in *dq* reference frame is depicted in Figure 2b. Considering the cross-decoupling of the capacitor voltage and the inductance current, the cross-coupling between the *d*-axis and *q*-axis can be approximately eliminated, so Figure 2b only shows the control block diagram in the *d*-axis. $G_v(s)$ and $G_i(s)$ are the transfer functions of the voltage controller and the current controller, respectively; $e^{-sTs}$ is used to represent the calculation delay; $G_h(s)$ is the transfer function of zero-order holder, which is used to represent the modulation delay, and in this paper it can be expressed as $e^{-0.5\,sTs}$. $K_{pwm}$ is the gain of the switching circuit. The switching frequency of the inverter is 10 kHz, and asymmetric regular sampling method is used in the pulse-width modulation (PWM), so the sampling period $T_s$ is equal to 50 μs. In order to improve the response speed of the system, the feedforward of capacitor voltage and grid current is used in the control block diagram, indicated by dotted lines in Figure 2b. The parameters of the system are listed in Table 1.

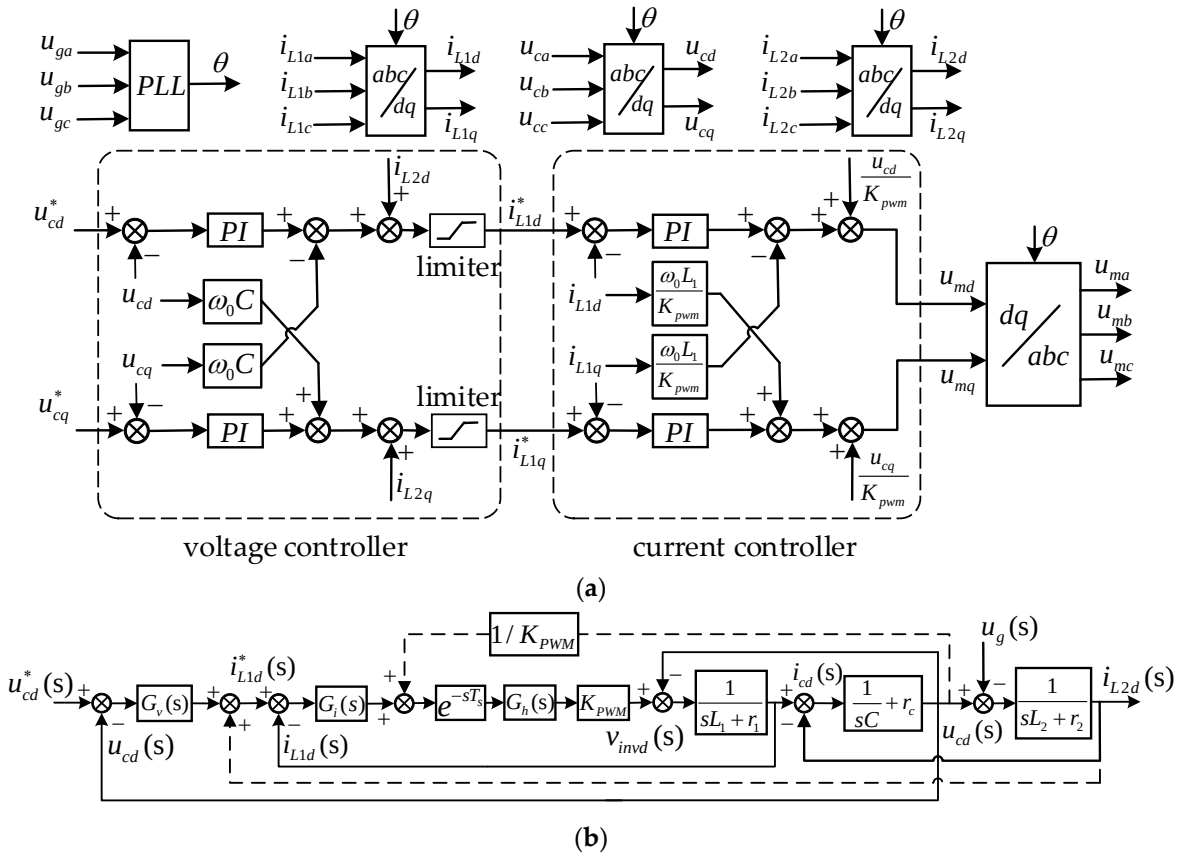


**Figure 2.** Schematic diagram and model of the control part: (**a**) Schematic diagram of the voltage and current controllers; (**b**) Control block diagram of the voltage and current loops in *d*-axis.

**Table 1.** Parameters of the system.

| Elements | Parameters and Values |
| --- | --- |
| DC source | $U_{dc}$ = 380 V |
| Switching circuit | $K_{pwm}$ = 12 |
| LCL filter | $L_1$ = 1.85 mH, $r_1$ = 0.018 Ω<br>$C$ = 35 μF<br>$L_2$ = 570 μH, $r_2$ = 0.23 Ω |
| Utility grid | phase RMS voltage $U_g$ = 110 V |
| PWM modulation | asymmetric regular sampling<br>switching frequency: 10 kHz<br>sampling frequency: 20 kHz |

In order to derive the transfer function of the voltage loop, it is necessary to simplify the control block diagram. The result of the transformation is depicted in Figure 3. The detailed transformation process of the control block diagram is shown in Appendix A.

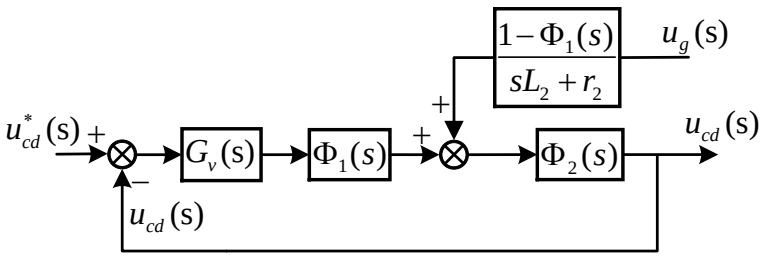


**Figure 3.** Control block diagram of voltage loop after transformation.

The transfer function $\Phi_1(s)$ and $\Phi_2(s)$ can be expressed as:

$$\Phi_1(s) = \frac{G_1(s)}{1 + G_1(s)} = \frac{e^{-1.5sT_s}}{\tau s + e^{-1.5sT_s}}, \tag{1}$$

$$\Phi_2(s) = \frac{G_c(s)}{1 + G_c(s)H_1(s)}, \tag{2}$$

where $H_1(s)$ and $G_c(s)$ can be expressed as:

$$H_1(s) = (\frac{1 - e^{-1.5sT_s}}{sL_1 + r_1} + \frac{1}{sL_2 + r_2})(1 - \Phi_1(s)), \tag{3}$$

$$G_c(s) = \frac{1}{sC} + r_c. \tag{4}$$

In Figure 3, the open-loop transfer function of the voltage loop can be derived as:

$$G_{open}(s) = G_v(s)\Phi_1(s)\Phi_2(s), \tag{5}$$

so the closed-loop transfer function of the voltage loop can be derived as:

$$\Phi_{close}(s) = \frac{G_{open}(s)}{1 + G_{open}(s)}. \tag{6}$$

The detailed transfer functions of the voltage loop are shown in Appendix B.

## 3. Parameter Design of Current Controller

### *3.1. Model of the Current Loop*

The control block diagram of the current loop in *dq* reference frame is depicted in Figure 4.

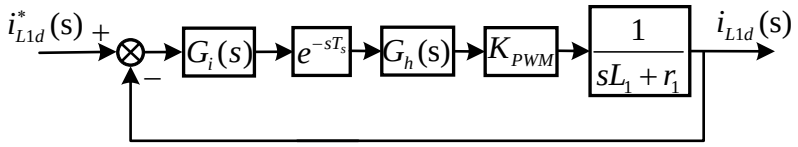


**Figure 4.** Schematic diagram of the current loop.

In Figure 4, the open-loop transfer function of the current loop can be derived as:

$$G_1(s) = G_i(s) \cdot e^{-1.5sT_s} \cdot K_{pwm} \cdot \frac{1}{sL_1 + r_1}, \tag{7}$$

where $G_i(s)$ is the transfer function of current controller, and it can be expressed as $(K_{ip}s + K_{ii})/s$. If $K_{ip}$ and $K_{ii}$ are selected as $K_{ip}/L_1 = K_{ii}/r_1 = k$, then:

$$G_1(s) = \frac{k \cdot K_{pwm}}{s} e^{-1.5sT_s} \tag{8}$$

The closed-loop transfer function of the current loop can be derived as:

$$\Phi_1(s) = \frac{G_1(s)}{1 + G_1(s)} = \frac{e^{-1.5sT_s}}{\tau s + e^{-1.5sT_s}}, \tag{9}$$

where $\tau = 1/(k \cdot K_{pwm})$. If the value of $\tau$ is determined, the value of $k$ is also determined. Then the value of $K_{ip}$ and $K_{ii}$ can also be calculated according to the equation $K_{ip}/L_1 = K_{ii}/r_1 = k$. The cut-off frequency $f_c$ of the current loop can be selected as 2 kHz firstly. Due to $f_c \approx k \cdot K_{pwm}/(2\pi)$, the coefficient $k$ can be derived as $k = 1047.2$, so $\tau = 1/(k \cdot K_{pwm}) = 1.59T_s$. In this case, the frequency characteristics of the current loop are depicted in Figure 5.

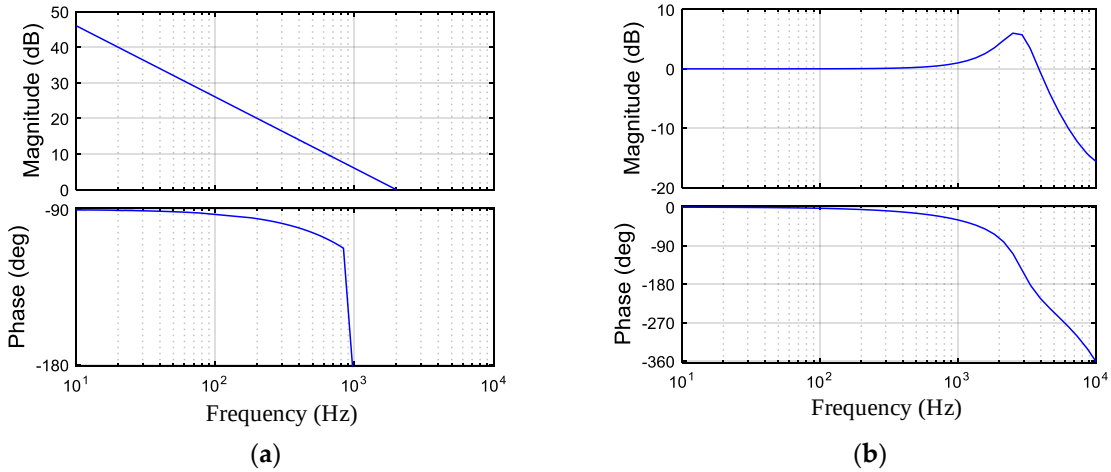


**Figure 5.** Bode diagrams of the current loop with discrete control when $\tau = 1.59T_s$: (**a**) Open-loop Bode diagrams; (**b**) Close-loop Bode diagrams.

In order to show the difference between discrete control and continuous control, frequency characteristics of the current loop with continuous control, in which there is no calculation delay, are depicted in Figure 6.

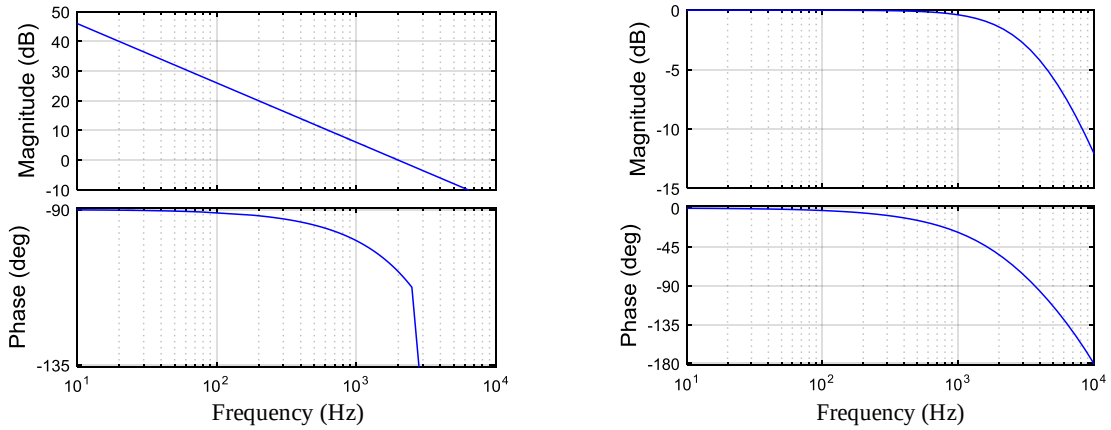


**Figure 6.** Bode diagrams of the current loop with continuous control when $\tau = 1.59T_s$: (**a**) Open-loop Bode diagrams; (**b**) Close-loop Bode diagrams.

Comparing Figure 5 with Figure 6, it can be obviously seen that in the discrete control system there is great phase lag in the phase-frequency curve between the medium and high frequency sections. In addition, there is a resonance peak in the amplitude-frequency curve of closed-loop transfer function in discrete control system, when $\tau$ is equal to $1.59T_s$.

### *3.2. Parameter Design of the Current Loop*

Due to the resonance peak in the amplitude-frequency curve of current closed-loop transfer function when $\tau$ is equal to $1.59T_s$, the harmonic current around resonant frequency is amplified, which is not acceptable, so the suppression of the resonance peak is necessary when designing the parameter $\tau$.

In order to suppress the resonance peak, the amplitude-frequency characteristic of current closed-loop transfer function is analyzed in detail as follows. Replacing $s$ with $j2\pi f$, Equation (9) can be rewritten as:

$$\Phi_1(j2\pi f) = \frac{1}{\tau \cdot j2\pi f \cdot e^{j3\pi f T_s} + 1} = \frac{1}{1 - 2\pi f\tau \sin(3\pi f T_s) + j2\pi f\tau \cos(3\pi f T_s)} \tag{10}$$

Then, the amplitude-frequency characteristic of current closed-loop transfer function can be derived as:

$$\begin{aligned} |\Phi_1(j2\pi f)| &= \frac{1}{\sqrt{[1-2\pi f\tau \sin(3\pi f T_s)]^2 + [2\pi f\tau \cos(3\pi f T_s)]^2}} \\ &= \frac{1}{\sqrt{1-4\pi f\tau \sin(3\pi f T_s) + \tau^2 (2\pi f)^2}} \end{aligned} \tag{11}$$

Defining $g(f) = 1 - 4\pi f\tau \sin(3\pi f T_s) + \tau^2 (2\pi f)^2$, the curve of $g(f)$ is depicted in Figure 7. It can be seen that there is a minimum value point in the curve of $g(f)$, which implies a resonant point in the amplitude-frequency curve of the current loop shown in Figure 5b.

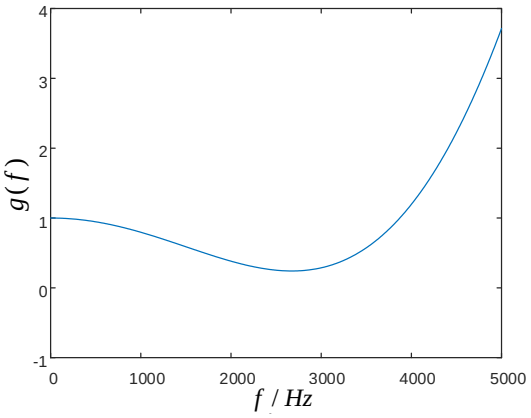


**Figure 7.** The curve of $g(f)$.

In order to suppress the resonance peak in the amplitude-frequency curve of current closed-loop transfer function, it is necessary to increase the minimum value of $g(f)$. The derived function of $g(f)$ can be written as:

$$g'(f) = \tau[4\pi\tau f - 2\sin(3\pi f T_s) - 6\pi f T_s \cos(3\pi f T_s)] \tag{12}$$

When $\tau$ is equal to $1.59T_s$, the curve of the derived function is depicted in Figure 8.

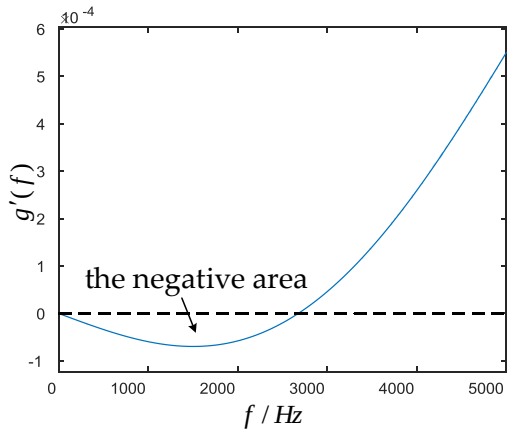


**Figure 8.** The curve of $g'(f)$

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In order to increase the minimum value of $g(f)$, it is necessary to make the negative area of the derived function equal to zero. The derived function is consisted of two parts, which can be expressed as:

$$h_1(f) = 4\pi\tau f \tag{13}$$

$$h_2(f) = -2\sin(3\pi f T_s) - 6\pi f T_s \cos(3\pi f T_s) \tag{14}$$

The curves of $h_1(f)$ and $h_2(f)$ are depicted in Figure 9.

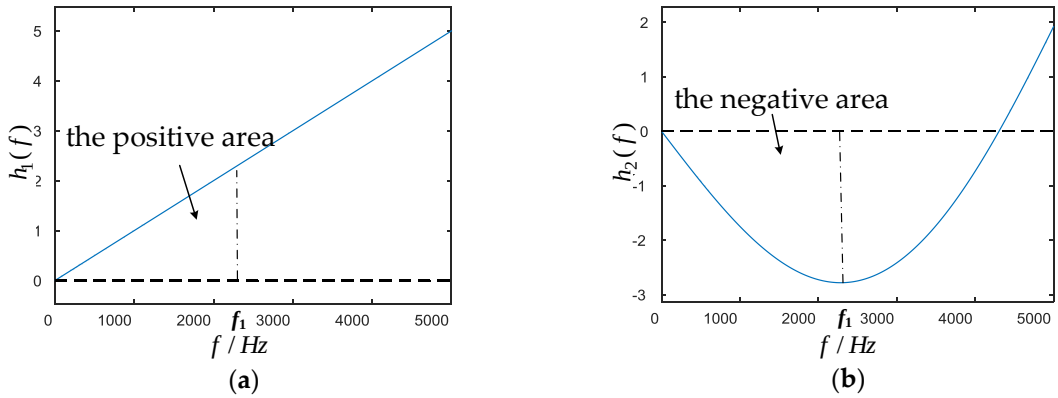



**Figure 9.** The curves of $h_1(f)$ and $h_2(f)$: (**a**) $h_1(f)$; (**b**) $h_2(f)$.

By controlling the positive area of $h_1(f)$ equal to the negative area of $h_2(f)$ between 0 and $f_1$ in number, the negative area of the derived function can be equal to zero. This purpose can be realized approximately by making $h_1{}'(0) = -h_2{}'(0)$. The values of derived function $h_1{}'(f)$ and $h_2{}'(f)$ at $f = 0$ can be expressed as $h_1{}'(0) = 4\pi\tau$ and $h_2{}'(0) = -12\pi T_s$. Then $\tau$ can be derived as $\tau = 3T_s$ according to the equation $h_1{}'(0) = -h_2{}'(0)$. The Bode diagrams of current closed-loop transfer function are depicted in Figure 10, in which it can be seen that the resonance peak is suppressed completely. In addition, it can also be found the bandwidth of the current loop is narrower than that when $\tau = 1.59T_s$, so if the value of $\tau$ is larger, the bandwidth of the current loop is narrower.

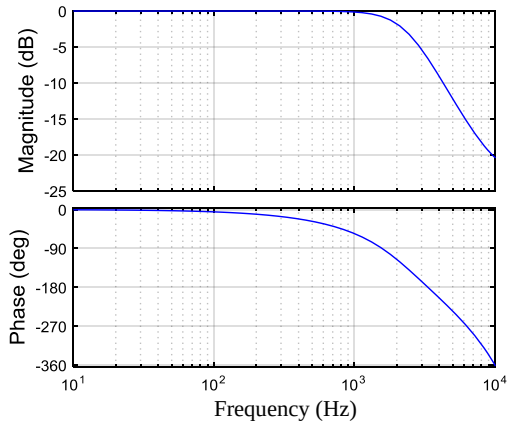



**Figure 10.** Bode diagrams of current closed-loop transfer function when $\tau = 3T_s$.

### *3.3. Summary*

In discrete control system, if the value of $\tau$ is too small, there is a resonance peak in the amplitude-frequency curve of current closed-loop transfer function. However, if the value of $\tau$ is too large, the bandwidth of the current loop will be narrow, so the parameter design of $\tau$ is vital. In this paper, considering the resonance peak suppression and the bandwidth of the current loop, the value of $\tau$ is selected as $3T_s$ to reach a compromise.

## 4. Parameter Design of Voltage Controller

The parameters of the whole system include controller parameters and circuit parameters, such as $U_{dc}$, $L_1$, C and $L_2$. There have been many studies on LCL filters, so the focus of this paper is the parameter design of controllers and the damping resistance in capacitor, including $\tau$, $K_{vp}$, $f_z$ and $r_c$. The current loop parameter $\tau$ has been analyzed in Section 3. $K_{vp}$ is the proportion coefficient of

the voltage controller. $f_z$ is the corner frequency of the voltage controller, and it can be expressed as $K_{vi}/2\pi K_{vp}$. If $f_z$ is determined, the integration coefficient $K_{vi}$ of the voltage controller is also determined. $r_c$ is the value of damping resistances, which are connected in series to the capacitors in LCL filter to suppress the resonance in the LCL filter.

### *4.1. The Effects of These Parameters on the Voltage Loop*

Before designing the parameters $\tau$, $K_{vp}$, $f_z$ and $r_c$, it is necessary to analyze the effects of these parameters on the voltage loop.

#### 4.1.1. The Effects of $\tau$ on the Voltage Loop

We set the various parameters as $r_c = 5\ \Omega$, $K_{vp} = 0.5$, $f_z = 250$ Hz. If we select $\tau$ as $2.5T_s$, $3T_s$ and $4T_s$, respectively, then the Bode diagrams of voltage closed-loop transfer function are as depicted in Figure 11. It can be seen that increasing $\tau$ can suppress the resonance peak in the amplitude-frequency curve. This is consistent with the conclusion that increasing $\tau$ can suppress the resonance peak in the current loop, as analyzed in Section 3.

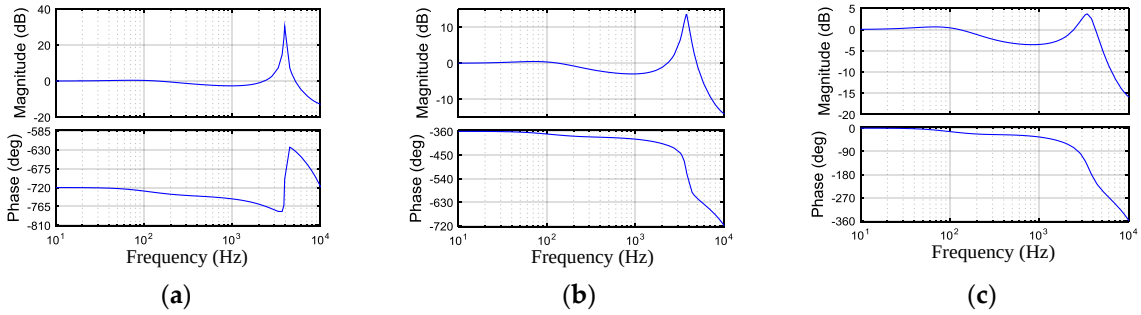



**Figure 11.** Bode diagrams of voltage closed-loop transfer function: (**a**) $\tau = 2.5T_s$; (**b**) $\tau = 3T_s$; (**c**) $\tau = 4T_s$.

#### 4.1.2. The Effects of $r_c$ on the Voltage Loop

We set the several parameters as $\tau = 3T_s$, $K_{vp} = 0.3$, $f_z = 750$ Hz. Selecting $r_c$ as 1 Ω, 2 Ω and 3 Ω, respectively, then the Bode diagrams of voltage closed-loop transfer function are as depicted in Figure 12. It can be seen that increasing $r_c$ can also suppress the resonance peak in the amplitude-frequency curve.

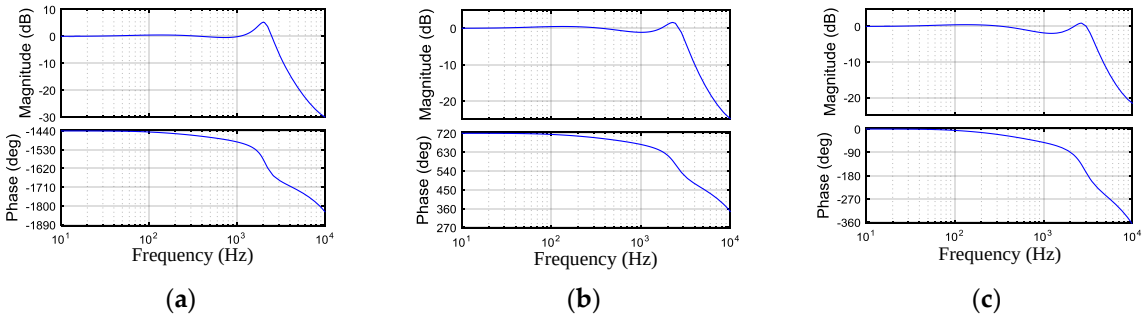



**Figure 12.** Bode diagrams of voltage closed-loop transfer function: (**a**) $r_c = 1\ \Omega$; (**b**) $r_c = 2\ \Omega$; (**c**) $r_c = 3\ \Omega$.

#### 4.1.3. The Effects of $K_{vp}$ on the Voltage Loop

Setting the several parameters as $\tau = 3T_s$, $r_c = 5\ \Omega$, $f_z = 750$ Hz and selecting $K_{vp}$ as 0.3, 0.5 and 0.7, respectively, then the Bode diagrams of voltage closed-loop transfer function are as depicted in

Figure 13. It can be seen that decreasing $K_{vp}$ can suppress the resonance peak in amplitude-frequency curve, which is different from the cases of $\tau$ and $r_c$, so the value of $K_{vp}$ cannot be too large.

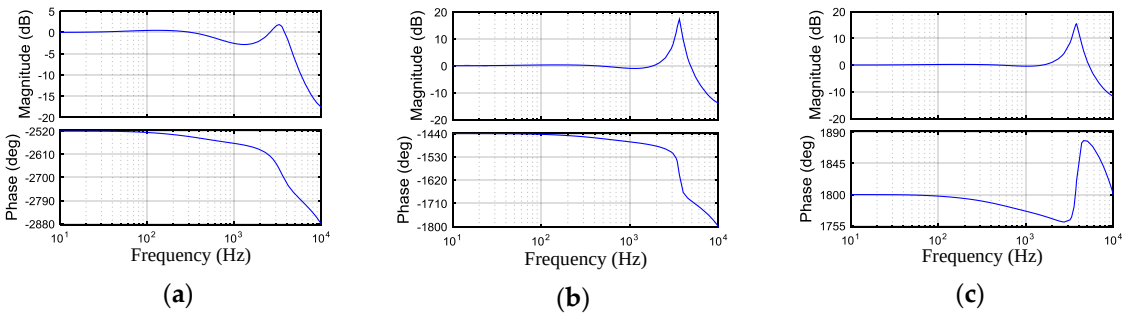



**Figure 13.** Bode diagrams of voltage closed-loop transfer function: (**a**) $K_{vp}$ = 0.3; (**b**) $K_{vp}$ = 0.5; (**c**) $K_{vp}$ = 0.7.

#### 4.1.4. The Effects of $f_z$ on the Voltage Loop

If we set the several parameters as $\tau = 3T_s$, $r_c = 5\Omega$, $K_{vp}$ = 0.5 and select $f_z$ as 250 Hz, 550 Hz and 750 Hz, respectively, then the Bode diagrams of voltage closed-loop transfer function are as depicted in Figure 14. It can be seen that increasing $f_z$ can increase the minimum of the concave part in amplitude-frequency curve, but cannot suppress the resonance peak. If the minimum of the concave part is large enough, the bandwidth of the voltage loop is also wide, so increasing $f_z$ can widen the bandwidth of the voltage loop.

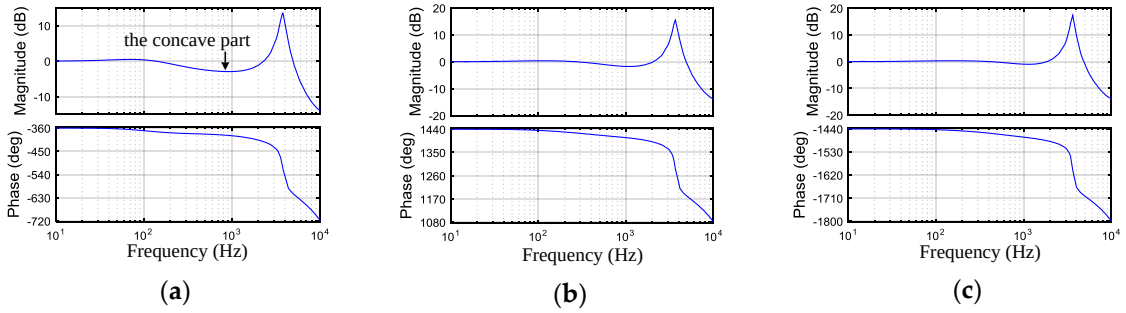



**Figure 14.** Bode diagrams of voltage closed-loop transfer function: (**a**) $f_z$ = 250 Hz; (**b**) $f_z$ = 550 Hz; (**c**) $f_z$ = 750 Hz.

### *4.2. The Optimum Parameter Design*

It can be observed from the above analysis that the improper design of control parameters will lead to resonance peak in the amplitude-frequency curve of the voltage loop. The closed-loop transfer function of the voltage loop is a high order system, which makes it difficult to design the parameters in an analytical way, so in this paper numerical calculation and visualization with slice figures are used in optimum design of parameters. The purposes of the optimum design are as follows:

(1) Considering the resonance peak suppression, make the gain of the resonance peak equal to the minimum of the concave part as possible.
(2) Considering the bandwidth of the voltage loop, make the gain of the resonance peak and the minimum of the concave part larger than –5 dB to ensure the bandwidth of the voltage loop wide enough.
(3) Considering the dynamic properties, make both the overshoot and the settling time of step response as small as possible.

According to the analysis in Section 3, if $\tau$ is larger than $3T_s$, the resonance peak in the current closed-loop transfer function can be suppressed completely, but if $\tau$ is too large, the bandwidth of the current loop is narrow, so the value of $\tau$ is selected as $3T_s$. As analyzed before, increasing $r_c$ can suppress the resonance peak in amplitude-frequency curve, but if $r_c$ is too large, the power dissipation of damping resistances also obviously increases, so the value of damping resistance $r_c$ is usually smaller than 10 Ω in engineering practice. When $r_c$ = 1 Ω and $\tau = 3T_s$, in order to keep the system stable, the proportion coefficient $K_{vp}$ should smaller than 0.63 according to root locus, so we make the range of $K_{vp}$ from 0 to 1 firstly. In a continuous control system, $f_z$ is selected between 100 Hz and 200 Hz, but a discrete control system is different from a continuous control system. It is shown in Figure 14 that increasing $f_z$ can increase the minimum of the concave part in amplitude-frequency curve, which can widen the bandwidth of the voltage loop to realize the purposes of the optimum parameter design, so $f_z$ is selected between 100 Hz and 1000 Hz. Among the range of $r_c$, $K_{vp}$ and $f_z$, we select five datapoints, respectively, so 125 sets of parameters can be used to calculate the properties of the system. The results of this numerical calculation are depicted in Figure 15 in the form of a slice figure, in which different colors are used to represent different values of the properties.

Figure 15a is the slice figure of the gain of the resonance peak in amplitude-frequency curve of voltage closed-loop transfer function. As the color changes from blue to red, the gain of the resonance peak is larger. The blue area in Figure 15a implies small resonance peak, while the red area implies large resonance peak.

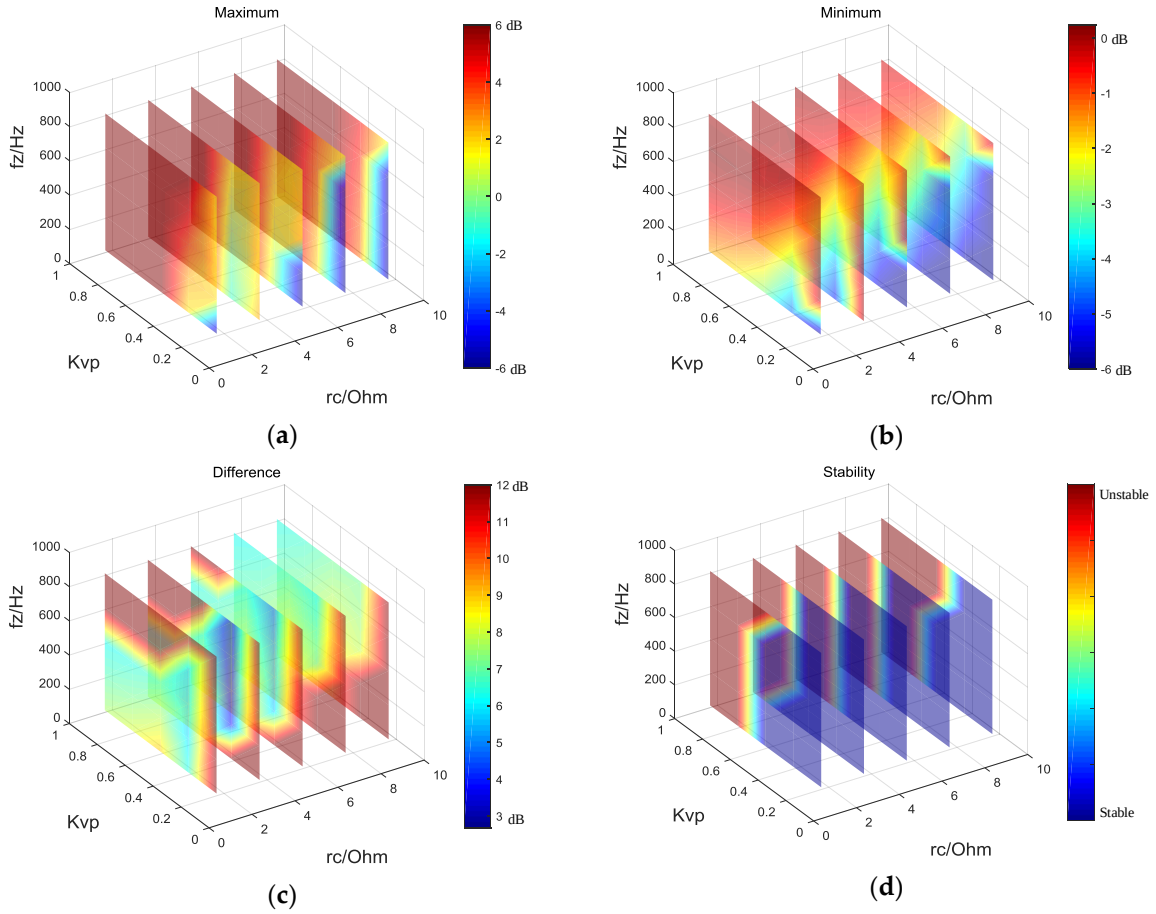



**Figure 15.** *Cont.*

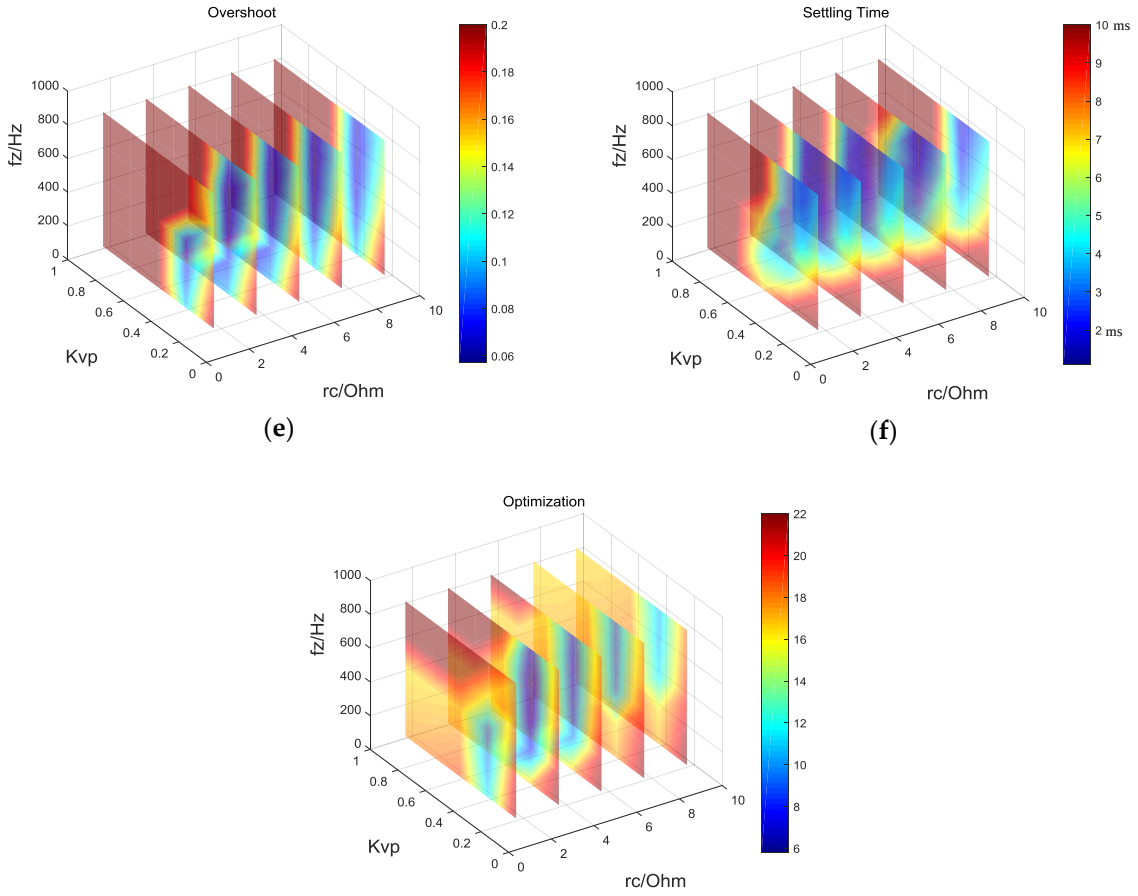



**Figure 15.** The results of numerical calculation: (**a**) the gain of the resonance peak; (**b**) the minimum of the concave part; (**c**) difference between the gain of the resonance peak and the minimum of the concave part; (**d**) stability; (**e**) overshoot; (**f**) settling time; (**g**) the result of the optimum design.

Figure 15b is the slice figure of the minimum of the concave part in the amplitude-frequency curve. As the color changes from blue to red, the minimum of the concave part is larger. Figure 15c is the slice figure of the difference value between the resonance peak in Figure 15a and the minimum in Figure 15b when the minimum of the concave part is larger than $-5$ dB. If the minimum of the concave part is lower than $-5$ dB, the bandwidth of the voltage loop is narrow. According to the purposes of the optimum parameter design, the difference should be small, so the blue area is the ideal area. Figure 15d is the slice figure of the stability. The stability of the voltage loop can be determined by the step response. If the step response converges, the voltage loop is stable, otherwise unstable. In Figure 15d, the blue area implies that the voltage loop is stable, while the red area implies the voltage loop is unstable. Figure 15e,f are the slice figures of overshoot and settling time of the step response, respectively.

In order to design the parameters optimally, we select 1 dB as the benchmark value of the difference in Figure 15c, and select 0.02 as the benchmark value of the overshoot in Figure 15e, then the per-unit values of the difference and the overshoot can be calculated. Figure 15g depicts the sum of the per-unit values of the difference and the overshoot. The blue area in Figure 15g implies small sum, so the numerical values of $r_c$, $K_{vp}$ and $f_z$ can be selected in the blue area.

### *4.3. Stability and Dynamic Property*

Three sets of parameter of $r_c$, $K_{vp}$ and $f_z$ are selected to analyze the stability and dynamic property of the system. The first set of parameters is $r_c = 2.5\ \Omega$, $K_{vp} = 0.2$, $f_z = 700$ Hz, which is in the blue area shown in Figure 15g. The second set of parameters is $r_c = 2.5\ \Omega$, $K_{vp} = 0.15$, $f_z = 400$ Hz, which is also in the blue area. The third set of parameters is $r_c = 2.5\ \Omega$, $K_{vp} = 0.1$, $f_z = 200$ Hz, which is outside the blue area.

#### 4.3.1. Set 1: $r_c = 2.5\ \Omega$, $K_{vp} = 0.2$, $f_z = 700$ Hz, in the Blue Area

The open-loop frequency characteristics of the voltage loop are depicted in Figure 16a. In this case, the phase margin of the system is 81°, and the gain margin is 10.1 dB, so the system has a good stability margin. The close-loop frequency characteristics of the voltage loop are depicted in Figure 16b. The gain of the resonance peak is suppressed to −4.5 dB, and the minimum of the concave part is about −4.54 dB. The bandwidth of the voltage loop is about 700 Hz. Hence, the closed-loop frequency characteristics of the voltage loop realize the purposes of the optimum design.

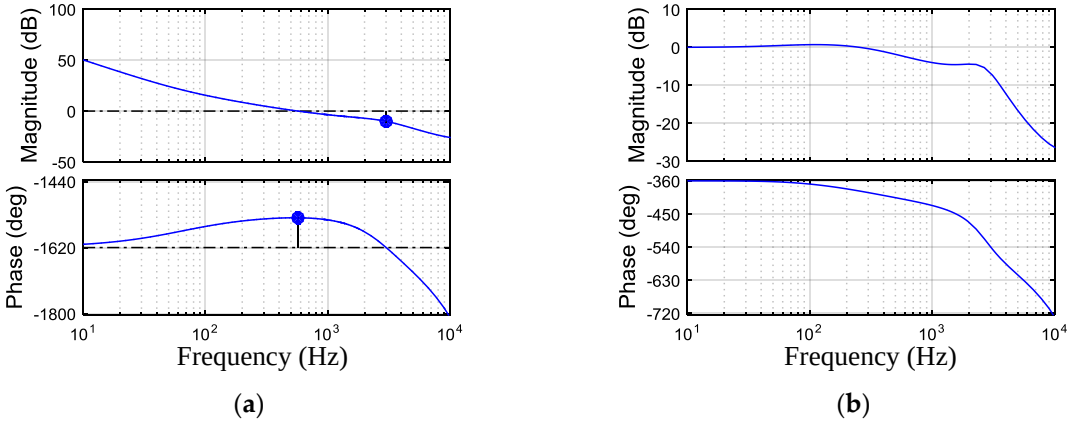



**Figure 16.** Frequency characteristics of the voltage loop with discrete control: (**a**) Open-loop Bode diagrams; (**b**) Close-loop Bode diagrams.

The step response of the system is depicted in Figure 17. It can be seen from the figure that the overshoot of unit step response is small, only about 8%, and the settling time is about 3 ms, indicating that the system has good dynamic performance.

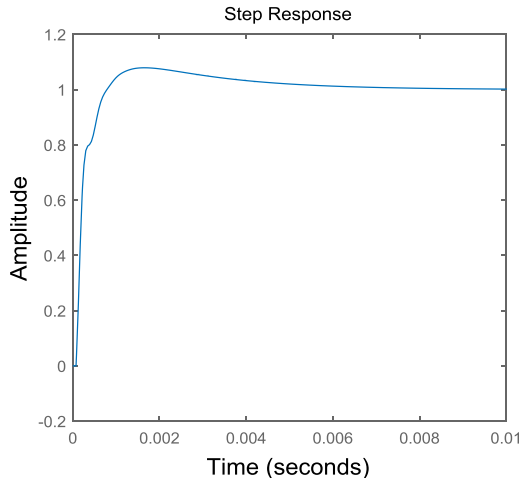



**Figure 17.** Step response of voltage closed-loop transfer function with set 1.

4.3.2. Set 2: $r_c$ = 2.5 Ω, $K_{vp}$ = 0.15, $f_z$ = 400 Hz, in the Blue Area

The open-loop frequency characteristics of the voltage loop are depicted in Figure 18a. In this case, the phase margin of the system is 88.4°, and the gain margin is 13.2 dB. Thus, the system has a good stability margin. The close-loop frequency characteristics of the voltage loop are depicted in Figure 18b. The resonance peak is suppressed completely. The bandwidth of the voltage loop is about 264 Hz, which is lower than that of set 1.

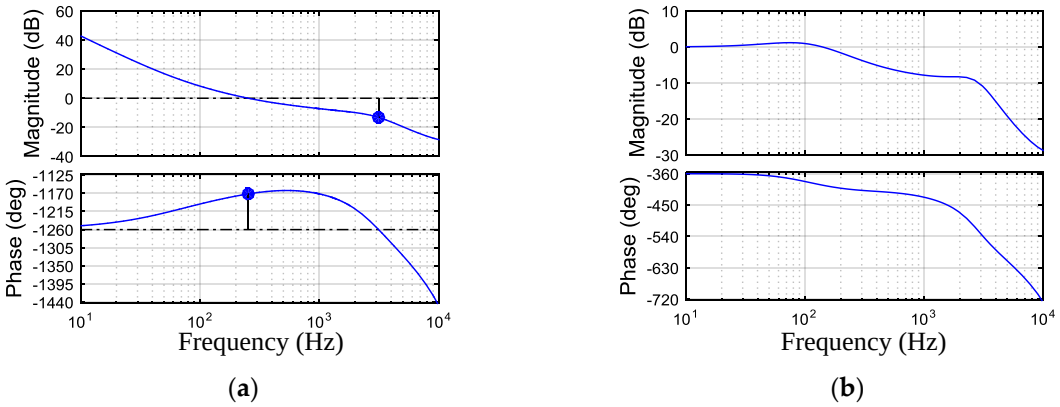



**Figure 18.** Frequency characteristics of the voltage loop with discrete control: (**a**) Open-loop Bode diagrams; (**b**) Close-loop Bode diagrams.

The step response of the system is depicted in Figure 19. The settling time is about 6 ms, and the overshoot is about 12%.

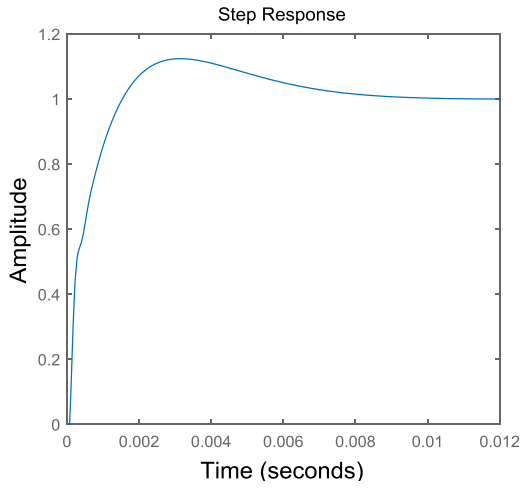



**Figure 19.** Step response of voltage closed-loop transfer function with set 2.

4.3.3. Set 3: $r_c$ = 2.5 Ω, $K_{vp}$ = 0.1, $f_z$ = 200 Hz, outside the Blue Area

The open-loop frequency characteristics of the voltage loop are depicted in Figure 20a. In this case, the phase margin of the system is 70°, and the gain margin is 17.2 dB. The close-loop frequency characteristics of the voltage loop are depicted in Figure 20b. The resonance peak is also suppressed completely, but the bandwidth of the voltage loop is only 72 Hz, which does not meet the purposes of the optimum design, so this set of parameters is not good.

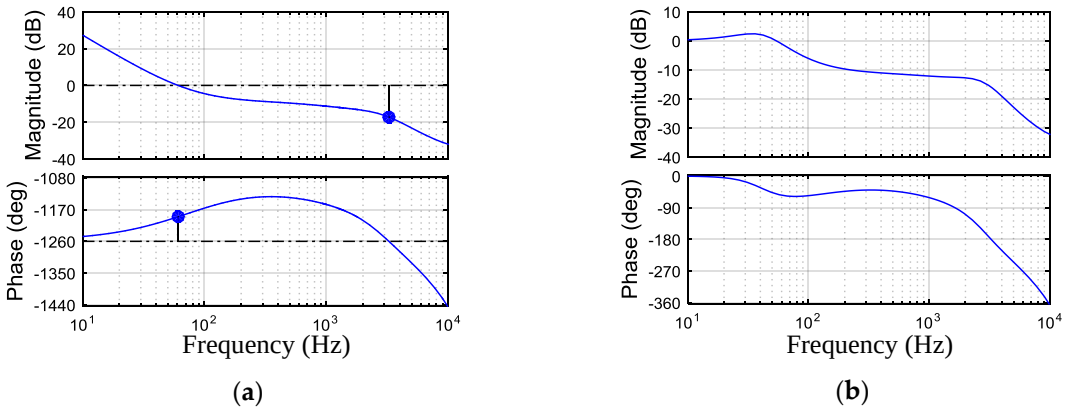



**Figure 20.** Frequency characteristics of the voltage loop with discrete control: (**a**) Open-loop Bode diagrams; (**b**) Close-loop Bode diagrams.

The step response of the system is depicted in Figure 21. Due to the decrease of $f_z$, the integration coefficient $K_{vi}$ and the gain of open-loop transfer function among low and medium frequency section also decrease, which makes the dynamic response speed slower. The settling time is about 11 ms, and the overshoot is about 20%, which are worse than those of set 1 and set 2.

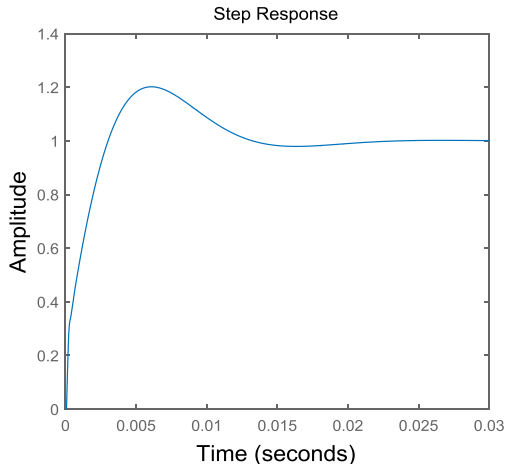



**Figure 21.** Step response of voltage closed-loop transfer function with set 3.

## 5. Simulation Results and Analysis

In order to verify the correctness of the mathematical model and the validity of the parameter design, a simulation model was built in Simulink, and the discrete control algorithm is written in an m-file, so as to simulate the discrete control in digital signal processor (DSP). The parameters of the simulation model are listed in Table 1.

The parameter design is analyzed in detail in Section 4, and the same three sets of parameter of $r_c$, $K_{vp}$ and $f_z$ are selected to verify the mathematical model and the parameter design. The reference value of capacitor voltage $u_{cq}$ is 0 V initially. When the time is 0.3 s, the reference value of $u_{cq}$ is changed to 7 V. The reference value of $u_{cd}$ is 155.6 V, which is equal to the grid voltage $u_{gd}$ (155.6 V). The grid voltage $u_{gq}$ is equal to 0 V. The simulated results are shown in Figures 22 and 23. The waveform of capacitor voltage $u_{ca}$ with set 1 is depicted in Figure 22, which implies that the system is stable with this set of parameters. Figure 23 depicts the step response of capacitor voltage $u_{cq}$, and they are consistent with that shown in Figures 17, 19 and 21, respectively, during the transient process, which implies that the mathematical model of the voltage loop is correct. Figure 23a shows that the system

can respond to the reference value rapidly with set 1, and the overshoot is small, which indicates that the parameter optimum design is effective.

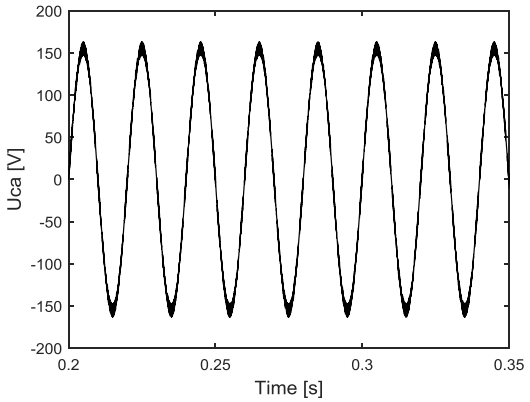



**Figure 22.** Waveform of capacitor voltage $u_{ca}$ with set 1: $r_c$ = 2.5 Ω, $K_{vp}$ = 0.2, $f_z$ = 700 Hz.

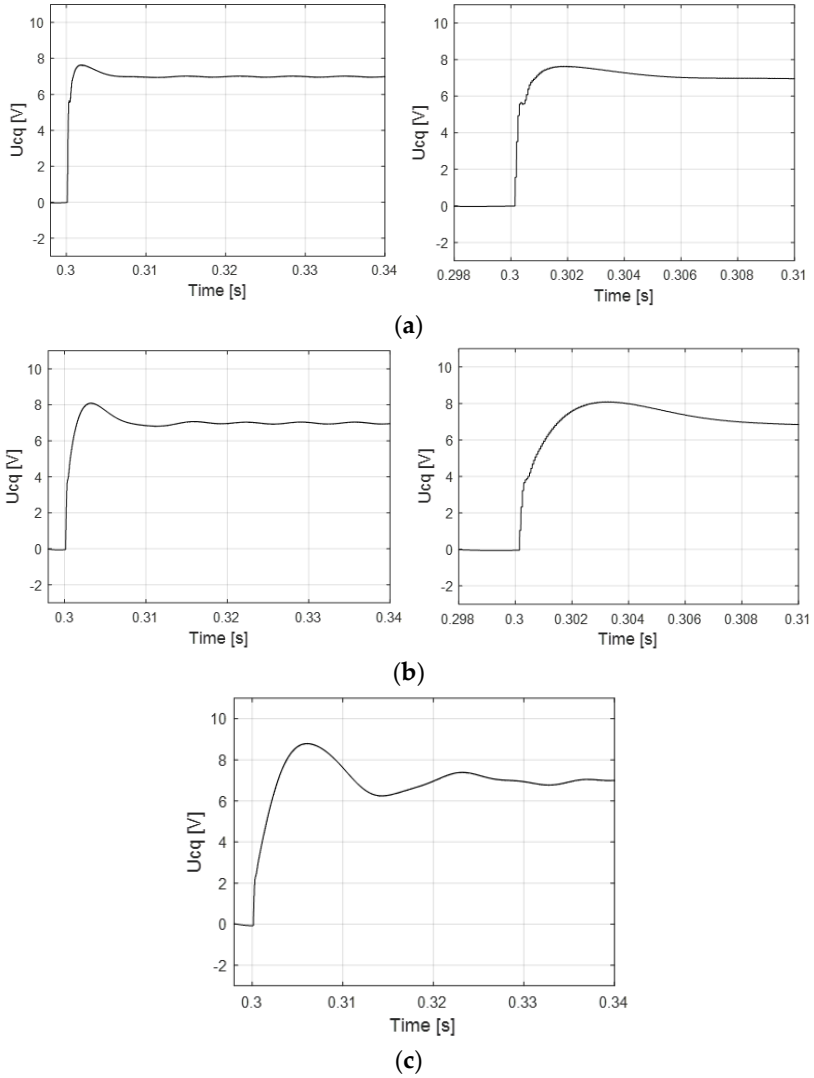
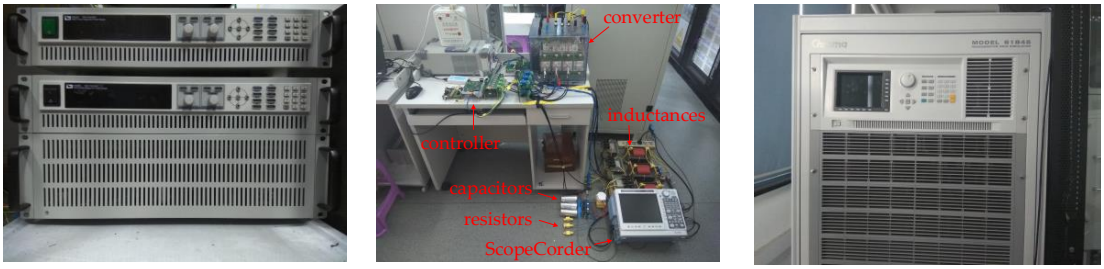



**Figure 23.** Step response of capacitor voltage $u_{cq}$: (**a**) set 1: $r_c$ = 2.5 Ω, $K_{vp}$ = 0.2, $f_z$ = 700 Hz; (**b**) set 2: $r_c$ = 2.5 Ω, $K_{vp}$ = 0.15, $f_z$ = 400 Hz; (**c**) set 3: $r_c$ = 2.5 Ω, $K_{vp}$ = 0.1, $f_z$ = 200 Hz.

## 6. Experimental Validation

To verify the validity and feasibility of the proposed parameter design strategy, a voltage-controlled grid-connected inverter was built and tested. The experimental test bed is shown in Figure 24. The DC voltage source is an ITECH 6526C (ITECH, Nanjing, China), and the grid simulator is a Chroma 61845 (Chroma, Taoyuan, China). The converter is a Semikron IGBT Power Electronics Teaching System (Semikron, Nuremberg, Germany). The digital signal processor is a TMS320F28335 (Texas Instruments, Dallas, TX, USA). The ScopeCorder is a Yokogawa DL850EV (Yokogawa, Tokyo, Japan).




(**a**) (**b**) (**c**)

**Figure 24.** The experimental test bed: (**a**) DC voltage source; (**b**) main circuit, controller and ScopeCorder; (**c**) grid simulator.

The key parameters of the system are listed in Table 2. In order to protect the switching devices, the output current of the inverter cannot exceed 40 A, and the maximum output power of the DC voltage source is 6 kW, so the grid voltage is selected as 55 V to reduce the output current and the output power of the inverter, which can ensure the security of the system. In Figure 2, it can be seen that grid voltage is a disturbance term, so grid voltage does not affect the closed-loop transfer function, which can also be found from the voltage closed-loop transfer function shown in Appendix B. Therefore, with the same LCL filter and control parameters, the experimental test bed and the simulation model have the same stability and dynamic properties, although the grid voltage is different.

**Table 2.** Parameters of the experimental test bed.

| Elements | Parameters and Values |
|---|---|
| DC source | $U_{dc}$ = 190 V |
| Switching circuit | $K_{pwm}$ = 12 |
| LCL filter | $L_1$ = 1.85 mH, $r_1$ = 0.018 Ω<br>$C$ = 35 μF<br>$L_2$ = 570 μH, $r_2$ = 0.23Ω |
| Utility grid | phase RMS voltage $U_g$ = 55 V |
| PWM modulation | asymmetric regular sampling<br>switching frequency: 10 kHz<br>sampling frequency: 20 kHz |

The reference value of capacitor voltage $u_{cq}$ is 0 V initially, and the step reference is 7 V. The reference value of $u_{cd}$ is 77.78 V, which is equal to the grid voltage $u_{gd}$ (77.78 V). The grid voltage $u_{gq}$ is equal to 0 V. The experiment results are shown in Figures 25 and 26. The waveforms of grid voltage $u_{ga}$, capacitor voltage $u_{ca}$ and grid current $i_{ga}$ with set 1 are depicted in Figure 25, which implies that the system can work stably with this set of parameters, when $u_{cq}$ is 7 V and $u_{cd}$ is 77.78 V. The step response of capacitor voltage $u_{cq}$ from 0 V to 7 V with different control parameters are shown in Figure 26. It can be seen that the experiment results are consistent with the simulation

results during the transient process, which indicates that the proposed parameter design strategy is correct and useful. Due to the capacitor voltage distortion, it can be observed that there are ripples, which cause the difference between simulation and experiment results, in capacitor voltage $u_{cq}$.

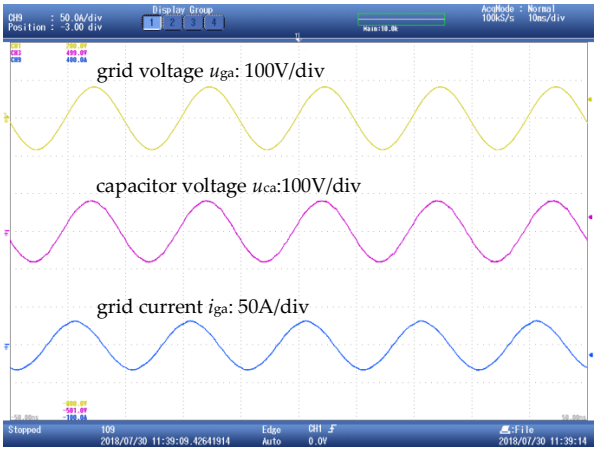
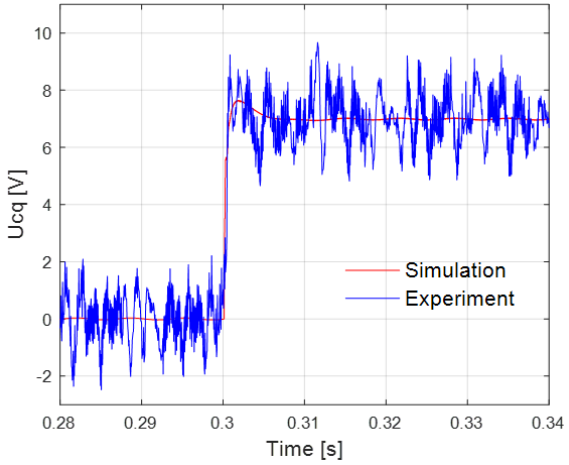
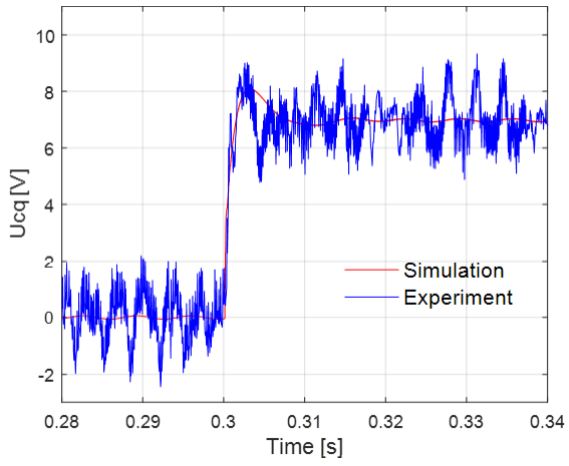



**Figure 25.** Waveforms of grid voltage $u_{ga}$, capacitor voltage $u_{ca}$ and grid current $i_{ga}$ with set 1.

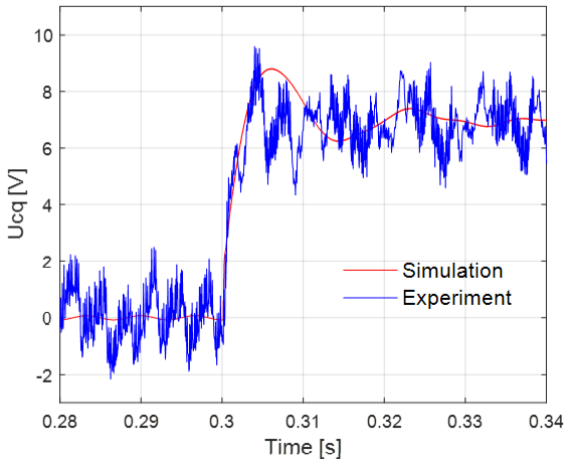



(**a**)




(**b**)

**Figure 26.** *Cont.*




(**c**)

**Figure 26.** Step response of capacitor voltage $u_{cq}$: (**a**) set 1: $r_c = 2.5\ \Omega$, $K_{vp} = 0.2$, $f_z = 700$ Hz; (**b**) set 2: $r_c = 2.5\ \Omega$, $K_{vp} = 0.15$, $f_z = 400$ Hz; (**c**) set 3: $r_c = 2.5\ \Omega$, $K_{vp} = 0.1$, $f_z = 200$ Hz.

## 7. Conclusions

This paper has proposed a parameter design strategy for voltage-controlled inverters based on discrete control. The mathematical models of the voltage and current loops are developed. Due to the calculation delay and modulation delay, there is phase lag in the phase-frequency curve. If the parameters are designed improperly, there is a resonance peak in the amplitude-frequency curve. The parameters of the current controllers are designed in an analytical way, by which the resonance peak can be suppressed. Due to the complexity of the mathematical model of the voltage loop, numerical calculation and visualization with slice figures are proposed for optimum parameter design. Considering stability, overshoot, settling time and the resonance peak suppression, the optimum parameter area can be shown in a slice figure by numerical calculation. By employing such an optimum parameter design method, the design of a voltage-controlled inverter becomes much easier, without too many repeated efforts and trial of PI controller parameters, so such an optimum parameter design method is especially suitable for engineering practice because it can greatly improve the efficiency of the parameter design. Simulated and experimental results have verified the validity of the proposed parameter design strategy.

**Author Contributions:** N.D. proposed the main idea and performed the experiments; N.D. and H.Y. wrote this paper; J.H. provided some resources and assisted with paper writing; R.Z. managed the project.

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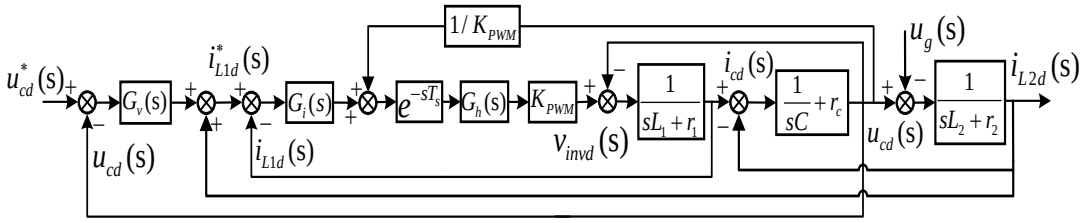
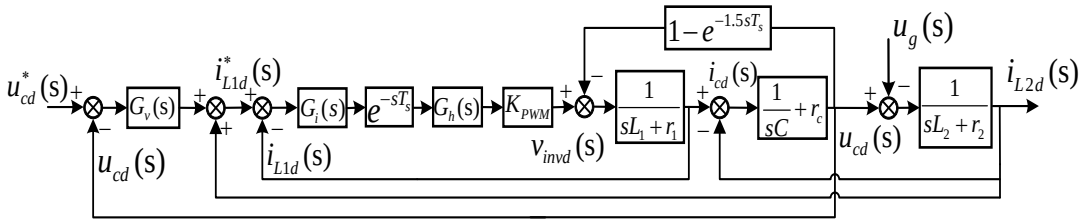
**Conflicts of Interest:** The authors declare no conflict of interest.

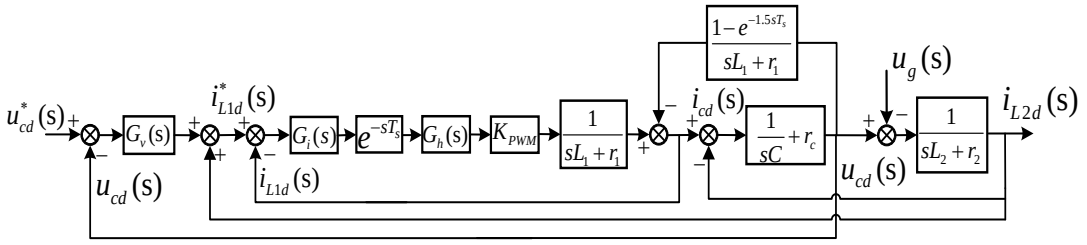
## Appendix A



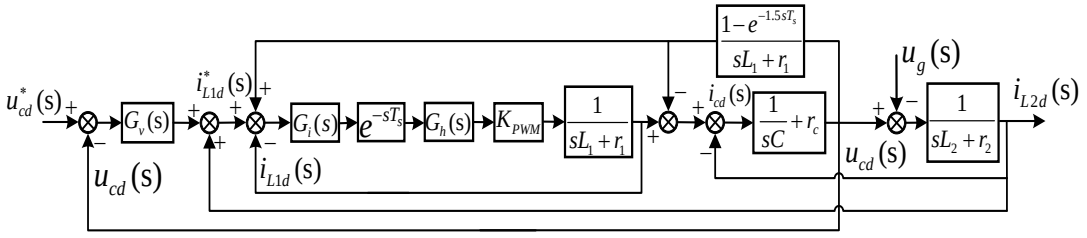

(**a**)



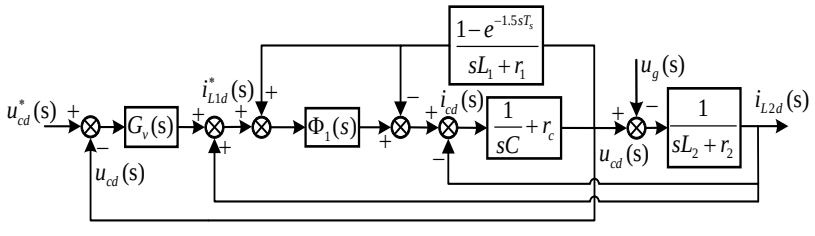

(**b**)



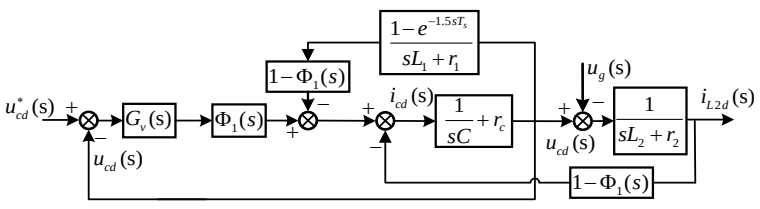

(**c**)




(**d**)




(**e**)




(**f**)

**Figure A1.** *Cont.*

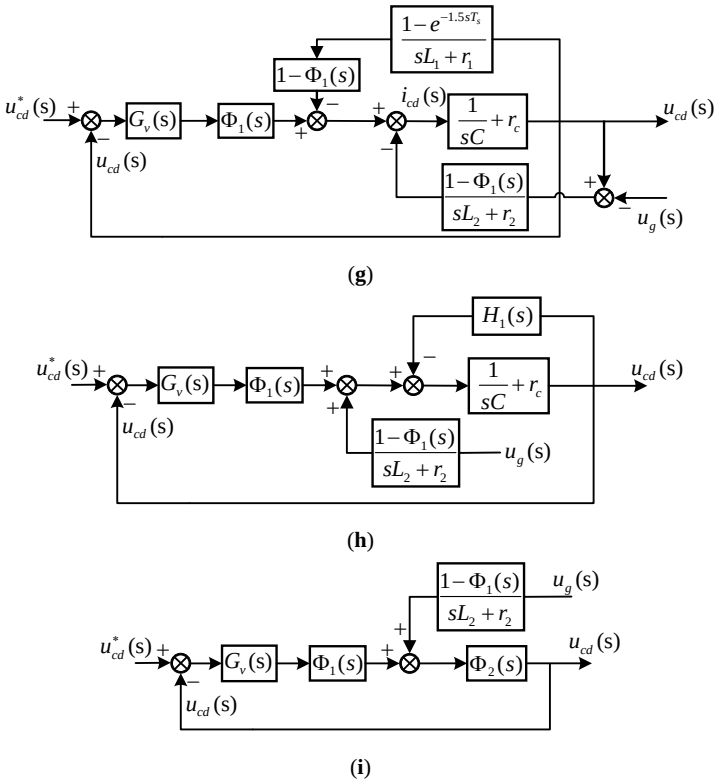



**Figure A1.** The detailed transformation processes. (**a**) control block diagram of the voltage and current loops in d-axis; (**b**) making the feedforward point of $u_{cd}$ backward; (**c**) making the feedback point of $u_{cd}$ backward; (**d**) exchanging the feedback point and the tapping point; (**e**) simplifying the current loop; (**f**) making the feedforward point of $u_{cd}$ backward; (**g**) selecting $u_{cd}$ as the output of the system; (**h**) combining the inner loops; (**i**) simplifying the voltage loop.

## Appendix B

The open-loop transfer function and closed-loop transfer function of voltage loop are expressed as:

$$G_{open}(s) = \frac{G_v(s)\cdot(sL_1+r_1)(sL_2+r_2)(1+sCr_c)e^{-1.5sT_s}}{(\tau s+e^{-1.5sT_s})(sL_1+r_1)(sL_2+r_2)sC+(1+sCr_c)[(1-e^{-1.5sT_s})(sL_2+r_2)+(sL_1+r_1)]\cdot\tau s}$$

$$\Phi_{close}(s) = \frac{G_v(s)\cdot(sL_1+r_1)(sL_2+r_2)(1+sCr_c)e^{-1.5sT_s}}{[G_v(s)(1+sCr_c)e^{-1.5sT_s}+(\tau s+e^{-1.5sT_s})sC](sL_1+r_1)(sL_2+r_2)+(1+sCr_c)[(1-e^{-1.5sT_s})(sL_2+r_2)+(sL_1+r_1)]\cdot\tau s}$$

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