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A Single-Phase Nine-Level Boost Inverter

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Abstract: A novel single-phase nine-level boost inverter is proposed in this paper. The proposed inverter has an output voltage which is higher than the input voltage by switching capacitors in series and in parallel. The maximum output voltage of the proposed inverter is determined by using the boost converter circuit, which has been integrated into the circuit. The proposed topology is able to invert the multilevel voltage with the high step-up output voltage, simple structure and fewer power switches. In this paper, the circuit configuration, the operating principle, and the output voltage expression have been derived. The proposed converter has been verified by simulation and experiment with the help of PSIM software and a laboratory prototype. The experimental results match the theoretical calculation and the simulation results.

Keywords: single-phase inverter; switched-capacitors; switched-diode-capacitors; multilevel inverters; H-bridge

1. Introduction

Recently, multilevel inverters (MIs) have played important roles for high-power applications because of their advantages as better output voltage waveforms quality, a reduced rating of power semiconductor devices, and low electromagnetic interference [1]. The traditional MI topologies are neutral-point-clamped (NPC), flying-capacitor (FC), and cascade H-Bridge (CHB) inverters [2–5]. Diodes and capacitors are used to generate multilevel at the output voltage in NPC and FC inverters, respectively. On the other hand, to attain voltage levels, the direct current (DC) source must be increased. Nevertheless, both the circuit configurations and their controls become very complicated along with the increasing number of the output voltage levels. Furthermore, these topologies also make capacitors' imbalanced. Some in-depth studies for NPC's topologies have been presented in References [6–8]. To operate at the higher voltage level, the CHB inverters are used thanks to easy modularization and facilitate to expansion extension [9,10]. However, the topologies request more and more power devices with separate DC voltage sources. When the output voltage has more levels, the number of the required input DC sources is increased. Construction of a multilevel converter was introduced in Reference [11] with the use of multiple modules that made it easy to expand. However, this also increases the number of capacitors and switches required.

A seven-level inverter using series-connected DC voltage sources was presented in Reference [12] with the use of multiple DC voltage sources supplies to reduce switching losses. However, the number of output voltage levels depends on the number of DC voltage sources. A circuit of (4n + 3)-level inverter using voltage sources in serial/parallel operation was introduced in Reference [13] to increase the number of output voltage levels with the complex pattern and increase the conductive losses. By using an additional boost converter to create a multi-step output with capacitors, a seven-level

grid-connected inverter for photovoltaic systems was presented in Reference [14], but an imbalance between capacitors is very likely to occur.

Nowadays, the switched-capacitor (SC)-based MIs are a popular solution for single-phase systems because they have a simple topology and reduce the component count. In Reference [15], a serial/parallel connection-based MI was presented. The topology of a SCMI for high-frequency aternative current (AC) microgrids was proposed in Reference [16]. SCMIs are recommended in Reference [17] with the ability to balance capacitor voltage and step-up voltage. The formerly SCMI topologies consist of SC elements with a high-voltage DC source. Then, they are divided into several floating DC sources [15–19] or a cascaded combination of multiple SC converters [20–23]. However, in most of these topologies, the voltage across the capacitors is only equal to the supply voltage. Therefore, the output voltages are limited. To overcome this limitation, the topology of the single-phase step-up five-level inverter was introduced in Reference [24], which uses the switch-diode-capacitor (SDC) circuit [25] and an additional booster circuit to increase the input voltage. In summary, Table 1 shows the advantages and disadvantages of the multilevel inverters with reduced switch count.

Table 1. Advantages and disadvantages of multilevel inverters with reduced switch count.

Topology	Literature	Advantages	Disadvantages
Series-connected DC voltage sources	Proposed in Reference [12]	• Reduce switching losses	• Number of output voltage levels depends on the number of DC sources • Buck voltage
Switched serial/parallel DC voltage sources	Proposed in Reference [13]	• Simple topology • Input sources can be integrated in both parallel and series	• Complex switching pattern • Increase conductive losses • Buck voltage
Additional boost converter	Proposed in References [14,24]	• Single source • Boost voltage	• Capacitor imbalance is very likely to occur • Two-stage conversion
Series/parallel connection	Proposed in References [15,18]	• Single source • Boost voltage	• Large number of switches
Based on switched capacitor	Proposed in References [16,17,19–21]	• Self-balancing in capacitor voltage • Voltage boost capability	• Reduce switch count but increase number of diodes • High capacitor current stress
Cascaded multilevel inverter	Proposed in References [22,23]	• Reduce voltage stress on H-bridge switches • Boost voltage	• Only show in high-frequency AC output voltage [20] • Using separate dc source

In this paper, a new nine-level boost inverter (NLBI) is suggested. The NLBI is an extension of the five-level inverter in Reference [24]. The NLBI combines structure switched-diode-capacitor, switched-capacitor, a conventional boost converter, and an H-bridge circuit to be able to enhance boost ability of output voltage levels with the reduced circuit components. In Section 2, the topology, operating principles and circuit analysis of the proposed inverter are presented. Section 3 presents the selection of the inductor and the capacitor. Simulation and experimental results are shown in Section 4. Finally, the conclusion is summarized in Section 5.

2. Proposed Single-Phase Nine-Level Boost Inverter

Figure 1 shows the proposed single-phase NLBI. As shown in Figure 1, the proposed NLBI consists of a single DC source (V_{dc}), a conventional boost converter, a switched-diode-capacitor (SDC) circuit [25], a switched-capacitor (SC) circuit [17], an H-bridge circuit, a low-pass filter (L_f–C_f) and a load (R). In the SDC circuit, two capacitors C_1 and C_2 are discharged in serial when the switch S_1 is switched ON. When the switch S_1 is switched OFF, two capacitors C_1 and C_2 are charging by the diodes D_1 and D_2. In the SC circuit, the capacitor C_3 is charged through the body diode of switch S_4

when the switch S_5 is switched ON and the switch S_3 is switched OFF. When the switch S_3 is switched ON and the switch S_5 is switched OFF, the capacitor C_3 is discharged.

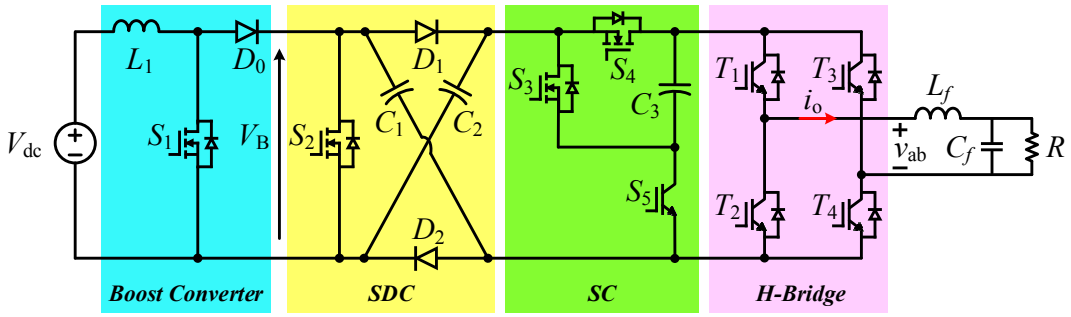

Figure 1. Proposed single-phase nine-level boost inverter (NLBI) topology.

2.1. Operating Principle of the Proposed Inverter

Figure 2 describes the level shift multicarrier-based pulse-width modulation (PWM) scheme for the proposed single-phase NLBI. A control waveform (e_x) is compared to four carrier waveforms (e_1–e_4) which these waveforms have the identical phase and amplitude to handle the switches. A constant voltage, e_n is compared to the carrier voltage e_1 to generate a control signal for S_1, which works with duty cycle d_{S1} for each cycle T_s. In Figure 1, V_B is the boost voltage value of the boost converter which equals to the collector-emitter voltage of the switch S_2. Figures 3 and 4 show the operating states of the proposed NLBI.

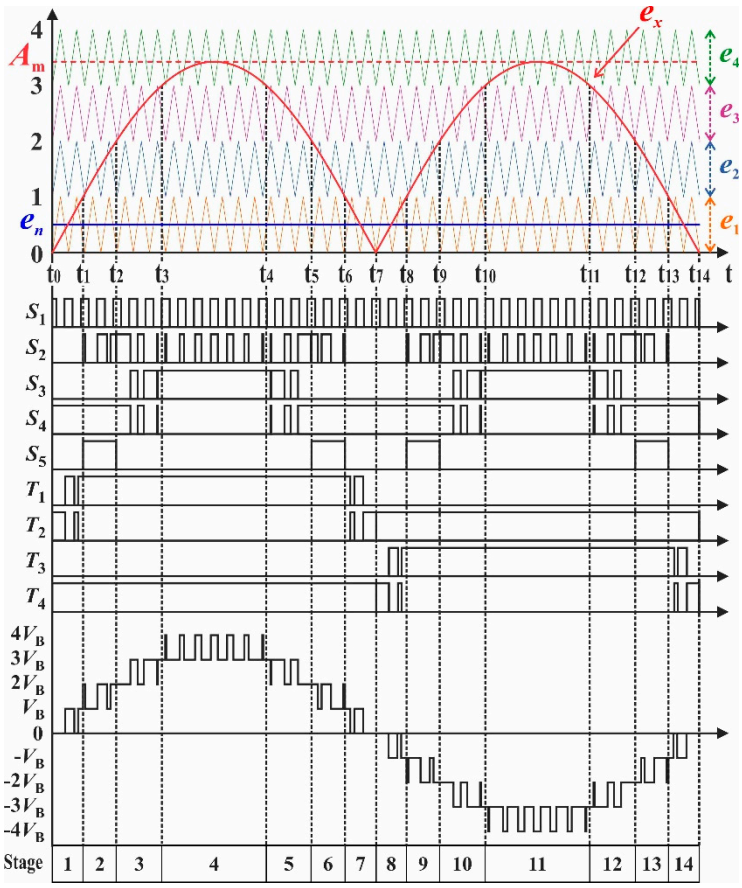

Figure 2. Modulation method for the proposed single-phase NLBI.

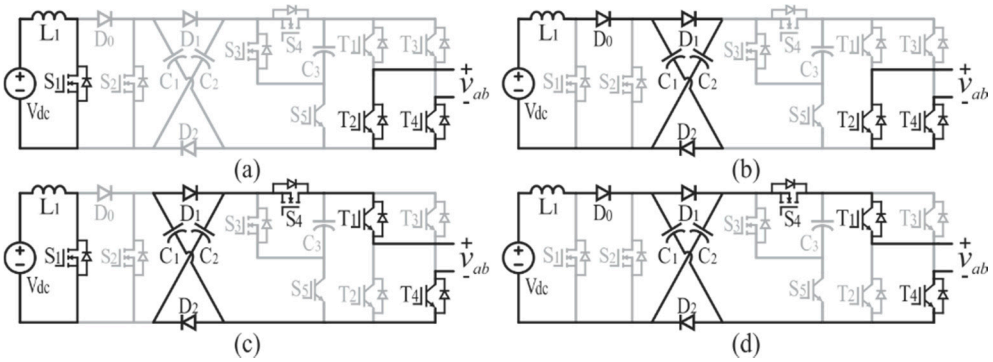

Figure 3. Operation states in the positive output voltage period of the proposed NLBI. (**a**) State 1, (**b**) State 2, (**c**) State 3 and (**d**) State 4.

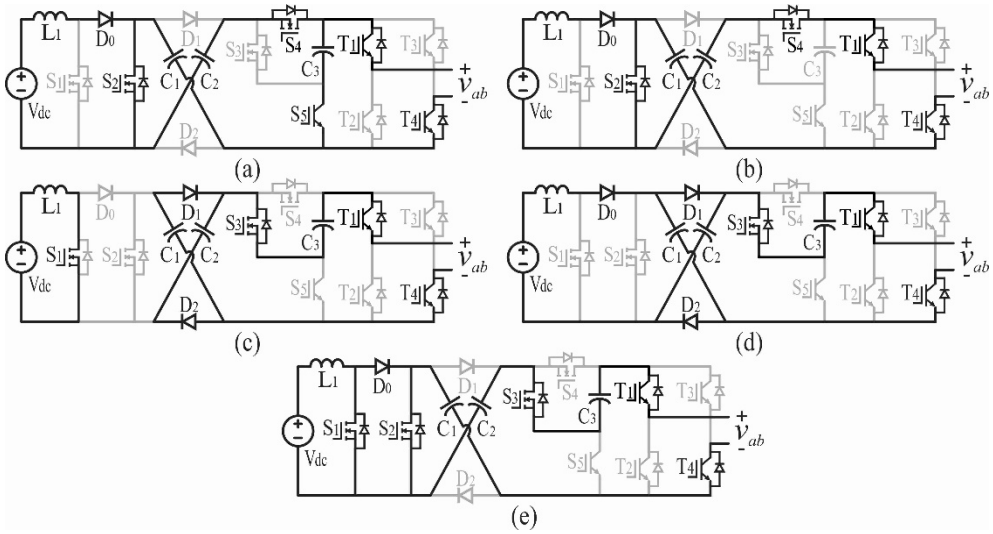

Figure 4. Operation states in the positive output voltage period of the proposed NLBI (continuous). (**a**) State 5, (**b**) State 6, (**c**) State 7, (**d**) State 8 and (**e**) State 9.

The output voltage is positive from t_0 to t_7 with corresponding to Stages 1–7. Between t_7 and t_{14}, the output voltage is negative, corresponding to Stages 8–14. In the positive period from t_0 to t_7, the circuit operation includes seven stages and nine states (State 1 to State 9, Figures 3 and 4).

Stage 1 (t_0–t_1, Figure 3a–d): When S_1 is switched ON, the inductor L_1 stores energy from the DC source. If T_1 is switched OFF, the output voltage is equal to zero (V_{ab} = 0) as shown in Figure 3a for State 1. If T_1 is switched ON, the output voltage is equal to the boost voltage ($V_{ab} = V_B$) as shown in Figure 3c for State 3.

When S_1 is switched OFF, the diode D_0 is forward-biased, and the inductor L_1 is discharged to the capacitors C_1 and C_2. If T_1 is switched OFF, the output voltage is zero (V_{ab} = 0) as shown in Figure 3b for State 2. When T_1 is switched ON, the output voltage equals the boost voltage ($V_{ab} = V_B$) as shown in Figure 3d for State 4. The operating duty cycle of the boost inductor in this stage is the duty cycle of switch S_1, d_{S1}.

Stage 2 (t_1–t_2, Figures 3c,d and 4a): The switches S_5 and T_1 are fully switched ON. When S_2 is turned ON, whereas S_1 is switched OFF, the capacitors C_1 and C_2 are working in series supplying power to the load. The capacitor C_3 is charged by C_1 and C_2 through S_5 simultaneously. As shown in Figure 4a for State 5, the load voltage is equal to twice boost voltage ($V_{ab} = 2V_B$).

When S_2 is switched OFF, while S_1 is switched ON, the inductor L_1 stores energy from V_{dc}. The capacitors C_1 and C_2 are working in parallel to feed the load. Although S_5 is switched ON in this state, the current from the capacitors C_1 and C_2 cannot pass through the capacitor C_3 because the capacitor C_3 voltage is greater than the capacitor C_1 and C_2 voltages. Consequently, there is no current

flow to S_5 and the load is connected to the capacitors C_1 and C_2 in parallel. This state is the same as the State 3 as shown in Figure 3c, the output voltage equals the boost voltage ($V_{ab} = V_B$). The control signal of S_5 during this stage can be changed in another way, which is similar to the control signal for S_2. To reduce the switching losses, the control signal of S_5 is always controlled ON during this stage.

Similarly, when S_1 is switched OFF, whereas S_5 is turned ON, the output voltage is equal to the boost voltage ($V_{ab} = V_B$), which is the same as the State 4 as shown in Figure 3d.

As shown in Figure 2, the duty cycle of S_2 in this stage is gradually increased, while the duty cycle of S_1 is fixed at d_{S1}. The time interval of Stage 2 is divided into two subintervals. In the first subinterval (t_1–t_{1m}, see Figure 5a), the duty cycle of S_1 is greater than that of S_2. The operating duty cycle of the boost inductor in the first subinterval is d_{S1}. In the second subinterval (t_{1m}–t_2, see Figure 5a), the duty cycle of S_2 is more than that of S_1. As a result, the operating duty cycle of the boost inductor in the second subinterval depends on the duty cycle of S_2. The average duty cycle of the boost inductor in this sub-stage can be approximated as

$$d_{S2} \approx \frac{1 + d_{S1}}{2}, \tag{1}$$

The time t_{1m} is calculated as

$$t_{1m} = \frac{\sin^{-1}\left(\frac{1+d_{S1}}{A_m}\right)}{2\pi f_{out}}, \tag{2}$$

where f_{out} and A_m are the frequency of the output voltage and the peak amplitude of control waveform e_x, respectively.

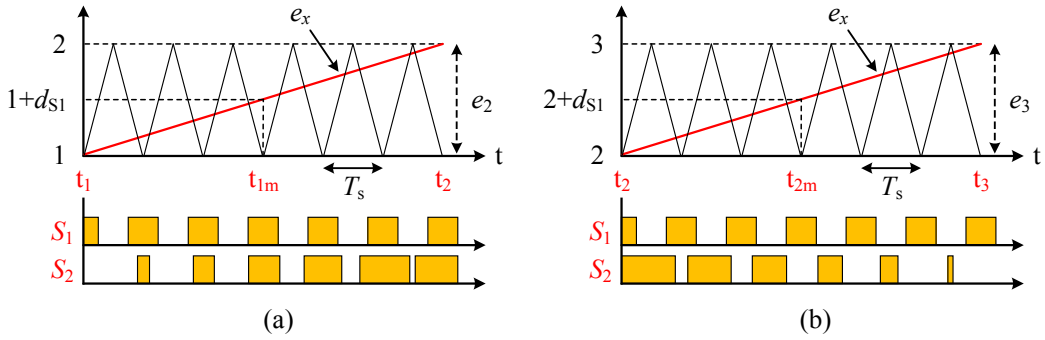

Figure 5. Operational analysis of switches S_1 and S_2 in the interval of (**a**) Stage 2 and (**b**) Stage 3.

Stage 3 (t_2–t_3, Figure 4b–d): The switch S_3 is complementary to the switch S_2. When S_3 is switched ON, the load voltage is equal to three times the boost voltage ($V_{ab} = 3V_B$). If S_1 is switched ON, the inductor L_1 stores energy from V_{dc}, while the capacitors C_1 and C_2 working in parallel are connected in series to the capacitor C_3 for supplying power to the load as shown in Figure 4c for State 7. When S_1 is switched OFF, the capacitors C_1 and C_2 are charged by the DC voltage source, while the capacitor C_3 is still connected in series with the capacitors C_1 and C_2 as shown in Figure 4d for State 8.

When the switch S_2 is switched ON and the switch S_3 is switched OFF, the inductor L_1 stores energy while the capacitors C_1 and C_2 are in series for supplying power to the load. From Figure 4b for State 6, it can be seen that the output voltage of the inverter equals to twice boost voltage ($V_{ab} = 2V_B$).

As shown in Figure 2, the duty cycle of S_2 in this stage is gradually decreased, while the duty cycle of S_1 is fixed at d_{S1}. The time interval of Stage 3 is divided into two subintervals. In the first subinterval (t_2–t_{2m}, see Figure 5b), the duty cycle of S_2 is more than that of S_1. The inductor is almost charged during the first subinterval. Therefore, the operating duty cycle of the boost inductor is 1.

In the second subinterval (t_{2m}–t_3, see Figure 5b), the duty cycle of S_1 is greater than that of S_2. The operating duty cycle of the boost inductor in the second subinterval is total duty cycle of the switches S_1 and S_2, we have

$$d_x = d_{S1} + d_{S2}, \tag{3}$$

where d_{S2} is average duty cycle of the switch S_2 in the second subinterval and calculated approximately as (1).

The time t_{2m} is defined as

$$t_{2m} = \frac{\sin^{-1}\left(\frac{2+d_{S1}}{A_m}\right)}{2\pi f_{out}}, \quad (4)$$

Stage 4 (t_3–t_4, Figure 4c–e): When the switches S_1, S_2 and S_3 are switched ON, whereas the switch S_5 is switched OFF, the capacitors C_1, C_2 and C_3 are working in series for supplying power to the load. The load voltage is equal to four times the boost voltage ($V_{ab} = 4V_B$) as shown in Figure 4e for State 9. Other states in this stage to reach the output voltage at three times boost voltage are the same as those in Stage 3. In the control method as shown in Figure 2, the duty cycle of S_1 is always greater than S_2 in terms of time (t_3–t_4) and (t_{10}–t_{11}) so that the calculation becomes simpler. Therefore, the following condition is obtained as

$$d_{S1} > A_m - 3 \quad (5)$$

The operating duty cycle of the boost inductor in Stage 4 is d_{S1}.

Stage 5—(t_4–t_5, Figure 4b–d: the same as Stage 3)

Stage 6—(t_5–t_6, Figures 3c,d and 4a: the same as Stage 2)

Stage 7—(t_6–t_7, Figure 3a–d: the same as Stage 1)

In the negative period from t_7 to t_{14} including seven stages and nine states, the switch T_2 is fully switched ON, while T_1 is fully switched OFF. The signal T_3 is obtained by comparing the carrier e_1 and the control waveform e_x. The signal T_4 is the opposite. All the remaining switches have the same states as in the positive period. The load voltage of the proposed inverter is summarized in Table 2.

Table 2. Different Switching, Capacitor, and Inductor States of the Proposed NLBI.

State	Stage	ON Diodes	ON Switches	Capacitor State			Inductor L_1 State	Output Voltage
				C_1	C_2	C_3		
1	1, 7		S_1, S_4, T_2, T_4	I	I	I	+	0
2	1, 7	D_0, D_1, D_2	S_4, T_2, T_4	+	+	I	−	0
3	1, 2, 6, 7	D_1, D_2	S_1, S_4, T_1, T_4	−	−	I	+	V_B
4	1, 2, 6, 7	D_0, D_1, D_2	S_4, T_1, T_4	+	+	I	−	V_B
5	2, 6	D_0	S_2, S_4, S_5, T_1, T_4	−	−	+	+	$2\,V_B$
6	3, 5	D_0	S_2, S_4, T_1, T_4	−	−	I	+	$2\,V_B$
7	3, 4, 5	D_1, D_2	S_1, S_3, T_1, T_4	−	−	−	+	$3\,V_B$
8	3, 4, 5	D_0, D_1, D_2	S_3, T_1, T_4	+	+	−	−	$3\,V_B$
9	4	D_0	S_1, S_2, S_3, T_1, T_4	−	−	−	+	$4\,V_B$
10	8, 14		S_1, S_4, T_2, T_4	I	I	I	+	0
11	8, 14	D_0, D_1, D_2	S_4, T_2, T_4	+	+	I	−	0
12	8, 9, 13, 14	D_1, D_2, D_3	S_1, S_4, T_2, T_3	−	−	I	+	$-V_B$
13	8, 9, 13, 14	D_0, D_1, D_2, D_3	S_4, T_2, T_3	+	+	I	−	$-V_B$
14	9, 14	D_0, D_3	S_2, S_4, S_5, T_2, T_3	−	−	+	+	$-2\,V_B$
15	10, 12	D_0, D_3	S_2, S_4, T_2, T_3	−	−	I	+	$-2\,V_B$
16	10, 11, 12	D_1, D_2	S_1, S_3, T_2, T_3	−	−	−	+	$-3\,V_B$
17	10, 11, 12	D_0, D_1, D_2	S_3, T_2, T_3	+	+	−	−	$-3\,V_B$
18	11	D_0	S_1, S_2, S_3, T_2, T_3	−	−	−	+	$-4\,V_B$

Here "I", "+" and "−" refer to the idle, charging and discharging states, respectively.

2.2. Circuit Analysis of the Proposed Inverter

The circuit analysis is begun with the following assumptions: the capacitors C_1 and C_2 are equal, the capacitance is large enough to the voltage across the capacitor is constant, and the pairs of diodes–capacitors (D_1–C_1 and D_2–C_2) are symmetrical and balanced. The operating states of the proposed NLBI simplify into two operating modes: charging inductor and discharging inductor.

The charging inductor modes are given in Figure 3a–e. These states are controlled by switch S_1 and S_2, and the inductor L_1 is charged at this time.

Assuming that the T_{avg} is the average time interval of the charging inductor mode during the period T_s, and $d_{avg} = T_{avg}/T_s$ is the average duty cycle of the boost inductor in each period T_s. When S_1 or S_2 is switched ON, the inductor stores energy as shown in Figure 3a–e for States 1, 3, 5, 6, 7 and 9, respectively. The inductor L_1 voltage is:

$$V_L = V_{dc} \tag{6}$$

When both S_1 and S_2 switches are switched OFF, the inductor is discharged as shown in Figure 3b,d and Figure 4d for States 2, 4 and 8, respectively. The average time of this mode is $(1 - d_{avg})T_s$. The following equations are obtained as

$$\begin{cases} V_L = V_{dc} - V_B \\ V_B = V_{C1} = V_{C2} \end{cases} \tag{7}$$

Because the average voltage crossing the inductor during a period of T_s is zero, from (6) and (7), the boost voltage is calculated as

$$V_B = \frac{1}{1 - d_{avg}} V_{dc} \tag{8}$$

The boost factor of the NLBI is determined as

$$B = \frac{V_B}{V_{dc}} = \frac{1}{1 - d_{avg}}. \tag{9}$$

From the analysis of the proposed NLBI in Section 2. The operating duty cycle of the boost inductor is summarized as

$$d_{L1} = \begin{cases} d_{S1} & t_0 \le t < t_{1m} \text{ and } t_3 \le t < t_4 \\ 0.5(1 + d_{S1}) & t_{1m} \le t < t_2 \\ 1 & t_2 \le t < t_{2m} \\ 0.5(1 + d_{S1}) & t_{2m} \le t < t_3, \end{cases} \tag{10}$$

where

$$t_2 = \frac{\sin^{-1}\left(\frac{2}{A_m}\right)}{2\pi f_{out}},\ t_3 = \frac{\sin^{-1}\left(\frac{3}{A_m}\right)}{2\pi f_{out}}$$

The influence of the operating states of S_1 and S_2 on the duty cycle of the circuit is not the same in each operating state. However, the operation of S_1 and S_2 is repeated after a quarter cycle of the output cycle. In one-four time interval of the output voltage time period, the average duty cycle of the boost inductor is calculated as

$$d_{avg} = d_{S1} + 2(1 - d_{S1})\left(\frac{t_3 + t_{2m} - t_2 - t_{1m}}{T_{out}}\right), \tag{11}$$

where $T_{out} = 1/f_{out}$ is the period of the output voltage. The voltage gain (G) is expressed as

$$G = A_m B \tag{12}$$

3. Inductor and Capacitor Selections

Figure 6 shows the inductor current and capacitor voltage waveforms in the positive output voltage. In Figure 6, the voltage waveforms on capacitors C_1 and C_2 are the same and equal to V_C.

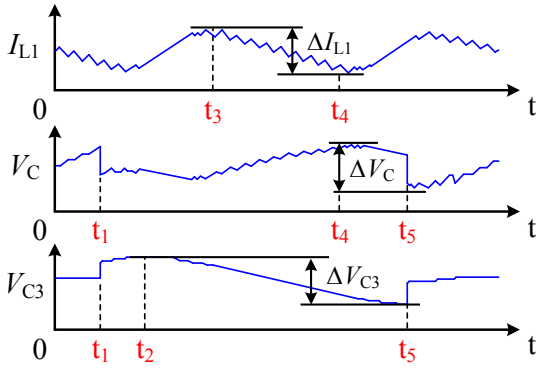

Figure 6. Inductor current ripple and capacitors voltage ripple.

Assuming that the output power (P_{OUT}) equals the input power, the average input current can be calculated as

$$I_{L1} = \frac{P_{OUT}}{V_{dc}} \tag{13}$$

The current ripple of the inductor is defined as

$$\Delta I_{L1} \approx \int_{t_3}^{t_4} \frac{di_{L1}}{dt} dt = \frac{1}{L_1} \int_{t_3}^{t_4} [d_{S1} V_{dc} + d_{S1}(V_{dc} - V_C)] dt = d_{S1} \frac{V_{dc}(2 - B)}{L_1} (t_4 - t_3), \tag{14}$$

where

$$t_4 = \frac{\pi - \sin^{-1}\left(\frac{3}{A_m}\right)}{2\pi f_{out}}$$

The inductance is determined by the current ripple factor K_L as

$$K_L = \frac{\Delta I_{L1}}{I_{L1}} = \frac{d_{S1} {V_{dc}}^2 (2 - B)}{P_{OUT} L_1} (t_4 - t_3). \tag{15}$$

The inductance is selected as

$$L_1 \geq \frac{d_{S1} {V_{dc}}^2 (2 - B)}{P_{OUT} K_L} (t_4 - t_3). \tag{16}$$

The capacitance C_i (i = 1, 2 and 3) can be calculated based on the voltage ripple on the capacitors C_i. In this case, the capacitor C_i is determined by the maximum voltage ripple at k% of the maximum voltages of the capacitors. The capacitors C_1 and C_2 are charged when the switches S_1 and S_2 are switched OFF. The capacitors C_1 and C_2 are discharged in the remaining cases of the switches S_1 and S_2. The capacitor C_3 is charged when the switch S_5 is switched ON, whereas it is discharged when the switch S_5 is switched OFF.

Assuming that the output load has the power factor ($\cos\varphi$) of 1, the longest discharging term of the capacitor C_3 in the proposed NLBI is between t_2 and t_5 as shown in the Figure 6. The maximum discharge amounts Q_3 of the capacitor C_3 is:

$$Q_3 \simeq I_o(t_4 - t_3) + I_o \sin(2\pi f_{out} t_3)(t_3 - t_2), \tag{17}$$

where I_o is the amplitude the output current. When the Q_3 is less than k% of the maximum charge of C_3, the capacitance C_3 needs to meet the condition as:

$$C_3 \geq \frac{Q_3}{kV_{C3}}. \tag{18}$$

The reduction of the capacitor C_1 or C_2 voltages is equal to the incensement of the capacitor C_3 voltage at times t_1 and t_5 as shown in Figure 6. At this time, the charging of capacitor C_3 affects the ripple of capacitors C_1 or C_2. Because the capacitor C_3 voltage is twice the capacitor C_1 voltage, the ripple of capacitor C_1 will be larger than that of the capacitor C_3. Therefore, the capacitance of selected capacitors C_1 and C_2 will be greater than or equal to the capacitance of capacitor C_3.

4. Simulation and Experimental Results

4.1. Simulation Results

PSIM 9.1.1 software was studied to verify the operational principle of NLBI. The input voltage is set at V_{dc} = 24 V and the simulation power is 680 W. The inductor L_1 = 2 mH. The capacitors C_1 = C_2 = C_3 = 2200 µF. The switching frequency is 15 kHz. Connect the resistor R = 36 Ω and use the inductor capacitor (LC) filter L_f = 2.5 mH, C_f = 1 µF.

Figure 7 shows the simulation results of the NLBI when A_m = 3.4, d_{S1} = 0.4. Figure 7a shows the nine-level output voltage V_{ab}, the load current i_o and the ripple voltage of the capacitors (V_{C1}, V_{C2}, V_{C3}). Figure 7b shows the voltage waveform of the switches S_1, S_2, S_3, S_5 and the voltage waveform of the H-bridge switches T_1–T_4. The capacitor voltages V_{C1}, V_{C2} and V_{C3} are boosted to 65 V from the input voltage of 24 V. The maximum voltage of the switches S_1 and S_2 is 65 V, while the maximum voltage of the switches S_3 and S_5 is 130 V. The maximum voltage on the switches T_1–T_4 is 260 V. Figure 7c,d show the harmonic spectrum of the output voltage V_{ab} and the load current i_o in the frequency domain, respectively. As seen in Figure 7c, the main component appears around the frequency of 15 kHz and 30 kHz.

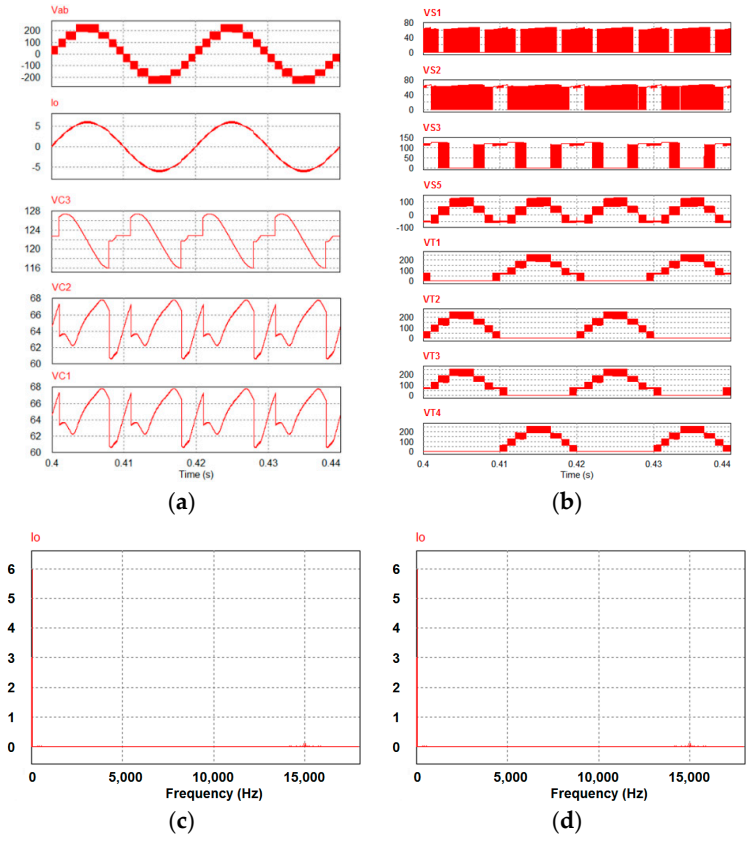

Figure 7. Simulation results of the proposed NLBI when d_{S1} = 0.4. The waveforms from top to bottom: (**a**) nine-level output voltage V_{ab}, load current i_o, capacitors C_3–C_1 voltage; (**b**) switches S_1, S_2, S_3, S_5 voltage and switches T_1–T_4 voltage of H-bridge circuit, (**c**) harmonic spectrum of nine-level output voltage and (**d**) harmonic spectrum of load current.

4.2. Experimental Results

A 350 W prototype based on TMS320F28335 DSP was built as shown in Figure 8. The input DC voltage is 24 V. The output voltage is 110 V_{rms}/50 Hz. The specifications of the experiment are given in Table 3. The switches S_1, S_2, S_3 and S_4 are 47N60C3 MOSFETs, whereas the other switches are G40N120 IGBTs. Note that the switch S_5 refers to MOSFET. Because the MOSFET without body diode is not available in the laboratory, a G40N60 IGBT without body diode is used in the experiment.

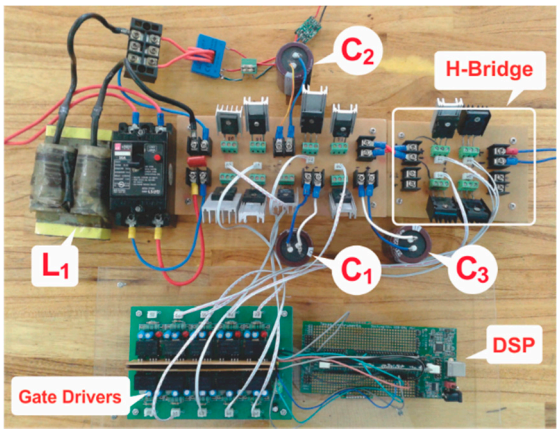

Figure 8. A laborotary prototype of single-phase NLBI.

Table 3. Operating Parameters for the Proposed Inverter.

Parameter		Value
Power rating		350 W
Input voltage (V_{dc})		24 V
Output voltage (V_{ab})		110 V_{rms}/50 Hz
Carrier ware frequency (f_s)		15 kHz
Inductors	L_1	2 mH
	L_f	1 mH
Capacitors	C_1, C_2, C_3	2200 µF/200 V
	C_f	1 µF
Power switches	S_1, S_2, S_3, S_4	47N60C3
	S_5	G40N60
	T_1, T_2, T_3, T_4	G40N120
Diodes (D_0, D_1, D_2, D_3)		DSEI60-06A
Gate drives		TLP250 (Photo-coupler)

Figure 9 shows the experimental results of the NLBI when A_m = 3.4, d_{S1} = 0.4. Figure 9a shows the waveforms of the output voltage V_{ab} and the load current i_o. As shown in Figure 9a, the output voltage has nine levels. As shown in Figure 9b, the capacitors C_1, C_2 and C_3 voltage are boosed to 52.2 V, 52.2 V and 92.5 V from the input voltage of 24 V, respectively. Figure 9c,d show the experiment results of switches S_1, S_2, S_3, S_5 voltage and switches T_1–T_4 voltage of the H-bridge circuit, respectively. Figure 9e,f shows the harmonic spectrum of the output voltage, V_{ab} and harmonic spectrum of output current.

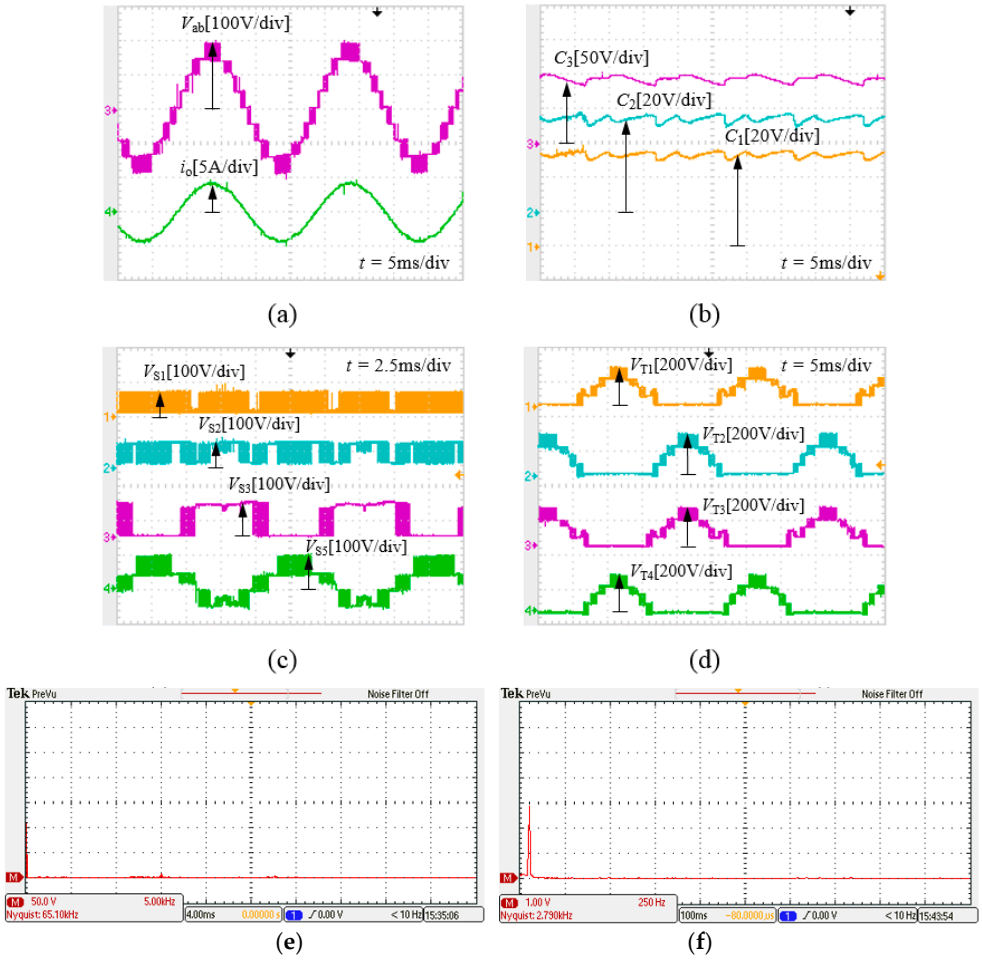

Figure 9. Experimental results of NLBI when A_m = 3.4, d_{S1} = 0.4 and V_{dc} = 24 V. The waveforms from top to bottom: (**a**) Output voltage V_{ab}, output current i_o inverter; (**b**) capacitors C_3, C_2, C_1 voltages; (**c**) voltage of switches V_{S1}, V_{S2}, V_{S3}, V_{S5}; (**d**) voltage of switches V_{T1}, V_{T2}, V_{T3}, V_{T4}; (**e**) harmonic spectrum of the nine-level output voltage; and (**f**) harmonic spectrum of output current.

Table 4 lists the theoretical, simulation and experimental values of B, V_{C1}, V_{C2} and V_{C3} when d_{S1} = 0.4, V_{dc} = 24 V, and A_m = 3.4. It can be seen from Table 4 that the simulation value is approximately equal to the theoretical value, which shows the correctness of the theoretical analysis. Moreover, the experimental value is less than that of corresponding theoretical value because the power losses are found in the experimental prototype. The voltage on capacitor C_3 is not equal to the sum of capacitors C_1 and C_2 because the discharge time of capacitor C_3 is longer associated with the losses on switches S_2, S_4, S_5 when charging capacitor C_3.

Table 4. Comparison between Calculated, Simulated and Experimental Values.

Data from	V_{ab} (V)	ΔV_{ab} (%)	B	V_{C1} and V_{C2} (V)	V_{C3} (V)
Theory	156.2	0	2.7	65	130
Simulation	152.2	2.56	2.7	64.6	122.3
Experiment	110	29.57	2.17	52.2	92.5

Here "ΔV_{ab}" is the percentage change between experiment and simulation versus theory.

5. Conclusions

In this paper, a nine-level boost inverter which decreases the number of switching elements by switching the capacitor in series and in parallel has been suggested. The main advantage of the

NLBI in comparison with the traditional topology is that the number of switches is reduced with using only a single DC voltage source. Therefore, the economic benefits from the proposed inverter come from the size and cost reduction of the inverter system. The output voltage expression and the parameter calculation are presented. Moreover, a control method based on the PWM technique is proposed for the proposed inverter. Finally, the simulation and experimental results of the NLBI are presented to validate its viability, well-performance, and effectiveness of suggested modulation strategy. The proposed inverter is suitable for low-power applications, where a low input voltage from renewable energy sources such as solar cell, fuel cell and battery needs to convert to a single-phase AC source.

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Nomenclature

A_m	peak amplitude of control waveform e_x
B	boost factor
CHB	cascade H-bridge
d_{avg}	average duty cycle of the boost inductor in each period T_s
d_{L1}	duty cycle of the boost inductor
d_{S1}	duty cycle generated by switch S_1
d_{S2}	duty cycle generated by switch S_2
d_x	duty cycle generated by switch S_1 and S_2
e_n	constant voltage
e_x	control waveform
f_{out}	output frequency
FC	flying-capacitor
G	voltage gain
i_o	load current
I_o	amplitude of output current
I_{L1}	average input current
ΔI_{L1}	current ripple of the inductor
K_L	current ripple factor of the inductor
MI	multilevel inverter
NLBI	nine-level boost inverter
NPC	neutral-point-clamped
PWM	pulse-width modulation
SC	switched-capacitor
SCMI	switched-capacitor multilevel inverter
SDC	switch-diode-capacitor
T_{avg}	average time interval of the charging inductor mode during the period T_s
T_s	period time
V_{ab}	output voltage
V_B	boost voltage
V_{dc}	dc source
V_L	inductor L_1 voltage

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