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A New Modular Multilevel Inverter Based on Step-Up Switched-Capacitor Modules

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Abstract: A new structure of switched capacitor multilevel inverter (SCMLI) capable of voltage boosting and with self-balancing ability is introduced in this article. This advantage is the result of a step by step rise of capacitor voltages in each module, supplied by just one DC voltage source. The proposed topology generates a sinusoidal output waveform with a magnitude several times greater than the input one. Higher output staircase AC voltage is obtained by applying a nearest level control (NLC) modulation technique. The most significant features of this configuration can be mentioned as: fewer semiconductor devices, remarkably low total harmonic distortion (THD), desirable operating under high/low frequency, high efficiency, inherent bipolar voltage production, easy circuit expansion, ease of control and size reduction of the circuit thanks to utilizing neither bulky transformer nor inductor. Moreover, the proposed SCMLI is comprehensively surveyed through theoretical investigation and a comparison of its effectiveness to recent topologies. Eventually, the operating principle of a 25-level prototype of the suggested SCMLI is validated by simulation in the MATLAB SIMULINK environment and experimental results.

Keywords: multilevel inverter; single-source converter; switched-capacitor; step-up converter; self-balancing

1. Introduction

The growth of energy consumption and reduction in fossil fuel reserves has led to renewable energy penetration in power system. In order to transmit the electricity generated by these sources to grids, power electronic devices are widely required. Hence, the noticeable role of power electronic converters in these applications have attracted the attention of many researchers aiming for augmentation of quality, efficiency and costs of such systems [1]. Among all kinds of power electronic converters, inverters are vitally required in such equipment. According to [2], the necessity of high voltage and high power inverters are significantly observed in bulk power controls.

Initial inverters, built in three-level topologies, suffered from high voltage stresses and total harmonic distortion (THD) [3]. Consideration of these limitations, resulted in the introduction of the multilevel inverter (MLI). These inverters are considered favorably for their special characteristics in less THD, lower dv/dt stress, better electromagnetic compatibility and of course lower switching losses [3–5]. Quality improvement of output voltage wave form depends on the number of voltage

levels in multilevel inverters (the greater the output voltage level, the greater the sinusoidal wave form). Based on the quality and type of source and high/medium power demand of circuit, different topologies for multilevel inverters are presented. These inverters are widely implemented in devices used daily such as ac motor equipment (like ac fans, mills, conveyers and pumps) which are commonly utilized in metal, power, oil and gas, water, mining, marine and chemistry industries [6].

The most applicable MLI topologies can be named as neutral point clamp (NPC) [7], flying capacitor (FC) [8], cascade H-bridge (CHB) [9] and switched capacitor (SC) [10] arrangement inverters. Each topology has its own weaknesses that made it necessary to introduce newer structures. For example, NPC and FC suffer from voltage balancing in their DC link capacitors due to their limited switching states. In CHB topology, the requirement of several DC sources causes considerable increase in the cost and size of the inverter.

Among these, the SC is more utilized in power electronic devices, thanks to its less source requirement (single DC source) and boosting capability with no need of any transformers or inductors and ease of controllability. The performance of SC inverter is summarized in charging several capacitors and then discharging them over the load in a predetermined pattern to make a staircase near the sinusoidal voltage. The output voltage amplitude is several times bigger than the input source depending on the structure and number of capacitors included. Recently, these topologies are used in applications such as: lasers, radars, X-rays [11], fuel-cell systems [12], UPS (uninterruptible power supplies) [13], White Light Emitting Diode (WLED), LCD drivers, fluorescent lamp [14], electrical vehicles [15], mobile equipment [16], Induction heating [17], grid integration of renewable energy systems [18], high-frequency AC micro grids [19], high-frequency AC power distribution systems [20], high-frequency-link DC transformers for a Medium Voltage Direct Current (MVDC) power distribution [21] and MRI (Magnetic Resonance Imaging) [22].

A new single-source multi-level inverter (MLI) based on the SC concept with the minimum number of switches is proposed by [23]. Reference [24] proposed another SC-based MLI. In this structure, not only is there no inductors but also larger voltage than the input one is produced. This increase is reached by connecting the capacitors in a series or parallel fashion. On the other hand, introducing two new MLIs consisting of SC units and H-bridges is presented by [25]. A single source SC-based MLI which makes it possible to reach several output levels is introduced by [26]. A different number of output levels is accessible by changing the number of SC cells. References [27,28] introduce new single-source switched capacitor multilevel inverter (SCMLI) structures producing high output voltage levels, aiming for reduction of both active and passive components. Considering power loss analysis is another noticeable aspect of these studies that further discussion over circuit loss is fundamentally investigated in [29,30].

Producing a 5-level output with 7 switches based on the SCMLI technique is presented in [31]. This structure is single source and requires 2 capacitors. Similarly, references [32,33] SC-based topologies are fed by one source aiming to boost the input voltage.

The presented article reveals a new single-source SCMLI topology, which is expected to operate in both high power and high voltage applications. In Section 2 the topology of proposed new SCMLI module and its cascaded structure is described. In Section 3 the operating principles of this topology is discussed. A comprehensive discussion on the proposed topology and others with similar criteria is performed in Section 4. Then, in Section 5, first, simulation results are presented and then experimental tests of the proposed topology are undertaken in the laboratory environment to verify the proposed inverter performance. Finally, Section 6 is devoted to the conclusion of this paper.

2. Proposed Topology

The structure of proposed SCMLI consists of two different parts which are connected one after another to achieve the desired performance (Figure 1). Each part consists of several switches and capacitors in order to generate predetermined voltage levels. The first part includes four capacitors and 14 switches (including 6 unidirectional and 4 bidirectional ones) controlled by 10 driver circuits.

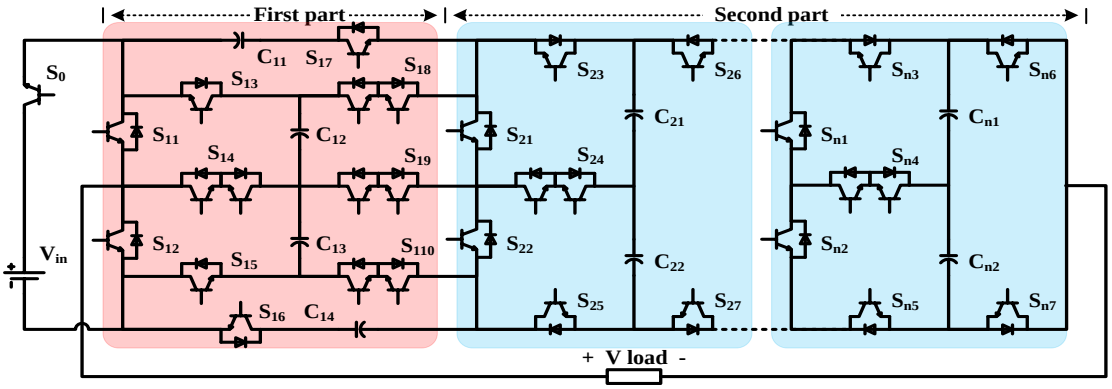


Figure 1. The overall structure of the proposed switched capacitor multilevel inverter (SCMLI).

Notice that the connection of two switches one after another form a unit to control the current flow bi-directionally. The topology is capable of generating 9 voltage levels containing 4 positive levels, 4 negative levels and a zero level. While the first part is made of one main module, the second part can be made by combining one or more sub-modules together. Each sub-module is made up of 2 capacitors and 8 switches (including 6 unidirectional and 1 bidirectional). By implementing 7 driver circuits, 5 different voltage levels (consist of 2 positive, 2 negative and a zero one) are achievable in each sub-module. Eventually, the predefined output voltage is achieved by combination of the two parts, which the number of sub-modules in the second part fundamentally depends on the desired output level.

3. Operating Principles

Figure 2 shows a 25-level prototype based on the proposed structure which consist of the main module and one sub-module in the second part. The output staircase waveform includes 12 positive, 12 negative and the zero level where each level is reached by synthesizing the different capacitors voltages. It is noticeable that, generating the required staircase waveform can be achieved considering the fact that all capacitors should be charged to the predetermined voltage. Besides, the limitation of rated voltage of the semiconductor devices must be taken into account during charge and discharge.

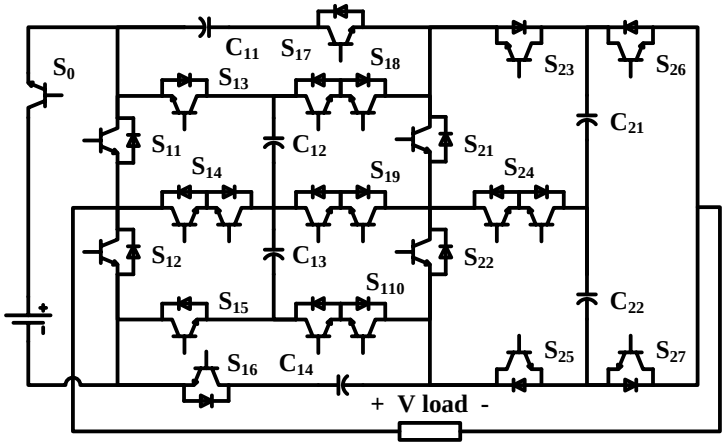


Figure 2. A 25-level prototype based on the proposed SCMLI structure.

To reach the aforementioned essentials, specific switching patterns for capacitors charging and discharging should be considered.

3.1. Capacitors Charging Pattern

Achieving the favorable voltage waveform requires predetermined charging paths for the capacitors. To reach this goal, the initial step is to charge the capacitors placed in the first part (main module). Regarding Figure 3a capacitor C_{12} is charged directly by the input source via S_0, S_{12}, S_{13} and S_{14} switches up to V_{in}. Similarly, C_{13} is supplied by the source up to V_{in} via S_0, S_{11}, S_{14} and S_{15} switches (Figure 3b). Then, capacitors C_{11}, C_{14} are charged to the $2V_{in}$ voltage by the serial connection of C_{12} and C_{13} (Figure 3c,d).

The next step is to charge the capacitors of the second part (the sub-module) by the serial combination of the capacitors voltages from the previous part. As shown in Figure 3e,f, by using 5 switches and 3 anti-parallel diodes, C_{21} and C_{22} are charged to $4V_{in}$. Then, for rest of the modules, two different approaches could be considered. This is either to charge all the other modules with the same voltage, or keep on multiplying (doubling) the capacitor voltages in each step. As a result, for an n-module structure the charging mode for the first and second method could be indicated by $(1,\ 2,\ 4,\ 4,\ 4, \ldots) \times V_{in}$ and $(1,\ 2,\ 4,\ 8,\ \ldots\ , 2^n) \times V_{in}$ respectively. Choosing each method depends on the amplitude of the input source, required output voltage level and the rated values of the semiconductors.

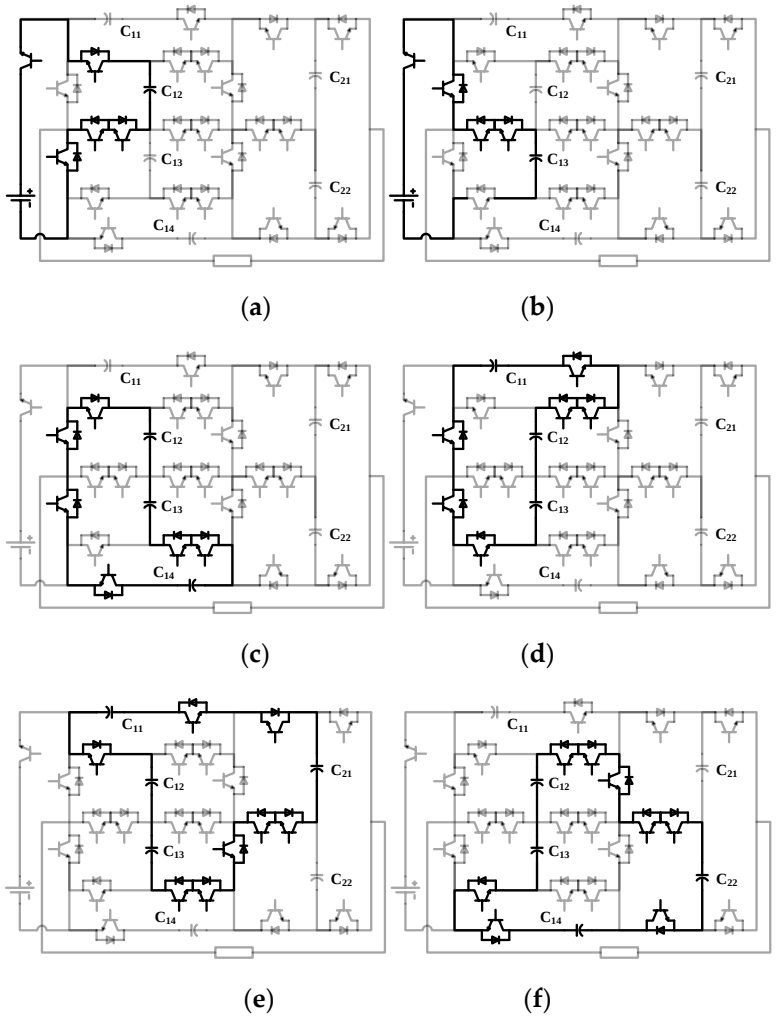


Figure 3. Capacitors charging paths for proposed SCMLI introduced in Figure 2 for (**a**) C12; (**b**) C13; (**c**) C14; (**d**) C11; (**e**) C21; (**f**) C22.

3.2. Output Multilevel Generation

The selected switching states for charge and discharge of the capacitors for the proposed SCMLI introduced in Figure 2 are brought in Table 1. Besides, the state of charge for each capacitor is shown by either ↑, ↓ or – representing charging, discharging and no change, respectively. As the main module requires 10 gate signals for its 14 switches, then its switching state consists of a 10-digit binary number (including 0 and 1), which 1 means that the corresponding switch in the defined row is in ON state and 0 means that it is in OFF state. Moreover, the switching state of the submodule consists of a 7-digit number. To simplify the demonstration, we separated this 17-digit number into 4-digit parts and turned them from binary to hexadecimal numbers. Then, each switching state is revealed by a 5-digit hexadecimal vector as S = (S_0, S_{11}, m_{11}, m_{12}, m_{21}, m_{22}). Where each term means m_{11} = (S_{12}, S_{13}, S_{14}, S_{15}), m_{12} = (S_{16}, S_{17}, S_{18}, S_{19}), m_{21} = (S_{110}, S_{21}, S_{22}, S_{23}), m $_{22}$ = (S_{24}, S_{25}, S_{26}, S_{27}).

Table 1. Selected switching states for charge and discharge of the capacitors (state of charge).

Levels	Switching States (C_{11}, C_{12}, C_{13}, C_{14}, C_{21}, C_{22})
+12 V_{in}	15871(-↓↓↓↓↓)
+11 V_{in}	33871(–↑↓↓↓)
+10 V_{in}	1C8F1(-↓↓↑↓↓)/140F1(-↓↓-↓↓)
+9 V_{in}	330F1(–↑-↓↓)/14151(-↓–↓↓)
+8 V_{in}	15829(-↓↓↓-↓)/090F1(—-↓↓) 1CA91(-↓↓↑↓↓)/2E151(-↑–↓↓)
+7 V_{in}	09151(–↓-↓↓)/33829(–↑↓-↓)/03A39(-↓↓↓↑↓)
+6 V_{in}	19611(↑↓↓-↓↓)/09A39(-↓↓↓↑↓)/140A9(-↓↓–↓)
+5 V_{in}	064B9(↓↓↓-↑↓)/330A9(–↑–↓)/14109(-↓—↓)
+4 V_{in}	0D411(↓↓↓-↓↓)/33109(–↑–↓)/15A4D(-↓↓↓-↑)
+3 V_{in}	33805(–↑↓–)/09109(–↓–↓)/2E249(-↑—↓)
+2 V_{in}	19E05(↑↓↓↓–)/1C885(-↓↓↑–) 09249(-↓↓–↓)/140F2(-↓↓—)
+1 V_{in}	14125(-↓—-)/064CD(↓↓↓–↑) 2E0F2(-↑↓—)/1C9D2(-↓↓↑–)
0	19685(↑↓↓—)/2E125(-↑—-) 33152(–↑—)/15A3A(–↓↑–)
−1 V_{in}	03A3A(-↓↓↓↑-)/19725(↑↓↓—) 2E265(-↑—-)/09152(–↓—)
−2 V_{in}	11C3A(↓↓↓↓↑-)/09212(-↓↓—) 1C8AA(-↓↓↑↓-)/140AA(-↓↓-↓-)
−3 V_{in}	2E412(↓↑—-)/064BA(↓↓↓-↑-)/1410A(-↓–↓-)
−4 V_{in}	3310A(–↑-↓-)/0D412(↓↓↓—)/15A4E(-↓↓↓↓↑)
−5 V_{in}	03A4E(-↓↓↓↓↑)/197A(↑↓↓-↓-)/03806(–↓↓↓↓)
−6 V_{in}	11E4E(↓↓↓↓↓↑)/0924A(-↓↓-↓-)/19E06(↑↓↓↓↓↓)
−7 V_{in}	064CE(↓↓↓-↓↑)/14126(-↓–↓↓)/33086(–↑-↓↓)
−8 V_{in}	1944A(↑↓↓-↓↓)/0D44A(↓↓↓-↓-) 33126(–↑-↓↓)/14266(—-↓↓)
−9 V_{in}	2E266(-↑–↓↓)/19726(↑↓↓-↓↓)
−10 V_{in}	19666(↑↓↓-↓↓)/09266(-↓↓-↓↓)
−11 V_{in}	2E466(↓↑–↓↓)
−12 V_{in}	0D466(↓↓↓-↓↓)

Figure 4 illustrates a few selected discharging paths related to the switching states of Table 1 resulting in a specific mixture of multiple capacitors shaping the staircase output voltage.

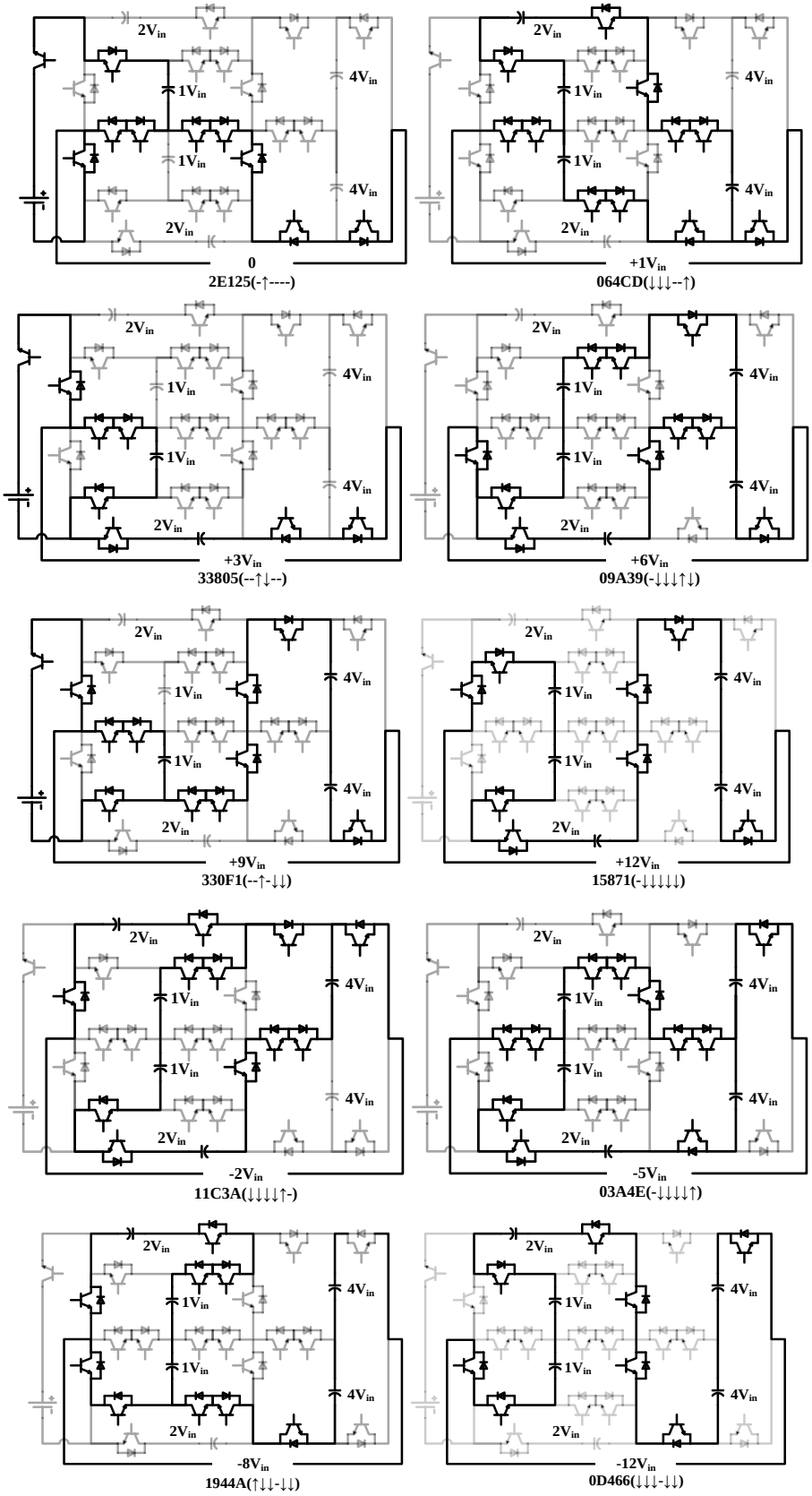


Figure 4. A few selected discharging paths related to the switching states of Table 1.

3.3. Modulation Strategy

The NLC (nearest level control) technique is utilized for operation of the proposed SCMLI in order to generate the desired staircase voltage. This method generates voltage level by converting the nearest voltage level (V_{nl}) to the predetermined voltage reference (V_{ref}) [29]. Implementation of this technique not only leads to augmentation of process speed but also eases the calculations by its conceptual and implementation simplicity.

Furthermore, small voltage steps beside low switching frequency allowance makes this technique one of the most suitable methods for high level MLIs. Considering mentioned options, proper switching states could be adapted for each voltage level by the help of switching table (see Table 1). As it is shown in Figure 5, initially the waveform is formed by comparing the V_{ref} and desired output voltage waveform. Then the V_{nl} can be determined with:

$$V_{nl} = \frac{1}{V_{in}} \text{round}(V_{ref}) \tag{1}$$

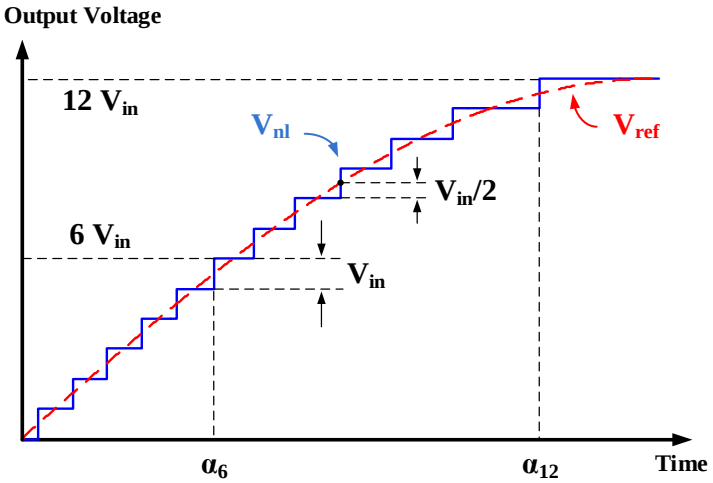


Figure 5. The operation schematic of the nearest level control (NLC) method.

3.4. Calculations of the Capacitances

To prevent capacitors undercharging and maintaining their voltage ripple in an acceptable range, the capacitances should be determined carefully in the SCMLI topologies. Two main factors should be considered while calculating the circuit capacitances: (1) amplitude of the output current and the phase difference between output voltage and current (2) capacitors discharging time in the worst case. Therefore, maximum discharging of each capacitor can be calculated as [24]:

$$\Delta Q_{Ci} = \int_{t_{1i}}^{t_{2i}} I_{out} \sin(2\pi f_o t - \phi)\, dt \tag{2}$$

where f_o is fundamental output frequency and I_{out} is the amplitude of the output current. $[t_{1i}, t_{2i}]$ is the longest discharging period for each capacitor to demonstrate the worst case. Notice that each pair of (C_{12}, C_{13}), (C_{11}, C_{14}) and (C_{21}, C_{22}) have the same capacitance values.

Considering k as the maximum acceptable voltage ripple, the equivalent capacitance of the circuit while supplying the load is obtained as:

$$C_{eq} \geq \frac{\Delta Q_C}{k\, V_{eq}} \tag{3}$$

As the capacitors C_{12} and C_{13}, are charged directly by the input source (see Figure 3a,b), thus their voltage is equal to:

$$V_{12} = V_{13} = V_{in} \tag{4}$$

Considering p percent tolerance for voltage drop while charging each capacitor, C_{11} and C_{14} are charged by series combination of C_{12} and C_{13} (see Figure 3c,d). Thus their voltage would be calculated as:

$$V_{11} = V_{14} = (1-p) \times (V_{12} + V_{13}) = \frac{\frac{C_{12}}{2}}{\frac{C_{12}}{2} + C_{11}} \times (V_{12} + V_{13}) \tag{5}$$

Meaning that $V_{11} = V_{14} = 2(1-p) \times V_{in}$. Also the voltages across C_{12} and C_{13} would decrease to $V_{12} = V_{13} = (1-p) \times V_{in}$, unless they are charged again by the DC source. Consequently C_{11} is obtained by $C_{11} = C_{14} = \frac{C_{12}}{2} \times \frac{p}{(1-p)}$. Finally, C_{21} and C_{22} are charged by series combination of either C_{11}, C_{12} and C_{13} or C_{14}, C_{12} and C_{13} (see Figure 3e,f) up to:

$$V_{21} = V_{22} = 4(1-p)^2 \times V_{in} \tag{6}$$

Which means that $C_{21} = C_{22} = \frac{C_{12}}{2} \times \frac{p^2}{(1-p)}$. Afterwards, in order to transfer the voltage of each sub-module to the next one properly with minimum possible voltage drop, the capacitance values in each sub-module should be $\frac{1}{2} \times \frac{p}{(1-p)}$ times of the previous one. By knowing the value of C_{eq} and the aforementioned equations, the exact value of every capacitor can be obtained.

4. Discussion

This section presents a discussion on the proposed topology, including two parts: comparison of the proposed structure with a few existing ones, and determination of losses and efficiency.

4.1. Comparison

Table 2 reveals a comprehensive study on the proposed SCMLI structure and six others, for a (2N + 1) level output voltage. The study is categorized into seven parts considering: number of active switches, series diodes, capacitors, driver circuits, the ability to produce bipolar output, peak inverse voltage (PIV) and total standing voltage (TSV).

Table 2. Comparison of the Suggested SCMLI with six other topologies for a (2N + 1) level output.

Items	Proposed	[10]	[23]	[24]	[25]	[26]	[28]
Switches	$-18+8\log_2(2N+8)$	2N + 4	2N + 2	3N + 4	2N + 2	N + 4	3N + 1
Diodes	0	2N − 2	N − 1	0	N − 1	2N − 2	0
Capacitors	$-4+2\log_2(2N+8)$	N − 1	N − 1	N - 1	N − 1	N − 1	N − 1
Drivers	$-18+7\log_2(2N+8)$	2N + 4	2N + 2	3N + 4	2N + 2	N + 4	3N + 1
Bipolar output	inherent	With H-Bridge	With H-Bridge	With H-Bridge	With H-Bridge	With H-Bridge	inherent
PIV(*V_{in})	$\frac{2N+8}{4}$	N	N	N	N − 1	N	N
TSV(*V_{in})	$-20+\frac{11(2N+8)}{4}$	N^2+5N+1	$\frac{N^2+11N-4}{2}$	7N	7N − 7	N^2+4N-1	$\frac{N^2+5N}{2}$
Output levels	2N + 1	2N + 1	2N + 1	2N + 1	2N + 1	2N + 1	2N + 1

The comparison results are illustrated in Figure 6. As shown in Figure 6a, in terms of the semiconductor devices the presented SCMLI utilizes much less active switches and diodes to produce the same output voltage. One may note that [26] needs less active switches, but it is important that [26] uses two series diodes to generate each voltage level. Figure 6b in which the aforementioned topologies are compared in terms of number of capacitors involved in their circuit, implies that the presented topology requires less than 10 capacitors to produce high level output voltages thanks to its multiplying characteristic.

It is noteworthy that unlike most other SCMLIs, the proposed concept requires no auxiliary circuit like H-bridge to generate a bipolar voltage. A closer look at Figure 6c reveals that the suggested topology can operate by using semiconductor devices with lower ratings, consequently reducing the total cost of the circuit. In addition, having the lowest amount of the TSV (see Figure 6d) makes the proposed structure suitable for high-voltage applications.

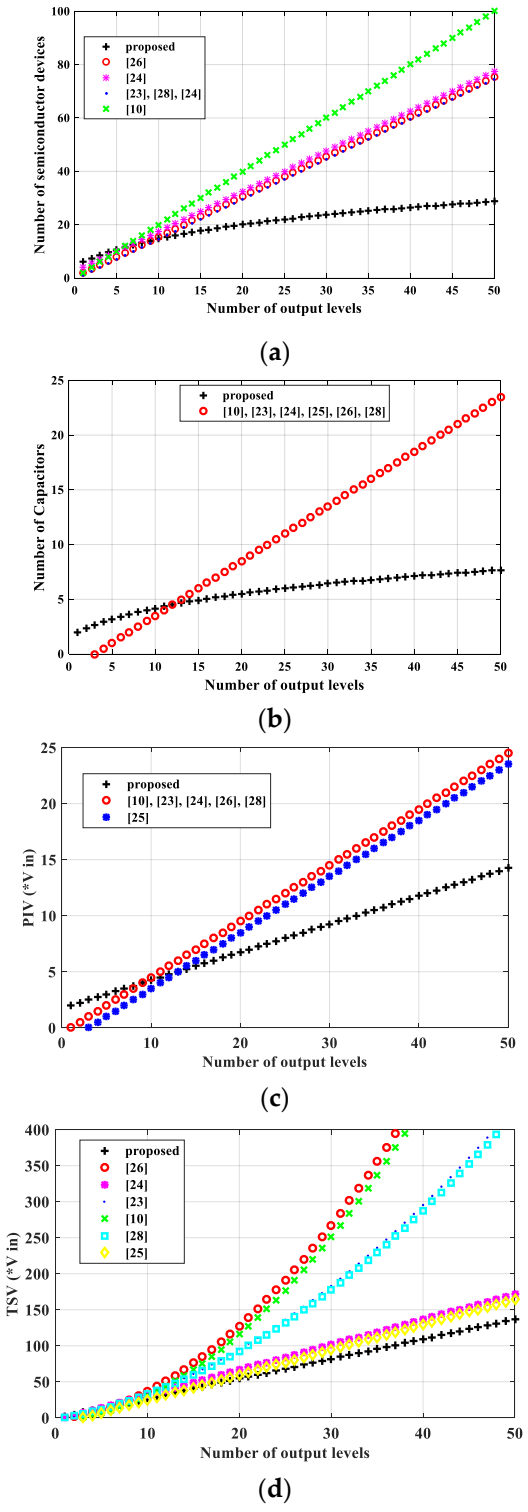


Figure 6. Comparison results of Table 2 in terms of (**a**) number of semiconductor devices (**b**) number of capacitors (**c**) peak inverse voltage (PIV) (**d**) total standing voltage (TSV).

4.2. Determination of Losses and Efficiency

Total circuit loss fundamentally depends on two important sources namely switching and conduction losses [30]. Switching loss enrolls the most important part of circuit loss caused by switching delays which are semiconductor devices inherent characteristics. This source of loss occurs in the course of turning ON and OFF of the active switches determined by the following Equations [27]:

$$P_{sw-i(ON)} = f_{sw} \int_0^{t_{on}} V_{off\,state-i}(t) \cdot i(t)dt = \frac{1}{6} f_{sw}\, V_{off\,state-i}\, I_{on\ state1-i}\, t_{on} \tag{7}$$

$$P_{sw-i(OFF)} = f_{sw} \int_0^{t_{off}} V_{off\,state-i}(t) \cdot i(t)dt = \frac{1}{6} f_{sw}\, V_{off\,state-i}\, I_{on\ state2-i}\, t_{off} \tag{8}$$

Note that in these equations, f_{sw} represents the switching frequency of each switch of the circuit, $V_{off\,state-i}$ stands for the off-state voltage of ith switch, $I_{on\ state1-i}$ is the current of ith switch when the switch is entirely turned on, and $I_{on\ state2-i}$ shows the current of ith switch before turning off. Therefore, overall switching loss of the whole circuit can be obtained from the following equation:

$$P_{sw} = \sum_{i=1}^{N-switch} \left(\sum_{j=1}^{N_{on(i)}} P_{sw-on(ij)} + \sum_{j=1}^{N_{off(i)}} P_{sw-off(ij)} \right) \tag{9}$$

Consider that $N_{on(i)}$ and $N_{off(i)}$ are the number of times which ith switch turns on and off, throughout one cycle. On the other hand, conduction loss is basically generated due to current of semiconductors and hence the load. This loss is calculated by [29]:

$$P_{con-L} = P^{sw}_{con-L} + P^{D}_{con-L} = (k_1 \cdot V^{sw}_{on} + k_2 \cdot V^{D}_{on}) \cdot i_{av-L} + (k_1 \cdot R^{sw}_{on} + k_2 \cdot R^{D}_{on}) \cdot i^2_{rms-L} \tag{10}$$

where $i_{av\text{-}L}$ and $i_{rms\text{-}L}$ are average and RMS current of voltage level L, respectively. Coefficients k_1 and k_2 are the number of switches and diodes involved in each level, respectively. Finally, total conduction losses can be calculated as:

$$P_{con} = \sum_{L=-12}^{12} P_{con-L} \tag{11}$$

Efficiency (η) is obtained from:

$$\eta = \left(\frac{P_{out}}{P_{out} + P_{loss}} \right) \times 100 \tag{12}$$

where P_{loss} includes switching losses (P_{sw}) and conduction losses (P_{con}). For the proposed SCMLI with $V_{in} = 30$ V, $V_{out-max} = 360$ V, $f_{out} = 50$ Hz and using IRF740MOSFET switches, exact calculations were made and the efficiency reached to 92.63%. It is worth highlighting that in the proposed topology of this article the f_{sw} is considerably lower than conventional structures (in the range of 50 Hz up to 1 KHz). Consequently, achieving both lower switching loss and total circuit loss is accessible.

Moreover, in Table 3 the proposed inverter has been compared with other recently introduced topologies in terms of the efficiency. The results depict that the proposed converter not only has the least possible number of components (including active switches with lower TSV, drivers and capacitors), but also enjoys higher efficiency under different load conditions.

The overall efficiency of the proposed 25-level converter is investigated experimentally and theoretically with different loadings as depicted in Figure 7. As can be seen, the lower efficiencies have been recorded by increasing the output power. These high-efficiency values occurred as a result for the few involved components in the current flow paths. The measured efficiencies are in good agreement with theoretical ones.

Table 3. Comparison of the proposed topology with other recently introduced ones in terms of efficiency.

Topologies	I Load (A)	P Out (W)	Efficiency (%)	
			Theoretical	Experimental
Proposed	1	180	92.13	90.22
	2	360	92.63	90.85
	4	720	91.65	88.69
	8	1440	91.17	87.61
[24]	0.5	5.8	85.9	84.9
[26]	3.1	247.5	Not mentioned	89.2
[28]	2	1000	90	87.5

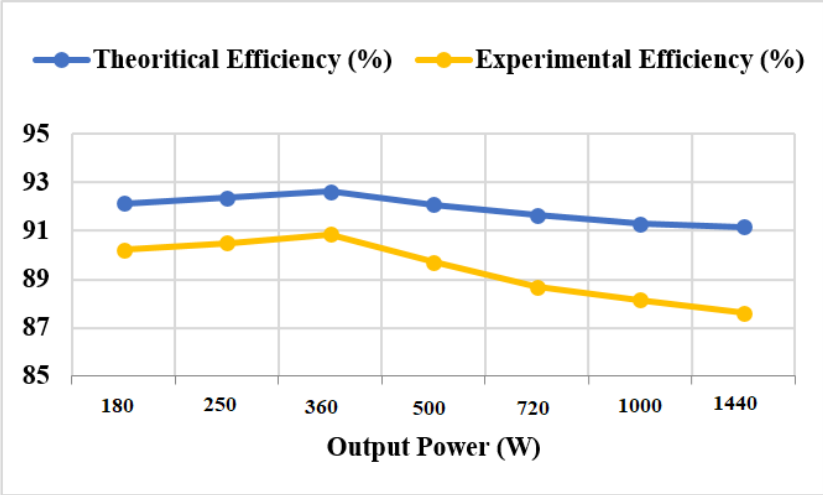


Figure 7. The overall efficiency of the proposed inverter for different output powers.

5. Results

Evaluation of the proposed theory is comprehensively accomplished in both simulation and experimental sections which are exclusively explained in the following parts.

5.1. Simulation Results

In order to prove the concept of the presented structure, MATLAB simulations were done on a 25-level (30 volts each level) inverter of the proposed topology, using NLC modulation. Figure 8a shows the output voltage and current waveforms for an input of 30 volts (DC) and a resistive load of R = 180 Ω.

It is worth noting that the amplitude of the output voltage is 12 times the input. The FFT (fast Fourier transform) of the load voltage is illustrated in Figure 8b. This reveals that the amount of Voltage THD is 3.27% and the amplitude of all voltage harmonics are below 0.6% of the fundamental one.

On the other hand, Figure 8c illustrates the output waveforms of a resistive-inductive load with a power factor of 0.75 (R = 180 Ω and L = 500 mH). In this case, the harmonic content of the load current is 0.18%, which is considerably lower (Figure 8d).

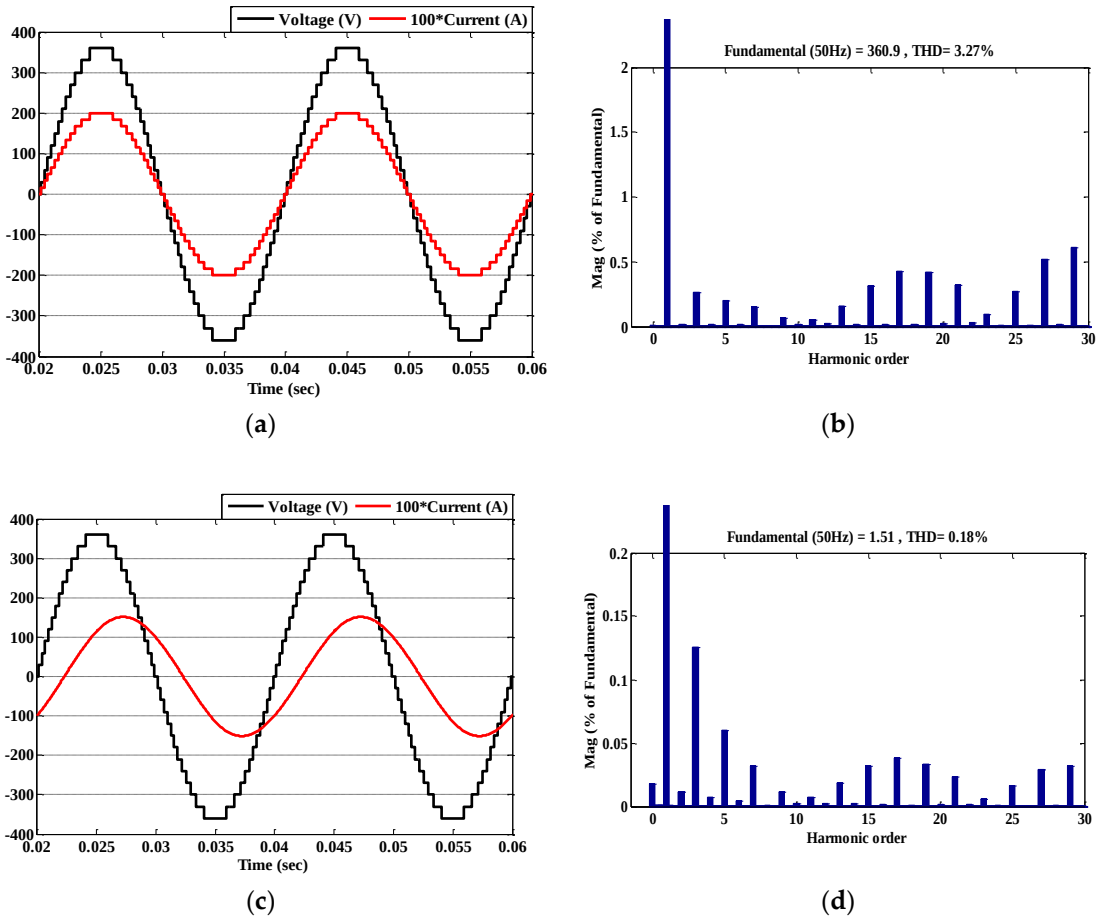


Figure 8. Simulation results of a 25-level inverter of the proposed topology: (**a**) output waveforms of a resistive load (R = 180 Ω); (**b**) fast Fourier transform (FFT) analysis on the output voltage; (**c**) output waveforms of a resistive-inductive load (R = 180 Ω, L = 500 mH); (**d**) FFT analysis on the load current.

5.2. Experimental Results

In order to validate the simulation results, a laboratory prototype of a 25-level inverter of the presented SCMLI is made. Figure 9 shows the test setup which is fabricated using the parameters of Table 4.

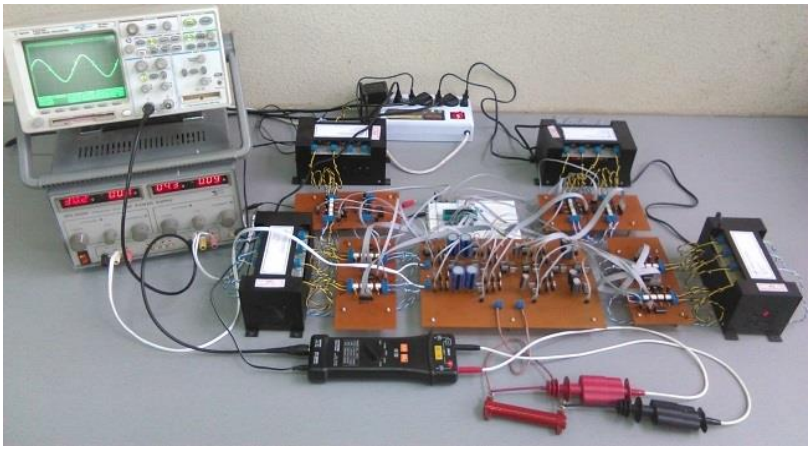
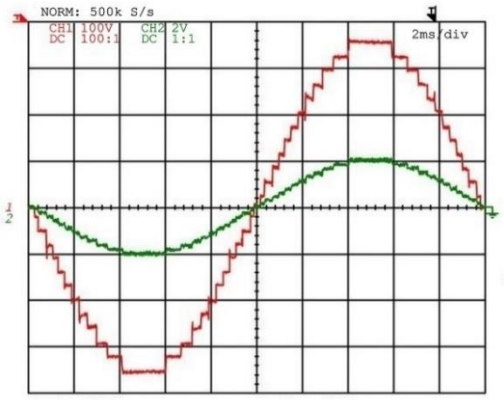


Figure 9. Laboratory test setup of a 25-level inverter of the presented SCMLI.

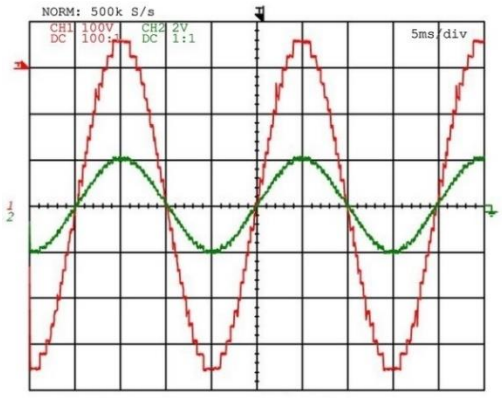
Table 4. Laboratory setup specifications.

Component	Specification
Input voltage (V_{in})	30 V
Output voltage levels	25
Output frequency	50 Hz
Switches	IRF740 MOSFET
Capacitors	$C_{11} = C_{14} = 1300$ µF $C_{12} = C_{13} = 23{,}000$ µF $C_{21} = C_{22} = 130$ µF
Switches gate driver	HCPL3120
Voltage probe	PINTEK DP-50
Current probe	FLUKE 80i-110s AC/DC
R load	180 Ω
R-L load	180 Ω, 500 mH

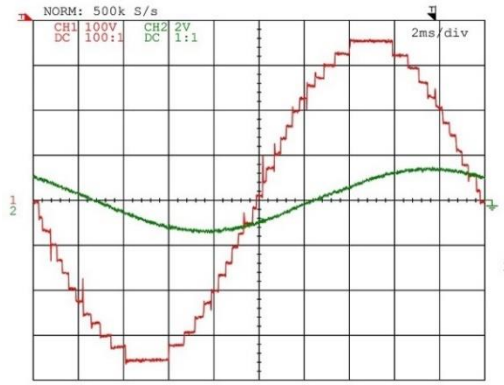
Figure 10a,b illustrate the experimental results of the test setup, for a pure resistive load of R = 180 Ω. The voltage and current waveforms comprise 25 steps from peak to peak (each of 30 volts). Note that the voltage probe is set on 100:1 ratio. In addition, test results of a resistive-inductive load (R = 180 Ω, L = 50 mH) with a power factor of 0.75 is brought in Figure 10c,d.



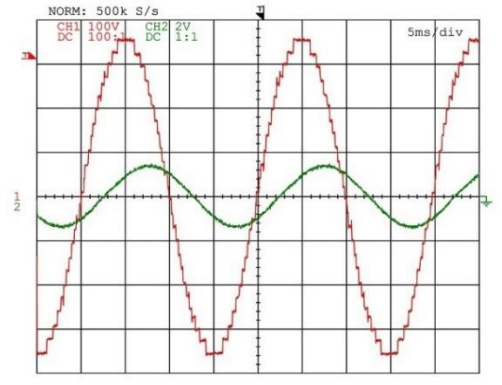
(**a**) CH1: 100 V/div, CH2: 2 V/div, 2 ms time/div



(**b**) CH1: 100 V/div, CH2: 2 V/div, 5 ms time/div



(**c**) CH1: 100 V/div, CH2: 2 V/div, 2 ms time/div



(**d**) CH1: 100 V/div, CH2: 2 V/div, 5 ms time/div

Figure 10. Experimental results of the proposed SCMLI: (**a**) R load (2 ms time/div); (**b**) R load (5 ms time/div); (**c**) RL load with a power factor of 0.75 (2 ms time/div); (**d**) RL load with a power factor of 0.75 (5 ms time/div).

6. Conclusions

The introduced novel switched-capacitor multilevel inverter (SCMLI) with self-balancing capability presents a modular structure with high gain modules in which each capacitor is charged by two capacitors through a predetermined path. The NLC modulation technique is applied for operation of the configuration resulting in a better sinusoidal output voltage waveform. Theoretical analysis, along with simulation in MATLAB software, represent the efficiency peak at 92.63% and also the THD reaching 3.27%. Moreover, comparative study implies that the suggested construction performs better in terms of PIV and TSV compared with recent topologies. The proposed topology not only needs fewer capacitors and semi-conductor devices, but also, thanks to inherent specifications of the module, it utilizes fewer driver circuits. Furthermore, the operation of the proposed structure is validated by test results of a 25-level prototype.

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Nomenclature

Parameter	Definition
V_{in}	Input Voltage
S_i	Switch number i
C_i	0Capacitor i
V_{nl}	Nearest Voltage Level
V_{ref}	Reference Voltage
ΔQ_{Ci}	The Charge drawn from each Capacitor
I_{out}	Output Current
PIV	Peak inverse Voltage
TSV	Total Standing Voltage
$P_{sw-i(ON)}$	Switching Loss of the i^{th} switch while turning on
$P_{sw-i(OFF)}$	Switching Loss of the i^{th} switch while turning off
$V_{off\ state-i}$	off-state voltage of i^{th} switch
$I_{on\ state1-i}$	Current of the i^{th} switch when the switch is entirely turned on
$I_{on\ state2-i}$	Current of the i^{th} switch before turning off
$N_{off(i)}$	Number of times which i^{th} switch turns off
$N_{on(i)}$	Number of times which i^{th} switch turns on
P_{con-L}	Conduction Loss of L^{th} level
P^{sw}_{con-L}	Conduction Loss of all switches in L^{th} level
P^{D}_{con-L}	Conduction Loss of all diodes in L^{th} level
V^{sw}_{on}	On-state voltage of the switches
V^{D}_{on}	On-state voltage of the diode
R^{sw}_{on}	On-state resistance of the switches
R^{D}_{on}	On-state resistance of the diodes
$\mathbf{i_{av-L}}$	Average current of voltage Level L
$\mathbf{i_{rms-L}}$	RMS current of voltage level L
η	Efficiency
fsw	Switching frequency

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