An MPC Reference Governor Approach for Enhancing the Performance of Precompensated Boost DC–DC Converters

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Abstract: This article addresses the problem of enhancing the performance of boost DC–DC converters that are already compensated either in voltage-mode by a common proportional–integral–derivative (PID, Type III) primary controller or in current-mode with a two-loop PI control law. Improved performance may be obtained with the addition of a secondary controller/prefilter in the form of a reference governor. This complementary scheme adjusts the imposed voltage reference input signal dynamically and can be designed in an optimal fashion via the model predictive control (MPC) methodology. Our evaluation with numerical simulation in MATLAB suggests that this two-level controller can effectively enhance the performance of a DC–DC boost converter in a wide operating range without imposing extra requirements or limitations. A simple linear MPC design in explicit form is employed in this approach, which is computationally tractable for digital microprocessor implementation. This work paves the way for future research involving reference governor ideas in the area of bilinear power electronic converters.

1. Introduction

Reference governor techniques have only very recently appeared in the power electronics field [1–3]. Such ideas have been developed theoretically for over two decades and already applied to other engineering fields, mainly in the automotive industry and robotics (see, e.g., [4–6] and references therein). Especially for the more demanding types of DC–DC converters (i.e., boost converters with nonlinear dynamics), many advanced control methods have been recently proposed with the aim of improving their transient response and robustness [7–13], including model predictive control (MPC) technology [14–19]. The vast majority of the control algorithms developed are replacements to the primal controller, resulting in an increased complexity and implementation cost. However, there are many cases in which the main controller is already hard-coded or implemented in low-cost hardware with certified performance, stability, and robustness, which we would not like to sacrifice or which is not possible to replace. Instead of replacing this controller, a new idea is to complement it with a secondary, higher-level controller that provides a dynamically modified reference signal to the primal controller. This idea results in a two-loop control structure, where the outer loop provides a modified reference to the inner loop and can also run in a different (slower) rate as it usually involves on-line (e.g., MPC) optimization.

In this paper, the idea of using an MPC reference governor scheme is applied for the first time, to the best of the author's knowledge, to a voltage-mode-controlled boost DC–DC converter. A similar technique has been recently tested for a DC–DC buck converter controlled by a simple

proportional–integral (PI) primary controller [1]. However, the case of a boost converter presents further nontrivial challenges as its dynamics are nonlinear (bilinear), it is a nonminimum phase system, and it requires a much more complicated primary controller. The so-called PI–derivative (PID) Type III controller is an industrial standard for boost converters [20,21]; however, further performance enhancement is possible using a predictive controller and a hybrid scheme combining PID and predictive controllers, as shown in [22]. Considering a standard PID Type III primary controller, this work demonstrates that an MPC reference governor in explicit form can be found that provides improved performance without imposing more stringent operational requirements (higher currents or component stress) or extra constraints. This framework can offer improvements and more degrees of freedom compared to the results of [22], at the expense of added complexity. These findings are supported by extensive simulation results.

Additionally, current-mode, two-loop PI controllers, which are quite common for boost converters, are also studied. Similar MPC reference governor ideas are applied and performance improvements are also obtained, especially in disturbance rejection tasks and soft-start startup situations.

This paper is structured as follows. Section 2 describes the DC–DC boost converter, and Section 3 outlines the basic controllers used in the literature. The main results are included in Sections 4–6. Section 4 provides a detailed exposition of the design procedure for the proposed voltage-mode MPC reference governor scheme, while Section 5 presents a thorough evaluation with numerical simulation results. The current-mode scheme is presented in Section 6. The final section concludes.

2. DC–DC Boost Converter

The circuit diagram of the boost converter considered in this paper is shown in Figure 1. A nonideal circuit with parasitic elements of the inductor and the capacitor was adopted. For comparison purposes, the values and the parameter ranges used were taken from [22], and they are summarized in Table 1, where f_s is the switching frequency of the pulse width modulator (PWM), and D is the duty cycle taking values in the interval [0, 1].
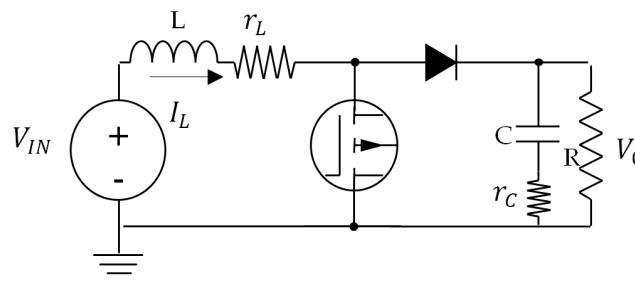

Figure 1. Boost converter circuit.

Table 1. Boost converter parameter values and ranges.

f_s (KHz)	V_{IN} (V)	L (μH)	r_L (Ω)	C (μF)	R (Ω)	r_C (Ω)	V_0 (V)	D
200	8–14	100	0.05	200	10–50	0.01	24	0.42–0.58

A common averaging small-signal analysis (see, e.g., [23]) leads to a typical transfer function from the duty cycle $d(t)$ to the output voltage $v_0(t)$ in the following form:

$$G_{v_0d}(s) = \frac{v_0(s)}{d(s)} = G_{d0} \frac{\left(1 + \frac{s}{\omega_{Z_1}}\right)\left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \tag{1}$$

with one zero ω_{ZC} in the left half plane, another zero ω_{RHPZ} in the right half plane (nonminimum phase behavior), and two poles parameterized by the frequency ω_0 and the quality factor Q, where

$$G_{d0} = \frac{V_{IN}}{(D')^2} = \frac{V_0^2}{V_{IN}}, \quad \omega_0 = \frac{1}{\sqrt{LC}}\sqrt{\frac{r_L + R\,(D')^2}{R}} \cong \frac{1}{\sqrt{LC}}\frac{V_{IN}}{V_0}, \quad D' = 1 - D, \quad \omega_{Z_1} = \frac{1}{C\,r_C},$$

$$\omega_{RHPZ} \cong \frac{R}{L}\left(\frac{V_{IN}}{V_0}\right)^2, \quad Q = \frac{\omega_0}{\frac{r_L}{L} + \frac{1}{C(R + r_C)}} \tag{2}$$

3. PID Type III and ARMarkov Predictive Control Design

A standard control strategy in industrial applications, including power electronics, is the PID controller. A special form of practical PID with three poles and two zeros, a double pole (second-order filter for high-frequency roll-off and noise mitigation), and a double zero (offering the necessary phase boost) is typically used in power electronics. It is known as the Type III compensator (see Figure 2), and its design is usually performed based on the so-called small-signal model of the converter in the frequency domain [23]. Typical requirements are a phase margin (PM) above 45° and a gain margin (GM) over 10 dB. In the present work, and as a reference point for assessing the performance of the proposed MPC reference governor scheme, the design presented in [22] was adopted. The transfer function of the Type III compensator is as follows:

$$G_{PID}(s) = \frac{k_{PID}}{s}\frac{\left(1 + \frac{s}{\omega_{ZC}}\right)^2}{\left(1 + \frac{s}{\omega_{PC}}\right)^2}, \quad \omega_{PC} = 10\,a_P\omega_{0dB}, \quad \omega_{0dB} = \omega_{RHPZ},$$

$$\omega_{ZC} = \frac{a_P\,\omega_{0dB}}{10}, \quad k_{PID} = \frac{(a_P\,\omega_{0dB})^3}{100\,G_{do}\omega^2}\rho \tag{3}$$

where the values a_P, ρ are design parameters selected by the tuning procedure in order to obtain the required PM and GM values. The Type III controller in [22] was tuned for the worst-case operating conditions $V_{IN} = 8$ V, $R = 10\ \Omega$, $D = 0.585$, which resulted in the following values:

$$G_{d0} = 72, \quad \omega_0 = 2.357\ \text{krad/s}, \quad \omega_{Z_1} = 50\ \text{krad/s}, \quad \omega_{RHPZ} = 11.111\ \text{krad/s}, \quad Q = 2.3582 \tag{4}$$
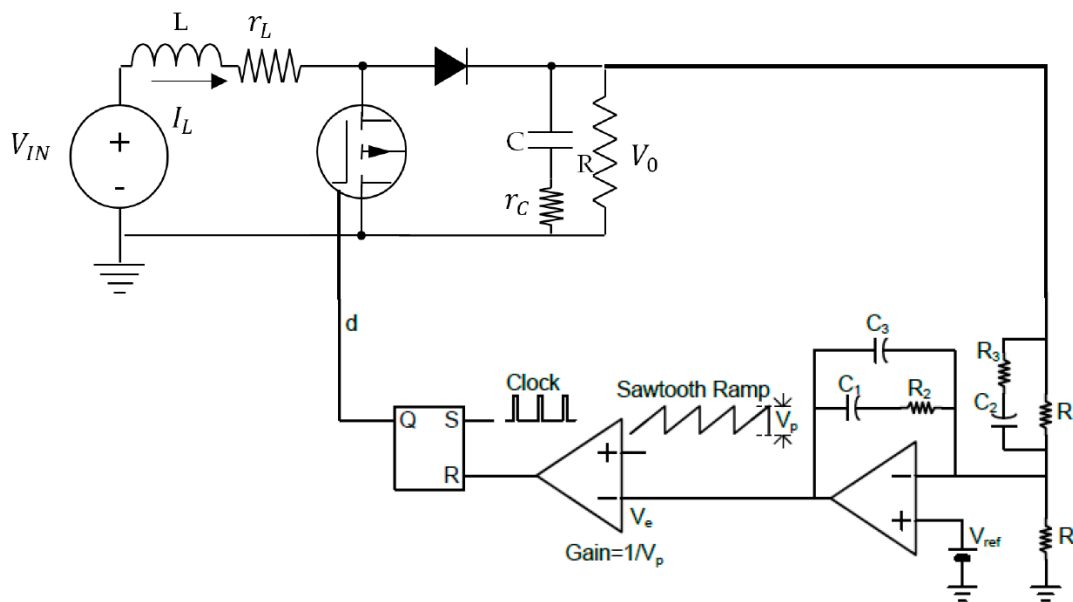

Figure 2. Type III voltage-mode compensation circuit.

For an appropriate selection $a_P = 1$, $\rho = 0.4$ the controller's transfer function takes the following form:

$$G_{PID}(s) = \frac{129}{s} \frac{\left(1 + \frac{s}{1111}\right)^2}{\left(1 + \frac{s}{111100}\right)^2} \tag{5}$$

As demonstrated in [22], this controller has good disturbance rejection properties but suffers from a slow startup response with a large average settling time of 15 ms. Another predictive controller called reduced-order ARMarkov-PFC (ROAPFC) has been designed, which exhibits significantly shorter average settling time without oscillations during the startup. However, this predictive controller has been shown to have noticeably worse disturbance rejection properties with oscillatory transients (three different perturbations, i.e., load, input, and set-point step changes, have been tested, as detailed later). The authors therefore produced the best results by combining the two controllers, Type III and ROAPFC, with appropriate weighting factors and additional feedforward compensation, in a new hybrid version termed APP controller (<u>A</u>RMarkov <u>P</u>lus <u>P</u>ID). In this way, the advantages of both controllers are exploited, and a good response in all operating conditions can be obtained. The predictive controller ensures a fast and acceptable transient during startup, while the Type III controller offers good disturbance rejection properties around normal operating conditions. Other recently proposed optimal techniques, e.g., [8,9], have been shown in [22] to perform equally well when dealing with disturbances, but they fail to offer consistent performance in the whole operating range or in unfavorable circumstances (due to very high gains, excessive currents during startup are required).

The ARMArkov-PFC controller is a special type of MPC controller with low computational burden, offering ease of practical implementation in quick processes. One of its advantages is the simple form of the controller, which is a difference equation of relatively low order, requiring only output measurements (inductor current measurements are avoided). More specifically, the PFC controller designed in [22] for the converter in (1), which is a fourth-order discrete transfer function, was converted to a continuous form using Tustin transformation, followed by a model-order reduction, hence producing the so-called ROAPFC. The final controller proposed takes a very simple analogue form:

$$G_{ROAPFC}(s) = \frac{0.174}{s} \frac{\left(s^2 + 1050s + 5540000\right)}{s + 4310} \tag{6}$$

In the following sections, we use the controllers (3), (6), and their hybrid combination (APP) as a reference point and propose an MPC reference governor scheme on top of the Type III controller capable of producing better results throughout the whole operating envelope, at the expense of increased complexity requiring a digital microprocessor implementation.

4. MPC Reference Governor Design for a Voltage-Mode-Controlled Converter

The development of an optimal and efficient reference governor using linear MPC ideas is commonly performed in a linear discrete-time state-space formulation. Hence, both the system and Type III controller dynamics have to be modeled in an appropriate linear discrete-time state-space form. To this end, a similar procedure to the one in [1] was followed.

4.1. Converter State-Space Modeling

An accurate state-space model of the boost circuit of Figure 1 can be found by following the common practice of defining the inductor's current $x_1 = I_L$ and the capacitor's voltage $x_2 = V_0$ as state variables. The model takes the following bilinear form (the tiny resistance r_C is ignored for simplicity):

$$\dot{x} = Ax + Bu + F_1 x_1 u + F_2 x_2 u + B_v, \quad y = Cx, \quad x = [I_L \ V_0]^T \in \mathbb{R}^{2 \times 1}$$

$$A = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}, \quad B = 0, \quad C = [0 \ 1]^T, \quad F_1 = \left[0 \ -\frac{1}{C}\right]^T, \tag{7}$$

$$F_2 = [1/L \ 0]^T, \quad B_v = [V_{IN}/L \ 0]^T$$

The next step is to linearize the dynamics about the equilibrium point using small signal variations reflecting nominal operating conditions $\tilde{x} = x - x_e, \tilde{u} = u - u_e, \tilde{y} = y - y_e$ to obtain new matrices:

$$\dot{\tilde{x}} = A_{lin}\,\tilde{x} + B_{lin}\tilde{u}, \quad y = C_{lin}\,\tilde{x} + D_{lin}\tilde{u}$$

$$A_{lin} = \begin{bmatrix} -r_L/L & -(1-u_e)/L \\ (1-u_e)/C & -1/(RC) \end{bmatrix}, \quad B_{lin} = [x_{2e}/L - x_{1e}/C]^T, \quad C_{lin} = [0\ 1]^T, \quad D_{lin} = 0$$

$$x_e = [x_{1e}\ x_{2e}]^T, \quad x_{1e} = \frac{V_{IN}}{r_L + R\,(1-u_e)^2},$$

$$x_{2e} = (R\,V_{IN}\,(1-u_e))/\left(r_L + R\,(1-u_e)^2\right)$$

(8)

These linear continuous-time dynamic equations may be further discretized for a fixed sampling period T to obtain the following discrete-time model in the new state variables $x_d \in \mathbb{R}^{2\times1}$:

$$x_d(k+1) = A_d\,x_d(k) + B_d\,u_d(k), \quad y_d(k) = C_d\,x_d(k)$$

$$A_d = e^{A_{lin}\,T}, \quad B_d = \int_0^T e^{A_{lin}\,\tau}\,d\tau, \quad C_d = C$$

(9)

4.2. PID Controller State-Space Form

A reliable discretization method for small sampling periods is the approximate backward difference (It is well known that, for a sufficiently high sampling frequency, all approximation methods are safe and guarantee satisfactory performance. However, the backward difference method is the simplest possible representation and hence advantageous for subsequent modeling and control design.) method, for which it is well known that the Laplace-transform variable s and the Z-transform z are related by $= \frac{z-1}{Tz}$ as the time derivative of a time variable $x(t)$ is approximated by $\dot{x}(t) = \frac{x(k)-x(k-1)}{T}$. Direct substitution of s in the Type III controller transfer function $G_{PID}(s)$ as in (3) leads to the following discrete-time transfer function $G_{PID}(z)$:

$$G_{PID}(s) = \frac{k_{PID}}{s}\frac{\left(1+\frac{s}{\omega_{ZC}}\right)^2}{\left(1+\frac{s}{\omega_{PC}}\right)^2} \underset{s=\frac{z-1}{Tz}}{\Rightarrow} G_{PID}(z) = K_0\frac{z\,(z-z_1)^2}{(z-1)(z-z_2)^2}$$

$$K_0 = k_{PID}\,T\,\frac{(1+\alpha)^2}{(1+\beta)^2}, \quad z_1 = \frac{\alpha}{1+\alpha}, \quad z_2 = \frac{\beta}{1+\beta}, \quad a = \frac{1}{T\omega_{ZC}}, \quad \beta = \frac{1}{T\omega_{PC}}$$

(10)

Subsequently, a state-space formulation is obtained by partial fraction expansion of $G_{PID}(z)$ as

$$G_{PID}(z) = K_0\frac{z\,(z-z_1)^2}{(z-1)(z-z_2)^2} = K_0 + \frac{K_1}{z-1} + \frac{K_2}{z-z_2} + \frac{K_3}{(z-z_2)^2}$$

$$K_1 = K_0\frac{(z_1-1)^2}{(z_2-1)^2}, \quad K_2 = K_0\frac{2z_2^3-(3+2z_1)z_2^2+4z_1z_2-z_1^2}{(z_2-1)^2}, \quad K_3 = K_0\frac{z_2^2z_2-2z_1z_2^2+z_2^3}{z_2-1}$$

(11)

Further introduction of a new controller state variable vector $x_c = [x_{c1}, x_{c2}, x_{c3}]^T \in \mathbb{R}^{3\times1}$ as

$$X_{c1}(z) = \frac{K_1}{z-1}, \quad X_{c2}(z) = \frac{K_2}{z-z_2}, \quad X_{c3}(z) = \frac{K_3}{(z-z_2)^2}$$

(12)

This leads, after some trivial calculations, to a simple state-space formulation in discrete-time:

$$x_c(k+1) = A_c\,x_c(k) + B_c\,u_c(k), \quad y_c(k) = C_c\,x_c(k) + D_c\,x_c(k)$$

$$A_c = \begin{bmatrix} 1 & 0 & 0 \\ 0 & z_2 & 0 \\ 0 & 1 & z_2 \end{bmatrix}, \quad B_c = \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix}, \quad C_c = [K_1, K_2, K_3]^T, \quad D_c = K_0$$

(13)

4.3. Reference Governor MPC Design and Tuning

For an MPC reference governor design on top of an already controlled plant, a discrete-time state-space model of the combined converter–controller closed-loop system is required. This may be found by noting that the output of the controller is the input to the converter, i.e., $y_c(k) = u_d(k)$, and that the input of the controller $u_c(k)$ is the error $e(k) = r(k) - y(k)$; hence, an augmented system-controller closed-loop discrete-time state-space formulation may be formed with a new extended state vector $x_a = [x_c \ x_d]^T \in \mathbb{R}^{5\times1}$ and corresponding matrices from (9), (13) as follows:

$$x_a(k+1) = A_a \, x_a(k) + B_a \, r(k), \quad y_a(k) = C_a \, x_a(k)$$

$$A_a = \begin{bmatrix} A_c & -B_cC_d \\ B_dC_c & A_d - B_dD_cC_d \end{bmatrix} \in \mathbb{R}^{5\times5}, \quad B_a = \begin{bmatrix} B_c \\ B_dD_c \end{bmatrix} \in \mathbb{R}^{5\times1}, \quad C_a = [0 \ C_d]^T \in \mathbb{R}^{1\times5} \qquad (14)$$

It is important to note that, in this formulation, the input coincides with the reference signal $r(k)$, while the output $y_a(k)$ coincides with the real output of the system, i.e., the output voltage V_0. The role of the reference governor is explained pictorially in Figure 3. It is a secondary controller responsible for producing a dynamically modified optimal reference signal $r(k)$ from a desired set-point signal $r_d(k)$, which is usually constant or at least slowly time-varying. The MPC reference governor is using the measured (sampled) output $y(k)$ to extract knowledge of the full state vector $x_a(k)$. There are five state variables, which are all known except the inductor current for which a specialized observer is included, as explained below in Section 4.4. The MPC scheme operates by resorting at the linear closed-loop model in (14) to predict future trajectories and generate optimal decisions for $r(k)$. This scheme can be combined either with an analogue Type III compensation circuit (Figure 2) or with a purely digital implementation, as implied by Figure 3.
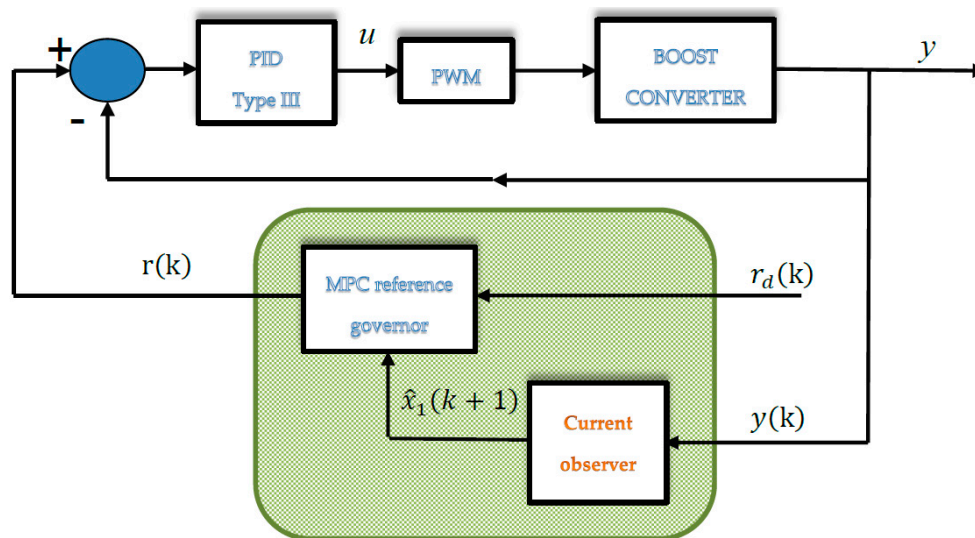

Figure 3. Model predictive control (MPC) voltage-mode reference governor scheme.

One of the simplest possible and computationally tractable ideas for an MPC formulation was adopted in this work, along the same lines with relevant design in [1], which proved surprisingly effective as the simulations results reveal in the next sections. An unconstrained formulation was used, which allowed the derivation of an explicit form of the corresponding MPC control law, hence avoiding the computationally demanding on-line optimization procedures. The gains of the controller were fixed and a priori determined, and this resulted in a computationally tractable implementation, especially because it is a single-input and single-output (SISO) system with low control and prediction horizon demands. Simple constraints regarding the size or the rate of change of the controller's signal

can also be dealt with easily with the same explicit MPC formula and without compromising the optimality, as explained in the sequel.

The first observation is that our MPC reference governor controller must be equipped with an extra integrator because the controller's decisions for $r(k)$ must converge to the desired values $r_d(k)$. The simple formulation in ([24], Chapter 1) was adopted, where an embedded integrator augmented state-space model was used for control design and optimization.

The first step was to take a difference operation on both sides of (14) to obtain the following:

$$\Delta x_a(k+1) = A_a \, \Delta x_a(k) + B_a \, \Delta r(k) \tag{15}$$

where the differences of the control variables and the input need to be defined as follows:

$$\Delta x_a(k+1) = x_a(k+1) - x_a(k), \; \Delta r(k+1) = r(k+1) - r(k) \tag{16}$$

A new extended state vector $x(k) \in \mathbb{R}^{6 \times 1}$ was formed next with an embedded integrator:

$$x(k) = \left[\Delta x_\alpha(k)^T \; y(k) \right]^T \tag{17}$$

Combining (16) and (17) yielded a new state-space model of an increase by one order given by the following equation:

$$x(k+1) = A \, x(k) + B \, \Delta r(k), \quad y(k) = C \, x(k)$$
$$A = \begin{bmatrix} A_a & 0_5^T \\ C_a A_a & 1 \end{bmatrix} \in \mathbb{R}^{6 \times 6}, \; B = \begin{bmatrix} B_a \\ C_a B_a \end{bmatrix} \in \mathbb{R}^{6 \times 1}, \; C = [0_5 \; 1]^T \in \mathbb{R}^{1 \times 6}, \; 0_5 = [0, 0, 0, 0, 0] \tag{18}$$

Note that the input to the new state-space model (A, B, C) is now $\Delta r(k)$. Assuming that, at the sampling instant $k_i > 0$, the state variable vector $x(k_i)$ is available and the control horizon is N_c, the future control trajectory is given by the sequence $\Delta r(k_i), \; \Delta r(k_i + 1), \cdots, \Delta r(k_i + N_c - 1)$. Moreover, for a prediction horizon (optimization window) N_p, the future state variables are specified as $x(k_i + 1), \; x(k_i + 2), \cdots, x(k_i + N_p)$. The model equation in (18) can be sequentially applied to yield the future state and output variables as a function of the future control parameters (for a detailed exposition see [24]). By defining the vectors

$$\Delta R = [\Delta r(k_i), \; \Delta r(k_i + 1), \cdots, \Delta r(k_i + N_c - 1)]^T,$$
$$Y = [y(k_i + 1), \; y(k_i + 2), \cdots, y(k_i + N_p)]^T \tag{19}$$

which have dimensions N_c, N_p in the SISO case, respectively, all prediction equations can be collected in a compact matrix form as follows:

$$Y = F \, x(k_i) + \Phi \, \Delta R$$
$$F = \left[CA, \, CA^2, CA^3, \cdots, CA^{N_p} \right]^T,$$
$$\Phi = \begin{bmatrix} CB & B & 0 & \cdots & 0 \\ CAB & CB & 0 & \cdots & 0 \\ CA^2B & CAB & CB & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ CA^{N_p-1}B & CA^{N_p-2}B & CA^{N_p-3}B & \cdots & CA^{N_p-N_c}B \end{bmatrix} \tag{20}$$

Assuming that the setpoint signal $r_d(k_i)$ at sample time k_i is constant in the optimization window, the data vector containing the setpoint data is $R_d^T = \overbrace{[1\ 1\ \cdots 1]}^{N_p} r_d(k_i) = \overline{R}_d r_d(k_i)$, and the cost function J to be minimized is the sum of two terms:

$$J = (R_d - Y)^T (R_d - Y) + \Delta R^T \overline{R} \Delta R \tag{21}$$

where the first term is related to the tracking errors and the second to the size of ΔR, while the weighting matrix $\overline{R} = r_w I_{N_c \times N_c}$ is a diagonal matrix, with $r_w \geq 0$ the main tuning parameter affecting closed-loop performance. By zeroing the first derivative of J, the unconstained optimal solution for the control problem is given as follows (assuming that $\Phi^T \Phi + \overline{R}$ is invertible):

$$\Delta R = \left(\Phi^T \Phi + \overline{R}\right)^{-1} \Phi^T \left(\overline{R}_d r_d(k_i) - F\, x(k_i)\right) \tag{22}$$

Due to the receding horizon principle, only the first element Δr of ΔR at time k_i is applied:

$$\Delta r(k_i) = K_r \cdot r_d(k_i) - K_x \cdot x(k_i) \tag{23}$$

where K_r is the first element of $\left(\Phi^T \Phi + \overline{R}\right)^{-1} \Phi^T \overline{R}_d$, and K_x is the first row of $\left(\Phi^T \Phi + \overline{R}\right)^{-1} \Phi^T F$. Hence, the optimal MPC reference governor takes an explicit static state-feedback form, where the gains of the controller are fixed and can be a priori determined. This is important for a computationally tractable implementation. Moreover, as we have a SISO system, simple constraints regarding the size of $r(k_i)$ and/or the rate of change $\Delta r(k_i)$ of the reference signal can also be dealt with easily with the same explicit MPC formula and without compromising the optimality. This is explained in ([24], Chapter 3). When constraints are violated, the only action needed is to clamp the imposed $r(k_i)$ at the limit and notify the observer accordingly. These simple constraints are of the following form:

$$\Delta r_{min} \leq \Delta r(k_i) \leq \Delta r_{max}, \ r_{min} \leq r(k_i) \leq r_{max} \tag{24}$$

4.4. Nonlinear Current Observer

The implementation of the MPC scheme introduced in the previous section requires knowledge of all five state variables in $x_a = [x_c\ x_d]^T \in \mathbb{R}^{5 \times 1}$, which include the inductor current $x_1 = I_L$. To avoid the addition of an extra current sensor, an efficient current observer can be a good alternative. In [1], a general linear observer (Kalman filter) was employed. In this work, a recently proposed robust and efficient nonlinear current observer [25] was selected with very good results due to its specialized nonlinear structure as well as the high sampling frequency used. A brief description of this structure is given below; for more details, please refer to [25].

With reference to the bilinear formulation of the converter dynamics as in (7), the observer formula proposed in [25] for the estimated state vector $\hat{x} = [\hat{x}_1\ \hat{x}_2]^T \in \mathbb{R}^{2 \times 1}$ based on the output estimation error $\widetilde{x}_2 = \hat{x}_2 - x_2$ (recall that $x_2 = V_0$ is the output voltage directly measured) is given by the following continuous-time equations:

$$\dot{\hat{x}} = A\,\hat{x} + F_1 \hat{x}_1 u + F_2 \hat{x}_2\, u + B_v + W(x_2, \widetilde{x}_2)$$
$$W(x_2, \widetilde{x}_2) = \begin{bmatrix} 0 \\ -K\widetilde{x}_2 + \eta(x_2, \widetilde{x}_2) \end{bmatrix}, \ \eta(x_2, \widetilde{x}_2) \equiv C^{-1} sgn(\widetilde{x}_2)(\rho\,|x_2| + a) \tag{25}$$

In this formula, the value of the parameter ρ is determined by the a priori assumed perturbation bounds of the unknown load R. The tuning parameters are K, a. After some experimentation with the tuning suggestions in [25], appropriate values $K = 1$, $a = 10^{-4}$ were found for $\rho = -0.1$ (corresponding to load resistance R in the designated range 10–50 Ω).

The observer was tested numerically in a discrete-time formulation using the backward difference method for approximating the derivatives in (25). The difference update equations used take a straightforward form that can be directly coded to a microprocessor in the following form:

$$\hat{x}_1(k+1) = \hat{x}_1(k) + T\cdot\left[-r_L L^{-1}\hat{x}_1(k) - L^{-1}\hat{x}_2(k) + L^{-1}\hat{x}_2(k)u(k) + V_{IN}L^{-1}\right]$$
$$\hat{x}_2(k+1) = \hat{x}_2(k) + T\cdot\left[C^{-1}\hat{x}_1(k) - R^{-1}C^{-1}\hat{x}_2(k) - C^{-1}\hat{x}_1(k)u(k) - K\tilde{x}_2(k) + \eta(k)\right] \qquad (26)$$
$$\eta(k) = C^{-1}sgn(\tilde{x}_2(k))(\rho\,|x_2(k)| + a)$$

## 5. Numerical Simulation Results

In this section, the performance enhancement achieved with the proposed MPC reference governor is presented with the help of Figures 4–8. A detailed comparison with the two controllers used in [22] was made, where the distinctive features of all schemes were revealed. The simulations were performed in two environments: in Simulink with the help of the PowerSim library, which uses the exact switching model, and in MATLAB with the nonlinear averaging model in discrete-time with sampling frequency equal to the switching frequency $f_s = 200$ kHz. For such a high sampling frequency, the results obtained by both methods are very close to each other; however, the advantage of the second method is that it contains transparent code (close to microprocessor level) that runs significantly faster and also produces clearer diagrams for comparison purposes. Hence, a decision was made to present these results in the following figures.
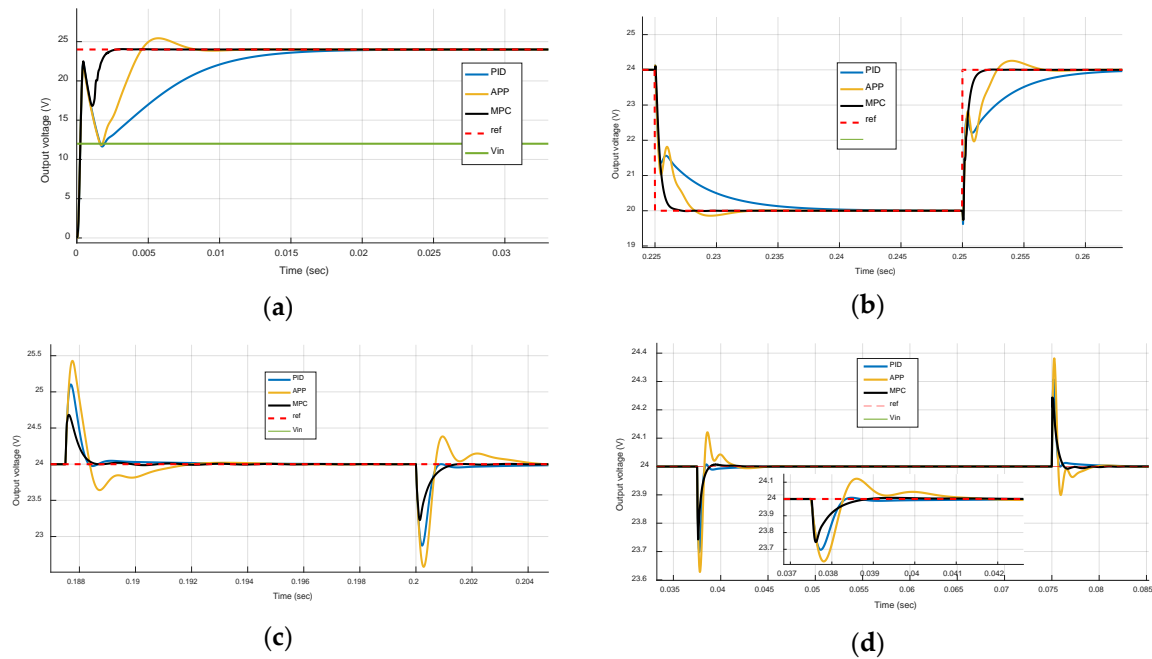

Figure 4. Comparative transient responses of the three controllers PID, APP (PID + ROAPC), and MPC. (**a**) Startup transient response for tracking a reference input of 24 V with an input voltage Vin = 12 V; (**b**) reference input changes from 24 V to 20 V and back; (**c**) rejection of load step changes (from 10 to 50 Ω and back); (**d**) dealing with step changes in the input voltage (from 12 to 10 V and back).

It is noted that a lower sampling frequency is enough for a successful reference governor scheme. A frequency of 100 kHz, i.e., equal to half of the main controller sampling frequency, was used for the MPC scheme when obtaining the results shown below. The specifications of the MPC reference governor scheme are given in Table 2. While experimenting with different values for the control and prediction horizons, we realized that we could afford to reduce the control horizon N_c to unity as long as the prediction horizon was long enough to deal with the nonminimum phase characteristic of the

transient responses of the boost converter. The values $N_c = 1$, $N_p = 45$ were found suitable in order to obtain very satisfactory results.
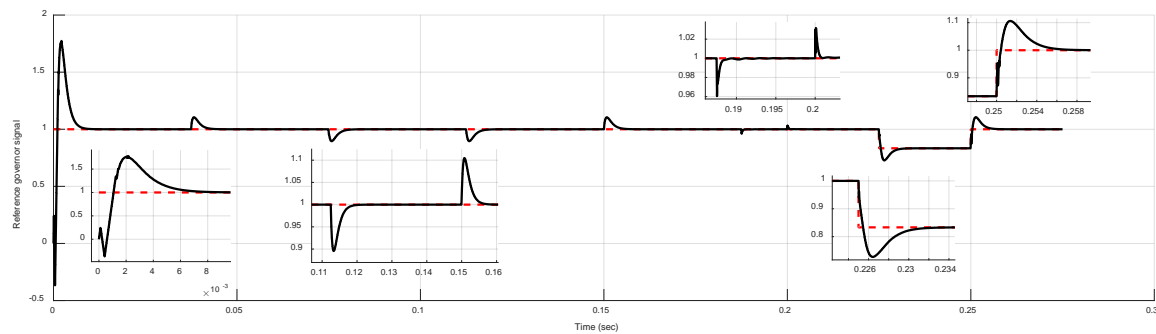

Figure 5. Reference governor signal (normalized to 1) corresponding to the cases in Figure 1. Zoomed pictures of the waveforms are given above or below, where appropriate, to improve visibility.
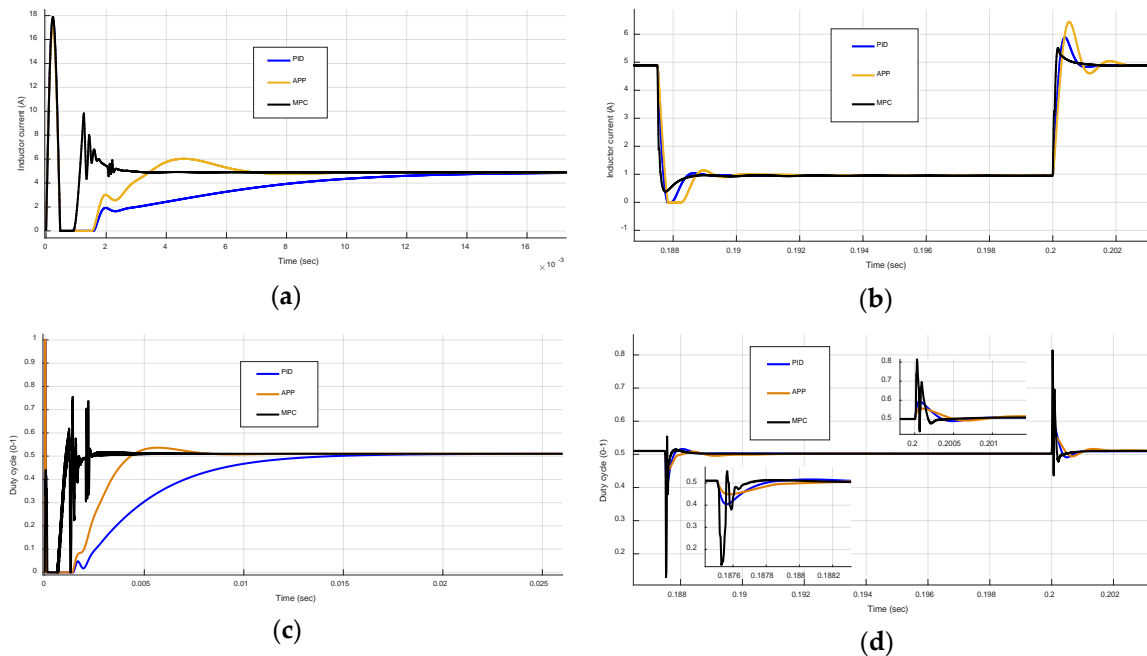

Figure 6. Inductor current and control signal (duty cycle) corresponding to cases Figure 1a,b. (**a**) Inductor current in the startup; (**b**) inductor current for reference input changes; (**c**) control signal in the startup; (**d**) control signal for reference input changes. Zoomed pictures of the waveforms are given above or below, where appropriate, to improve visibility.

Figure 4 compares the performance of the three controllers in four different cases covering the most important situations, i.e., startup transient, reference input changes, load perturbations, and line voltage changes. The notation used is as follows: the MPC reference governor scheme on top of the Type III controller is denoted as MPC, the combination of ROAPFPC with the Type III is called APP (ARMarkov Plus PID), while the Type III controller alone is termed as PID.

It is clear from Figure 4a,b that APP was 3–4 times faster than PID when it came to reference tracking, and it is clear from Figure 4c,d that APP was slightly worse than PID as far as disturbance rejection (load or input voltage changes) was concerned. It is also evident that the proposed strategy in this work, i.e., MPC, outperformed both APP and PID in all four situations, as depicted in Figure 4, where it appeared to be at least two times faster in terms of rise time and three times faster in terms of settling time, approximately.
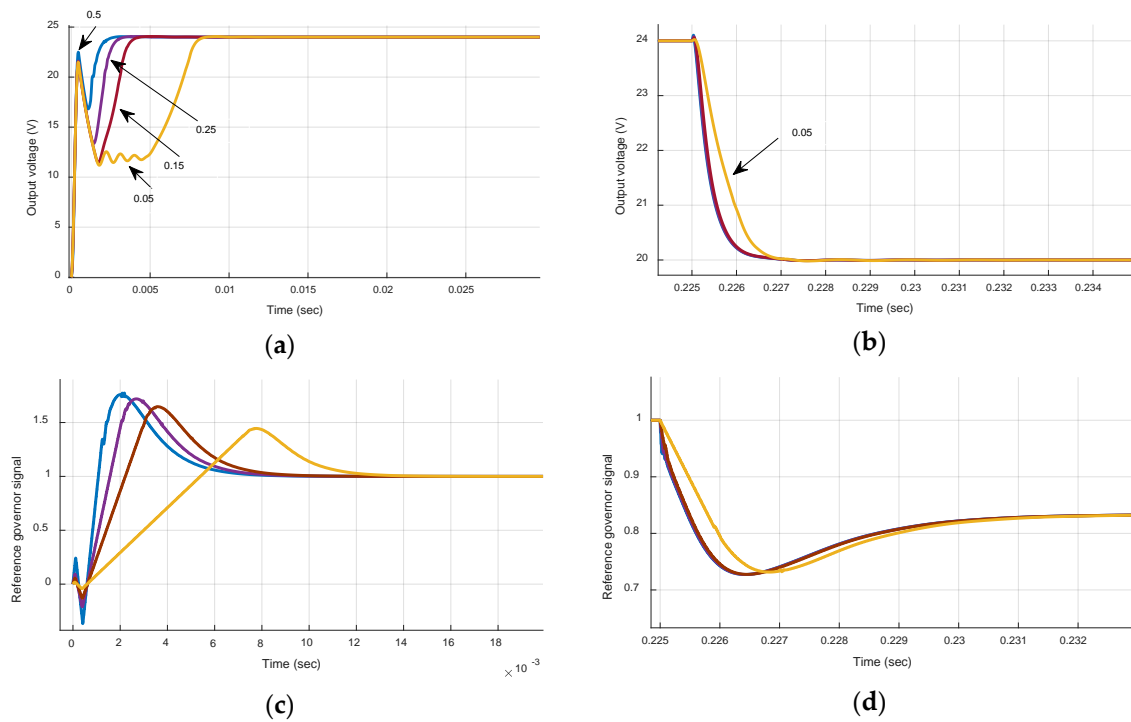
Figure 7. Effect of rate constraints (Δr_w = 0.05, 0.15, 0.25, 0.5) corresponding to cases Figure 1a,b. (**a**) Startup transient response for tracking a reference input of 24 V with an input voltage Vin = 12 V; (**b**) reference input changes from 24 V to 20 V; (**c**) reference governor signal of case (**a**); (**d**) reference governor signal of case (**b**).
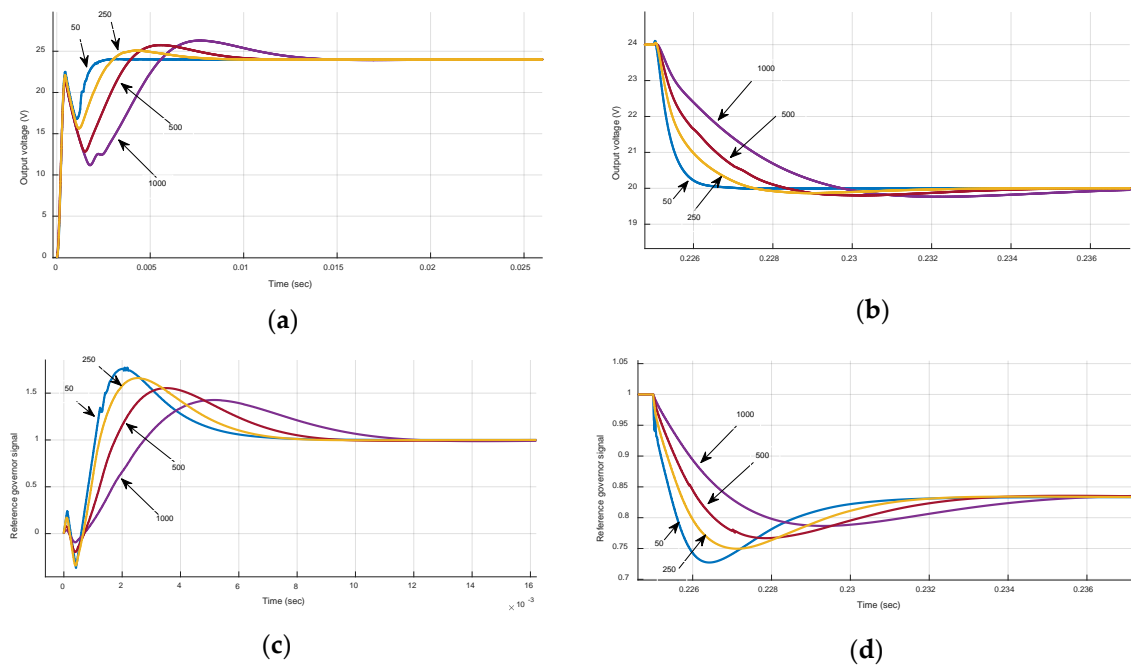
Figure 8. Effect of control weighting factor r_w (50, 250, 500, 1000) corresponding to cases Figure 1a,b. (**a**) Startup transient response for tracking a reference input of 24 V with an input voltage Vin = 12 V; (**b**) reference input changes from 24 V to 20 V; (**c**) reference governor signal of case (**a**); (**d**) reference governor signal of case (**b**).

Prediction Horizon N_p	Control Horizon N_c	Control Weight r_w	Rate Limits Δr_{max}	Main Control Frequency	MPC Control Frequency
45	1	50	0.5	200 kHz	100 kHz

The key to achieving this performance enhancement was the dynamic modification of the reference input by which the Type III controller was commanded. The command history corresponding to all four cases of Figure 4 is shown in Figure 5, where the values are normalized to unity for better illustration.

Further details of the three control laws for the first two cases (startup and reference changes) are given in Figure 6. The inductor current and duty cycle waveforms (i.e., the main control signals) reveal that the performance benefits obtained were not due to higher absolute values of currents or duty cycles or extensive use of energy but rather to a smarter use of the available energy, which was characterized by higher variability. The MPC controller appeared to act in a much more flexible manner, allowing large excursions of the control signals in a short time scale, without imposing extra operational requirements, e.g., higher inductor currents or energy consumption or excessive duty cycles. In fact, in MPC, the maximum current imposed did not increase, while the duty cycle never came close to saturation.

Further justification of this claim is provided by the simulation results depicted in Figure 7. Four different responses were obtained by imposing different rate constraints Δr_{max} = 0.05, 0.15, 0.25, 0.5, as in (24), which restrict the flexibility of the dynamically modified reference governor signals. Although there was little effect when considering perturbations around the nominal working point, it was obvious that, during the startup, they played a crucial role in the performance enhancement that may be achieved. Nevertheless, it was clear that in all cases the MPC controller inevitably did a good job, at least within the imposed constraints envelope.

Finally, a last test was performed to assess the proper MPC operation; a set of different weighting factor values r_w (50, 250, 500, 1000) were used, and the comparative results are shown in Figure 8. The controller behaved exactly as expected, i.e., larger r_w values gave rise to more sluggish responses, which also exhibited increased overshoot. The values r_w = 50, Δr_{max} = 0.5 were the ones selected for the nice results shown in Figures 4–6. The explicit MPC gains in (21) are given next:

$$K_r = 0.1737, \ K_x = \begin{bmatrix} 0.0001535 & -0.064 & -0.0847 & 1.2691 & 5.3893 & 0.1737 \end{bmatrix}^T \tag{27}$$

6. MPC Reference Governor Design for a Two-Loop Current-Mode-Controlled Converter

The developments in the previous sections considered a voltage mode control (VMC) structure, which consists of a single loop for output voltage regulation. This simplifies the control structure because the use of a current sensor is avoided, but it requires a more complicated controller (Type III). The alternative for simplifying the converter's dynamics and the controller form is to adopt the so-called current mode control (CMC) structure, which takes a two-loop cascaded form, resulting in an indirect linear control approach in the analog [26] or the digital domain [27]. The main advantage is that the current/voltage dynamics may be separated, and simple PI controllers for each loop may be designed using trivial pole placement procedures, which simplifies the control task while also ensuring faster transient response. The shortcoming is the need for a current sensor. The cascaded two-loop scheme used for analog design [26] is shown in Figure 9.
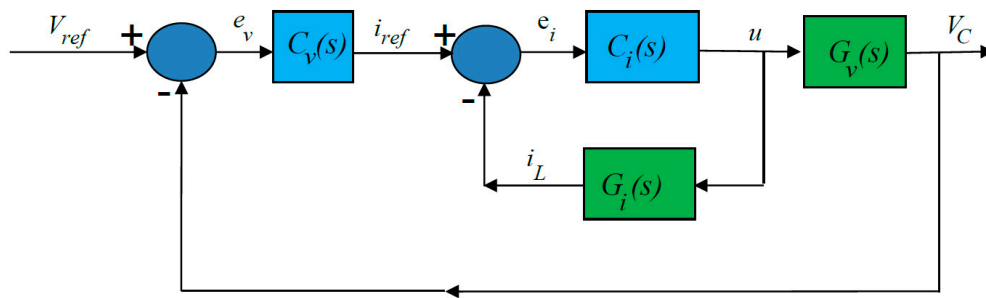
Figure 9. Two-loop cascade current-mode control structure.

An averaged current-mode structure is followed, which involves the design of two nested control loops with a current (inner loop) controller $C_i(s)$ and a voltage (outer loop) controller $C_v(s)$. The transfer functions $G_i(s) = \frac{I_L(s)}{U(s)}$, $G_v(s) = \frac{V_C(s)}{U(s)}$ are given based on the linearization of (8) as follows:

$$G_i(s) = \frac{u'_e x_{1e} + x_{2e}/R}{r_L/R + u'^2_e} \frac{Cx_{2e}/(u'_e x_{1e} + x_{2e}/R) \, s + 1}{\frac{LC}{r_L/R + u'^2_e} s^2 + \frac{L/R + r_L C}{r_L/R + u'^2_e} s + 1}$$

$$G_v(s) = \frac{u'_e x_{2e} - x_{1e} r_L}{r_L/R + u'^2_e} \frac{-L/(u'_e x_{2e}/x_{1e} - r_L) \, s + 1}{\frac{LC}{r_L/R + u'^2_e} s^2 + \frac{L/R + r_L C}{r_L/R + u'^2_e} s + 1} \tag{28}$$

where $u'_e = 1 - u_e$ and the presence of a right-half plane zero in $G_v(s)$ (which is not affected by the control law) dictates the design procedure. For dynamics separation between the two loops, the inner loop's bandwidth must not be placed near this zero; otherwise, the designed performance cannot be guaranteed. The desirable dynamic performance of the faster inner loop is imposed first by appropriate pole placement on the basis of certain bandwidth and damping features. The control design of the outer loop follows after closing the inner loop and designing the slower outer loop to be at least 5 times slower than the inner closed loop [26]. Trivial PI controllers are sufficient for both designs, where a simple root locus procedure can be used to establish the dominant pole's position.

6.1. Two-Loop PI Controller State-Space Form

Again, we adopt the backward different method for which a PI control law $C_{PI}(s) = K_p + K_i/s$ with gains K_p, K_i is approximated in dicrete-time by $C_{PI}(z) = \frac{(K_p + K_i T)z - K_p}{z - 1}$. This is a first-order equation admitting a simple state-space formulation. For the two PI control laws in Figure 9, by assuming gains K_{p1}, K_{i1} for the inner law $C_i(z)$, gains K_{p2}, K_{i2} for the outer law $C_v(z)$, and by defining corresponding state (integrator) variables x_i, x_v, and a controller state variable vector $x_c = [x_i, x_v]^T \in \mathbb{R}^{2 \times 1}$, new state equations are obtained:

$$\begin{aligned} x_i(k+1) &= x_i(k) + u_i(k), \quad y_i(k) = K_{I1} \, x_i(k) + K_{PI1} \, u_i(k) \\ x_v(k+1) &= x_v(k) + u_v(k), \quad y_v(k) = K_{I2} \, x_i(k) + K_{PI2} \, u_i(k) \end{aligned} \tag{29}$$

where the inputs u_i, u_v and the outputs y_i, y_v of the PI blocks in Figure 8 are specified as follows:

$$u_i = e_i = i_{ref} - i_L = i_{ref} - y_v \, , u_v = e_v = V_{ref} - V_C, y_i = u \, , y_v = i_{ref} \tag{30}$$

and the new gains are defined as $K_{I1} = K_{i1} \, T$, $K_{I2} = K_{i2} \, T$, $K_{PI1} = K_{p1} + K_{i1} \, T$, $K_{PI2} = K_{p2} + K_{i2} \, T$.

6.2. Current-Mode Reference Governor MPC Formulation

Similarly to Section 4.3, for an MPC reference governor an augmented system-controller closed-loop discrete-time state-space formulation is formed with a new extended state vector $x_a = [x_c \ x_d]^T \in \mathbb{R}^{4 \times 1}$ and corresponding matrices from (9) and (29) as follows:

$$x_a(k+1) = A_a \, x_a(k) + B_a \, r(k), \quad y_a(k) = C_a \, x_a(k)$$

$$A_a = \begin{bmatrix} -1 & -K_{PI2} & 1 & K_{I2} \\ 0 & -1 & 0 & 1 \\ A_{d1} - K_{PI1}B_d & A_{d2} - K_{PI}B_d & K_{I1}B_d & K_{PI1}K_{I2}B_d \end{bmatrix}, \, B_a = \begin{bmatrix} K_{PI2} \\ 1 \\ K_{PI} \, B_d \end{bmatrix}, \, C_a = [0 \ C_d]^T \qquad (31)$$

where $\boldsymbol{K_{PI}} = \boldsymbol{K_{PI1}} \, \boldsymbol{K_{PI2}}$ and $\boldsymbol{A_{d1}}$, $\boldsymbol{A_{d2}}$ are the two columns of A_d in (9). This result can be obtained after simple algebraic manipulations by noting that the controller/converter connection is established by the relations $\boldsymbol{u_v} = \boldsymbol{r} - \boldsymbol{x_d}$ (2), $\boldsymbol{y_i} = \boldsymbol{u}$. Compared to the voltage-mode-controlled system (14), it is noted that the current-mode-controlled one is lower order due to the simpler second-order controller (two PI controllers) as opposed to the third-order controller of the Type III scheme.

6.3. Numerical Simulation Results

Following the guidelines of the previous sections, two different current-mode designs were performed, with the specifications given in Table 3. The first design (PI 1) had smaller bandwidth (settling time T_s of 3 ms) and notably smaller gains compared to the second (PI 2). The transient responses of these two-loop PI current-mode designs with the APP (PID + ROAPC) design of Section 3 are compared in all possible situations in Figure 10.

Table 3. Two-loop PI current-mode control designs and specs.

Design	K_{p1}	K_{i1}	K_{p2}	K_{i2}	T_s (ms)	ζ
PI 1	0.025	126	0.84	922	3	0.7
PI 2	0.046	357	1.4	1448	1	0.7

(a)

(b)

(c)

(d)
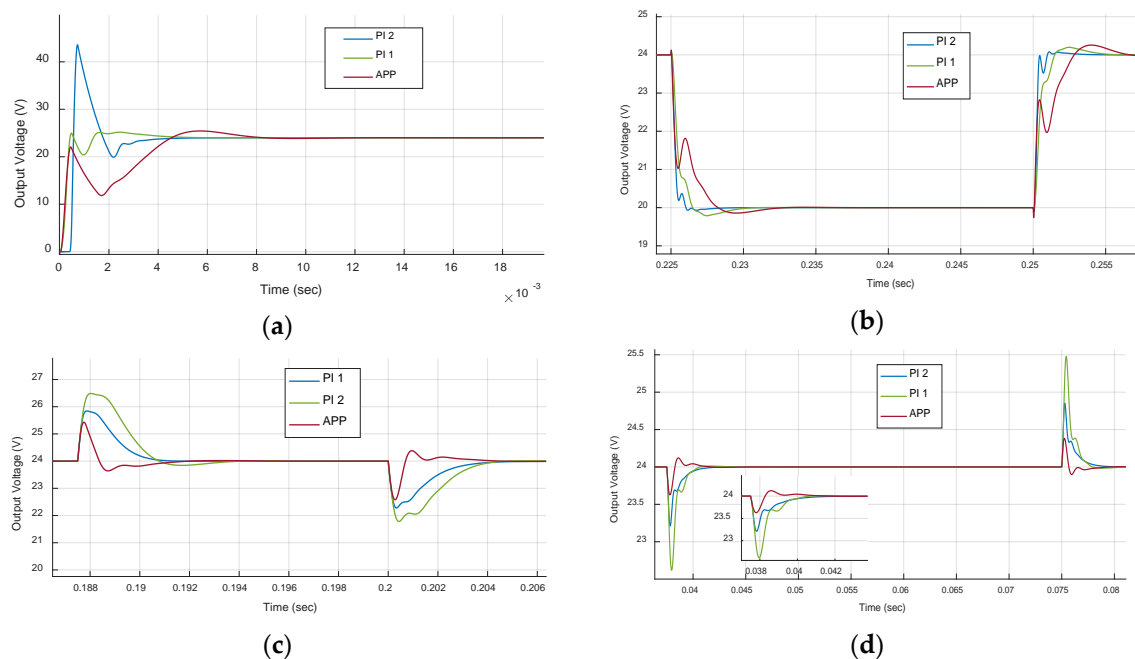
Figure 10. Comparative transient responses of the two PI designs of Table 3 with APP (PID + ROAPC). (**a**) Startup transient response for tracking a reference input of 24 V with an input voltage Vin = 12 V; (**b**) reference input changes from 24 V to 20 V and back; (**c**) rejection of load step changes (from 10 to 50 Ω and back); (**d**) dealing with step changes in the input voltage (from 12 to 10 V and back).

Figure 10a,b confirms the reference tracking of superior performance of the current-mode control, while Figure 10c,d shows its inferior disturbance rejection properties. This is expected as current-mode control exploits the faster current dynamics in the inner loop, while PID control offers better disturbance rejection. Using higher gains, as in PI 2, offers some improvements; however, it also results in a startup transient with unacceptably high overshoot, which requires some form of soft-start procedure. Can a reference governor scheme offer any remedies to these situations? This question is answered with the results shown in Figure 11 for the PI 2 design. The disturbance rejection was drastically improved, while the reference tracking problem in the startup was tackled. The MPC current-mode reference governor specifications for obtaining the results of Figure 11 are listed in Table 4.
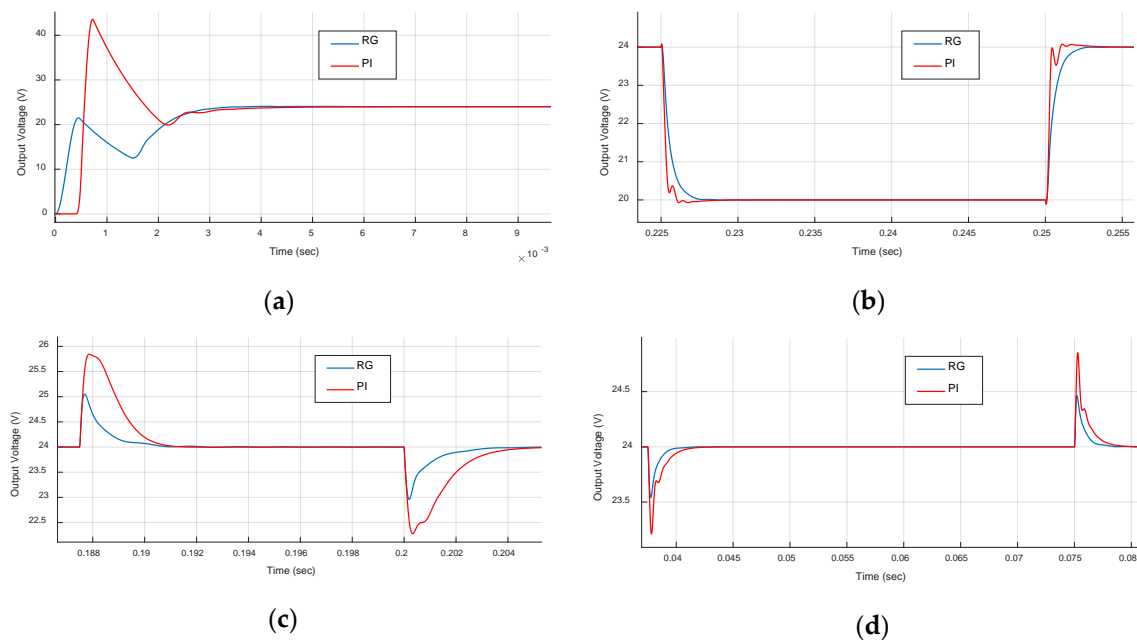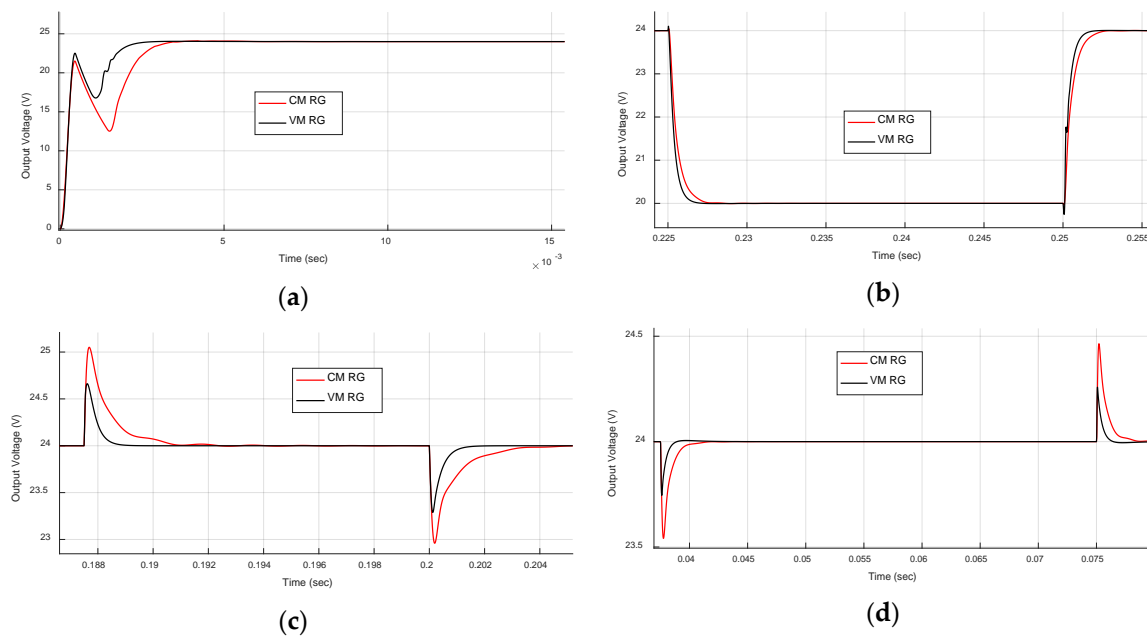

Figure 11. Comparative transient responses of PI 2 design of Table 3 with and without current-mode reference governor, with specs as in Table 4. (**a**) Startup transient response for tracking a reference input of 24 V with an input voltage Vin = 12 V; (**b**) reference input changes from 24 V to 20 V and back; (**c**) rejection of load step changes (from 10 to 50 Ω and back); (**d**) dealing with step changes in the input voltage (from 12 to 10 V and back).

Table 4. MPC current-mode reference governor specifications.

Prediction Horizon N_p	Control Horizon N_c	Control Weight r_w	Rate Limits Δr_{max}	Main Control Frequency	MPC Control Frequency
100	1	200	0.5	200 KHz	100 KHz

Finally, this MPC current-mode reference governor (CM RG) design was compared with the corresponding voltage-mode reference governor (VM RG) design of Section 5, in Figure 12. The two designs had comparable reference tracking capabilities, while VM RG had better disturbance rejection properties. This was attributed to the PID Type III controller around which the VM RG was designed and the important fact that the relatively inferior reference tracking properties of the PID Type III controller were cured using a VM RG. All in all, the merits of combining an optimal MPC RG scheme in voltage-mode with a typical PID Type III controller have become obvious. The best results in terms of reference tracking and disturbance rejection were obtained without the need to resort to a current-mode two-loop policy, which is also less efficient with disturbance rejection.

Figure 12. Comparative transient responses of voltage mode (VM RG) and current-mode reference governor (CM RG), with specs as in Tables 2 and 4. (**a**) Startup transient response for tracking a reference input of 24 V with an input voltage Vin = 12 V; (**b**) Reference input changes from 24 V to 20 V and back; (**c**) rejection of load step changes (from 10 to 50 Ω and back); (**d**) dealing with step changes in the input voltage (from 12 to 10 V and back).

7. Conclusions

This article presents one of the first attempts in the literature to apply reference governor ideas to the power electronics field for obtaining performance enhancements without replacing the main controller, which may be worth keeping for a cheap and/or safe modern implementation. Assuming that a digital microprocessor can be integrated into the existing control circuit, a secondary controller in the form of a reference governor that dynamically modifies the set-point of the primary controller may be a good idea, provided the implementation cost and complexity are kept low.

More specifically, this research considered the problem of enhancing the performance of boost DC–DC converters that are precompensated in voltage-mode or current-mode by a typical primary controller such as a Type III (or a double PI for current-mode), which is a standard industrial practice. A secondary controller–prefilter in the form of a reference governor was systematically designed, which operates by introducing dynamic adjustments to the imposed voltage reference input signal. It was shown that such a scheme, designed optimally via a simple linear MPC methodology, can enhance the performance in a wide operating range without imposing extra requirements or limitations. Clear improvements compared to recently reported results in the literature were found. It is noteworthy that even for such a highly nonlinear (bilinear) and nonminimum phase system like a boost converter, the shortcomings of a linear controller like PID, which is designed with a linear model for a particular operating point, can be dealt with by complementing it with a relatively simple linear unconstrained MPC scheme that takes a simple explicit form.

It is quite common to use current-mode two-loop controllers for nonminimum phase boost converters as they offer some advantages. Our simulation results revealed that the voltage-mode MPC RGs outperformed the current-mode designs, especially in disturbance rejection situations. Current-mode MPC RGs were also tested, which offered some improvements; however, voltage-mode MPC RGs combined with PID Type III primary controllers delivered the best results while also avoiding the use of a current sensor.

Of course, these advancements come at a price. The proposed controller is more complicated as it is expressed in a state-space form, and it requires extra knowledge of the inductor current and a digital microprocessor implementation. However, the computational demands of the proposed scheme are light enough and can be addressed with a modern cheap microprocessor. Moreover, placing an inductor current sensor is not necessary as reliable nonlinear observers for bilinear systems are available.

A light MPC algorithm with short horizons and trivial constraints, allowing an explicit solution through unconstrained optimization, was proven to be sufficient enough for our main purpose in the present work. These first positive results pave the way for further research with a reference governor flavor in the area of power electronics, e.g., in more complicated converter topologies or using more advanced techniques. Only few possibilities offered by MPC technology were explored in this research. There is a multitude of methods in the literature that are worth testing, including many more sophisticated constrained linear or nonlinear MPC schemes. The vast literature in MPC techniques, as well as the various optimal reference governor ideas developed thus far, imply that many other constrained optimization methodologies are available to be explored for future improvements.

Conflicts of Interest: The authors declare no conflict of interest.

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