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# A Method for the Simultaneous Suppression of DC Capacitor Fluctuations and Common-Mode Voltage in a Five-Level NPC/H Bridge Inverter

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**Abstract:** To suppress the direct current (DC) capacitor voltage fluctuations and the common-mode voltage (CMV) in a three-phase, five-level, neutral-point-clamped (NPC)/H-bridge inverter, this paper analyzes the influence of all voltage vectors on the neutral point potential of each phase under different pulse mappings in detail with an explanation of the CMV distribution. Then, based on the traditional space vector pulse width modulation (SVPWM) algorithm, a dual-pulse-mapping algorithm is proposed to suppress the DC capacitor fluctuations and the CMV simultaneously. In the algorithm, the reference voltage synthesis selects the voltage vector that has the smallest CMV value as the priority. In addition, the two kinds of pulse mappings that have opposite effects on the neutral point potential are switched to output. At the same time, regulating factors are introduced to adjust the working time of each voltage vector under the two pulse mappings; then, the capacitor voltages can be balanced. Both the simulation and experiment demonstrate the algorithm's effectiveness.

**Keywords:** NPC/H Bridge; five-level; Balance of capacitor voltage; Suppression of CMV; SVPWM

## 1. Introduction

In the past several decades, multilevel power topologies have increasingly been used in high-power, medium-voltage drives [1,2]. Due to the advantages of a higher voltage capability, lower switching frequencies, better power quality, and smaller voltage jumps ($dv/dt$), multilevel converters have become more popular and are applied to high-voltage variable frequencies, flexible alternating current (AC) transmissions, high-voltage direct current (HVDC), and so on [3]. Several strategies have been proposed for multilevel converters, such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination pulse width modulation (SHEPWM), and space vector pulse width modulation (SVPWM). Compared to SPWM, SVPWM has lower total harmonic distortion (THD) and a high utilization of direct current (DC)-side voltage [4]. SHEPWM is kind of offline strategy that requires excellent storage performance [5]. Moreover, various multilevel converter topologies have been studied, such as neutral-point-clamped (NPC) [6], cascaded H-Bridge (CHB) [7], modular multilevel converter (MMC) [8], and Matrix converter [9]. Among all of the topologies, the neutral-point-clamped and the cascaded H-Bridge are the two most widely used, and they are suitable for medium-voltage, high-power drives [10,11]. By combining the NPC and H-bridge topologies, a five-level NPC/H-bridge topology was proposed in 1990 [12] and since then has been applied in industrial drive applications. Figure 1 shows a schematic diagram of a three-phase, five-level NPC/H bridge inverter's main circuit with $RL$ (resistance and inductance) load. Each phase has an independent DC power $V_{dc}$, and the DC-side is connected by two capacitors in series. Under ideal conditions, the voltage of each is $V_{dc}/2$.

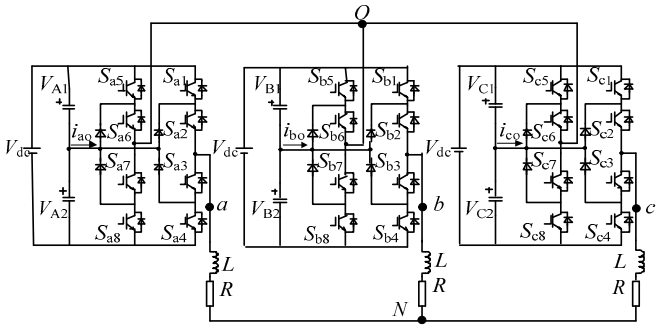



**Figure 1.** A diagram of a five-level, neutral-point-clamped (NPC)/H-bridge inverter's main circuit.

However, the NPC/H bridge topology has two crucial problems: an imbalance in capacitor voltages in three phases and a requirement that the common-mode voltage be suppressed. In fact, there are some reports about solving the imbalance in capacitor voltages of the NPC/H bridge topology. Most use two six-pulse rectifying devices to obtain two independent DC powers to supply each phase, which not only increases the complexity of the topology, but also increases the cost of the system circuit [13,14].

The best way to solve the problem is to utilize software balancing techniques because of the cost. In other five-level topologies, the object function optimization, zero sequence voltage injection, and virtual space-vector PWM methods are common techniques that mainly utilize the redundant vectors with a different combination of switching sequences [15,16]. In [15], for a five-level, diode-clamped converter (DCC), the duty cycles are calculated for the redundant states and adjusted between two zero vectors to control the capacitor voltages. This method is not suitable for the NPC/H bridge topology because the redundant states have the same influences on the neutral potential of capacitors. In [16], the authors propose to solve the capacitor voltage balancing issue of the five-level DCC based on a Model Predictive Control strategy. Although this strategy balances the capacitor voltages, it causes voltage jumps that could damage the switches.

In addition, the common-mode voltage in the NPC/H topology also deserves more attention. High common-mode voltage and its common-mode current will produce electromagnetic interference that will damage the motor. There are many methods to solve the problem. In [17], a five-level NPC/H inverter is considered to be equivalent to two three-level NPC inverters. One equivalent inverter always operates with zero common-mode voltage to suppress CMV, and the other one operates with the conventional three-level SVPWM. This measure can inhibit the CMV to $V_{dc}/3$. Another author proposes a strategy called hierarchical model predictive voltage control (HMPVC) [18], which can suppress CMV effectively.

In this paper, a dual-pulse-mapping algorithm is proposed for the simultaneous suppression of DC-side capacitor midpoint potentials and CMV in five-level NPC/H bridge inverter. In fact, the algorithm is suitable for NPC/H-Bridge converters with any number of voltage levels. In the analysis in Section 2, each voltage vector is found to correspond to a variety of pulse mappings, so the two pulse mappings (A) and (C), which have completely opposite effects on the midpoint potential of capacitors in each phase, are selected. In the proposed algorithm, the first step is to select the voltage vectors with the smallest CMV based on a line-voltage coordinate system. In order to ensure the output performance, the target of the algorithm is to suppress the CMV to $V_{dc}/6$. The second step is to synthesize the reference voltage based on space vector modulation (SVM) with six segments. The first three segments work under pulse mapping (A) and the other three segments work under pulse mapping (C). The key of the algorithm is to choose regulating factor for each vector. The value of the factor decides the working time of each vector that influences the charge or discharge of capacitors under the two pulse mappings. So, adjusting the regulating factor can balance the capacitor voltages effectively. The algorithm proposed in this paper can perfectly solve the two crucial problems of the

NPC/H bridge topology, which makes the NPC/H bridge topology play a better role in high-voltage and high-power applications.

## 2. Switching States of the Five-Level NPC/H Bridge Converter

In Figure 1, each phase has four pairs of complementary switches. They are ($S_{x1}$, $S_{x3}$), ($S_{x2}$, $S_{x4}$), ($S_{x5}$, $S_{x7}$), and ($S_{x6}$, $S_{x8}$), x = (a, b, c). Each phase has five switching states, such as $S_x$ = {2, 1, 0, −1, −2}, where every state has different pulse mappings, which are shown in Table 1.

**Table 1.** The switching states and pulse mappings.

| Switching State $S_x$ | Pulse Mapping Number | $S_{x1}$, $S_{x2}$, $S_{x3}$, $S_{x4}$, $S_{x5}$, $S_{x6}$, $S_{x7}$, $S_{x8}$ | Phase Voltage $u_{xo}$ |
|---|---|---|---|
| 2 | 1 | 11000011 | $V_{dc}$ |
| 1 | 2<br>3 | 11000110<br>01100011 | $V_{dc}/2$ |
| 0 | 4<br>5<br>6 | 11001100<br>01100110<br>00110011 | 0 |
| −1 | 7<br>8 | 01101100<br>00110110 | $-V_{dc}/2$ |
| −2 | 9 | 00111100 | $-V_{dc}$ |

Based on the main circuit diagram of the system shown in Figure 1 and the corresponding switching states in Table 1, the output voltage of each phase of the inverter is

$$\begin{cases} u_{ao} = V_{dc} * S_a/2 \\ u_{bo} = V_{dc} * S_b/2 \\ u_{co} = V_{dc} * S_c/2 \end{cases} \quad (1)$$

## 3. Analysis of the Midpoint Potential and CMV

### 3.1. Mechanism of DC-Side Capacitor Voltage Imbalance

We take the phase A of the five-level NPC/H Bridge inverter as an example to analyze the effect of nine pulse mappings on the midpoint potential.

Figure 2 shows the circuit of pulse mapping 1, where $S_{x1}$, $S_{x2}$, $S_{x7}$, $S_{x8}$ are equal to 1. The phase voltage is $V_{dc}$ and the midpoint potential has no change because the current of the load is not linked to the midpoint potential. Similar to pulse mapping 1, the circuits of pulse mapping 4, 5, 6, and 9 also have no influence on the midpoint potential.

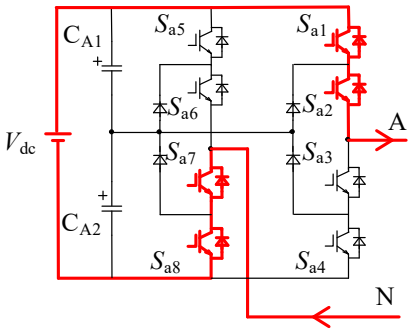



**Figure 2.** The circuit of pulse mapping 1.

Figure 3 shows the circuit of pulse mapping 2. Assuming that the direction of phase current $i_a$ is the same as in Figure 3, the current flows through $S_{a1}$, $S_{a2}$, $S_{a7}$, and $D_{a4}$ and then arrives at the midpoint

potential. Due to the effect of $i_a$, the midpoint potential increases and the voltage of capacitor $C_{A1}$ decreases. If the current direction is opposite to that shown in Figure 3, the current flows through $D_{a3}$, $S_{a6}$ and the freewheeling diodes of $S_{a2}$, $S_{a1}$, then arrives at the positive pole. At this time, the midpoint potential decreases and the voltage of capacitor $C_{A1}$ increases. In these two situations, the current has an opposite influence on the midpoint potential. Figure 4 shows the circuit of pulse mapping 3. If the current direction is same as the definition of Figure 4, the current flows through $D_{a1}$, $S_{a2}$'s freewheeling diode, $S_{a7}$ and $S_{a8}$, then arrives at the negative pole. The midpoint potential decreases and the voltage of capacitor $C_{A1}$ increases. If the current direction is opposite to the definition, the current flows through the freewheeling diodes of $S_{a8}$ and $S_{a7}$, $S_{a3}$, and $D_{a2}$. At this time, the midpoint potential increases and the voltage of capacitor $C_{A1}$ decreases. We can conclude that different directions of $i_a$ have different effects on the midpoint potential. The changes caused by pulse mapping 7 and 8 are same as those caused by pulse mapping 2 and 3. Table 2 shows the changes in midpoint potential when using pulse mapping 2, 3, 7, and 8 with opposite direction currents.

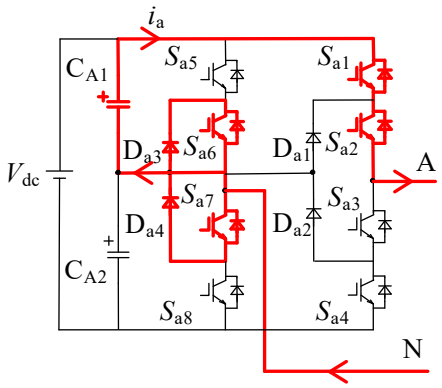



**Figure 3.** The circuit of pulse mapping 2.

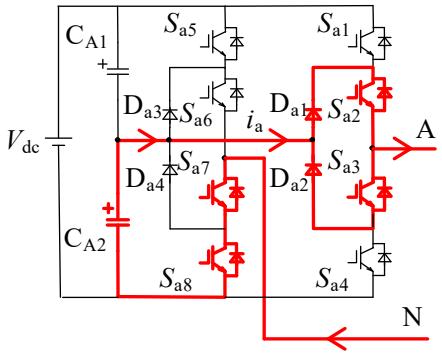



**Figure 4.** The circuit of pulse mapping 3.

**Table 2.** Changes in midpoint potential in pulse mapping 2, 3, 7, and 8 with different direction currents.

| Switching State $S_x$ | Pulse Mapping Number | $S_{x1}$, $S_{x2}$, $S_{x3}$, $S_{x4}$, $S_{x5}$, $S_{x6}$, $S_{x7}$, $S_{x8}$ | Direction of $i_a$ | Midpoint Potential |
|---|---|---|---|---|
| 1 | 2 | 11000110 | + ↑<br>− ↓ | |
| | 3 | 01100011 | + ↓<br>− ↑ | |
| −1 | 7 | 01101100 | + ↑<br>− ↓ | |
| | 8 | 00110110 | + ↓<br>− ↑ | |

As shown in Table 2, the changes caused by pulse mapping 2 are the total opposite of those caused by pulse mapping 3. This situation also exists between pulse mapping 7 and 8. So, we select pulse mapping 2 and 7, which have the same influence on the midpoint potential, to form pulse mapping (A), and pulse mapping 3 and 8 constitute pulse mapping (B), as listed in Table 3.

Based on the analysis of Tables 2 and 3, we know that pulse mapping (A) and (B) have a completely opposite effect on the midpoint potential whatever the direction of $i_a$ is. If the pulse mapping (A) and (B) are used properly, the midpoint potential can be balanced.

**Table 3.** The two pulse mappings of the five-level NPC/H-Bridge inverter.

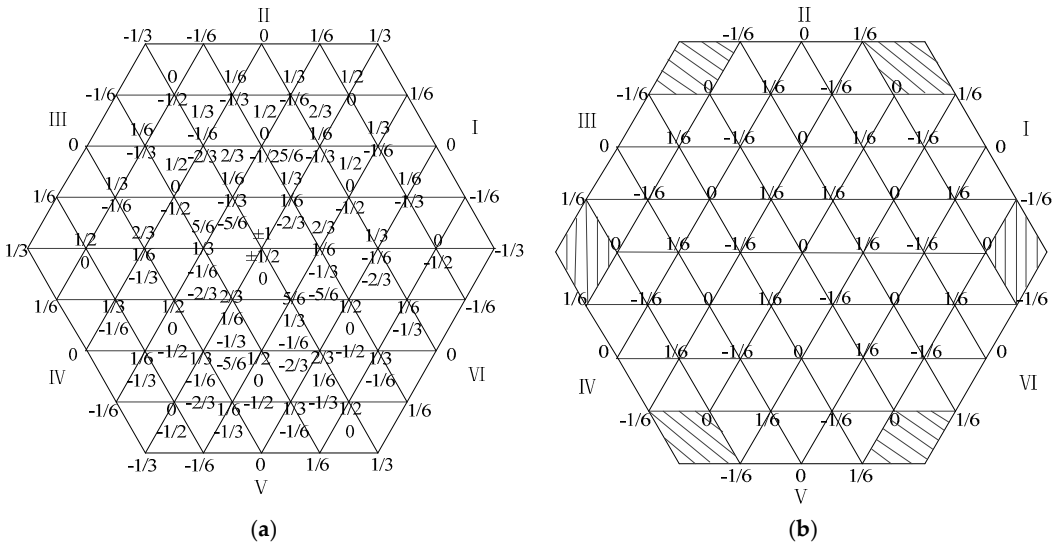
| State | (A) | (B) |
|---|---|---|
| 2 | 11000011 | 11000011 |
| 1 | 11000110 | 01100011 |
| 0 | 01100110 | 01100110 |
| −1 | 01101100 | 00110110 |
| −2 | 00111100 | 00111100 |

### 3.2. Distribution of CMV

In a five-level NPC/H bridge inverter, the common-mode voltage $U_{CMV}$ is expressed as Equation (2):

$$U_{CMV} = \frac{u_{ao} + u_{bo} + u_{co}}{3} \tag{2}$$

where $u_{ao}$, $u_{bo}$, and $u_{co}$ are the output voltage of each phase, which are obtained by Equation (1). Their values are: $\pm V_{dc}$, $\pm V_{dc}/2$, 0. So, all of the values of $U_{CMV}$ can be calculated as: $\pm V_{dc}$, $\pm 5V_{dc}/6$, $\pm 2V_{dc}/3$, $\pm V_{dc}/2$, $\pm V_{dc}/3$, $\pm V_{dc}/6$, and 0. The common-mode voltage distribution of the five-level NPC/H bridge inverter is shown in Figure 5 (where the $V_{dc}$ is omitted).




(**a**) (**b**)

**Figure 5.** The common-mode voltage distribution. (**a**) Common-mode-voltage distribution diagram of traditional strategy; and (**b**) Common-mode-voltage distribution diagram of proposed strategy.

Figure 5a shows the traditional common-mode voltage distribution of the five-level NPC/H bridge inverter. In order to suppress the common-mode voltage of the system while not affecting the output performance of the inverter, this paper retains the vector that has the smallest common-mode voltage among all the redundant vectors. Additionally, the six vertex vectors of the outer hexagon are eliminated. So, the common-mode voltage distribution in Figure 5a can be simplified as shown in Figure 5b.

When the reference voltage is located in the shaded quadrangle of Figure 5b, the closest three voltage vectors are utilized in the synthesis. Thus, the common-mode voltage of the five-level NPC/H bridge inverter is suppressed to $\pm V_{dc}/6$ and 0 while the output performance of the inverter is ensured.

## 4. The Proposed Dual-Pulse-Mapping Algorithm

In order to balance the DC-side capacitor voltages of a five-level NPC/H bridge inverter and suppress the CMV effectively at the same time, a dual-pulse-mapping algorithm is proposed. From the analysis above, we found that mapping (A) and (B) have the completely opposite influence on the DC-side capacitor voltages. When mapping (A) and (B) work, the influences of each vector on the three-phase midpoint potentials of capacitors are opposite. Thus, this paper selects mapping (A) and (B) to control the voltage alternately based on the six-segment SVPWM.

### *4.1. Vector Selection and Vector Duration Time*

In this paper, the vector selection and calculation are based on the line-voltage coordinate system [6]. Assuming the three-phase reference voltages are $U_a$, $U_b$, and $U_c$, the *a-b-c* coordinate is converted to the *ab-bc-ca* line-voltage coordinate and unitized as Equation (3). The components of the reference voltage $V_{ref}$ on the axis *ab*, *bc*, and *ca* are $U_{ab}$, $U_{bc}$, and $U_{ca}$, respectively.

$$\begin{bmatrix} U_{ab} \\ U_{bc} \\ U_{ca} \end{bmatrix} = \frac{2}{V_{dc}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} \tag{3}$$

The per unit values of components are rounded up and down to an integer. In the equation, "floor" means rounding down to an integer and "ceil" represents rounding up to an integer.

$$\begin{cases} F_{ab} = floor(U_{ab}),\ C_{ab} = ceil(U_{ab})\ ; \\ F_{bc} = floor(U_{bc}),\ C_{bc} = ceil(U_{bc})\ ; \\ F_{ca} = floor(U_{ca}),\ C_{ca} = ceil(U_{ca})\ ; \end{cases} \tag{4}$$

All of the triangles can be separated into regular and inverted ones. If $F_{ab} + F_{bc} + F_{ca} = -1$, the end of the reference voltage vector is located in the regular triangle, and the coordinates of the three triangle vertexes ($U_A$, $U_B$, and $U_C$) and the time duty ratio of three basic vectors are as follows.

$$\begin{cases} U_A = (C_{ab}, F_{bc}, C_{ca}),\ d_A = U_{ab} - F_{ab}\ ; \\ U_B = (F_{ab}, C_{bc}, F_{ca}),\ d_B = U_{bc} - F_{bc}\ ; \\ U_C = (F_{ab}, F_{bc}, C_{ca}),\ d_C = U_{ca} - F_{ca}\ ; \end{cases} \tag{5}$$

If $F_{ab} + F_{bc} + F_{ca} = -1$, the end of the reference voltage vector is located in the inverted triangle. The coordinates and the time duty ratio are as follows.

$$\begin{cases} U_A = (C_{ab}, F_{bc}, C_{ca}),\ d_A = C_{ab} - U_{ab}\ ; \\ U_B = (F_{ab}, C_{bc}, C_{ca}),\ d_B = C_{bc} - U_{bc}\ ; \\ U_C = (C_{ab}, C_{bc}, F_{ca}),\ d_C = C_{ca} - U_{ca}\ ; \end{cases} \tag{6}$$

After selecting the three basic vectors, it is essential to find all the switching states corresponding to each basic vector. ($S_a$, $S_b$, $S_c$) represents the switching states of basic vectors in the $\alpha - \beta$ coordinate

system. $U_X$ = (a, b, c) represents the coordinates of triangle-vertex vectors in the line-voltage coordinate system (where X = A, B, or C).

$$\begin{cases} S_a = S_a \\ S_b = S_a - a \\ S_c = S_a + c \\ 0 \le S_a, S_b, S_c \le 4 \end{cases} \tag{7}$$

Equations (5)–(7) can quickly determine the triangle-vertex vectors and their time duty ratios. The relationship between common-mode voltage and switching states is obtained by Equations (1) and (2) as the following:

$$U_{CMV} = \frac{S_a + S_b + S_c}{6} V_{dc} \tag{8}$$

The dual-pulse-mapping algorithm proposed in this paper utilizes Equation (8) to select the vectors that have the smallest CMV among redundant vectors.

### *4.2. Voltage Balancing Algorithm*

Based on the traditional SVPWM, this paper presents a new algorithm, called the dual-pulse-mapping algorithm, which is composed of six segments. The first three segments are controlled by pulse mapping (A), and the other segments are controlled by mapping (B). At the same time, the regulating factor $k$ is adopted for each vector. According to the midpoint potentials of the three phases, adjusting the working time of each vector under the two pulse mappings can balance the capacitor voltages effectively and stably. Taking sector I as example, the vectors with the smallest value of CMV are shown in Figure 6.

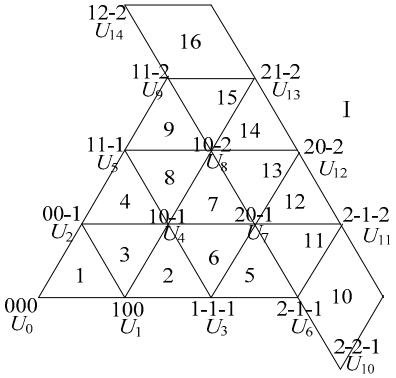



**Figure 6.** The vectors with the minimum common-mode voltage (CMV) in Sector I.

We take the 13th triangle in Figure 6 as an example to explain how the dual-pulse mapping works. Because the reference voltage is in the 13th triangle, the vector synthesizing sequence is showing as Figure 7.

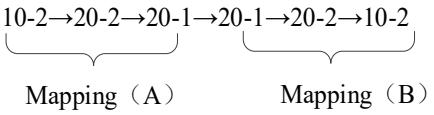



**Figure 7.** The vector synthesizing sequence of dual-pulse mapping strategy.

As shown in Tables 2 and 3, the pulse mappings (A) and (B) have the opposite effect on the midpoint potential. Based on this, the regulating factors $k_a$ and $k_c$ are adopted. Assuming that the working time of the three vectors are $T_1$, $T_2$, and $T_3$, the working time of the six segments is assigned as Figure 8.

$$\underbrace{\underset{10\text{-}2}{k_aT_1}\rightarrow\underset{20\text{-}2}{0.5T_2}\rightarrow\underset{20\text{-}1}{k_cT_3}}_{\text{Mapping（A）}}\rightarrow\underbrace{\underset{20\text{-}1}{(1\text{-}k_c)T_3}\rightarrow\underset{20\text{-}2}{0.5T_2}\rightarrow\underset{10\text{-}2}{(1\text{-}k_a)T_1}}_{\text{Mapping（B）}}$$

**Figure 8.** The assigned working time of sex segments.

If the midpoint potential of phase A is equal to $V_{dc}/2$, then $k_a$ is 0.5. If the midpoint potential of phase A is higher than $V_{dc}/2$, we only need to reduce the value of $k_a$ to <0.5, for example 0.4, in order to increase the working time of 10-2 under mapping (B) (because the time if the follow current's state is much smaller than the sampling time and a follow current also exists when using pulse mapping (B), so this state will not be taken into consideration). It is all the same when the midpoint potential of phase A is lower than $V_{dc}/2$. By adjusting the operating time of 10-2 under the two kinds of pulse mappings, the midpoint potential of phase *A* will be balanced.

## 5. Simulation Verification and Analysis

In order to show the performance of the proposed method, simulation studies were carried out in the MATLAB/Simulink software environment. The condition were set as follows: the DC-side voltage equals 1000 V, the rated DC-side capacitor voltages $V_{dc}$ equal 500 V, the DC capacitances are 3300 μF, the output voltage frequency $f$ is 50 Hz, the load power factor cos$\varphi$ is 0.985, and its impedance $Z$ equals 26.43.

### *5.1. Simulation Results of the Conventional SVPWM Strategy*

Figure 9a shows the three-phase midpoint potentials (which are defined as the difference values between the midpoint potentials of the unbalanced three-phase capacitors and the midpoint potentials of the balanced capacitors) when using the conventional SVPWM, which only adopts mapping (A). The DC-side voltage equals 1000 V, so the midpoint potentials of the balanced capacitors are 500 V. The midpoint potentials of the three-phase capacitors are continuously increased from 0 V to 500 V, which is consistent with the theoretical analysis. Figure 9b shows the line voltage between phase A and phase B; the nine-level line voltage attenuates to five-level as time goes by. When the modulation index $m$ has high values, the midpoint current of the inflow capacitor is large, and the voltage of the capacitor changes greatly. Therefore, the midpoint potential of the capacitor rises rapidly. On the contrary, when $m$ has low values, the midpoint potential of the capacitor rises slowly.

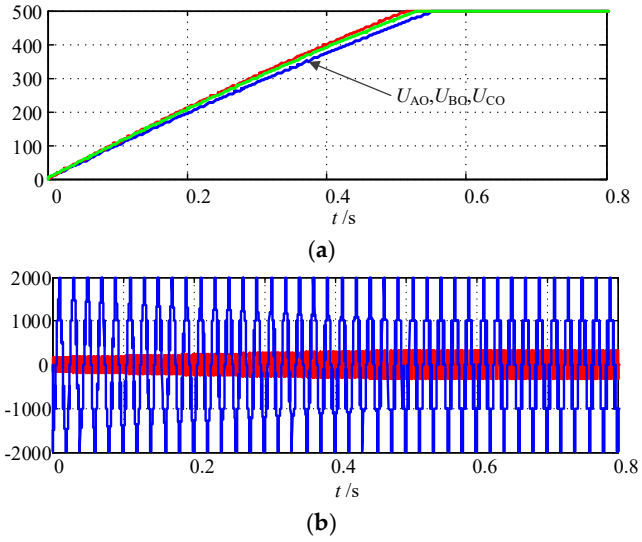
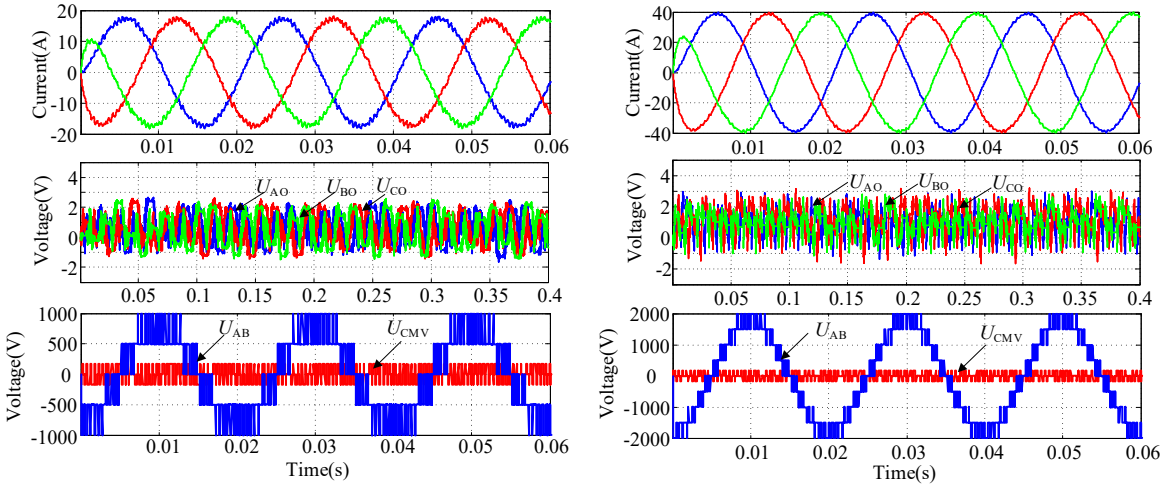



**Figure 9.** The inverter without capacitor voltage control. (**a**) Midpoint Potential of three phases; and (**b**) Line voltage and common mode voltage.

The line voltage between phase A and phase B is degraded to five-level from the original nine-level. The imbalanced DC-side voltages inject harmonics into the output voltage of the inverter, thereby distorting the output voltage waveform. If the inverter continues to work in an unbalanced capacitor voltage state, the power electronics in the system will be unevenly pressed or will even break down, and eventually the entire system will not work properly.

### *5.2. Simulation Results with the Proposed Dual-Pulse-Mapping Strategy*

The proposed dual-pulse-mapping strategy was also analyzed using simulations, and the simulation parameters were the same as those for the simulations of the conventional SVPWM. Figure 10 shows the three-phase current, the midpoint potentials of the three-phase DC-side capacitors, the line voltage between phase A and phase B, and the common-mode voltage under the modulation index of 0.4 and 0.9 when the power factor of the load equals 0.984.




(**a**) $m$ = 0.4, $PF$ = 0.984 (**b**) $m$ = 0.9, $PF$ = 0.984

**Figure 10.** The simulation waveforms under the algorithm. (**a**) The three-phase current, midpoint potentials, line voltage between phase A and phase B, and common-mode voltage when $m$ is 0.4; and (**b**) The three-phase current, midpoint potentials, line voltage between phase A and phase B, and common-mode voltage when $m$ is 0.9.

According to the Figure 10, under the modulation index of 0.4 and 0.9, the proposed dual-pulse-mapping strategy could control the operation of the inverter stably. The midpoint potentials of the three-phase DC-side capacitors fluctuate within ±3 V, which indicates that the proposed algorithm can effectively balance the midpoint potentials of DC-side capacitors. The largest ripple in the common voltage is $1/6V_{dc}$, which means that the common voltage has effectively been suppressed.

### *5.3. Simulation Results of Dynamic Performance*

We performed a simulation with the conventional strategy in which the modulation index was 0.9, the power factor was 0.984, and the pre-charged voltage of the DC-side capacitor was 500 V. When the midpoint potentials of the DC-side capacitors reached $V_{dc}/2$, the proposed dual-pulse-mapping strategy was used to balance the voltage. Figure 11 shows the simulation diagram of the midpoint potentials of the DC-side capacitors, the voltages of phase A's two capacitors, and the line voltage between phase A and phase B. Under the pulse mapping (A), the midpoint potentials of the three-phase capacitors rise rapidly from 0 V to 500 V and the two capacitor voltages of phase A also change from 500 V to 0 V and 1000 V, respectively. The line voltage between phase A and phase B degrades to five-level. Then, the dual-pulse-mapping algorithm was adopted. The midpoint potentials of three-phase capacitors return to a balanced state and the line voltage also returns to nine-level. The two

capacitor voltages of phase A change from 0 V and 100 V to 50 V. These simulation results show that the proposed algorithm has intelligent dynamic performance.

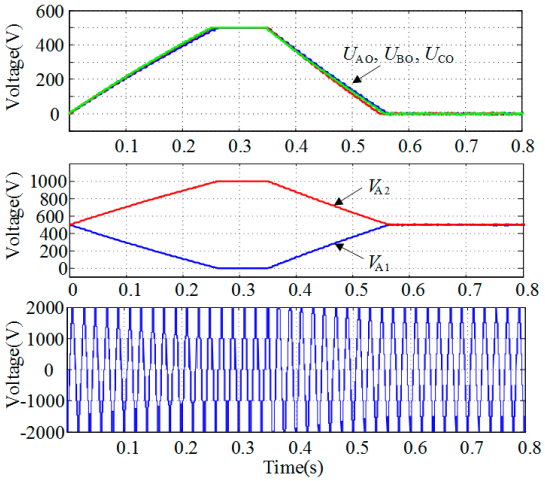



**Figure 11.** The simulation waveform of dynamic performance.

## 6. Experimental Results

In order to further verify the effectiveness of the proposed control algorithm for balancing DC-side (Direct Current) capacitor voltages and the suppression of the common-mode voltage and its dynamic response capability, a three-phase, five-level NPC/H Bridge inverter with an *RL* load experimental platform was built as shown in Figure 12. The structure is composed of a 12-pulse uncontrolled rectifier and a five-level NPC/H-bridge-type inverter. The basic parameters of the experiment are shown in Table 4.

**Table 4.** The experimental parameters of the system.

| Parameters | Values |
|---|---|
| DC-side voltage $V_{dc}$ | 100 V |
| Output voltage frequency $f_{AC}$ | 50 Hz |
| DC-side capacitance $C$ | 3300 μF |
| *RL* load | 26 Ω + 15 mH |
| Modulation index $m$ | 0.9 and 0.4 |
| Switching frequency $f_s$ | 800 Hz |

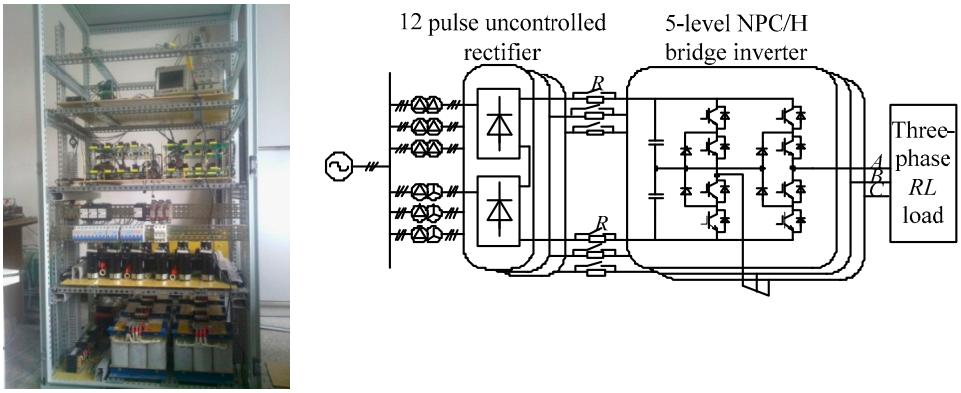



**Figure 12.** The experimental platform.

In Figure 13a,b, the DC-side capacitor voltages' fluctuations are very small regardless of whether the reference voltage locates in the high- or low-modulation index region, and the common-mode voltage of the system is suppressed at the $-V_{dc}/6$, 0, $V_{dc}/6$. This proves that the dual-pulse-mapping algorithm controls the stable operation of the three-phase, five-level NPC/H-bridge inverter. Figure 13c,d show the harmonic analysis of the line voltage. It can be seen that, when the modulation index $m$ is 0.9 and 0.4, the THD is 17.8% and 35.0%, respectively, which means that the output performance of the algorithm is the same as that of traditional SVPWM.

The pulse-width modulations (PWMs) of $S_{a1}$, $S_{a2}$, $S_{a3}$, and $S_{a4}$ in phase A are shown in Figure 14. The switching frequencies of the four switches in phase $A$ were calculated approximately during 250~350 Hz, with a modulation index $m$ of 0.4 and 0.9. The higher the modulation index is, the lower the switching frequency of each switch is. Phase $B$ and $C$ are both the same. Compared with the traditional SVPWM, the switching frequency of each switch just a little higher.

Figure 15a,b show the experimental waveforms of the dynamic response when the reference voltage modulation index suddenly decreases. The modulation index changes from $m$ = 0.9 to $m$ = 0.4. The line voltage and phase currents respond immediately during a very short time. The capacitor voltage is still balanced but has a little increase because of the uncontrolled rectifier.

In order to verify the strong self-balancing property of the algorithm, the conditions were set as follows: in the beginning, the modulation index was $m$ = 0.9, and the values of regulating factors were all 0.5, which means that the dual-pulse-mapping algorithm was equivalent to a common six-segment SVPWM. Under the mapping (A), the midpoint potentials $V_{AO}$, $V_{BO}$, and $V_{CO}$ rise quickly and achieve the maximum $V_{dc}/2$ after some time. The line voltage also degenerates to five-level from nine-level. The inverter works under an unstable condition. Then, the dual-pulse-mapping algorithm was adopted. In Figure 15c, the midpoint potentials of the three-phase capacitors return to a balanced state after a short time. The line voltage also returns to nine-level. The two capacitor voltages in phase $A$ change from 0 V and 100 V to 50 V in Figure 15d.

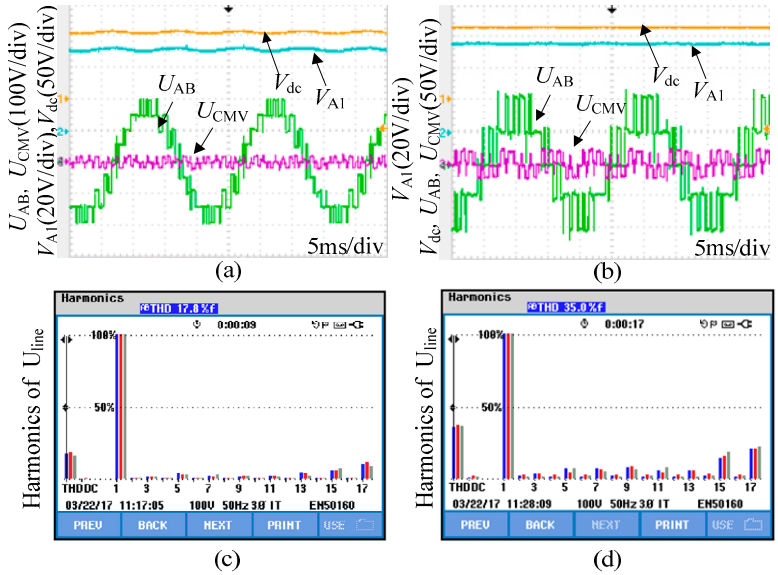



**Figure 13.** The experimental results of steady-state operation. (**a**) The DC-side voltage, the capacitance voltage of phase A, line voltage between phase A and phase B, and common-mode voltage when $m$ is 0.9; (**b**) The DC-side voltage, the capacitance voltage of phase A, line voltage between phase A and phase B, and common-mode voltage when $m$ is 0.4; (**c**) The harmonic analysis of the line voltage when m is 0.9; and (**d**) The harmonic analysis of the line voltage when m is 0.4.

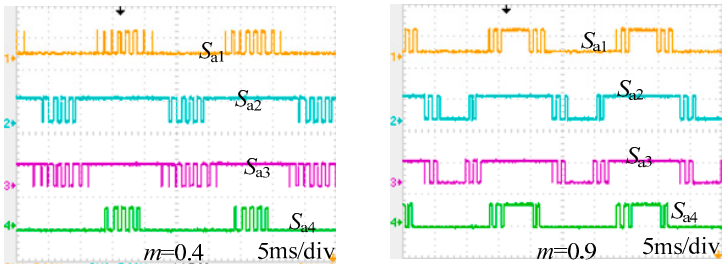



**Figure 14.** The pulse width modulations (PWMs) of phase *A* when $m = 0.4$ and $m = 0.9$.

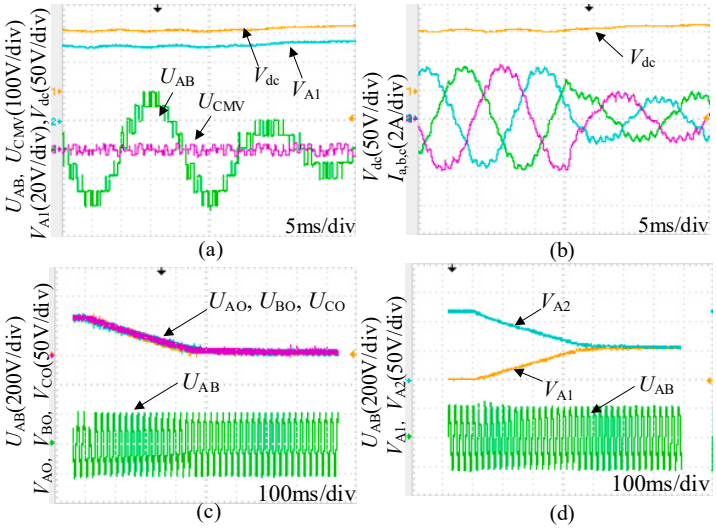



**Figure 15.** The experimental results of dynamic performance. (**a**) The DC-side voltage, the capacitance voltage of phase A, line voltage between phase A and phase B, and common-mode voltage with changing *m*; (**b**) The DC-side voltage and the currents of three-phase with changing *m*; (**c**) The midpoint potentials of three-phase and the line voltage between phase A and phase B after dual-pulse mapping strategy started to work; and (**d**) The two capacitor voltages in phase A after dual-pulse mapping strategy started to work.

## 7. Conclusions

In this paper, the balance of the midpoint potentials of three-phase DC-side capacitors and the suppression of common-mode voltage were studied in a three-phase, five-level NPC/H-bridge inverter. A dual-pulse-mapping algorithm was proposed based on the characteristics of this topology. In combination with the traditional six-segment SVPWM, the proposed algorithm selectively uses the two pulse mappings that have the opposite effects on the midpoint potentials of the capacitors. The simulation and experimental results show that the proposed algorithm can balance the midpoint potentials perfectly and can suppress the common-mode voltage effectively. Based on the dynamic experiments, we can conclude that the proposed algorithm has a good capability to respond and the output performance is as good as that of the traditional SVPWM. Compared with the hardware balancing method, the volume and the cost of the system are both reduced. So, the proposed algorithm has a certain significance for cascaded NPC/H-bridge multilevel topology research. In high-voltage and high-power applications, the NPC/H bridge topology will be more suitable with the proposed algorithm.

**Author Contributions:** Z.S. put forward the main idea of this paper. K.Z. and Q.C. performed the data analysis and the simulations/experiments. M.W. and Z.L. assisted with the idea's development and the paper's writing.

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