

Article

An Analysis of Non-Isolated DC-DC Converter Topologies with Energy Transfer Media

Se-Un Shin 

Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109, USA;
seuns@umich.edu

Received: 30 March 2019; Accepted: 15 April 2019; Published: 18 April 2019



Abstract: As miniaturized mobile devices with various functionalities are highly desired, the current requirement for loading blocks is gradually increasing. Accordingly, the efficiency of the power converter that supports the current to the loading blocks is a critical specification to prolong the battery time. Unfortunately, when using a small inductor for the miniaturization of mobile devices, the efficiency of the power converter is limited due to a large parasitic DC resistance (R_{DCR}) of the inductor. To achieve high power efficiency, this paper proposes an energy transfer media (ETM) that can make a switched inductor capacitor (SIC) converter easier to design, maintaining the advantages of both a conventional switched capacitor (SC) converter and a switched inductive (SI) converter. This paper shows various examples of SIC converters as buck, boost, and buck-boost topologies by simply cascading the ETM with conventional non-isolated converter topologies without requiring a sophisticated controller. The topologies with the ETM offer a major advantage compared to the conventional topologies by reducing the inductor current, resulting in low conduction loss dissipated at R_{DCR} . Additionally, the proposed topologies have a secondary benefit of a small output voltage ripple owing to the continuous current delivered to the load. Extensions to a multi-phase converter and single-inductor multiple-output converter are also discussed. Furthermore, a detailed theoretical analysis of the total conduction loss and the inductor current reduction is presented. Finally, the proposed topologies were simulated in PSIM, and the simulation results are discussed and compared with conventional non-isolated converter topologies.

Keywords: switched inductor capacitor converter; a power converter; energy transfer media; ripple voltage; efficiency; conduction loss

1. Introduction

The use of high-performance, power-hungry mobile devices has increased recently, prompting the need for longer battery life [1,2]. Accordingly, power management integrated circuits (PMICs) for mobile devices are becoming important. PMICs consist of a linear regulator, a switched capacitor (SC) converter, and a switched inductor (SI) converter [3,4]. Although linear regulators offer the advantage of low output voltage ripple, they have low power efficiency [5–8]. In contrast, SC converters have high power density with better power efficiency than linear regulators, but they suffer from severe degradation of efficiency when the conversion ratio of the SC converter differs from a pre-defined value [9–12]. Furthermore, when the load current (I_{LOAD}) increases, which is referred to as a heavy load condition, SC converters require many large external capacitors. Therefore, neither linear regulators nor SC converters are good candidates for powering high performance loading blocks that require a large I_{LOAD} . On the other hand, a SI converter with an external inductor is an efficient solution in heavy load conditions [13–16]. Buck, boost, and buck-boost SI converters exist for generating lower, higher, and lower or higher output voltage (V_O), respectively, compared with the battery voltage (V_{IN}).

In the SI converter, there are two representative power losses, as shown in Figure 1. One is the switching loss (P_{SW}) which is proportional to the switching frequency. When the switching frequency is fixed, the P_{SW} is a constant independent of the I_{LOAD} . The other is the conduction loss (P_{cond}). Since the P_{cond} is proportional to the square of the current, the P_{cond} is dominant in heavy load conditions. Therefore, reducing P_{cond} is important for improving power efficiency when I_{LOAD} is large.

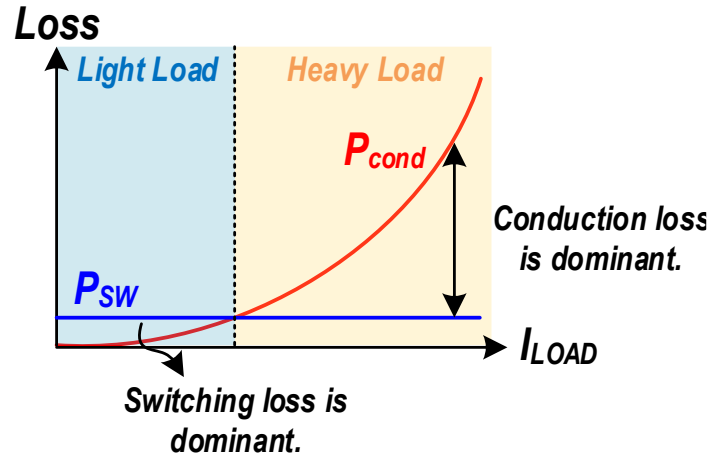


Figure 1. Graph of the switching loss and conduction loss in different conditions.

However, due to a large inductor current (i_L), under heavy load conditions, these efficient SI converters also suffer from significant conduction loss (P_{DCR}) dissipated at a parasitic DC resistance (R_{DCR}) of a small inductor for size-limited mobile devices as shown in Figure 2. This large P_{DCR} causes a severe thermal problem as well as low power efficiency in heavy load conditions. P_{DCR} is expressed as follows:

$$P_{DCR} = i_{L,RMS}^2 R_{DCR} = (I_L^2 + \frac{\Delta i_L^2}{12}) R_{DCR} \quad (1)$$

where $i_{L,RMS}$, I_L , and Δi_L are the root-mean-square value, the DC value, and the ripple of the i_L , respectively. Since the small inductor for the miniaturized mobile device can have much larger R_{DCR} than the on-resistance of switches, reducing P_{DCR} can achieve a significant improvement in power efficiency. To minimize the P_{DCR} , reducing $i_{L,RMS}$ is the only solution when a large R_{DCR} of the small inductor is used as shown in Equation (1). In particular, as the inductor with larger R_{DCR} than the on-resistance of the switch is adopted, the efficiency improvement due to low $i_{L,RMS}$ is significantly increased.

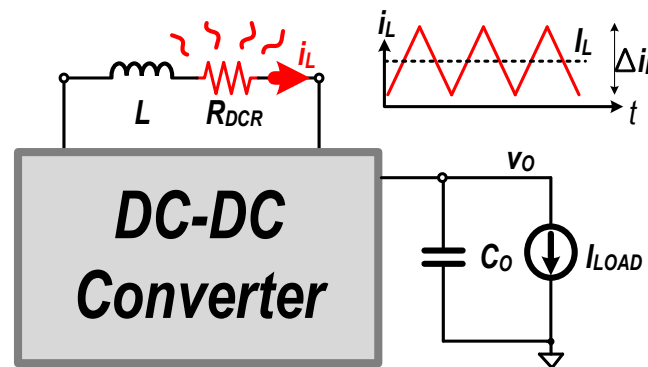


Figure 2. Conduction loss of a parasitic DC resistance (R_{DCR}) of the inductor in heavy load conditions.

There are some alternative topologies that can reduce $i_{L,RMS}$ in a SI converter. For example, Figure 3a shows a multi-level structure with an additional flying capacitor that reduces Δi_L , thereby improving power efficiency in light or medium load conditions [17,18]. However, under heavy loads,

since I_L is much larger than Δi_L , the reduction of P_{DCR} is limited. Alternatively, Figure 3b shows a multi-phase structure that can reduce I_L and can result in increased power efficiency compared with the multi-level structure in heavy load conditions. However, it requires an additional inductor that is larger and more expensive than other passive components [19–21]. Furthermore, both the multi-level and the multi-phase structures require complex balancing circuits, as shown in Figure 3.

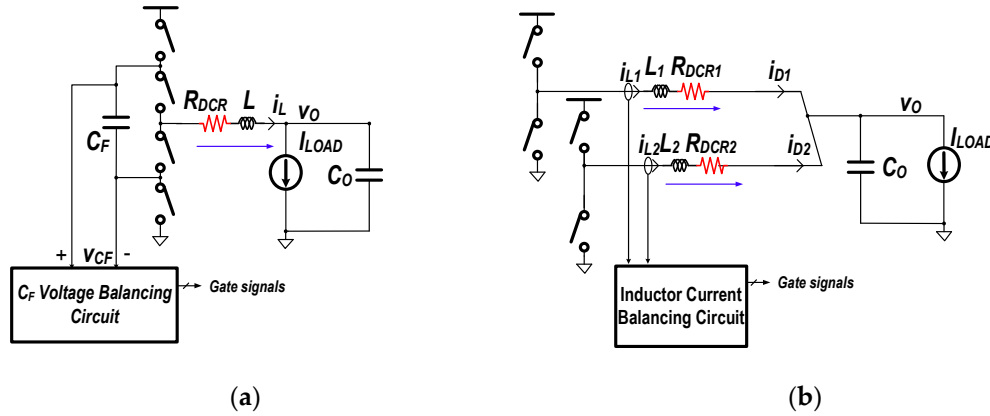


Figure 3. Alternative topologies for reducing conduction loss in R_{DCR} : (a) multi-level buck converter; (b) multi-phase buck converter.

To resolve these issues, this paper proposes and analyzes a new type of hybrid switched inductor capacitor (SIC) converter with energy transfer media (ETM) using an additional flying capacitor. The topologies with the ETM provide improved efficiency by lowering I_L owing to an additional current path in heavy load conditions.

The topologies with the proposed ETM are introduced in Section 2. In Sections 3 and 4, the operation principle and a detailed conduction loss analysis of both the buck and buck-boost topologies are provided. In Section 5, different examples of extension to other topologies are explained and discussed. The simulation results for verification are presented in Section 6. Finally, a brief concluding summary is given in Section 7.

2. Energy Transfer Media

A hybrid SIC converter that possesses the advantages of both a SC converter and a SI converter is an attractive solution [22–30]. However, it is complicated to design because of the many complex combinations of power switches and flying capacitors. Also, various factors such as conversion ratios, balancing circuits, and power loss should be considered. To make it easy to design, and to reduce P_{DCR} at the same time, this paper proposes an ETM that can be easily implemented with all types of non-isolated converters, such as buck, boost, and buck-boost topologies, with high efficiency under heavy load conditions. An ETM has been used previously to reduce only Δi_L [29,30]. However, similar to a multi-level converter, this structure is not effective at improving power efficiency under heavy load conditions. Therefore, we propose an ETM that uses an additional flying capacitor to obtain high efficiency in heavy load conditions, as shown in Figure 4.

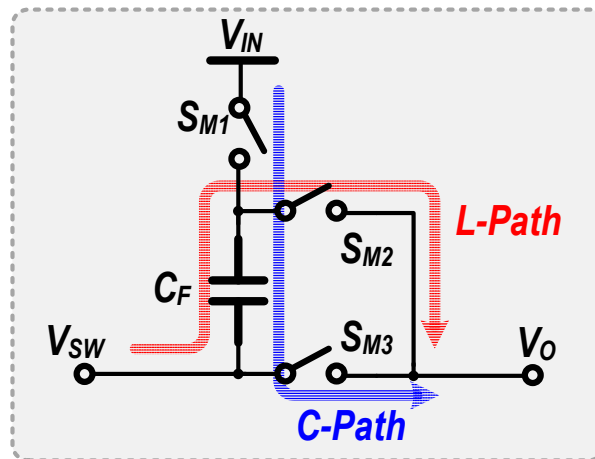


Figure 4. Energy transfer media with a flying capacitor.

The ETM uses one external flying capacitor (C_F) and three power switches (S_{M1} – S_{M3}). This approach offers the advantage of inserting the capacitor current path into the output current path (C-path) as well as the inductor current path (L-path). This ETM with dual current paths can be applied to conventional non-isolated topologies by simply cascading the ETM, as shown in Figure 5. Figure 5a is a conceptual structure showing that the ETM can be applied to conventional converter topologies. Figure 5b–d show examples of applying the ETM to buck, boost, and buck-boost converters, respectively. This paper analyzes buck type and buck-boost type topologies with ETMs as examples and discusses possible extensions to other topologies.

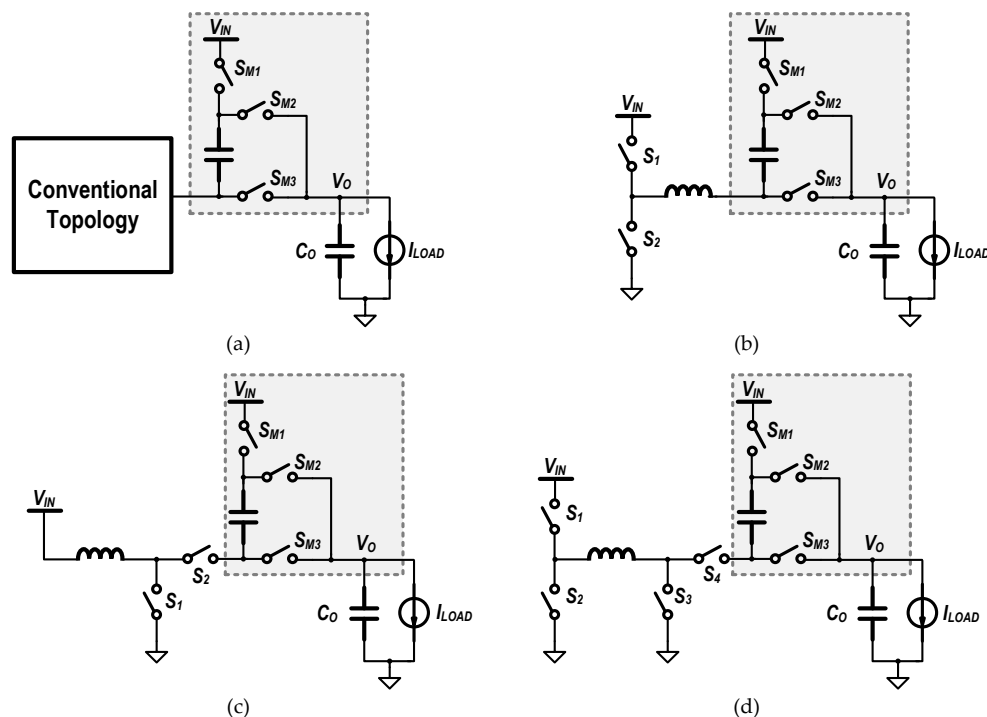


Figure 5. (a) Conventional topology with an energy transfer media; (b) buck converter; (c) boost converter; (d) buck-boost converter.

3. Buck Converter with Energy Transfer Media

Figure 5b shows a buck converter with ETM (BKETM), which is composed of power switches S_1 – S_2 and S_{M1} – S_{M3} , one inductor (L), one flying capacitor (C_F), and one output capacitor (C_O). The BKETM

uses two operating modes (Φ_1 , Φ_2), as shown in Figure 6a. The operation waveforms of the BKETM are shown in Figure 6b.

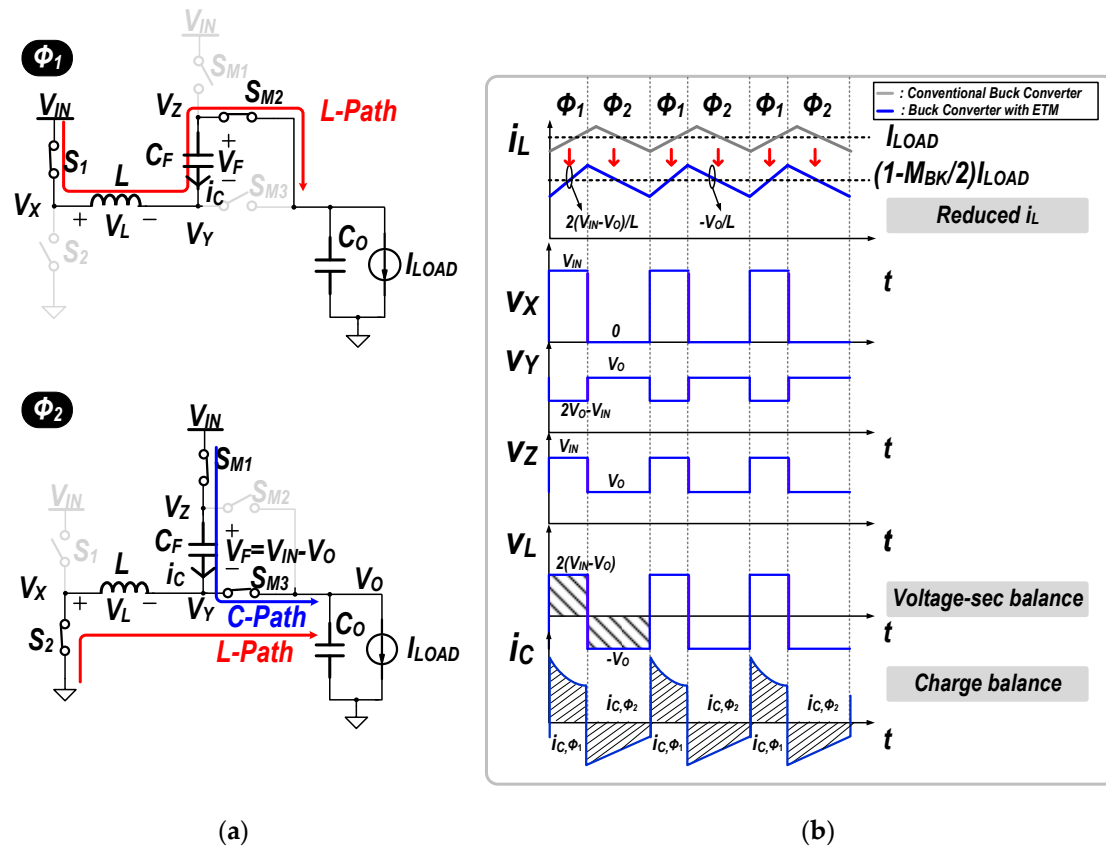


Figure 6. Operating mode (a) and waveforms (b) of buck converter with energy transfer media (BKETM).

In Φ_1 , S_1 and S_{M2} are turned on, and S_2 , S_{M1} , and S_{M3} are turned off. At this time, i_L is built up with a slope of $2(V_{IN} - V_O)/L$ and is delivered to the output. In Φ_2 , S_2 , S_{M1} , and S_{M3} are turned on, and S_1 and S_{M2} are turned off. While i_L is de-energized with a slope of $-V_O/L$, it is also delivered to the output. In the meantime, the capacitor current i_C of C_F flows to the output, while the voltage of C_F is charged to $V_{IN} - V_O$. To derive a conversion ratio (M_{BK}), applying the voltage sec balance to the inductor with duty cycle D is expressed as follows:

$$D(2V_{IN} - 2V_O) - (1 - D)V_O = 0. \quad (2)$$

Simplifying Equation (2), M_{BK} is given by:

$$M_{BK} = \frac{V_O}{V_{IN}} = \frac{2D}{1 + D} 0 < D < 1. \quad (3)$$

The M_{BK} of the BKETM from Equation (3) has a value between 0 and 1 as D varies from 0 to 1, which is the same as the range of a conventional buck converter (CBK). Therefore, in spite of the SIC converter, the BKETM behaves like a CBK without the limit of the conversion ratio.

To obtain the average value of the C-path current (I_{C,Φ_2}) delivered to the output in Φ_2 , we also apply charge balance to C_F as shown below:

$$DI_L - (1 - D)I_{C,\Phi_2} = 0. \quad (4)$$

Simplifying Equation (4), $I_{C,\Phi 2}$ is given by

$$I_{C,\Phi 2} = \frac{D}{1-D} I_L. \quad (5)$$

Applying the charge balance to the output capacitor C_O ,

$$D(I_L - I_{LOAD}) + (1-D)(I_L + I_{C,\Phi 2} - I_{LOAD}) = 0. \quad (6)$$

Substituting Equation (5) into Equation (6), I_L can be expressed with I_{LOAD} as shown below:

$$I_L = \frac{1}{1+D} I_{LOAD} = (1 - \frac{M_{BK}}{2}) I_{LOAD}. \quad (7)$$

For the CBK, I_L is always the same as I_{LOAD} [3,4,13–16]. In contrast, for the proposed BKETM, I_L is I_{LOAD} divided by $(1+D)$. As M_{BK} increases, I_L decreases. Therefore, I_L always has a smaller value than I_{LOAD} due to the two current paths (L -path and C -path). As I_L decreases, P_{DCR} also is reduced compared to that of the CBK. To compare the total conduction loss with that of the CBK, we assume that since the parasitic resistance (R_{ESR}) of the flying capacitors is typically much smaller than other resistances, the loss of R_{ESR} can be ignored for simplicity. Also, the on-resistance of each switch is assumed to be the same as R_{ON} . Thus, the total conduction loss ($P_{cond,CBK}$) of the CBK is expressed as follows:

$$P_{cond,CBK} = DI_L^2 R_{ON} + (1-D)I_L^2 R_{ON} + I_L^2 R_{DCR} = I_L^2 (R_{ON} + R_{DCR}) = I_{LOAD}^2 (R_{ON} + R_{DCR}). \quad (8)$$

On the other hand, the total conduction loss ($P_{cond,BKETM}$) of the BKETM is as follows:

$$P_{cond,BKETM} = 2DR_{ON}I_L^2 + (1-D)R_{ON}(I_L^2 + I_{C,\Phi 2}^2 + (I_L + I_{C,\Phi 2})^2) + I_L^2 R_{DCR} \quad (9)$$

$$= I_L^2 \left[(1+D + \frac{1}{1-D} + \frac{D^2}{1-D}) R_{ON} + R_{DCR} \right] \quad (10)$$

$$= I_L^2 \left(\frac{2-M_{BK}}{1-M_{BK}} R_{ON} + R_{DCR} \right) \quad (11)$$

$$= \frac{(2-M_{BK})^2}{4} I_{LOAD}^2 \left(\frac{2-M_{BK}}{1-M_{BK}} R_{ON} + R_{DCR} \right). \quad (12)$$

For the relative comparison with CBK, the ratio between $P_{cond,CBK}$ and $P_{cond,BKETM}$ is expressed as:

$$\frac{P_{cond,proposed}}{P_{cond,conv}} = \frac{\frac{(2-M_{BK})^2}{4} \left(\frac{2-M_{BK}}{1-M_{BK}} R_{ON} + R_{DCR} \right)}{R_{ON} + R_{DCR}}. \quad (13)$$

Figure 7 depicts the value calculated by Equation (13) versus the conversion ratio M_{BK} for different R_{DCR} . It shows that $P_{cond,BKETM}$ is lower than $P_{cond,CBK}$ across a wide range of M_{BK} values. As described by Equation (7), the total conduction loss decreases because I_L is reduced as M_{BK} increases. Also, the larger the R_{DCR} , the lower the $P_{cond,BKETM}$ is compared with $P_{cond,CBK}$. Therefore, BKETM is a useful topology for step-down when a small inductor with a large R_{DCR} is used in heavy load conditions.

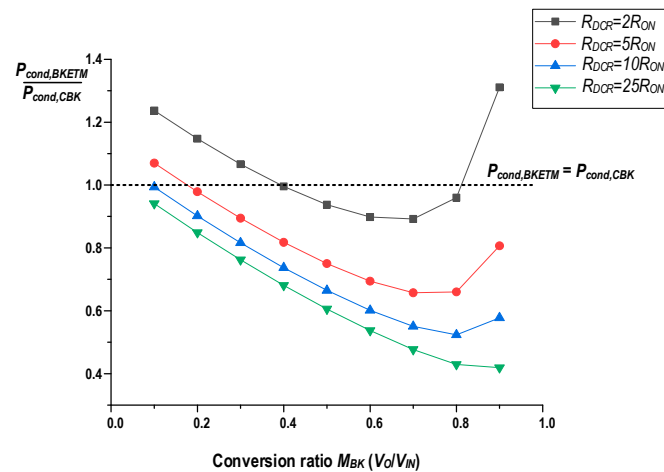


Figure 7. Conduction loss comparison for the buck converter with energy transfer media (BKETM) and conventional buck converter (CBK) with different R_{DCR} values.

4. Buck-Boost Converter with Energy Transfer Media

Since the boost converter with the ETM shown in Figure 5c has been previously described in detail in [27], this paper focuses on the buck-boost converter with ETM (BBETM) shown in Figure 5d. It is composed of power switches S_1 – S_4 , S_{M1} – S_{M3} , one inductor (L), one flying capacitor (C_F), and one output capacitor (C_O). The BBETM also uses two operating modes (Φ_1 , Φ_2), as shown in Figure 8a. Its operation waveforms are shown in Figure 8b.

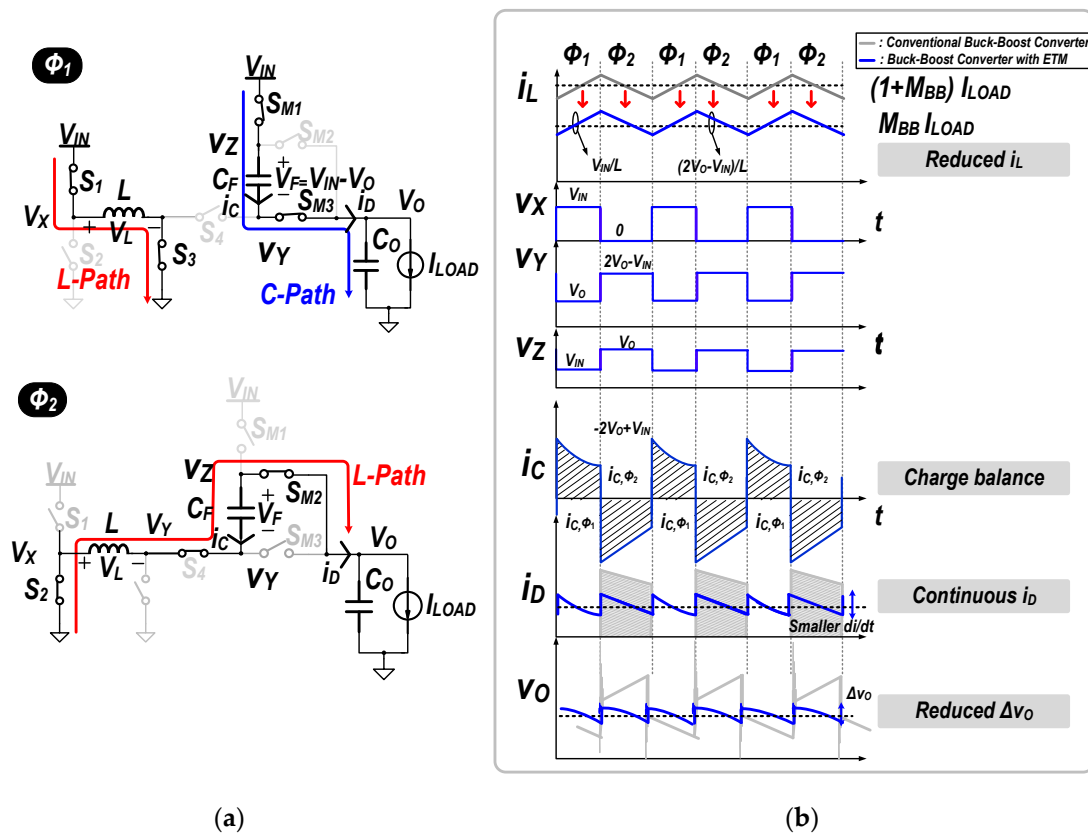


Figure 8. Operating modes (a) and waveforms (b) of buck-boost converter with ETM.

In Φ_1 , S_1 and S_3 are turned on while i_L increases with a slope of V_{IN}/L and is delivered to the output. At the same time, S_{M1} and S_{M3} turn on, and i_C flows to the output through the C-path, while the

voltage of C_F is charged to $V_{IN} - V_O$. With a conventional buck-boost (CBB) converter, current cannot be delivered to the output while i_L is building up. The ability of the BBETM to transfer the energy to the output during i_L build-up is one of the main differences between the BBETM and a CBB converter. Owing to this operation, the output delivery current (i_D) in the BBETM is continuous, resulting in a small output voltage ripple (ΔV_O). In Φ_2 , S_2 , S_{M2} , and S_{M3} turn on, and i_L is delivered to the output.

For the BBETM conversion ratio (M_{BB}), applying the voltage sec balance to the inductor based on the operation is expressed as follows:

$$DV_{IN} + (1 - D)(-2V_O + V_{IN}) = 0. \quad (14)$$

Simplifying Equation (14), M_{BB} is given by:

$$M_{BB} = \frac{V_{OUT}}{V_{IN}} = \frac{1}{2(1 - D)} \quad 0 < D < 1. \quad (15)$$

M_{BB} of the BBETM from Equation (15) has a value between 0.5 and infinity as D varies from 0 to 1. This means that the BBETM can operate for step-up and step-down output voltages. Since the conversion ratio is limited to less than 0.5, this approach is not appropriate for applications with a low conversion ratio. However, it offers several advantages compared with a CBB converter.

First, similar to the buck type converter, the BBETM I_L is reduced compared with that of a CBB converter. To analyze this, the average value of the C-path current (I_{C,Φ_1}) in Φ_1 can be obtained by applying charge balance to the C_F as shown below:

$$DI_{C,\Phi_1} - (1 - D)I_L = 0. \quad (16)$$

Simplifying Equation (16), I_{C,Φ_1} is given by

$$I_{C,\Phi_1} = \frac{1 - D}{D} I_L. \quad (17)$$

Applying the charge balance to C_O ,

$$D(I_{C,\Phi_1} - I_{LOAD}) + (1 - D)(I_L - I_{LOAD}) = 0. \quad (18)$$

Substituting Equation (17) into Equation (18), I_L can be expressed with load current (I_{LOAD}) as shown below:

$$I_L = \frac{1}{2(1 - D)} I_{LOAD} = M_{BB} I_{LOAD}. \quad (19)$$

Due to the two current paths in the ETM, the BBETM I_L is as low as $M_{BB} I_{LOAD}$, while the CBB I_L is $(1 + M_{BB}) I_{LOAD}$ [4]. Therefore, the BBETM P_{DCR} can be reduced. To compare the total conduction loss with that of the CBB, the on-resistance of each switch is assumed to be the same as R_{ON} , and the total conduction loss ($P_{cond,CBB}$) of the CBB is expressed as follows:

$$P_{cond,CBB} = 2I_L^2 R_{ON} + I_L^2 R_{DCR} = (1 + M_{BB})^2 I_{LOAD}^2 (2R_{ON} + R_{DCR}). \quad (20)$$

In contrast, the total conduction loss ($P_{cond,BBETM}$) of the BBETM is expressed as

$$P_{cond,BBETM} = I_L^2 R_{ON} + I_L^2 D R_{ON} + 2I_{C,\Phi_1}^2 D R_{ON} + 2I_L^2 (1 - D) R_{ON} + I_L^2 R_{DCR} \quad (21)$$

$$= I_L^2 \left[(3 - D + \frac{2(1 - D)^2}{D}) R_{ON} + R_{DCR} \right] \quad (22)$$

$$= M_{BB}^2 I_{LOAD}^2 \left[\left(\frac{1}{M_{BB}(2M_{BB} - 1)} - \frac{2M_{BB} - 1}{2M_{BB}} + 3 \right) R_{ON} + R_{DCR} \right]. \quad (23)$$

For the relative comparison with the CBB, the ratio between $P_{cond,CBB}$ and $P_{cond,BBETM}$ for the BBETM is expressed as

$$\frac{P_{cond,BBETM}}{P_{cond,CBB}} = \frac{M_{BB}^2 \left[\left(\frac{1}{M_{BB}(2M_{BB}-1)} - \frac{2M_{BB}-1}{2M_{BB}} + 3 \right) R_{ON} + R_{DCR} \right]}{(1 + M_{BB})^2 (2R_{ON} + R_{DCR})}. \quad (24)$$

Figure 9 depicts the values of Equation (24) versus the conversion ratio M_{BB} for different R_{DCR} values, showing that the $P_{cond,BBETM}$ is lower than the $P_{cond,CBB}$ for a wide range of M_{BB} values. This finding demonstrates that the BBETM is more efficient than CBB due to the dual current paths. Also, it shows that the larger the R_{DCR} , the lower $P_{cond,BBETM}$ is, compared with $P_{cond,CBB}$. Therefore, the BBETM is useful for step-up and step-down applications when a small inductor with a large R_{DCR} is used in heavy load conditions.

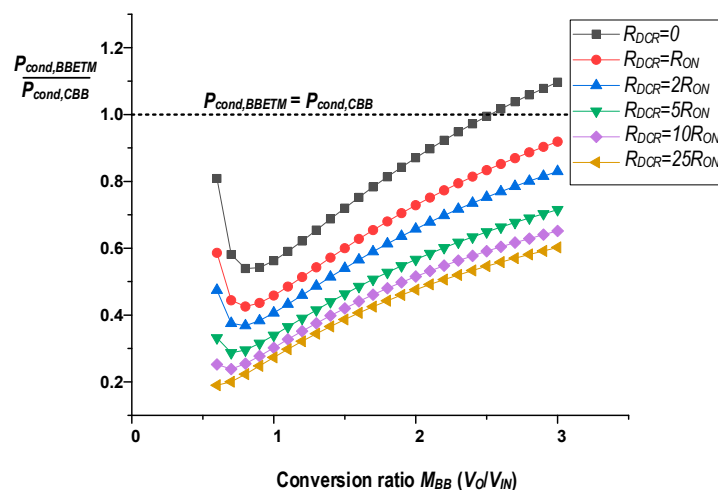


Figure 9. Conduction loss comparison of buck-boost converter with energy transfer media (BBETM) and conventional buck-boost (CBB) for different R_{DCR} values.

5. Extension to Other Topologies

5.1. Multi-Phase Buck Converter with ETM

The multi-phase converter is a structure that allows multiple inductors to transfer energy to the output when it is difficult to support sufficient energy for the output with only a single converter. The proposed ETM can also easily implement a SIC converter with a multi-phase structure. As shown in Figure 10a, the multi-phase buck converter can be designed with two ETMs for a single output with heavy I_{LOAD} . The proposed multi-phase buck converter with ETM (MBKETM) consists of one inductor and two flying capacitors, because two ETMs are used. Figure 10b shows the operation principle of the MBKETM. The advantage of the MBKETM over other topologies with an ETM is that the input frequency (f_{IN}) for the input duty (Φ_1, Φ_2) and the output switching frequency (f_{OUT}) for the output duty (Φ_{O1}, Φ_{O2}) can be independently controlled. As an example, in this paper, the input duty is controlled to regulate the output voltage, and the output duty is always fixed at 0.5 so that the C-path currents ($I_{C,\Phi_{O1}}, I_{C,\Phi_{O2}}$) can be maintained at the inductor current I_L . Then, applying charge balance to the output capacitor C_O in this condition,

$$I_L = I_{C,\Phi_{O1}} = I_{C,\Phi_{O2}} = \frac{1}{2} I_{LOAD}. \quad (25)$$

From Equation (25), I_L can also be maintained at half of I_{LOAD} , the same value as I_L of the conventional multi-phase buck converter (CMBK) with two inductors [19]. Thus, the MBKETM can generate triple current paths (one L -path, two C -paths) with a single inductor and two low-cost,

small flying capacitors, thus reducing cost and size compared with a CMBK. Moreover, owing to these triple current paths, the ripple of the output delivery current i_D is reduced such that the output voltage ripple ΔV_O is smaller than that of the BKETM. Furthermore, by adopting a higher output frequency (f_{OUT}) for the output duty (Φ_{O1}, Φ_{O2}) than the input frequency (f_{IN}) for the input duty (Φ_1, Φ_2), ΔV_O can be further reduced. These characteristics are verified with simulation results in the next section.

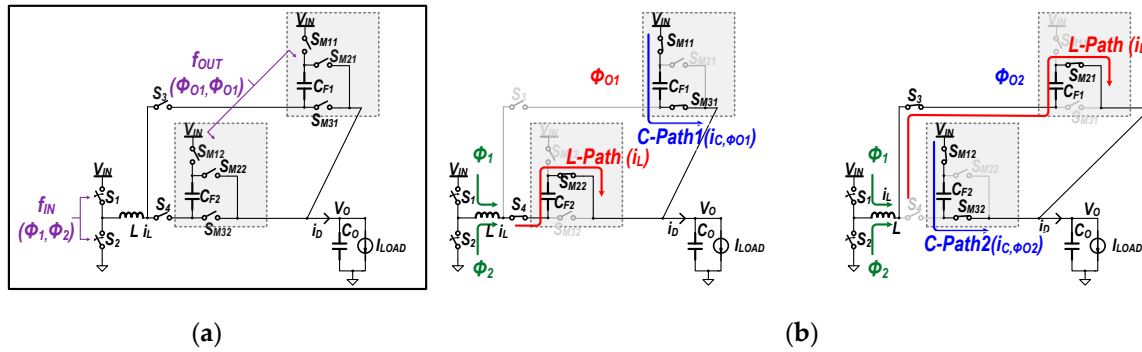


Figure 10. Topology (a) and operation (b) of a multi-phase buck converter with ETM.

5.2. Single-Inductor Multiple-Output Buck Converter with ETM

As the name suggests, a single-inductor multiple-output (SIMO) converter can regulate many outputs with one inductor [31–33]. As shown in Figure 11a as an example, it is also easy to make a dual-output structure with two ETMs. More outputs can be generated by increasing the number of ETMs. Figure 11b shows the operation of a single-inductor dual-output (SIDO) buck converter with two ETMs (SIDOETM). Because of the ETMs, I_L is reduced compared with that of a conventional SIMO converter (CSIMO). Moreover, since the SIDOETM has triple paths (one L-path and two C-paths), the currents (i_{D1}, i_{D2}) delivered to each output (V_{O1}, V_{O2}) are continuous. In contrast, with the CSIMO, the currents delivered to the output are discontinuous because a single inductor must be used to distribute the energy to each output during different time slots. Therefore, the CSIMO has the disadvantage of significant large voltage ripple at each output. In contrast, since the proposed SIDOETM has continuous i_{D1} and i_{D2} , the output voltage ripples ($\Delta V_{O1}, \Delta V_{O2}$) can be significantly reduced. Also, the CSIMO typically uses a comparator-based control for regulation of the outputs, which is very vulnerable to spike noise at the outputs [32,33]. Because the discontinuous output delivery currents can generate large spikes at every output due to the parasitic inductance that is connected to the output capacitors in series, it can cause a malfunction on the regulation control of the CSIMO. Therefore, the SIDOETM has an additional advantage of being able to alleviate the spike noise due to continuous output delivery current.

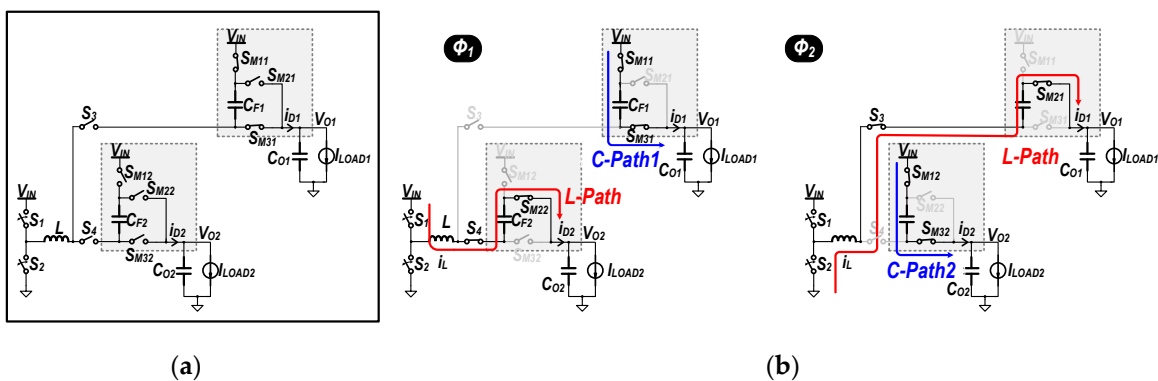


Figure 11. Topology (a) and operation (b) of a single-inductor dual-output buck converter with ETM.

6. Simulation Results and Discussion

6.1. Buck Converter with ETM

Table 1 shows the simulation conditions for the proposed BKETM. To obtain accurate simulation results, the switching loss model is included as well as the conduction loss in the simulation. C_{gate} and C_{oss} in Table 1 are the gate capacitance and the output capacitance of the power switch, respectively, for considering the switching loss. Figure 12 shows the simulated waveforms to confirm the operation of the converter.

Table 1. Simulation conditions for buck converter with ETM.

V_{IN}	V_{OUT}	I_{LOAD}	f_{IN}	L	R_{DCR}
5 V	2.8 V	1 A	1 MHz	4.7 μ H	0.2 Ω
C_F	C_O	R_{ON}	R_{ESR}	C_{gate}	C_{oss}
4.7 μ F	4.7 μ F	50 m Ω	20 m Ω	250 pF	100 pF

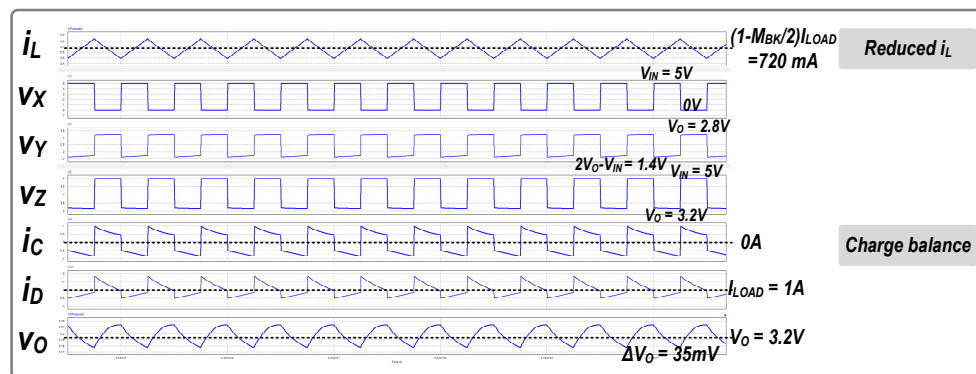


Figure 12. Simulation waveforms of a buck converter with ETM.

The results show a I_L of 720 mA, lower than the I_{LOAD} of 1 A. Also, the charge balance of the capacitor is satisfied through i_c , and the voltage and current values of each node match the calculation in Section 3. Owing to the lowered I_L , high efficiency can be achieved even when using a small inductor, reducing P_{DCR} . This type of converter can also solve the heat problems associated with high performance mobile devices. However, since the BKETM has a pulsating i_D due to the C-path, a large ΔV_O of 35 mV is observed, as shown in Figure 12.

Figure 13 shows the simulated efficiency plots for both the BKETM and CBK with different conversion ratios (M_{BK}). From Equation (7), the larger the value of M_{BK} , the larger the reduction in I_L . Thus, the efficiency of the BKETM is higher than that of the CBK when M_{BK} is high. However, as M_{BK} approaches 1, the C-path current, $I_{C,\Phi 2}$, rapidly increases according to Equation (5). Then, the total conduction loss increases again, resulting in the degradation of the efficiency of the BKETM.

Figure 14 shows the efficiency plots with different values of I_{LOAD} when M_{BK} is 0.6 or 0.3. When M_{BK} is high, as I_{LOAD} increases, the efficiency improves compared with that of the CBK. However, when M_{BK} is low, the reduction effect of I_L is not significant. Then, even if I_{LOAD} becomes large, the increment in efficiency is negligible. Therefore, the BKETM is an efficient topology when M_{BK} is high under heavy load conditions.

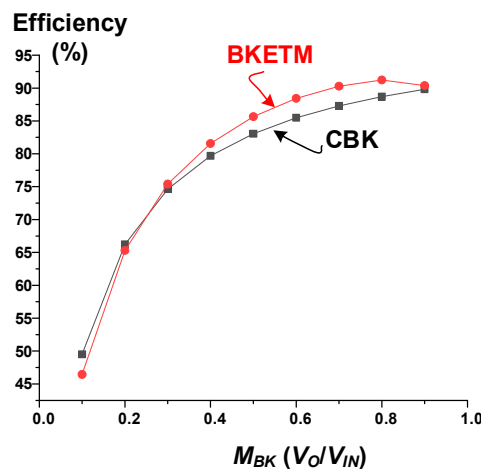


Figure 13. Simulated efficiency plot of a buck converter with ETM at different conversion ratios.

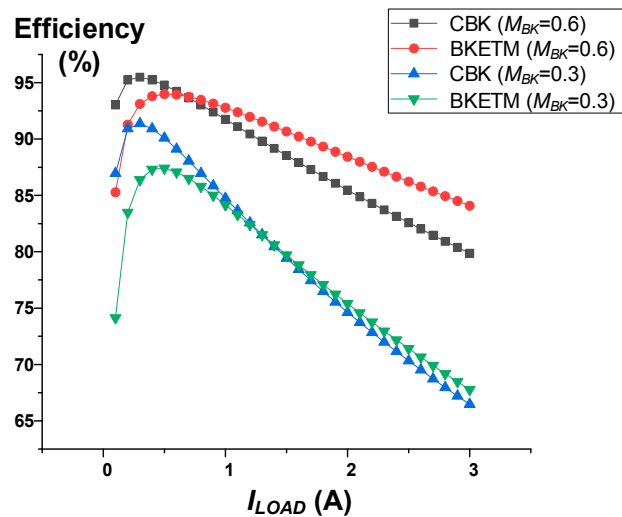


Figure 14. Simulated efficiency plot for a buck converter with ETM at different load currents.

6.2. Buck-Boost Converter with ETM

Table 2 shows the simulation conditions for the proposed BBETM. Figure 15 shows the simulation results to confirm the operation of the converter.

Table 2. Simulation conditions for buck-boost converter with ETM.

V_{IN}	V_{OUT}	I_{LOAD}	f_{IN}	L	R_{DCR}
5 V	6 V	1 A	1 MHz	4.7 μ H	0.2 Ω
C_F	C_O	R_{ON}	R_{ESR}	C_{gate}	C_{oss}
4.7 μ F	4.7 μ F	50 m Ω	20 m Ω	250 pF	100 pF

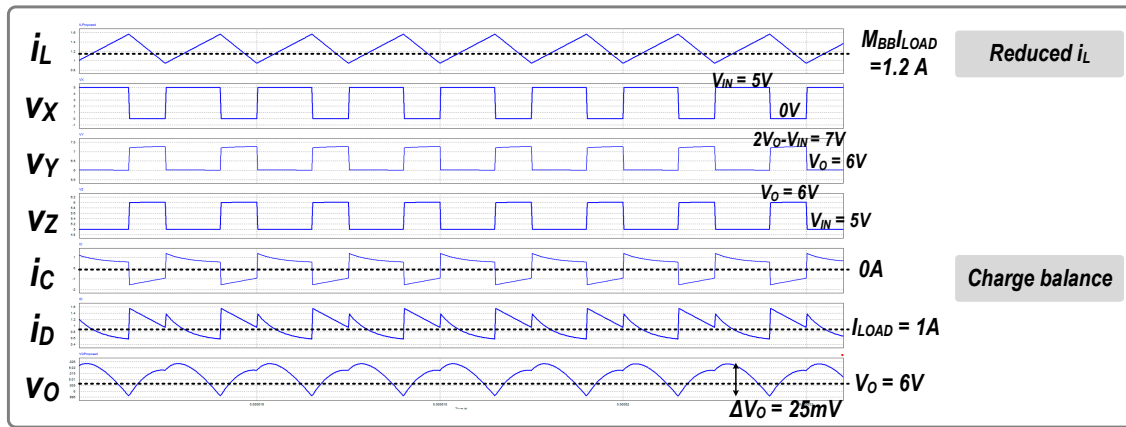


Figure 15. Simulation waveforms of buck-boost converter with ETM.

The simulation results show that the BBETM achieves a lower I_L (1.2 A) than that of the CBB (2.2 A). Also, the charge balance of C_F is satisfied through i_c , and the voltage and current values of each node are matched with the calculation in Section 4. Due to reduced inductor current, the conduction loss can be decreased even when a small inductor is used. Moreover, in contrast to the CBB i_D , the BBTEM i_D is continuous due to the addition of the C-path, resulting in a smaller ΔV_O of 25 mV compared with the 130 mV observed for the CBB under the same operating conditions, as shown in Figure 16.

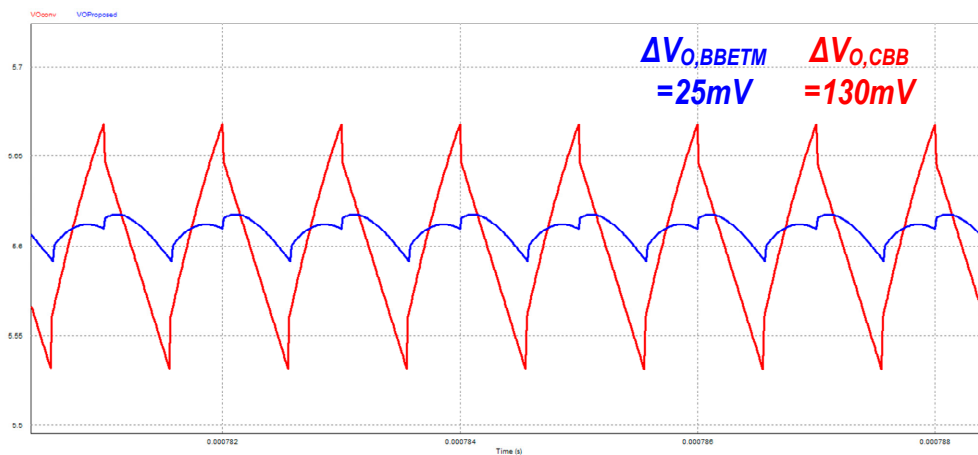


Figure 16. Simulated output voltage ripple of BBETM compared with CBB.

Figure 17 shows the simulated efficiency plots for both the BBETM and CBB with different conversion ratio values, M_{BB} . The BBETM has a much higher efficiency than the CBB across a wide range of M_{BB} values because the buck-boost topology generates a much larger I_L than the buck-type topology due to a structural characteristic.

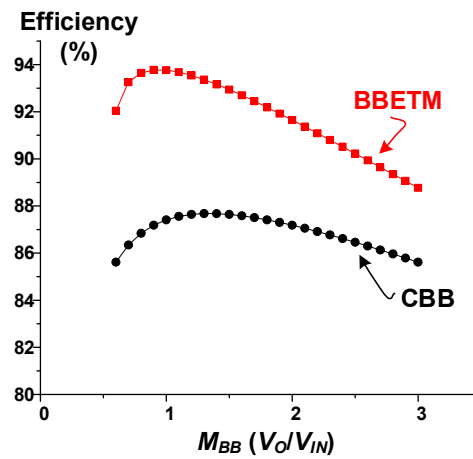


Figure 17. Simulated efficiency plot of a buck-boost converter with ETM at different conversion ratios.

Figure 18 shows the efficiency plots with different I_{LOAD} values when M_{BB} is 0.8 or 1.3. Based on Equation (19), a lower M_{BB} is associated with a larger reduction in I_L for the BBETM compared to the CBB. Thus, with a low M_{BB} , as I_{LOAD} increases, the increment in efficiency for BBETM compared with CBB becomes significant.

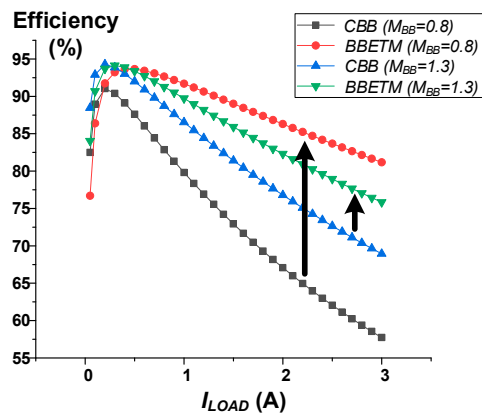


Figure 18. Simulated efficiency plot of a buck-boost converter with ETM at different load currents.

The BBETM has another benefit of a small ΔV_O . Figure 19 is a plot comparing the ΔV_O of the proposed BBETM and the CBB under the same operating conditions. The BBETM ΔV_O is lower than that of the CBB across a wide range of M_{BB} values. However, when M_{BB} is very low, which means there is a small duty cycle D , the C-path current rapidly increases as shown in Equation (17), resulting in a large ΔV_O again.

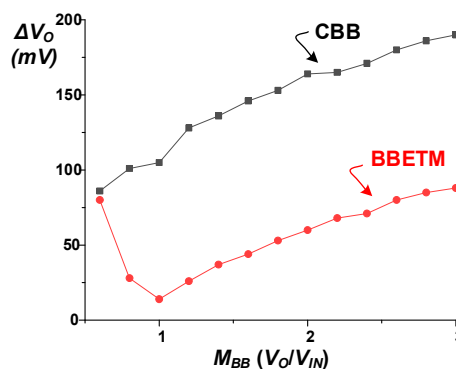


Figure 19. Simulated output voltage ripple plot of the BBETM and CBB across different conversion ratios.

6.3. Multi-Phase Buck Converter with ETM

The MBKETM is simulated under the operating conditions as shown in Table 3.

Table 3. Simulation conditions for multi-phase buck converter with ETM.

V_{IN}	V_{OUT}	I_{LOAD}	f_{IN}	L	R_{DCR}
5 V	3.7 V	1 A	1 MHz	4.7 μ H	0.2 Ω
C_F	C_O	R_{ON}	R_{ESR}	C_{gate}	C_{oss}
4.7 μ F	4.7 μ F	50 m Ω	20 m Ω	250 pF	100 pF

It is possible to separate f_{IN} and f_{OUT} as mentioned in Section 5. Figures 20–22 show the simulation waveforms of the MBKETM with different values of f_{OUT} . Figure 20 shows the waveforms when f_{IN} and f_{OUT} are both equal to 1 MHz. I_L is reduced to half of I_{LOAD} because the output duty is fixed at 0.5, as shown in Equation (25). Moreover, ΔV_O is as small as 25 mV because i_D is continuous due to the presence of both the L -path and the C -path. Figure 21 shows the waveforms when f_{OUT} is two times higher than f_{IN} . Under these conditions, ΔV_O is further reduced to 15 mV because the effective frequency seen at the output is increased. Figure 22 shows the waveforms when f_{OUT} is triple the value of f_{IN} . Under these conditions, ΔV_O is further reduced to 10 mV. However, since high f_{OUT} can increase the switching loss in the converter, causing degradation of efficiency, there is a trade-off between ΔV_O and power efficiency.

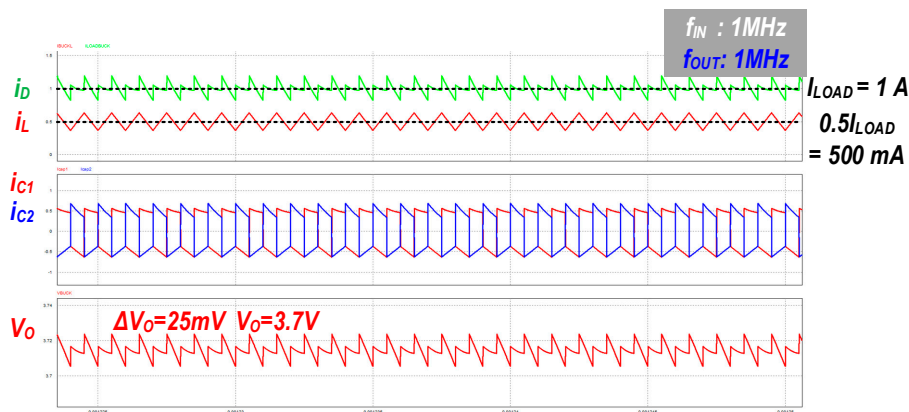


Figure 20. Simulated waveforms of the multi-phase buck converter with energy transfer media (MBKETM) with $f_{IN} = 1$ MHz and $f_{OUT} = 1$ MHz.

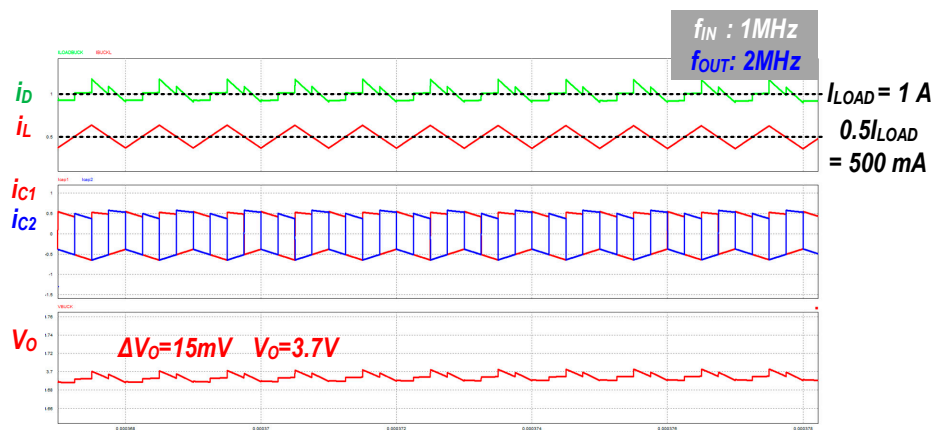


Figure 21. Simulated waveforms of the MBKETM with $f_{IN} = 1$ MHz and $f_{OUT} = 2$ MHz.

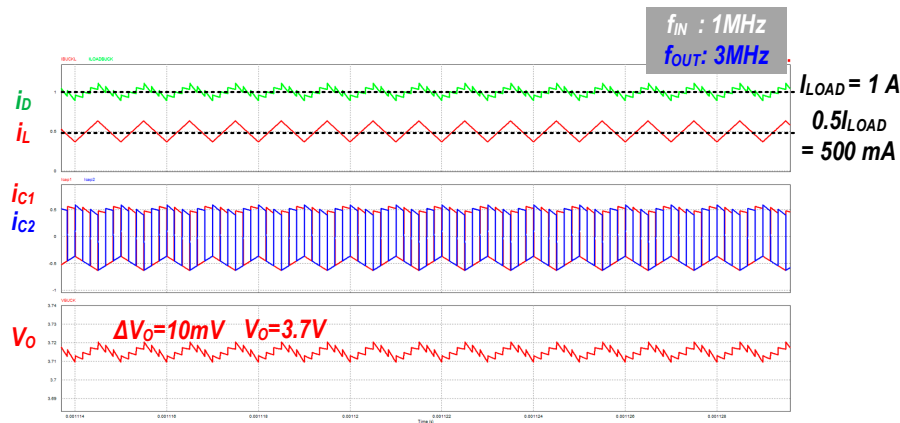


Figure 22. Simulated waveforms of the MBKETM with $f_{IN} = 1$ MHz and $f_{OUT} = 3$ MHz.

In summary, the proposed MBKETM, using one inductor and two flying capacitors, achieves a similar reduction of I_L to half of I_{LOAD} as the CMBK does with two large, expensive inductors, thereby reducing P_{DCR} significantly. Furthermore, because f_{IN} and f_{OUT} can be controlled independently, ΔV_O can be further reduced. Also, unlike the CMBK, the proposed MBKETM does not require a complex current balancing controller in spite of the multi-phase operation.

6.4. Single-Inductor Multiple-Output Buck Converter with ETM

Table 4 shows the simulation conditions of the proposed SIDOETM. Figure 23 shows the simulated i_L , i_{C1} , i_{C2} , i_{D1} , and i_{D2} of the proposed converter. Due to the dual current paths, I_L is lower than the sum of I_{LOAD1} and I_{LOAD2} .

Table 4. Simulation conditions for single-inductor multiple-output (SIDO) converter with ETM.

V_{IN}	V_{OUT1}/V_{OUT2}	I_{LOAD1}/I_{LOAD2}	f_{IN}	L	R_{DCR}
5 V	2.8 V/2 V	0.7 A/0.5 A	1 MHz	4.7 μ H	0.2 Ω
C_F	C_O	R_{ON}	R_{ESR}	C_{gate}	C_{oss}
4.7 μ F	4.7 μ F	50 m Ω	20 m Ω	250 pF	100 pF

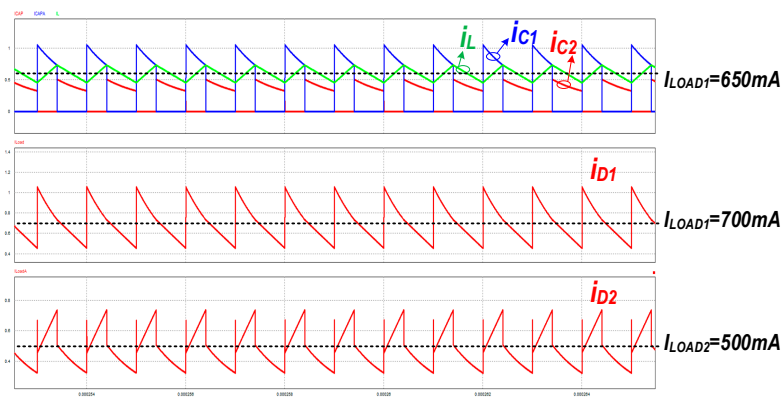


Figure 23. Simulated current waveforms of the proposed single-inductor dual-output converter with ETM (SIDOETM).

Moreover, since i_{D1} and i_{D2} do not drop to zero, the continuous current (i_{D1} , i_{D2}) flows to the respective output (V_{O1} , V_{O2}). Figure 24 shows that the output voltage is well regulated to 2.8 V and 2 V. The ripples of each output are 15 mV and 13 mV, respectively. It has a lower ΔV_O than the CSIMO [31–33].

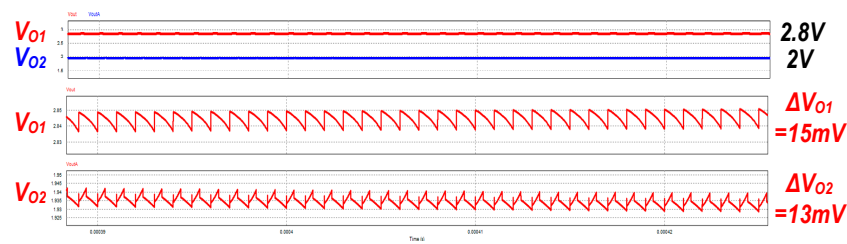


Figure 24. Simulated voltage waveforms of the proposed SIDOETM.

Tables 5 and 6 summarize the advantages of the proposed topologies with the ETM. The common advantage is the reduction of I_L , resulting in low total conduction loss in heavy load conditions. Moreover, unlike conventional topologies that have discontinuous i_D , such as the CBB and CSIMO topologies, the proposed ETM topologies have very low ΔV_O because of the continuous i_D . The MBKETM can control f_{IN} and f_{OUT} independently, resulting in further reduction of ΔV_O .

Table 5. Summary table with buck and buck-boost type converters.

Advantages	BKETM	CBK	BBETM	CBB
Reduction of I_L	O	×	O	×
Reduction of ΔV_O	×	×	O	×
Continuous i_D	O	O	O	×

O: Yes; ×: No.

Table 6. Summary table with multi-phase buck and single-inductor dual-output (SIDO) buck type converters.

Advantages	MBKETM	CMBK	SIDOETM	CSIMO
Reduction of I_L	O	×	O	×
Reduction of V_O	O	×	O	×
Continuous i_D	O	O	O	×
Separated frequency	O	×	×	×

O: Yes; ×: No.

7. Conclusions

In this paper, an ETM was proposed to make a promising hybrid switched inductor capacitor converter easier to design for heavy load conditions. New topologies with ETM, which generate dual current paths, were analyzed and compared with conventional topologies that have a single current path. Owing to the dual current paths (L -path and C -path), all of the topologies with the ETM shared the common advantage of reduced inductor current. Since it significantly decreases conduction loss dissipated at a considerable parasitic DC resistance of the inductor, the heating issue can be resolved at the same time as the power efficiency is improved, which was discussed with buck and buck-boost converters with ETMs as examples. Moreover, the buck-boost converter with ETM has continuous output delivery current, resulting in much smaller output voltage ripple than that of a conventional buck-boost converter. Also, a multi-phase converter and single-inductor multiple-output converter with several ETMs were proposed and simulated. The multi-phase converter with ETM offered the additional advantage of separating the switching frequency between the input frequency and the output frequency to further reduce the output ripple voltage. Additionally, the SIMO converter with ETM achieved a small output voltage ripple, similar to that of a buck-boost converter with ETM, due to the continuous output delivery current. In summary, the ETM can be implemented easily by combining with conventional topologies, and it has several merits such as reduced inductor current, small output voltage ripple, and independent frequency control. The proposed ETM can be applied to various non-isolated topologies as a promising solution for use in heavy load conditions with a small inductor.

Funding: This research received no external funding.

Conflicts of Interest: The author declares no conflicts of interest.

References

1. Carroll, A.; Heiser, G. An analysis of power consumption in a smartphone. In Proceedings of the 2010 USENIX Conference on USENIX Annual Technical Conference, Boston, MA, USA, 23–25 June 2010.
2. Lee, I.; Lee, Y.; Sylvester, D.; Blaauw, D. Battery Voltage Supervisors for Miniature IoT Systems. *IEEE J. Solid-State Circuits* **2016**, *51*, 2743–2756. [\[CrossRef\]](#)
3. Hella, M.M.; Mercier, P.P. *Power Management Integrated Circuits*, 1st ed.; CRC Press Publishers: Boca Raton, FL, USA, 2016.
4. Erickson, R.W.; Maksimović, D. *Fundamentals of Power Electronics*, 2nd ed.; Kluwer Academic Publishers: Norwell, MA, USA, 2001.
5. Park, J.; Ko, W.-J.; Kang, D.-S.; Lee, Y.; Chun, J.-H. An Output Capacitor-Less Low-Dropout Regulator with 0–100 mA Wide Load Current Range. *Energies* **2019**, *12*, 211. [\[CrossRef\]](#)
6. Hazucha, P.; Karnik, T.; Bloechel, B.A.; Parsons, C.; Finan, D.; Borkar, S. Area-Efficient Linear Regulator with Ultra-Fast Load Regulation. *IEEE J. Solid-State Circuits* **2005**, *40*, 933–940. [\[CrossRef\]](#)
7. Milliken, R.J.; Silva-Martinez, J.; Sanchez-Sinencio, E. Full On-Chip CMOS Low-Dropout Voltage Regulator. *IEEE Trans. Circuits Syst. I* **2007**, *54*, 1879–1890. [\[CrossRef\]](#)
8. Guo, J.; Leung, K.N. A 6-WChip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology. *IEEE J. Solid-State Circuits* **2010**, *45*, 1896–1905. [\[CrossRef\]](#)
9. Seeman, M.D.; Sanders, S.R. Analysis and optimization of switched-capacitor DC-DC converters. *IEEE Trans. Power Electron.* **2008**, *23*, 841–851. [\[CrossRef\]](#)
10. Le, H.P.; Sanders, S.R.; Alon, E. Design Technique for fully integrated Switched-Capacitor DC-DC Converters. *IEEE J. Solid-State Circuits* **2011**, *46*, 2120–2131. [\[CrossRef\]](#)
11. Bang, S.; Blaauw, D.; Sylvester, D. A Successive-Approximation Switched-Capacitor DC–DC Converter with Resolution of $V_{IN}/2N$ for a Wide Range of Input and Output Voltages. *IEEE J. Solid-State Circuits* **2016**, *51*, 543–556.
12. Saif, H.; Lee, Y.; Lee, H.; Kim, M.; Khan, M.B.; Chun, J.-H.; Lee, Y. A Wide Load Current and Voltage Range Switched Capacitor DC–DC Converter with Load Dependent Configurability for Dynamic Voltage Implementation in Miniature Sensors. *Energies* **2018**, *11*, 3092. [\[CrossRef\]](#)
13. Chiang, C.; Chen, C. Zero-Voltage-Switching Control for a PWM Buck Converter Under DCM/CCM Boundary. *IEEE Trans. Power Electron.* **2009**, *24*, 2120–2212. [\[CrossRef\]](#)
14. Suh, J.; Seok, J.; Kong, B. A Fast Response PWM Buck Converter with Active Ramp Tracking Control in Load Transient period. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *66*, 467–471. [\[CrossRef\]](#)
15. Calderón, A.; Vinagre, B.; Feliu, V. Fractional order control strategies for power electronic buck converters. *Signal Process.* **2006**, *86*, 2803–2819. [\[CrossRef\]](#)
16. Suh, J.-D.; Yun, Y.-H.; Kong, B.-S. High-Efficiency DC–DC Converter with Charge-Recycling Gate-Voltage Swing Control. *Energies* **2019**, *12*, 899. [\[CrossRef\]](#)
17. Abdulslam, A.; Mohammad, B.; Ismail, M.; Mercier, P.; Ismail, Y. A 93% Peak Efficiency Fully-Integrated Multilevel Multistate Hybrid DC–DC Converter. *IEEE Trans. Circuits Syst. I* **2018**, *65*, 2617–2630. [\[CrossRef\]](#)
18. Kim, W.; Brooks, D.; Wei, G.-Y. A fully-integrated 3-level DC-DC converter for nanosecond-scale DVFS. *IEEE J. Solid-State Circuits* **2012**, *47*, 206–219. [\[CrossRef\]](#)
19. Li, P.; Xue, L.; Hazucha, P.; Karnik, T.; Bashirullah, R. A delay-locked loop synchronization scheme for high-frequency multiphase hysteretic DC-DC converters. *IEEE J. Solid-State Circuits* **2009**, *44*, 3131–3145. [\[CrossRef\]](#)
20. Abedinpour, S.; Bakkaloglu, B.; Kiaei, S. A Multistage Interleaved Synchronous Buck Converter with Integrated Output Filter in 0.18 μm SiGe Process. *IEEE Trans. Power Electron.* **2007**, *22*, 2164–2175. [\[CrossRef\]](#)
21. Huang, C.; Mok, P.K.T. A 100 MHz 82.4% Efficiency Package-Bondwire Based Four-Phase Fully-Integrated Buck Converter with Flying Capacitor for Area Reduction. *IEEE J. Solid-State Circuits* **2013**, *48*, 2977–2988. [\[CrossRef\]](#)
22. Rodić, M.; Milanović, M.; Truntić, M.; Ošljaj, B. Switched-Capacitor Boost Converter for Low Power Energy Harvesting Applications. *Energies* **2018**, *11*, 3156. [\[CrossRef\]](#)

23. Tran, V.-T.; Nguyen, M.-K.; Choi, Y.-O.; Cho, G.-B. Switched-Capacitor-Based High Boost DC-DC Converter. *Energies* **2018**, *11*, 987. [[CrossRef](#)]
24. Ju, Y.; Shin, S.; Huh, Y.; Park, S.; Bang, J.; Kim, K.; Choi, S.; Lee, J.; Cho, G. A hybrid inductor-based flying-capacitor-assisted step-up/step-down DC-DC converter with 96.56% efficiency. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 184–185.
25. Liu, W.; Assem, P.; Lei, Y.; Hanumolu, P.K.; Pilawa-Podgurski, R. A 94.2%-peak-efficiency 1.53A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65nm CMOS. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 182–183.
26. Ko, M.; Kim, K.; Woo, Y.; Shin, S.; Han, H.; Huh, Y.; Kang, G.; Cho, J.; Lim, S.; Park, S.; et al. A 97% high-efficiency 6 μ s fast-recovery-time buck-based step-up/down converter with embedded 1/2 and 3/2 charge-pumps for li-ion battery management. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 428–430.
27. Shin, S.; Huh, Y.; Ju, Y.; Choi, S.; Shin, C.; Woo, Y.; Choi, M.; Park, S.; Sohn, Y.; Ko, M.; et al. A 95.2% efficiency dual-path DC-DC step-up converter with continuous output current delivery and low voltage ripple. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 430–432.
28. Huh, Y.; Shin, S.; Hong, S.; Woo, Y.; Ju, Y.; Choi, S.; Cho, G. A Hybrid Dual-Path Step-Down Converter with 96.2% Peak Efficiency Using a 250m Ω Large-DCR Inductor. In Proceedings of the 2018 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA, 18–22 June 2018; pp. 225–226.
29. Wang, S.; Woo, Y.; Yuk, Y.; Lee, B.; Cho, G.; Cho, G. Efficiency enhanced Single-Inductor Boost-Inverting Flyback converter with Dual Hybrid Energy transfer media and a Bifurcation Free Comparator. In Proceedings of the 2010 Proceedings of ESSCIRC, Seville, Spain, 14–16 September 2010; pp. 450–453.
30. Wang, S.; Woo, Y.; Yuk, Y.; Cho, G.; Cho, G. High efficiency Single-Inductor Boost/Buck Inverting Flyback converter with hybrid energy transfer media and multi level gate driving for AMOLED panel. In Proceedings of the 2010 Symposium on VLSI Circuits, Honolulu, HI, USA, 16–18 June 2010; pp. 59–60.
31. Dongsheng, M.; Wing-Hung, K.; Chi-Ying, T. A pseudo-CCM/DCM SIMO switching converter with freewheel switching. *IEEE J. Solid-State Circuits* **2003**, *38*, 1007–1014. [[CrossRef](#)]
32. Lu, D.; Qian, Y.; Hong, Z. 4.3 An 87%-peak-efficiency DVS-capable single-inductor 4-output DC-DC buck converter with ripple-based adaptive off-time control. In Proceedings of the 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA, 9–13 February 2014; pp. 82–83.
33. Goh, T.Y.; Ng, W.T. Single Discharge Control for Single-Inductor Multiple-Output DC–DC Buck Converters. *IEEE Trans. Power Electron.* **2018**, *33*, 2307–2316. [[CrossRef](#)]

