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A Step Up/Down Power-Factor-Correction Converter with Modified Dual Loop Control

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Abstract: A step up/down AC/DC converter with modified dual loop control is proposed. The step up/down AC/DC converter features the bridgeless characteristic which can reduce bridge-diode conduction losses. Based on the step up/down AC/DC converter, a modified dual loop control scheme is proposed to achieve input current shaping and output voltage regulation. Fewer components are needed compared with the traditional bridge and bridgeless step up/down AC/DC converters. In addition, the intermediate capacitor voltage stress can be reduced. Furthermore, the top and bottom switches still have zero-voltage turn-on function during the negative and positive half-line cycle, respectively. Hence, the thermal stresses can also be reduced and balanced. Simulation and experimental results are provided to verify the validity of the proposed step up/down AC/DC converter and its control scheme.

Keywords: bridgeless; AC/DC converter; power factor correction; zero-voltage switching (ZVS)

1. Introduction

Power factor correction is very popular and necessary for modern power sources in the ac grid. It decreases line current harmonics, line losses, and increases system power capacity due to reducing system reactive power flow [1–3]. Today, boost rectifiers are the most commonly-used circuit structures implemented for power factor correction. However, some consumer electronic devices, portable devices and server power applications [4,5] require lower dc voltage level than the main ac voltage source. The dc output voltage in boost rectifiers is always higher than the peak value of the main input ac voltage. Therefore, in low dc voltage level applications, another dc-dc step-down converter is necessary that follows the boost rectifier to form a two-stage structure as shown in Figure 1. Because of the two-stage structure, power efficiency may degrade and the total number of components in the system is increased. Thus, the efficiency, cost, and volume of the two-stage power conversion system are not a good choice and need to be improved.

Step-down PFC rectifiers, such as buck converters are therefore considered. However, the buck rectifier input current is discontinuous. A dead angle also exists when the line input voltage is lower than the output voltage so that the input current cannot be easily shaped [6–8]. As a result, the step up/down AC-DC topologies are developed including buck-boost, Cuk, and Sepic type rectifiers [9–11]. The buck-boost rectifier also has inherent discontinuous input current like the buck converter, and needs an additional filter to smooth the input current. Although the Sepic rectifier has continuous input current, the output current is still discontinuous and easily causes output voltage ripples.

Bridgeless rectifier topologies are explored in [12,13] to reduce the diode bridge conduction losses and increase the conversion efficiency. The bridgeless PFC boost rectifiers, such as the dual boost rectifier and the totem-pole boost rectifier, have been discussed [14]. Due to the need for lower output voltage applications, the bridgeless Cuk/Sepic rectifiers [15,16] with two dc/dc Cuk/Sepic circuit structures were proposed. The bridgeless Cuk rectifier [16] is shown in Figure 2. However,

four diodes are still needed to achieve step up/down output voltage. Other bridgeless Sepic [17] and Cuk [18] power-factor-correction rectifiers were also proposed with reduced number of components and conduction losses. These rectifiers were operated in discontinuous conduction mode without current loop control. A control method for bridgeless Cuk/Sepic power factor correction rectifier operated in continuous conduction mode was also proposed to achieve power decoupling [19]. Although, the bulky electrolytic capacitor can be replaced with a small film capacitor, this control method requires an extra voltage sensor for the intermediate capacitor and the system cost is increased.

Pulsating power buffering technology [8,20,21] has recently expanded, which can reduce the number of components including passive and active ones. Although rectifiers using pulsating power buffering technology have high power density, high conversion efficiency and high reliability, high voltage stress is still present in the switches and diodes [22], which leads to high switching and conduction losses and reduces the rectifier life-span.

This paper proposes a bridgeless Cuk rectifier with modified dual loop control scheme. The voltage stresses in the switches and diodes can be adjusted to low voltage levels by the proposed control scheme, which may reduce the switching and conduction losses and increase the rectifier life-span. The detailed operation principle and switching sequence of the bridgeless Cuk rectifier are explained. Simultaneously, a modified dual loop control scheme is also proposed to achieve input current shaping and output voltage regulation as well as voltage stress reduction.

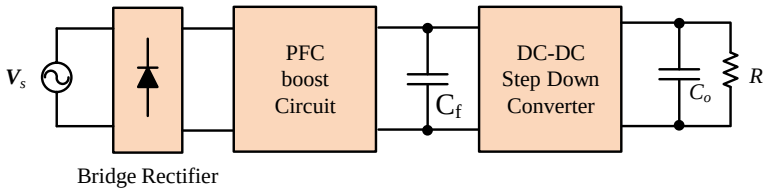

Figure 1. Two-stage AC/DC conversion structure.

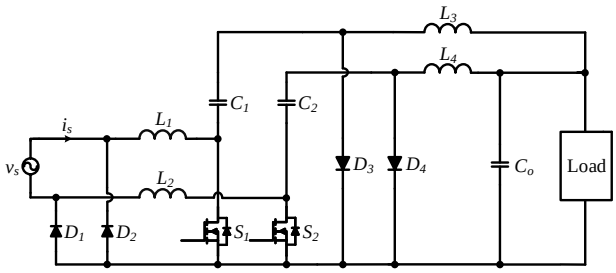

Figure 2. Bridgeless Cuk rectifier [16].

2. Circuit Topology and Switching Sequence

The bridgeless Cuk converter [19] discussed in this paper is shown in Figure 3. The proposed control switching sequence and key waveforms in one switching period during the positive and negative half line cycle are shown in Figure 4. For convenience of discussion the active switches are assumed to be ideal active switches with anti-paralleling body diode. Both the input inductor L_s and output inductor L_o are assumed to be operated in continuous conduction mode. The circuit operation can be divided into three operation states in one switching period T for both positive and negative half-line cycles. The circuit operation principle of the bridgeless Cuk converter during the positive half-line cycle is discussed first, as follows:

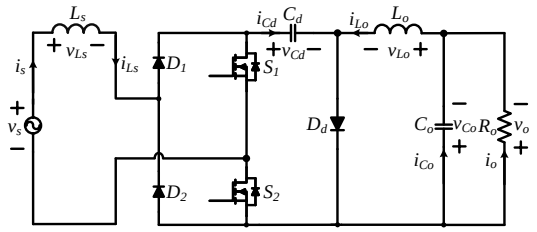

Figure 3. Bridgeless Cuk converter [19].

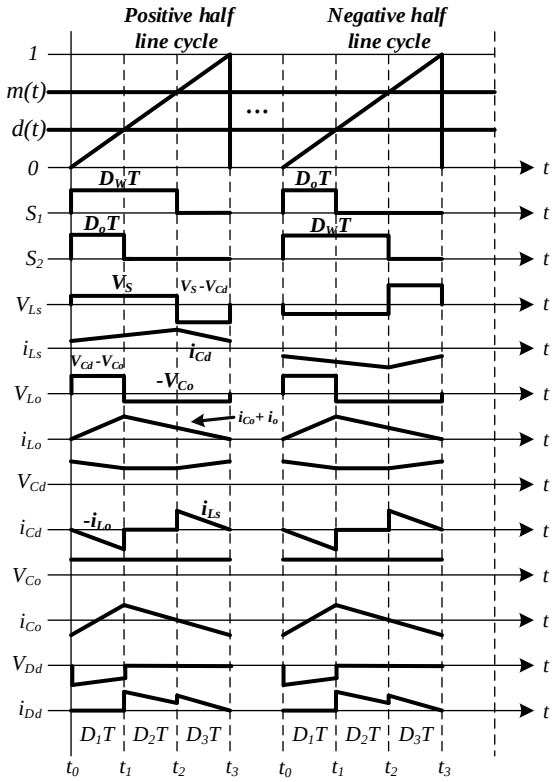

Figure 4. Control switching sequence and key waveforms in one switching period.

(1) State 1 ($t_0 \le t < t_1$): In this state, as shown in Figure 5, both switches S_1 and S_2 are turned on. The zero-voltage switching of S_2 is obtained due to body diode conducting in switch S_2 in the pre-state, i.e., State 3. The input inductor L_s is magnetized by the input voltage V_s so as to increase the inductor current i_{Ls}. The inductor current i_{Ls} flows through diode D_1 and switch S_1 and goes back to the main ac source. Simultaneously, the intermediate capacitor C_d releases energy to the output inductor L_o and load. The equivalent circuit equations are described as Equations (1)–(4).

$$L_s \frac{di_{Ls}}{dt} = v_s, \tag{1}$$

$$L_o \frac{di_{Lo}}{dt} = v_{Cd} - v_o, \tag{2}$$

$$C_d \frac{dv_{Cd}}{dt} = -i_{Lo}, \tag{3}$$

$$C_o \frac{dv_o}{dt} = i_{Lo} - \frac{v_o}{R_o}, \tag{4}$$

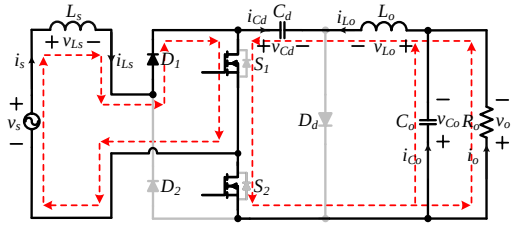

Figure 5. Equivalent circuit of the bridgeless Cuk converter in State 1 during positive half line cycle.

(2) State 2 ($t_1 \leq t < t_2$): In this state, as shown in Figure 6, switch S_1 is turned on and switch S_2 is turned off. Switch current i_{ds1} is increasing. Input inductor L_s is still magnetized by the input voltage V_s so as to increase the inductor current i_{Ls} which still flows through diode D_1 and switch S_1 and then goes back to the main ac source. The voltage of intermediate capacitor C_d remains constant. Simultaneously, the output inductor L_o is demagnetized and releases energy to the load through the diode D_d. The equivalent circuit equations are expressed as Equations (5)–(8).

$$L_s \frac{di_{Ls}}{dt} = v_s, \tag{5}$$

$$L_o \frac{di_{Lo}}{dt} = -v_o, \tag{6}$$

$$C_d \frac{dv_{Cd}}{dt} = 0, \tag{7}$$

$$C_o \frac{dv_o}{dt} = i_{Lo} - \frac{v_o}{R_o}, \tag{8}$$

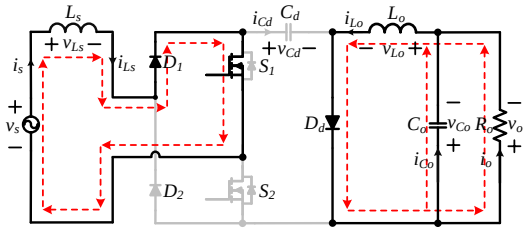

Figure 6. Equivalent circuit of the bridgeless Cuk converter in State 2 during positive half line cycle.

(3) State 3 ($t_2 \leq t < t_3$): In this state, as shown in Figure 7, switch S_1 is turned off and S_2 is also turned off. Input inductor L_s is demagnetized by the voltage $-(V_{cd}-V_s)$ so as to decrease the inductor current i_{Ls} which flows through diodes D_1 and D_d, and the body diode of switch S_2 and goes back to the main ac source. The intermediate capacitor C_d is charged by the input inductor current i_{Ls}. Simultaneously, the output inductor L_o still releases energy to the load through diode D_d. The equivalent circuit equations are given by Equations (9)–(12).

$$L_s \frac{di_{Ls}}{dt} = v_s - v_{Cd}, \tag{9}$$

$$L_o \frac{di_{Lo}}{dt} = -v_o, \tag{10}$$

$$C_d \frac{dv_{Cd}}{dt} = i_{Ls}, \tag{11}$$

$$C_o \frac{dv_o}{dt} = i_{Lo} - \frac{v_o}{R_o}, \tag{12}$$

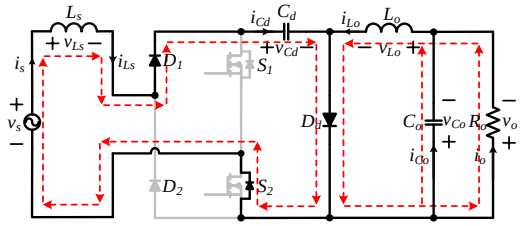

Figure 7. Equivalent circuit of the bridgeless Cuk converter in State 3 during positive half line cycle.

Referring the gate signals shown in Figure 4, while the bridgeless Cuk converter is operated during the negative half line cycle, the circuit operation principle in the proposed control switching sequence can be described as follows:

(1) State 1 ($t_0 \leq t < t_1$): In this state, as shown in Figure 8, both the switches S_1 and S_2 are turned on. The zero-voltage switching of S_1 is obtained due to body diode conducting in switch S_1 in the pre-state, i.e., State 3. The input inductor L_s is magnetized by the input voltage V_s so as to increase the inductor current i_{Ls} in the inverse direction. The inductor current i_{Ls} flows through diode D_2 and switch S_2 and goes back to the main ac source. Simultaneously, the intermediate capacitor C_d releases energy to the output inductor L_o and load. The equivalent circuit equations are described as Equations (13)–(16).

$$L_s \frac{di_{Ls}}{dt} = v_s, \tag{13}$$

$$L_o \frac{di_{Lo}}{dt} = v_{Cd} - v_o, \tag{14}$$

$$C_d \frac{dv_{Cd}}{dt} = -i_{Lo}, \tag{15}$$

$$C_o \frac{dv_o}{dt} = i_{Lo} - \frac{v_o}{R_o}, \tag{16}$$

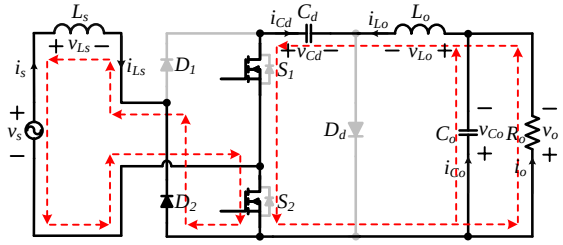

Figure 8. Equivalent bridgeless Cuk converter circuit in State 1 during negative half line cycle.

(2) State 2 ($t_1 \leq t < t_2$): In this state, as shown in Figure 9, switch S_2 is turned on and switch S_1 is turned off. The switch current i_{ds2} is increasing. Input inductor L_s is still magnetized by the input voltage V_s so as to increase the inductor current i_{Ls} in the inverse direction which still flows through diode D_2 and switch S_2 and then goes back to the main ac source. The intermediate capacitor C_d voltage remains constant. Simultaneously, the output inductor L_o is demagnetized and releases energy to the load through diode D_d. The equivalent circuit equations are expressed as Equations (17)–(20).

$$L_s \frac{di_{Ls}}{dt} = v_s, \tag{17}$$

$$L_o \frac{di_{Lo}}{dt} = -v_o, \tag{18}$$

$$C_d \frac{dv_{Cd}}{dt} = 0, \tag{19}$$

$$C_o \frac{dv_o}{dt} = i_{Lo} - \frac{v_o}{R_o}, \tag{20}$$

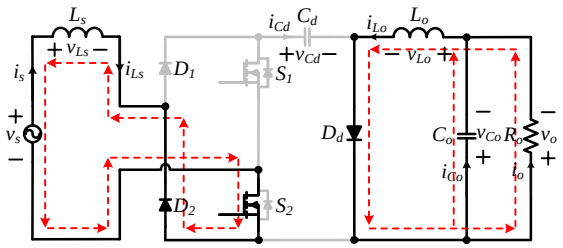

Figure 9. Equivalent circuit of the bridgeless Cuk converter in State 2 during negative half line cycle.

(3) State 3 ($t_2 \leq t < t_3$): In this state, as shown in Figure 10, switch S_2 is turned off and S_1 is also turned off. Input inductor L_s is demagnetized in the inverse direction by the voltage ($V_{cd} + V_s$) so as to decrease the inductor current i_{Ls} which flows through diodes D_2, D_d and the body diode of switch S_1 and goes back to the main ac source. The intermediate capacitor C_d is charged by the input inductor current i_{Ls} in the inverse direction. Simultaneously, the output inductor L_o still releases energy to the load through diode D_d. The equivalent circuit equations are given by Equations (21)–(24).

$$L_s \frac{di_{Ls}}{dt} = v_s + v_{Cd}, \tag{21}$$

$$L_o \frac{di_{Lo}}{dt} = -v_o, \tag{22}$$

$$C_d \frac{dv_{Cd}}{dt} = -i_{Ls}, \tag{23}$$

$$C_o \frac{dv_o}{dt} = i_{Lo} - \frac{v_o}{R_o}, \tag{24}$$

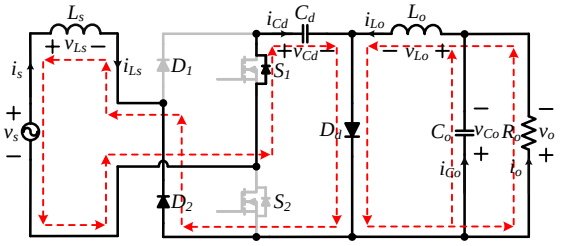

Figure 10. Equivalent circuit of the bridgeless Cuk converter in State 3 during negative half line cycle.

To further reveal the potential merits of the proposed step up/down converter with modified dual loop control, Table 1 is provided to summarize comparisons for the bridge Cuk [11], bridgeless Cuk [16], and the proposed step up/down converter with modified dual loop control. It is worth mentioning that the power levels of the three converters in Table 1 are all at small power levels like the fly-back converter. Although the control methods may be different, the harmonics of the three converters all meet the IEC61000-3-2 Class D standard.

Table 1. Comparisons of step up/down converters.

Topology	Bridge Cuk [11]	Bridgeless Cuk [16]	Proposed Step Up/Down Converter with Control
Control	Dual Loop	Dual Loop	Modified Dual Loop
Switch	1	2	2
Diode	5	4	3
Inductor	2	4	2
Capacitor	2	3	2
Total Number of Components	10	13	9
Voltage Gain	$\frac{v_o}{\lvert v_s \rvert} = \frac{D}{(1-D)}$	$\frac{v_o}{\lvert v_s \rvert} = \frac{D}{(1-D)}$	$\frac{v_o}{\lvert v_s \rvert} = \frac{D_o}{(1-D_w)}$
Voltage stresses of switches	v_o/D	v_o/D	v_o/D_o
D or D_o	one solution	one solution	Multiple solutions
Harmonics	meet the standard	meet the standard	meet the standard

3. Control Scheme and Parameter Design

3.1. Control Scheme

According to the circuit analysis in the previous section, assume the duty ratio $D_W = D_1 + D_2$ and $D_0 = D_1$. While the main ac voltage is operating in the positive half line cycle $v_s > 0$, by utilizing state-space averaged technique and flux balance theory in the input inductor L_s and output inductor L_o, one can obtain the equations

$$v_{Cd} = \frac{v_S}{(1 - D_W)}, \tag{25}$$

$$v_{Cd} = \frac{v_o}{D_o}, \tag{26}$$

Similarly, while the main ac voltage is operating in the negative half line cycle $v_s < 0$, the corresponding symmetrical equations can also be obtained as

$$v_{Cd} = \frac{-v_S}{(1 - D_W)}, \tag{27}$$

$$v_{Cd} = \frac{v_o}{D_o}, \tag{28}$$

Merging Equations (25)–(28) in both the positive and negative half line cycles of the main ac voltage, the voltage gain of the bridgeless Cuk converter is obtained as

$$\frac{v_o}{|v_S|} = \frac{D_o}{(1 - D_W)}, \tag{29}$$

As can be observed from Equation (29), the output voltage is related to the two parameters D_o and D_W. If the input and output voltages are given, infinite different kinds of solutions exist in the Equation (29). However, in the same operation condition for the conventional dual loop control scheme shown in Figure 11, only one solution is obtained, i.e., $D_o = D_W$. Therefore, in order to reduce the voltage stresses of all switches and diodes in the circuit, the conventional dual loop control scheme is not suitable.

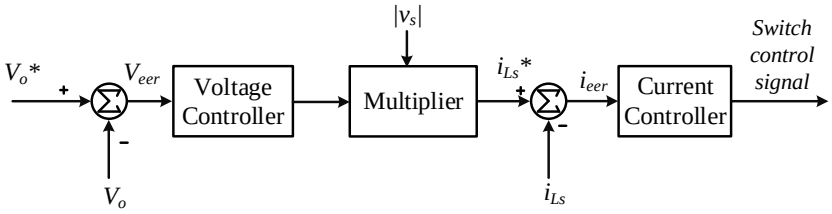

Figure 11. Conventional dual loop control scheme.

A modified dual loop control scheme is proposed. The proposed control scheme for the bridgeless Cuk converter is shown in Figure 12. The actual input current i_{Ls} compared with the current command i_{Ls}* to generate the current error as the input of the current controller and then produce the control signal V_{Dw}. The actual output voltage V_o compared with the output voltage command V_o* generates the voltage error as the voltage controller input. The voltage controller generates the current command amplitude and also the control signal V_{Do}. In the conventional dual loop control scheme, only one control signal is produced to achieve both input current shaping and output voltage regulation. In the proposed control scheme, two control signals V_{Dw} and V_{Do} are produced to control the input current shaping and output voltage regulation. Thus, the intermediate capacitor voltage is not fixed and can be adjusted to fit a better low voltage level. Hence, the intermediate capacitor voltage stress could be reduced and the adopted electrolytic capacitor life span could also be increased. According to the circuit analysis in Section 2, the voltage stresses of active switches S_1 and S_2, diodes D_1, D_2, and D_d are clamped and equal to the intermediate capacitor voltage. The average switching power loss P_s in one switching period caused by transitions can be defined as

$$P_s = 0.5 V_{DS} I_{DS} [t_{c(on)} + t_{c(off)}], \tag{30}$$

where $t_{c(on)}$ and $t_{c(off)}$ are the turn-on and turn-off crossover intervals, respectively. For simplification, the switches are operated in the same turn-on and turn-off crossover intervals and at the same switching frequency f_s. The average switching power loss is then proportional to the voltage across the switch V_{DS} and the entire current I_{DS} which flows through the switch as

$$P_s \propto V_{DS} I_{DS}, \tag{31}$$

According to the above equation, if the intermediate capacitor voltage is adjusted to fit a better low voltage level, the average switching power loss is also reduced. This is also true for the diodes. Therefore, the total losses in semiconductor devices can be reduced and the efficiency can be lifted.

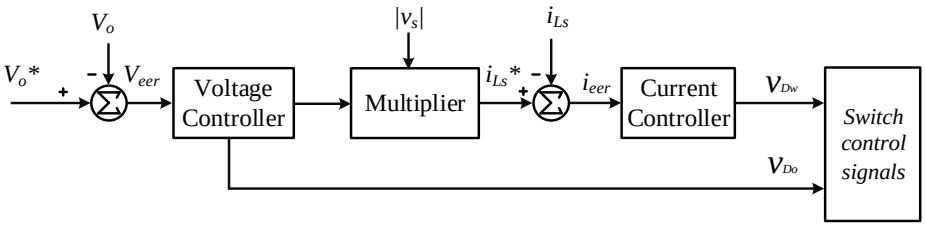

Figure 12. Proposed modified dual loop control scheme.

3.2. Parameter Design

To verify the feasibility of the proposed step up/down AC/DC converter with modified dual loop control, a parameter design for inductor and capacitor is discussed. In order to find the boundary between the continuous and discontinuous modes for input inductor L_s, one can find that the critical value of K_1 at boundary between modes, $K_{crit}(D_w)$, is function of duty cycle D_w and can be expressed as

$$K_1 > K_{crit}(D_w), \text{ where } K_1 = \frac{2L_s}{R_o T_s} \text{ and } K_{crit}(D_w) = \frac{(1 - D_w)^2}{D_w} \tag{32}$$

The critical value K_{cirt} (D_w) is plotted vs. duty cycle D_w in Figure 13. Consider inductor L_s is operated in CCM and the switching frequency is f_s. The maximum input current ripple is less than 25% of the fundamental current. The minimum input inductor L_s value can be derived by the equation

$$L_s \geq \frac{v_{s,\max}}{0.25 \cdot \Delta i_{Ls,BCM}} \cdot \frac{D_W}{f_s}, \tag{33}$$

where $\Delta i_{Ls,BCM}$ is the input current ripple while inductor L_1 is operated in BCM. Consider that inductor L_o is operated in BCM and one can find that the critical value for K_2 at the boundary between modes, $K_{crit}(D_o)$, is function of the duty cycle D_o and can be expressed as

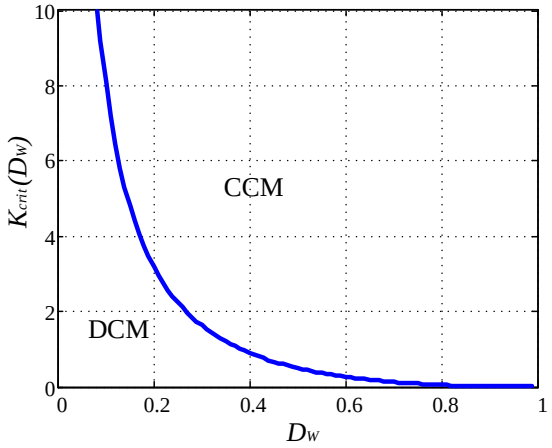

Figure 13. Proposed step up/down AC/DC converter K_{cirt} (D_w) vs. D_w.

$$K_2 > K_{crit}(D_o), \text{ Where } K_2 = \frac{2L_o}{R_o T_s} \text{ and } K_{crit}(D_o) = \frac{1 - D_o}{2} \tag{34}$$

The critical value K_{cirt} (D_o) is plotted vs. duty cycle D_o in Figure 14. Similarly, the minimum value of inductor *Lo* also can be derived as

$$L_o \geq \frac{v_{Cd,\max}}{\Delta i_{Lo,BCM}} \cdot \frac{D_o}{f_s}, \tag{35}$$

where $\Delta i_{Lo,BCM}$ is the output current ripple while inductor L_o is operated in BCM.

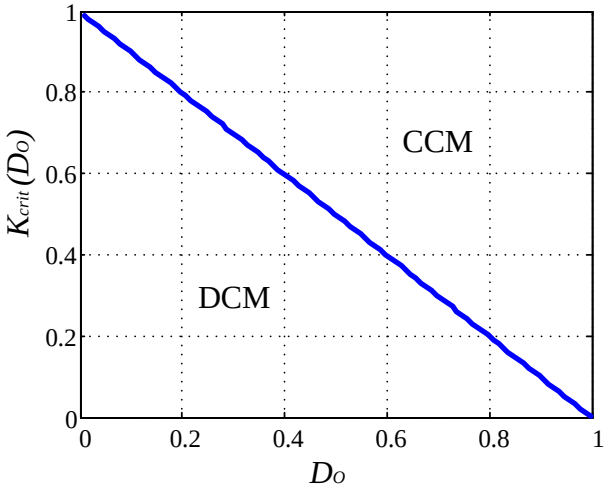

Figure 14. Proposed step up/down AC/DC converter K_{cirt} (D_o) vs. D_o.

Consider the output capacitor and assume the switching ripple is neglected. The output capacitor must be large enough to minimize the output ripple because the output voltage ripple frequency is twice the input line frequency. The output filter capacitor can be determined by

$$C_o = \frac{P_o}{\omega V_o (2\Delta V_o)}, \tag{36}$$

where ΔV_o is the output voltage ripple and ω is the input line angular frequency.

4. Simulation and Experimental Results

To verify the validity of the bridgeless step up/down AC/DC converter, some simulation results are executed and a prototype system is constructed to facilitate the theoretical results as verification. The simulation and experimental parameters are listed in Table 2. The input voltage is the AC grid with 110 V_{rms} and 60 Hz fundamental frequency. The controlled output voltage is 48 V and the load is 48 Ω. The assigned output power rating is 48 W. The simulation results for the input voltage V_s, input current i_s and the corresponding intermediate capacitor voltage V_{cd} are shown in Figure 15. It follows from Figure 15 that the input current shaping can be achieved. Figure 16 shows the switching control signals for switch S_1 and S_2 and the corresponding voltage and current of switch S_2 during the positive half-line cycle. As can be seen from Figure 16, the ZVS turn-on of switch S_2 is obtained during the positive half-line cycle. Similarly, Figure 17 shows the switching control signals for switch S_1 and S_2 and the corresponding voltage and current of switch S_1 during the negative half-line cycle. It also can be seen from Figure 17 that the ZVS turn-on of switch S_1 is obtained during the negative half-line cycle.

Consider that the load is a dynamic load and/or RL load such as a dc motor whose armature winding resistance is Ra = 0.5 Ω, armature winding inductance is La = 0.5 mH, back electromotive force is 47 V. Figure 18 shows the simulation results for the input voltage, input current and the corresponding intermediate capacitor voltage. As can be observed from Figure 18, the output power is about 120 W and the power factor correction is also achieved. Hence, the proposed converter can indeed be operated in the RL load. Consider the intermediate capacitor voltage which can be adjusted using the control signal V_{Do} based on Equations (26) and (28). Figure 19 shows the simulation results for the input voltage and the corresponding input current, and the control signal V_{Do} and the corresponding intermediate capacitor voltage V_{Cd} under the low control signal V_{Do} value. Figure 20 shows the same simulated condition under the high control signal V_{Do} value. It can be seen from Figures 19 and 20 that the lower the control signal V_{Do} value, the higher the intermediate capacitor voltage V_{Cd}. That the duty ratio Do affects the intermediate capacitor voltage level and also the voltage stresses of the switches and diodes in the circuit is very important information. This also implies that the duty ratio Do affects the converter power losses and efficiency. Finally, to facilitate understanding of the proposed step up/down converter with modified dual loop control and as verification, a prototype is constructed with a TMS320F28335 digital signal processor (DSP). The experimental hardware construction block diagram is shown in Figure 21. Figures 22 and 23 show the experimental results for the switching control signals and the corresponding voltage and current of switches S_2 and S_1 during positive and negative half-line cycles, respectively. As can be observed from Figures 22 and 23, the ZVS soft switching of switches S_2 and S_1 were indeed achieved and agreed with the simulation results. The measured harmonic distribution of the input current is shown in Figure 24. One can find that the measured harmonic currents meet the IEC 61000-3-2 Class D harmonic standards.

In order to understand the total harmonic distortion THD_i of the input currents in the three converters listed in Table 1, the PSIM software is adopted to carry out the simulation. The input voltage is 110Vrms, the output voltage is controlled at 48 V and the load is 2 A. The corresponding parameters and simulated results are shown in Table 3. As can be seen from Table 3, the input current THD_i of the bridge Cuk [11] is better than that of the bridgeless Cuk [16] and the proposed Cuk with modified dual loop control scheme. Nevertheless, the parameter value of the bridge Cuk input inductor [11] is larger than those for the other two. Although the bridge Cuk [11] has the smallest input current THD_i, the input inductor may make it appear bulky.

Table 2. Parameters of the bridgeless Cuk converter for simulation and experimentation.

Parameters	Value
Input Inductor L_s	1.5 mH
Output Inductor L_o	50 uH
Intermediate Capacitor C_d	5 uF
Output Capacitor C_o	470 uF
Switching frequency f_s	50 kHz

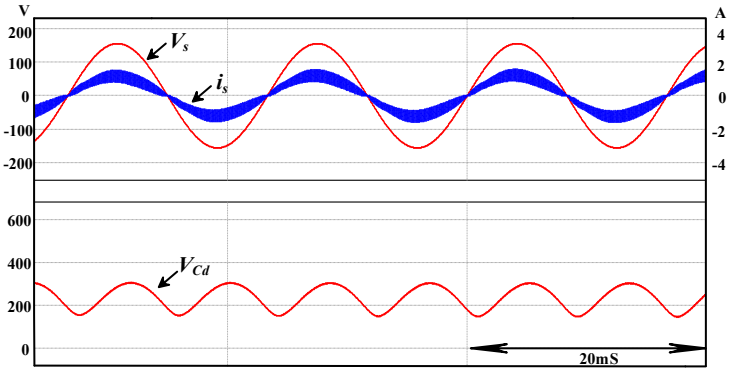

Figure 15. Simulation results for (top) the input voltage V_s, current i_s, and (bottom) corresponding intermediate capacitor voltage.

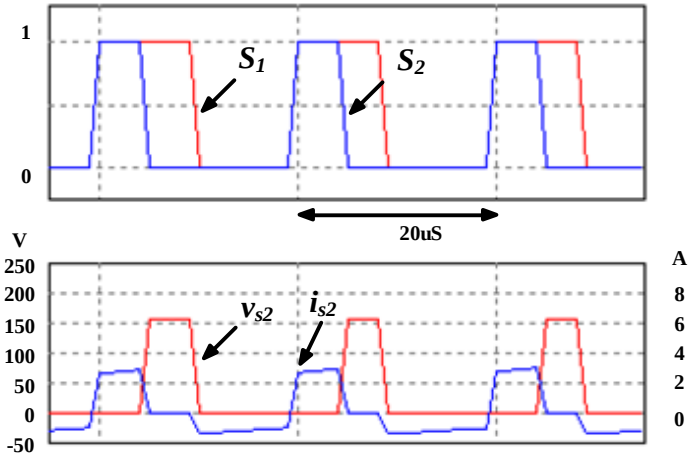

Figure 16. Simulation results for (top) switching control signals and (bottom) corresponding voltage and current of switch S_2 during positive half line cycle.

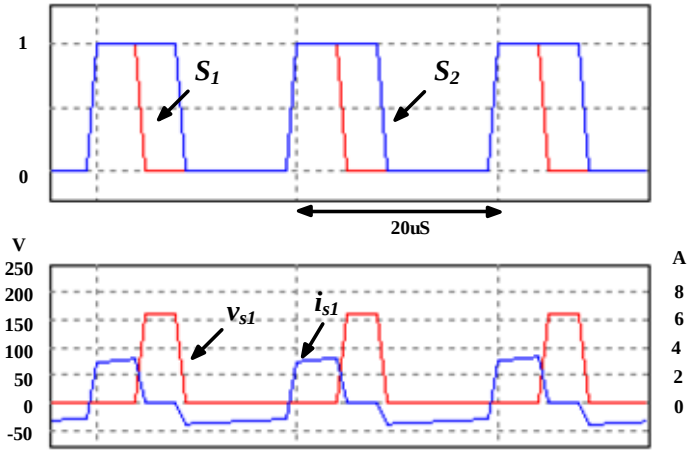

Figure 17. Simulation results for (top) switching control signals and (bottom) corresponding voltage and current of switch S_1 during negative half line cycle.

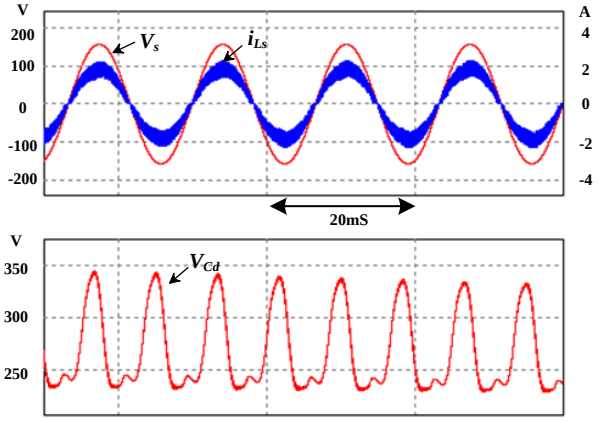

Figure 18. Simulation results for (top) the input voltage V_s, current i_s, and (bottom) corresponding intermediate capacitor voltage while the load is a dc motor.

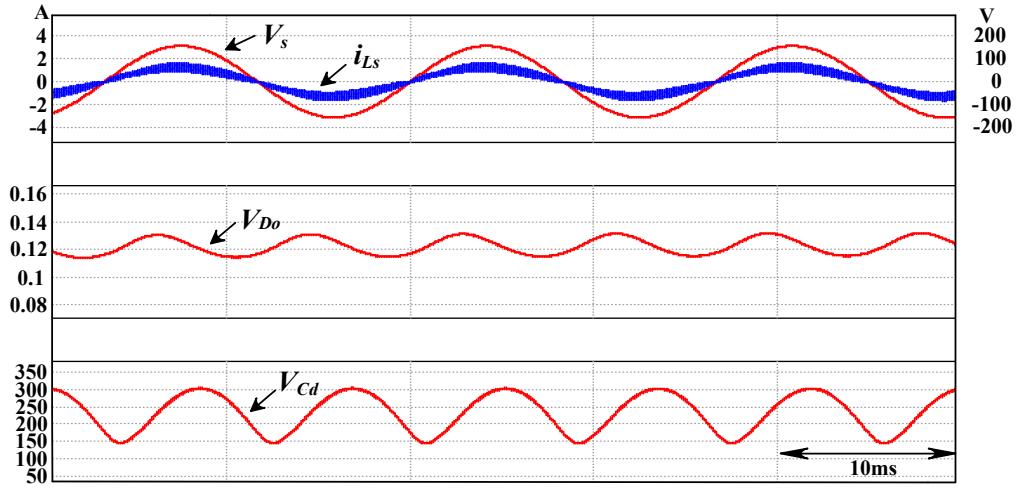

Figure 19. Simulation results for (top) the input voltage V_s, current i_s, (middle) the control signal V_{Do} with low parameter value, and (bottom) corresponding intermediate capacitor voltage.

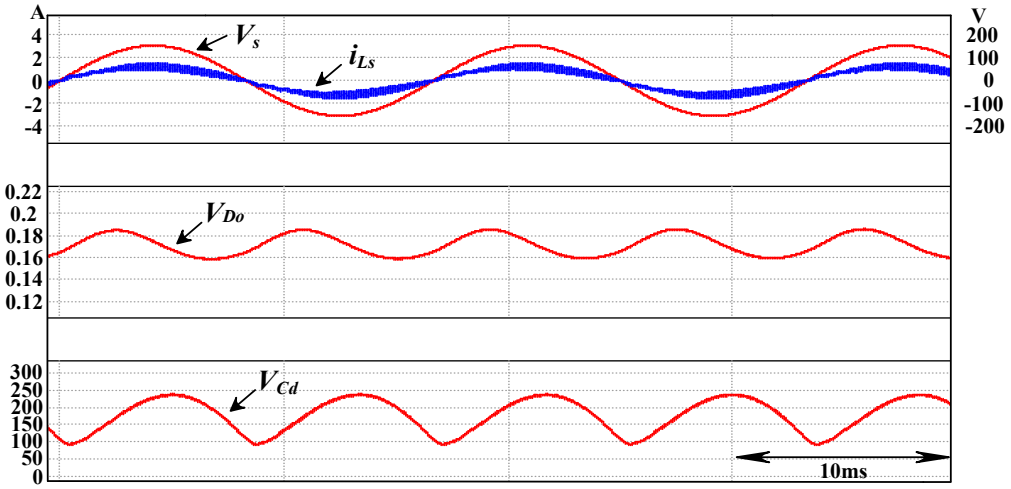

Figure 20. Simulation results for (top) the input voltage V_s, current i_s, (middle) the control signal V_{Do} with high parameter value, and (bottom) corresponding intermediate capacitor voltage.

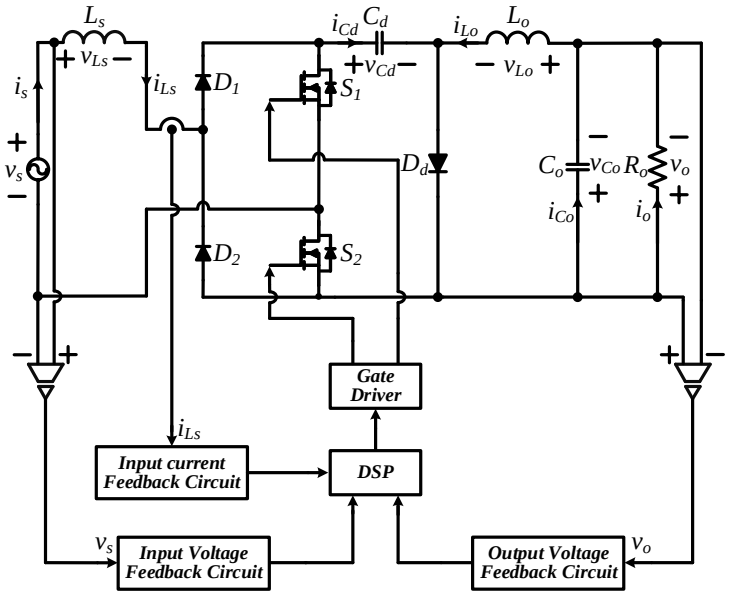

Figure 21. Experimental hardware construction block diagram.

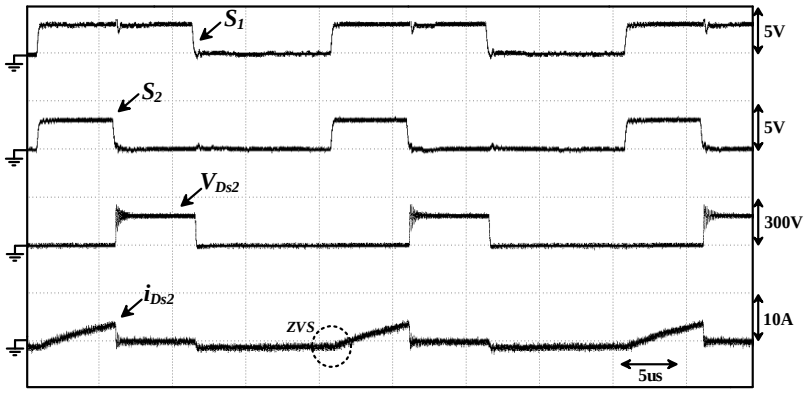

Figure 22. Experimental results for (top) switching control signals S_1, S_2 and (bottom) corresponding voltage and current of switch S_2 during positive half line cycle.

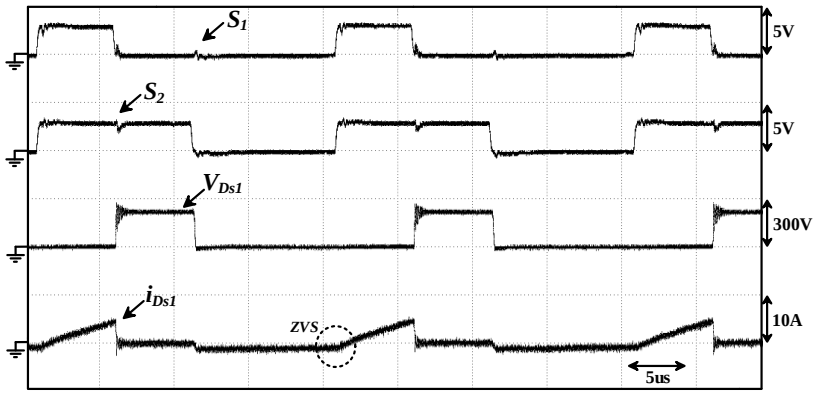

Figure 23. Experimental results for (top) switching control signals S_1, S_2 and (bottom) corresponding voltage and current of switch S_1 during negative half line cycle.

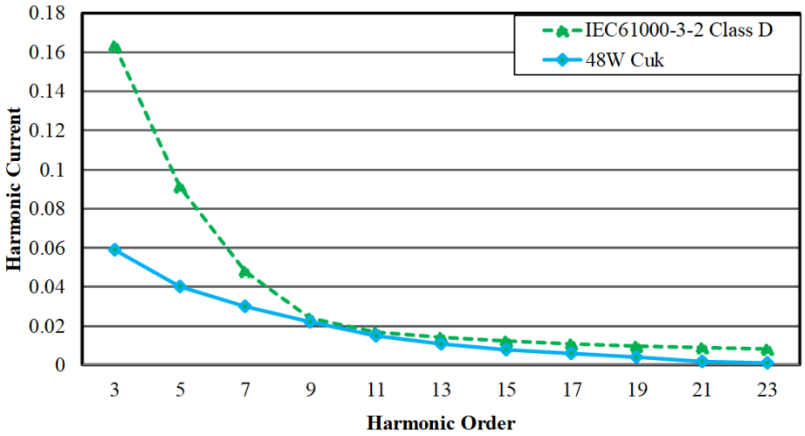

Figure 24. The measured harmonic distribution of the input current compared with IEC61000-3-2 Class D standard.

Table 3. Comparisons of the total harmonic distortion of the step up/down converters.

Parameters	Bridge Cuk [11]	Bridgeless Cuk [16]	Proposed Step Up/Down Converter with Control
Input inductor	6.4 mH	1mH × 2	1.5 mH
Output inductor	206 uH	22uH x 2	50 uH
Intermediate capacitor	0.61 uF	1uF x 2	5 uF
THD_i of Input current	5.6%	15.2%	13.3%

5. Conclusions

This paper presented a bridgeless step up/down converter with modified dual loop control scheme. The proposed system has ZVS soft switching in switches S_1 and S_2 during the negative and positive half-line cycle operation, respectively. Thus, the switching losses can be reduced and the thermal stress can be balanced between switches S_1 and S_2. There are fewer components compared to the bridge Cuk and the bridgeless dual Cuk configuration. Therefore, the size and cost can be reduced. In addition, based on the proposed control scheme, the voltage stresses of the intermediate capacitor, active switches, and diodes can all be reduced. To verify the validity of the proposed step up/down converter, simulation, and experimental results are offered. From simulation and experimental results, the proposed bridgeless step up/down converter can indeed achieve input current shaping and output voltage regulation as well as reduce the switching and conduction losses.

Author Contributions: The author contributed to the theoretical analysis, modeling, simulation, experiment, and manuscript preparation. The author have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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