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Multileg Interleaved Buck Converter for EV Charging: Discrete-Time Model and Direct Control Design

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Abstract: This paper presents the modeling and the implementation of the digital control of a multileg interleaved DC-DC buck converter for electrical vehicle (EV) charging. Firstly, we derive a discrete averaged model of an n-leg interleaved buck converter (IBC). Secondly, we present a direct tuning procedure for one primary discrete PIDF (PID + filter) and multiple secondary PI controller. The objective of the control system is to regulate the current flow in each leg of the converter. This task is accomplished by introducing a novel control paradigm that simultaneously addresses two aims: on the one hand, the control scheme must guarantee an acceptable level of robustness under load variations; while on the other, an even distribution of power on each leg must be ensured at any operational condition. The proposed strategy hinges on a technique that combines simplicity and precision in the fulfillment of design frequency specifications. We use simulations and a digital signal processor (DSP) based experimental implementation of the design technique to validate the proposed methodology.

Keywords: buck converter; interleaved converter; electric vehicle; phase margin; gain crossover frequency

1. Introduction

Electric vehicle (EV) technologies are facing huge developments in the last years because of their potential to reverse the carbon emissions trend and therefore to lead to a green shift in the coming years [1]. However, EV manufacturers are still addressing relevant problems such as charging times and users' range anxiety. In the field of power electronics, these targets can be achieved mainly by enhancing the performance of the power converter, and at the same time, by keeping the cost as low as possible. Electric vehicle charging facilities provided by fast charger feeders are expected to be one of the most significant players in building a reliable and efficient charging network to significantly increase range capabilities through a sharp reduction of current EVs' charging times [2]. Several configurations such as the Vienna rectifier [3], multilevel neutral point clamped (NPC) choppers [4], and interleaved converters have been proposed in the literature. Among them, the interleaved converter topology appears to fit the economic and technical constraints mentioned above. Because of its inherent modular structure, it is possible to take advantage of the low cost and highly standardized modules, while at the same time increasing the performance in terms of carried power and electric power quality. Interleaved topology is used for both AC/DC [5–7] and DC/DC [8,9] power converters. The DC/DC buck is the last active stage before the battery. It is, therefore, crucial to keep the output current (in terms of current ripple) within battery constraints. For this reason, this paper focuses on the chopper control system. One of the most well-known benefits of interleaved topology is the spontaneous output current ripple

reduction that the parallelized topology determines. In this way, no big inductors or high switching frequencies are necessary. Furthermore, the possibility to evenly assign the load among legs (phases) leads to improved heat distribution, faster dynamic response, and a higher reliability thanks to its potential redundancy [10]. However, keeping a balanced current share among the legs requires further advanced algorithms to compensate for any variations, differences, and faults in the system [11,12]. Therefore, a multitude of driving signals are involved. Despite the diffusion of non-linear control strategies, as the sliding mode or fuzzy methods, which are traditionally designed by trial-and-error, classical linear PI/PID controllers are still widely used in multi-loop structures to control multiple-input and multiple-output (MIMO) systems, see [13]. This is due to their simple structure, the capability to carry out stability, performance analysis, and comparison with other methods. For these reasons, we consider the method proposed in [13] as a benchmark for a comparison with the new control strategy developed here. Despite some other suitable EVs battery charging control strategies based on PI controllers were considered in [13], an explicit analytical designing procedure is still missing.

Several state-space models of DC/DC interleaved buck converters (IBCs) such as [14] can be found in the literature. However, as highlighted in [12], none of them use duty-cycles as input signals. Since the input voltage represents the constant bus voltage in battery charger systems, it is assumed that its value varies very slowly compared to the duty-cycle dynamics. It follows that the input voltage should be considered as a system parameter, and duty-cycles should be taken as model input. Moreover, the direct control of the duty cycles introduces a rebalancing action on each leg.

The primary purpose of this paper is to fill this gap by presenting a new discrete-time model for the interleaved buck converter. Moreover, a design procedure is delivered directly in the discrete-time, to exactly satisfy design specifications in the frequency domain, ensuring at the same time current sharing among all legs.

The state-space model of an n-leg interleaved buck converter used in this paper takes into account all the losses due to power switches, inductors' resistive component, and capacitor's equivalent series resistance (ESR). In this model, duty-cycles are considered as input signals. Finally, an exact discrete-time average model is introduced by applying the definition of the Z-transform to the continuous-time averaged model in series with the zero-order hold system. Tuning of the parameters can be carried out directly in a discrete setting, using, e.g., digital signal processors (DSPs) or microcontrollers, [15].

The strategy proposed in this paper relies on constant current charging profiles [16]. The control pattern is constituted by a "central" (primary) controller, which computes the average duty cycle on the basis of the aforementioned averaged model. The task of compensating the unbalances between one "master" leg and the remaining "slave" legs is carried out by a further group of N-1 (secondary) controllers. Although the theoretical study is carried out for N legs, the implementation in terms of simulations and measurements is evaluated on three parallel legs only. This design choice is congruent with previous considerations. Indeed, the highly standardized two-level three-phase modules can be effortlessly staked to obtain an interleaved connection and serve as a buck DC/DC converter [17,18].

Furthermore, the "master/slave" proposed strategy can be dynamically rerouted to deal with multiple three-phase modules. In this paper, the control was achieved by utilizing a discrete PIDF (PID + Filter) controller with complex conjugate zeros using the classical pole-zero cancellation method [19] combined with the so-called discrete inversion formulae introduced in [20]. As shown in [19], two parameters of the PIDF controller are used to cancel the detrimental effects of the complex poles of the converter. The inversion formulae were used to assign the values of the remaining two degrees of freedom in the parameters of the controller to satisfy standard frequency domain specifications on the phase margin and on the gain crossover frequency [21–23].

In order to overcome a converted power increase, additional legs are often introduced in the chopper stage. An increase in the number of legs typically increases the complexity of the tuning procedures of the parameters of each controller. For this reason, rules of thumb and trial-and-error methods may become inapplicable in these contexts. The approach that we propose is analytic, and therefore it is inherently not iterative. Moreover, the use of inversion formulae enables the

aforementioned frequency domain specifications to be exactly satisfied, thus ensuring not only the satisfaction of the steady-state performance, but also the shaping of the transient (avoidance of overshoot/undershoot, velocity of the convergence, etc.) and, at the same time, guarantees an acceptable level of robustness under load variations during battery charge.

The paper is organized as follows. The continuous and discrete-time models of standard multileg interleaved buck converter are presented in Section 2. In Section 3, we propose the control structure and PI/PIDF tuning procedure. Simulation results and analysis in comparison with the method introduced in [13] and results of DSP-based experimental implementation are presented in Section 4. Conclusions and possible future works finally end the paper.

2. Continuous and Discrete-Time Model of *n*-Leg Interleaved Buck Converter

Let us consider the n-leg interleaved buck converter shown in Figure 1. In this scheme, V_{in} denotes the input voltage, V_o represents the output voltage, while $L_1, L_2, \ldots, L_n$ and $i_1, i_2, \ldots, i_n$ denote the leg inductances and the corresponding currents, respectively. Here, C is the filter capacitance introduced to filter the high-frequency ripple produced by the switching operation, while R_L and R_C denote the parasitic series resistances of the inductors and capacitor, respectively. The load represents the battery to be charged. The n duty cycle signals $d_1, d_2, \ldots, d_n$ modulate the PWM signals to drive the buck converter switches according to the proposed control design. Using the Kirchhoff's current law (KCL), the total current $i_t(t)$ can be written as:

$$i_t(t) = \sum_{k=1}^{n} i_k(t)$$

The model of the buck converter is obtained using the average modeling technique described in [14,24], while the droop control design method is used to model the battery as a power load R [13,25]. This simplified model, compared to other dynamical models, such as Thévenin or non-linear models [26], is generally used in the design of the controller since the product of its voltage and current vary very slowly with respect to the converter dynamics [27]. In particular, the load droop coefficient R is selected by considering the allowable battery voltage range ΔV_o and the constant reference current I_{ref}, which is $R = \Delta V_o / I_{ref}$. In this contest, the state space equations of the interleaved converter are

$$\underbrace{\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \vdots \\ \frac{di_n}{dt} \\ \frac{dV_C}{dt} \end{bmatrix}}_{\dot{x}(t)} = \underbrace{\begin{bmatrix} \frac{-(R_{S1}+R_P)}{L_1} & \frac{-R_P}{L_1} & \cdots & \frac{-R_P}{L_1} & \frac{-R_P}{L_1 R_C} \\ \frac{-R_P}{L_2} & \frac{-(R_{S2}+R_P)}{L_2} & \cdots & \frac{-R_P}{L_2} & \frac{-R_P}{L_2 R_C} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \frac{-R_P}{L_n} & \frac{-R_P}{L_n} & \cdots & \frac{-(R_{Sn}+R_P)}{L_n} & \frac{-R_P}{L_n R_C} \\ \frac{R_P}{CR_C} & \frac{R_P}{CR_C} & \cdots & \frac{R_P}{CR_C} & \frac{-1}{C(R+R_C)} \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \\ V_C \end{bmatrix}}_{x(t)} + \underbrace{\begin{bmatrix} \frac{V_{in}}{L_1} & 0 & \cdots & 0 \\ 0 & \frac{V_{in}}{L_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{V_{in}}{L_n} \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} d_1 \\ d_2 \\ \vdots \\ d_n \end{bmatrix}}_{U}$$

$$i_t(t) = \underbrace{\begin{bmatrix} 1 & 1 & \cdots & 1 & 0 \end{bmatrix}}_{C} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \\ V_C \end{bmatrix}}_{x(t)} \tag{1}$$

where

$$R_P = \frac{RR_C}{R + R_C}, \; R_{Sk} = R_{Lk} + R_{Swk} \tag{2}$$

and R_{Swk} represents k-leg power switch conduction losses. It is assumed that the value of R_{Sw} is equal in both switches of the same leg.

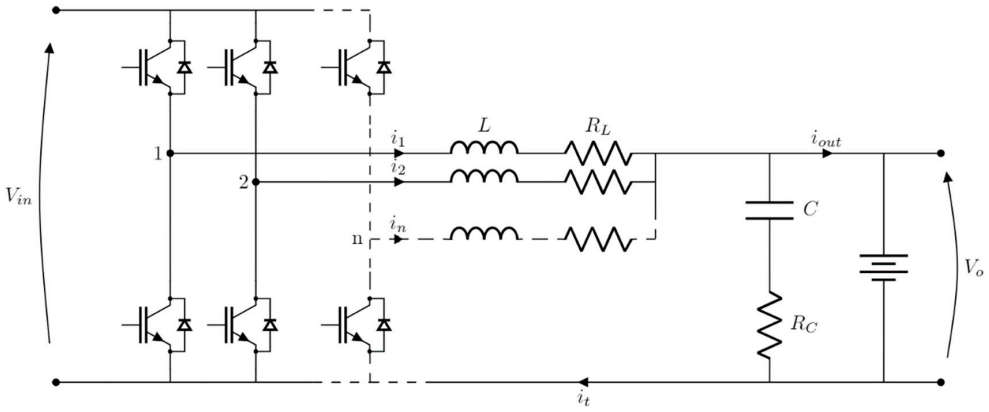


Figure 1. Interleaved buck converter.

Neglecting the effects introduced by the capacitor resistance R_C, the output voltage can be approximated to V_C, while the output current $i_{out}(t)$ can be approximated to the total current $i_t(t)$. In this way, the total current can be obtained by considering the summation of inductors' currents $i_k(t)$ only, and no additional sensor is required.

Let us now define the average duty cycle as

$$d_t(s) = \frac{d_1(s) + d_2(s) + \ldots + d_n(s)}{n} \tag{3}$$

Assuming

$$L = L_1 = L_2 = \ldots = L_n, \text{ and } R_S = R_{S1} = R_{S2} = \ldots = R_{Sn} \tag{4}$$

the average model transfer function of the n-leg interleaved buck converter is

$$G(s) = \frac{i_t(s)}{d_t(s)} = G_0 \frac{\left(1 + \frac{s}{\omega_o}\right)}{\left(1 + \frac{2\xi}{\omega_n}s + \frac{s^2}{\omega_n{}^2}\right)} \tag{5}$$

where

$$G_0 = \frac{nV_{in}}{nR + R_s},\ \omega_n = \sqrt{\frac{nR + R_s}{LRC}},\ \omega_o = \frac{1}{RC},\ \xi = \frac{\omega_n}{2}\frac{RR_sC + L}{(nR + R_s)} \tag{6}$$

The Bode diagrams of the frequency response $G\,(j\omega)$ when n is equal to 3, 6, and 9 are shown in Figure 2.

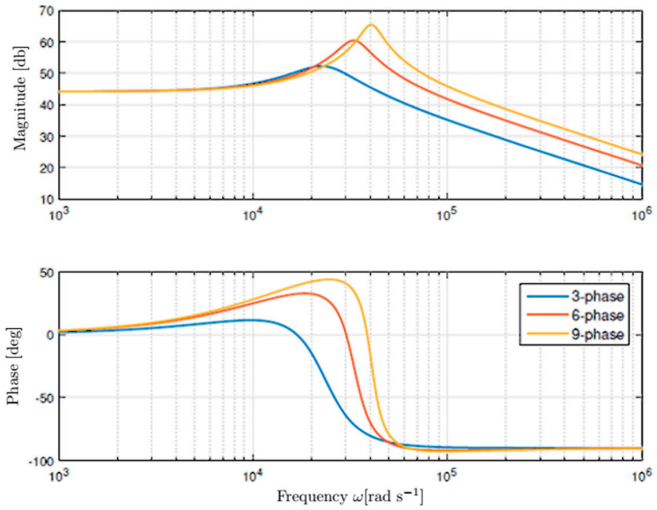


Figure 2. Bode diagrams of the frequency response $G(j\omega)$ of an interleaved buck converter.

The transfer function of the discrete model of the n-leg interleaved buck converter is given by

$$G(z) = \frac{nV_{in}}{nR + R_s} \frac{(1 - a - bc)z + e^{-2\xi\omega_n T_s} - a + bc}{z^2 - 2az + e^{-2\xi\omega_n T_s}} \tag{7}$$

where

$$a = e^{-\xi\omega_n T_s} \cos\left(\omega_n T_s \sqrt{1-\xi^2}\right),\ b = e^{-\xi\omega_n T_s} \sin\left(\omega_n T_s \sqrt{1-\xi^2}\right),\ c = \frac{\xi\omega_o - \omega_n}{\omega_o \sqrt{1-\xi^2}} \tag{8}$$

The transfer function (7) can be obtained by applying the definition of the Z-transform to the product of the continuous-time transfer function of the converter $G(s)$ and the transfer function of the zero-order hold

$$H_0(s) = \frac{1 - e^{-sT_s}}{s}$$

with sampling period T_s, i.e.,

$$G(z) = Z[H_0(s)G(s)]$$

Notice that $G(z)$ is characterized by two complex conjugate poles.

$$z_{1,2} = e^{\left(-\xi \pm j\sqrt{1-\xi^2}\right)\omega_n T_s} \tag{9}$$

which gives rise to well-documented detrimental oscillatory effects, see [28].

3. The Proposed Control

The battery charging profile for general battery chargers was described in [16]. After a pre-charging mode, during which the output current of the converter gradually ramps up with a staircase wave current control, a constant current control leads to a fast charge up to the maximum battery voltage. Then, the charging current gradually decreases under constant voltage control up to the final value of the output current, see Figure 3.

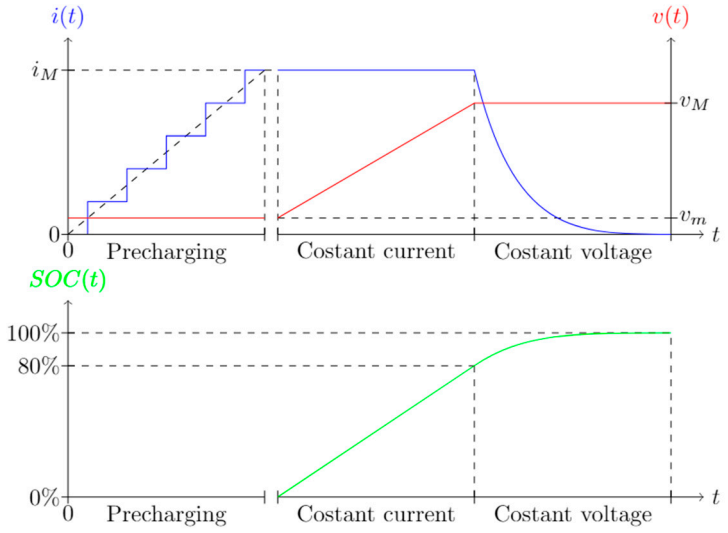


Figure 3. Battery charging profile.

The proposed control strategy for the interleaved buck converter topology shown in Figure 1 can be used both for pre-charging mode control and for constant current control. The main idea is to address the total output control problem and the inductor current sharing control separately. In particular, the average duty cycle $d_t(z)$ is computed by a discrete controller to track the total current reference signal, while leg duty cycles are computed by separate digital controllers using the current balancing technique as in [13].

3.1. Average Duty Cycle Control

Let us consider the discrete control scheme shown in Figure 4, where *G(s)* and *G(z)* represent the buck converter transfer Functions (5) and (7), respectively. Moreover, $r(z)$ is the discrete reference signal, while $i_t(z)$ denotes the sampled and hold current to be controlled. The value of the average duty cycle $d_t(z)$ is generated by the compensator *C(z)* to track the error signal $e(z) = r(z) - i_t(z)$. In addition, let $L(z)$ denote the loop-gain transfer function, i.e., $L(z) = C(z)\,G(z)$.

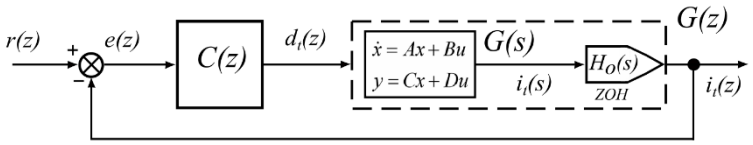


Figure 4. Block scheme of the whole current control system.

The proposed discrete-time controller is the following biquadratic filter

$$C(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}, \tag{10}$$

which can be directly implemented on a microcontroller. With the values

$$b_0 = \widetilde{K}_i, \quad b_1 = -2\widetilde{K}_i \delta_d \omega_d, \quad b_2 = \widetilde{K}_i {\omega_d}^2, a_1 = -\left(\frac{\omega_d}{\beta_d} + 1\right), \quad a_2 = \frac{\omega_d}{\beta_d}, \tag{11}$$

the controller (10) can be written in the equivalent form

$$C(z) = \widetilde{K}_i \frac{z^2 - 2\delta_d \omega_d z + {\omega_d}^2}{(z-1)\left(z - \frac{\omega_n}{\beta_d}\right)} \tag{12}$$

with complex conjugate zeros.

The proposed design procedure for the tuning of the parameters a_1, a_2, b_0, b_1, b_2 is based on the conjunction of the classical pole/zero cancellation and the so-called inversion formulae methods introduced in [25] for a standard single-leg buck converter. In this paper, the design procedure is summarized by giving the logical steps of the algorithm for the solution of the following design problem.

Control Problem

Find the values of the parameters a_1, a_2, b_0, b_1, b_2 to guarantee zero position error, and to assign the phase margin Φ_m and the gain crossover frequency ω_g of the open-loop frequency response $L(e^{j\omega T_s})$, where T_s is the sampling period:

Step 1: Calculate the values of ω_n, ω_o, ξ using (6) on the basis of the parameters of the circuit and determine the discrete transfer function $G(z)$ using (7) and (8).

Step 2: Compute the values of ω_d, δ_d by placing the zeros of (12) in the same location of the complex conjugate poles of $G(z)$ to cancel their detrimental effects using.

$$\omega_d = e^{-\xi \omega_n T_s}, \; \delta_d = \cos\left(\omega_n T_s \sqrt{1 - \xi^2}\right) \tag{13}$$

Step 3: Evaluate the magnitude and the phase of the frequency response $G(e^{j2\omega T_s})$ of the plant multiplied by the frequency response of the factor of the controller (12) that has already been determined

$$\widetilde{G}(e^{j\omega T_s}) = G(e^{j\omega T_s}) \frac{e^{j2\omega T_s} - 2\delta_d \omega_d e^{j\omega T_s} + {\omega_d}^2}{e^{j\omega T_s} - 1} \tag{14}$$

at the desired gain crossover frequency ω_g.

Step 4: Compute the magnitude and the phase that the controller should introduce to exactly satisfy the given specification on the phase margin Φ_m.

$$M_g \stackrel{def}{=} M(\omega_g) = 1/\left|\widetilde{G}(e^{j\omega_g T_s})\right| \tag{15}$$

$$\varphi_g \stackrel{def}{=} \varphi(\omega_g) = \Phi_m - \pi - \angle\widetilde{G}(e^{j\omega_g T_s}) \tag{16}$$

Step 5: Calculate the values of the remaining degrees of freedom of the controller (12) using the inversion formulae.

$$\beta_d = \frac{\omega_d}{\frac{\sin(\omega_g T_s)}{\tan(\varphi_g)} + \cos(\omega_g T_s)}, \tag{17}$$

$$\widetilde{K}_i = -M_g \sin(\varphi_g)\sin(\omega_g T_s)\left(1 + \frac{1}{\tan^2(\varphi_g)}\right). \tag{18}$$

The given control problem has a feasible solution if and only if $\beta_d > 0$ and $\widetilde{K}_i > 0$, see Remark 4.1 in [25].

Step 6: Compute the parameters a_1, a_2, b_0, b_1, b_2 using (11) to write the controller in the form (10) which is directly implementable on a microcontroller board.

3.2. Circulating Current Control

For the minimization of the ripple in the output current, the delay angle of the PWM carriers of each buck converter leg is $360°/n$. An example of inductor currents in 3-leg interleaved buck converter is shown in Figure 5.

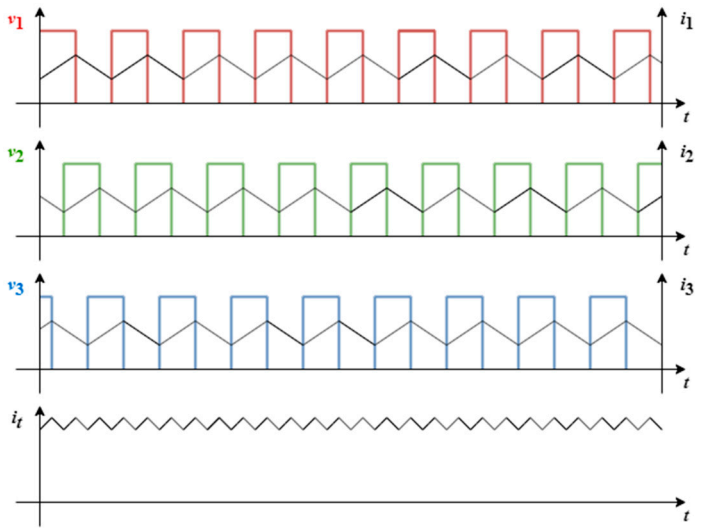


Figure 5. Pole voltages, inductor currents, and total current in 3-leg interleaved buck converter in case of $d_1 = d_2 = d_3 = 0.5$.

It is well known that applying the average duty cycle $d_t(z)$ to each PWM is not enough to guarantee a proper operation when the converter is exposed to variations of the inductor parameter. It follows that other control loops have to be considered in order to minimize the differences of the inductor currents both at steady-state and during the transient. For this purpose, let us consider the control system shown in Figure 6.

In particular, the signals to be controlled are

$$i_{12}(z) = i_1(z) - i_2(z),\ i_{13}(z) = i_1(z) - i_3(z), \ldots i_{1n}(z) = i_1(z) - i_n(z)$$

The control signals

$$d_{12}(z) = d_1(z) - d_2(z),\ d_{13}(z) = d_1(z) - d_3(z), \ldots d_{1n}(z) = d_1(z) - d_n(z) \tag{19}$$

denote the differences of duty cycles of the buck converter in each considered mesh.

The transfer function of the discrete plant to be controlled is

$$G_{12}(z) = \frac{i_{12}(z)}{d_{12}(z)} = [H_0(s)G_{12}(s)]$$

where

$$G_{12}(s) = \frac{V_{in}}{R_s + sL}$$

It can be proved that

$$G_{12}(z) = G_{13}(z) = \ldots = G_{1n}(z) = \frac{V_{in}}{R_s}\frac{1 - e^{-\frac{Rs}{L}Ts}}{z - e^{-\frac{Rs}{L}Ts}}$$

When R_s can be neglected, we obtain

$$G_{12}(z) = G_{13}(z) = \ldots = G_{1n}(z) = \frac{V_{in}T_s}{L}\frac{1}{z-1}$$

For the control problem considered in this paper, the following form of a discrete proportional-integral (PI) compensator can be taken into account:

$$C_{PI}(z) = K_P + K_I\frac{Z+1}{Z-1} \tag{20}$$

The values of parameters K_P and K_I can be selected to exactly satisfy design specifications on the gain crossover frequency ω_G and on the phase margin Φ_M, while the specification of zero position error is automatically fulfilled by the structure of the controller. The analytical solution of the control problem can be obtained using the following inversion formulae:

$$\begin{array}{ll} K_P & = M_G\cos(\varphi_G) \\ K_I & = -M_G\sin\varphi_G\tan\left(\frac{\omega_G T_s}{2}\right) \end{array} \tag{21}$$

where

$$M_G \stackrel{def}{=} M(\omega_G) = 1/\left|G_{12}(e^{j\omega_G T_s})\right|$$
$$\varphi_G \stackrel{def}{=} \varphi(\omega_G) = \Phi_M - \pi - \angle G_{12}(e^{j\omega_G T_s})$$

The pulse width modulation (PWM) duty cycles $d_1, d_2, \ldots, d_n$ can be computed solving Equations (3) and (19), i.e.,

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ \vdots \\ d_n \end{bmatrix} = \begin{bmatrix} \frac{1}{n} & \frac{1}{n} & \frac{1}{n} & \cdots & \frac{1}{n} \\ 1 & -1 & 0 & \cdots & 0 \\ 1 & 0 & -1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 0 & 0 & \cdots & -1 \end{bmatrix}^{-1} \begin{bmatrix} d_t \\ d_{12} \\ d_{13} \\ \vdots \\ d_{1n} \end{bmatrix}$$

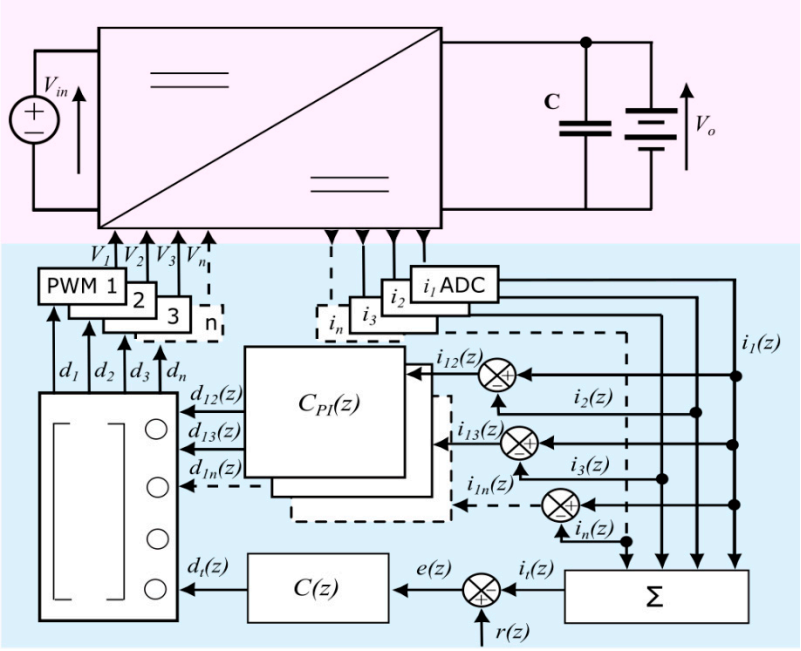


Figure 6. Block scheme of the buck converter and control system. The power circuit and the control scheme are respectively displayed with a pink and light blue background.

4. Numerical and Experimental Results

Let us consider the parameter configurations of the buck converter shown in Table 1. Case (a) refers to the simulated control system used to validate the proposed model and to evaluate the effectiveness of the proposed control procedure in comparison with the method described in [13]. For this reason, the parameters a) were selected to be equal to the parameters considered in [13] (in particular, see Table III. Case (b) refers to the parameters of the hardware device used for the experimental validation. According to the limited power capabilities of the devices available in our laboratory, the input nominal voltage and the output reference current were scaled down by a factor of 7 and 10, respectively. The A/D converter resolution (12 bits) and the sampling/switching frequency (3 × 20 kHz) were maintained the same in order to have a direct correspondence with the control system implemented in simulations (Case a).

Table 1. Parameters of the system.

Label	Description	Case (a) Simulations	Case (b) Experiments
n	Number of legs	3	3
V_{in}	DC-input nominal voltage	618 V	90 V
I_{ref}	Output reference current	125 A	10 A
f_{sw}, f_s	Switching and sampling frequencies	20 kHz, 60 kHz	20 kHz, 60 kHz
A/D	Converter resolution	12 bits	12 bits
R_L, L	Coupling resistance and inductance	0 Ω, 0.344 mH	0.91 Ω, 0.99 mH
C	Capacitance	16 μF	13.5 μF
R	Load	[0.10–3.84] Ω	[0.10–5.94] Ω

4.1. Proposed Control Procedure

The discrete models (7) and (8) of the converter with the parameters a) in Table 1 is

$$G(z) = \frac{87.81\,z - 66.72}{z^2 - 1.631\,z + 0.7624} \tag{22}$$

The average duty cycle control shown in Figure 4 can be designed to yield zero position error, a phase margin Φ_m and a gain crossover frequency ω_g of the open-loop frequency response equal to 80° and 3000 rad/s, respectively.

Using the proposed procedure, the complex poles of $G(z)$ can be cancelled by selecting $\delta_d = 0.934$ and $\omega_d = 0.87$ rad/s in (12). The gain and the phase that the controller (12) has to introduce at frequency ω_g to satisfy the design specification on the phase margin are $M_g = 0.0023$ and $\varphi_g = 339.6°$, respectively. Using (17) and (18) the remaining parameters of the PIDF controller (12) are $\beta_d = 1.01$, $\widetilde{K}_i = 3.346 \times 10^{-4}$. The discrete-time controller (10) thus obtained is

$$C(z) = \frac{3.346 - 5.46z^{-1} + 2.55z^{-2}}{1 - 1.86z^{-1} + 0.86z^{-2}} \times 10^{-4}$$

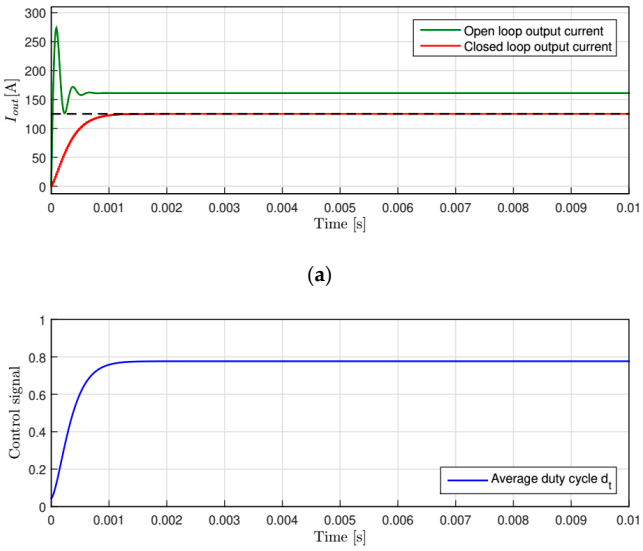
which follows directly from (11).

The step responses of the output current (0–125 A) of the open and closed-loop system are shown in Figure 7. Notice that the steady-state error of the uncompensated system was reduced to zero and the overshoot has been eliminated by the control. Also, the given dynamical control specifications were exactly satisfied, as highlighted by the Nyquist plot and the Bode diagrams of the frequency response of the controlled system shown in Figures 8 and 9.

Regarding the design of the discrete controller for the circulating current control, the zero position error was automatically achieved by the structure of the controller (20), while the specifications on the gain crossover frequency $\omega_G = 8000$ rad/s and phase margin $\Phi_M = 50°$ can be exactly met using the presented design procedure. The gain and the phase that the controller (20) has to introduce at frequency ω_G to satisfy the given dynamic specifications are $M_G = 0.0044$ and $\varphi_G = 323.8°$, respectively. From (21), the controller (20) that solves the problem is given by

$$C_{PI}(z) = \frac{3.763\ z - 3.413}{z - 1} \times 10^{-3}$$

The Nyquist plot of the open-loop frequency response of the control system is shown in Figure 10. Notice that the given specifications are exactly met.



(**a**)

(**b**)

Figure 7. (**a**) Open-loop step response (green), closed-loop step response (red) and (**b**) the corresponding average duty cycle $d_t(t)$ (blue).

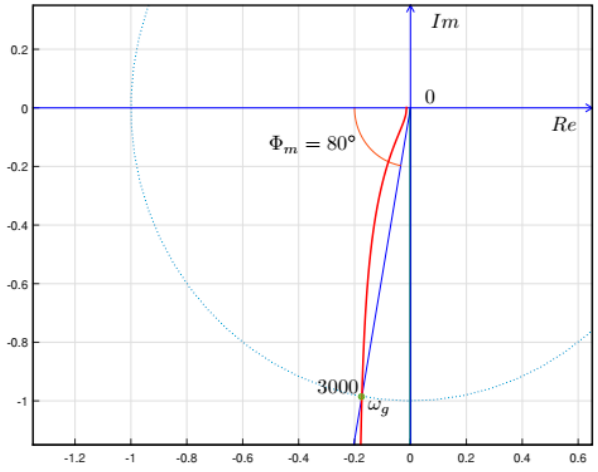


Figure 8. The Nyquist plot of the open-loop frequency response of the 3-leg interleaved buck converter with the proposed control.

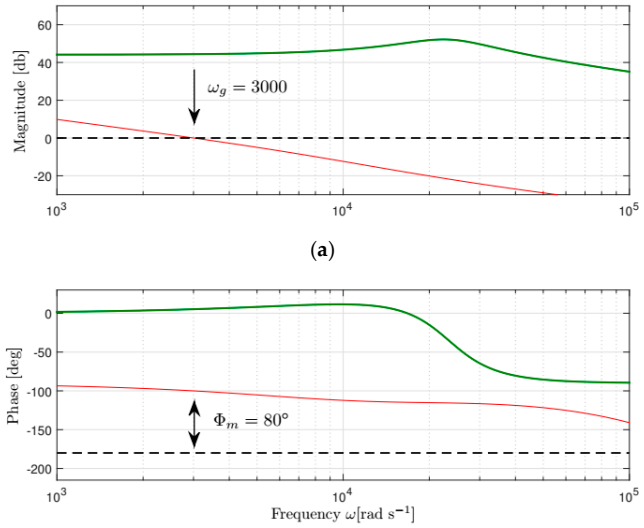


Figure 9. Bode diagrams of the frequency response of the 3-leg interleaved buck converter average model (green) and of the open-loop frequency response with the proposed control (red). (**a**) Bode magnitude plot; (**b**) Bode phase plot.

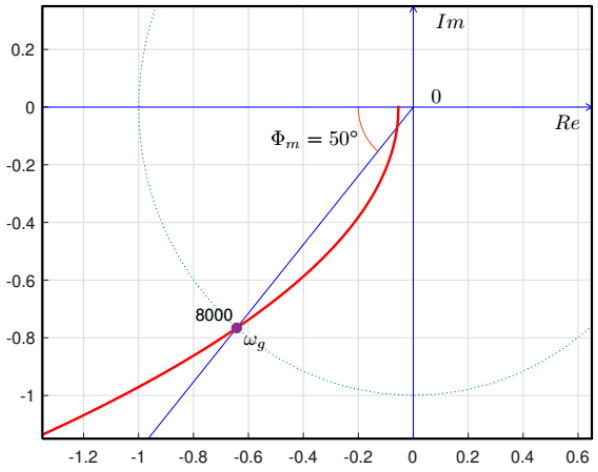


Figure 10. The Nyquist plot of the open-loop frequency response of the current control system.

4.2. Numerical Comparison

The proposed control system has been simulated using Matlab R2018a and Simulink 9.1 (solver: ode45), and compared with the method proposed in [13] by adopting the same system parameters (see Table III in [13]). In particular, all the blocks of the interleaved buck converter have been selected from the Simscape 4.4 Electrical toolset. The 3-leg buck converter has been controlled in [13] with a PI regulator to provide a phase margin of 71.3° and a gain margin of 4.83 dB in the continuous-time domain. The corresponding transfer function in the z domain is, see Equation (24) in [13]

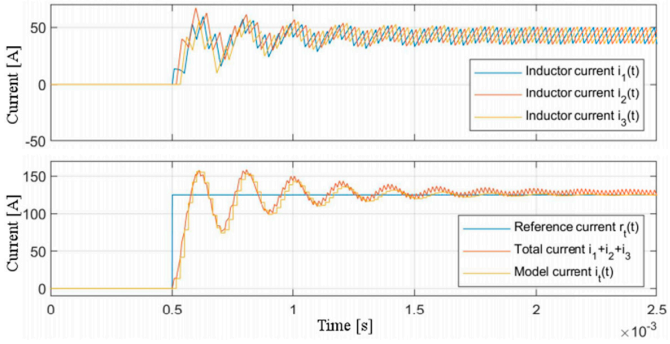
$$C_{PI}(z) = \frac{1.219 \cdot 10^{-3} z + 433.4601 \cdot 10^{-6}}{z - 1}$$

Notice that the resulting phase and gain margin of the loop-gain transfer function

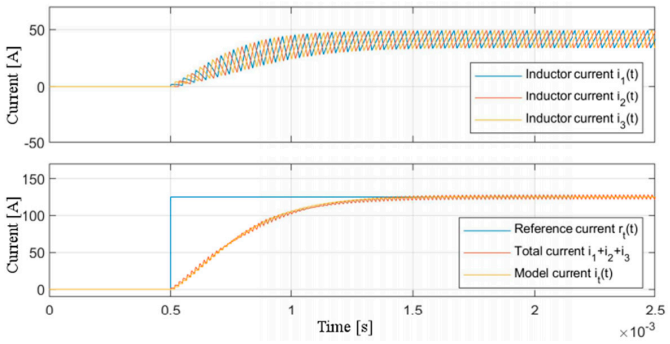
$$L_{av}(z) = [H_0(s)G(s)]C_{PI}(z)$$

were reduced to 18° and 6.53 dB, respectively. The consequent degradation in dynamic performance was due to the use of an indirect design procedure carried out in the continuous-time domain and was avoided with the direct method proposed in this paper.

The step responses of the inductor currents and of the total current obtained with the method described in [13] and the method presented in our paper are shown in Figure 11. The significant improvement of the dynamic behavior was the elimination of the oscillation during the transient, as well as the reduction of the settling time. In both cases, the total current flowing to the load presents a significant reduction of the ripple compared to the inductor currents. Moreover, the overlap of the total current with the output signal of the discrete system (22) confirmed the accuracy of the presented discrete model.



(**a**)



(**b**)

Figure 11. Current step responses with the method proposed in [13] (**a**) and with the method proposed in this paper (**b**).

The robustness to parameter variations and model uncertainties were considered to take into account discrepancies between the system model and the physical system. For this reason, the behavior of the inductor and load currents under 20% output load resistance variation was simulated, analyzed,

and compared with the method presented in [13]. The results are shown in Figure 12. While the load variation leads to quasi-persistent oscillations using the control described in [13], the considered variation was promptly stabilized in less than 1 ms using the method described in Section 3. Notice that the average value of the currents returns to the setpoint value, while the current ripple changes its value at steady-state due to the consequent duty cycle variation.

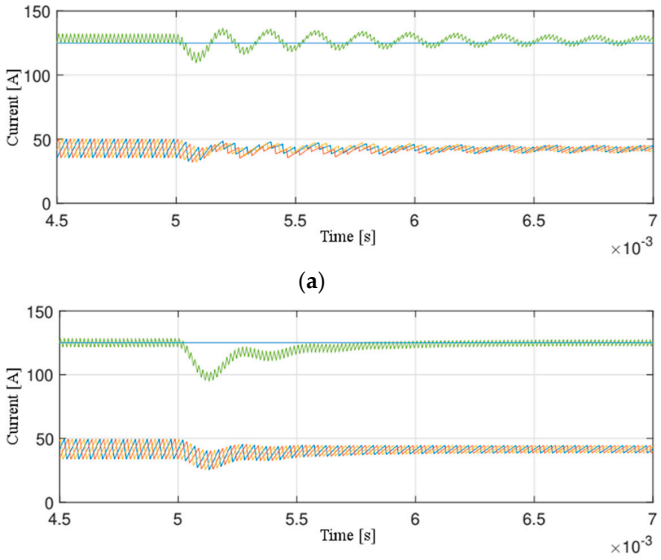


Figure 12. Total (green), reference (light blue), and inductors (blue, yellow, and red) currents under 20% output load variation with the method proposed in [13] (**a**) and with the method proposed in this paper (**b**).

Moreover, the designed control was tested under 50% inductance parameter variation and compared with the method presented in [13], see the corresponding step responses in Figure 13. Both controls compensated the induction variation and tracked the expected steady-state current values. However, the proposed procedure led to a significant improvement in the transient.

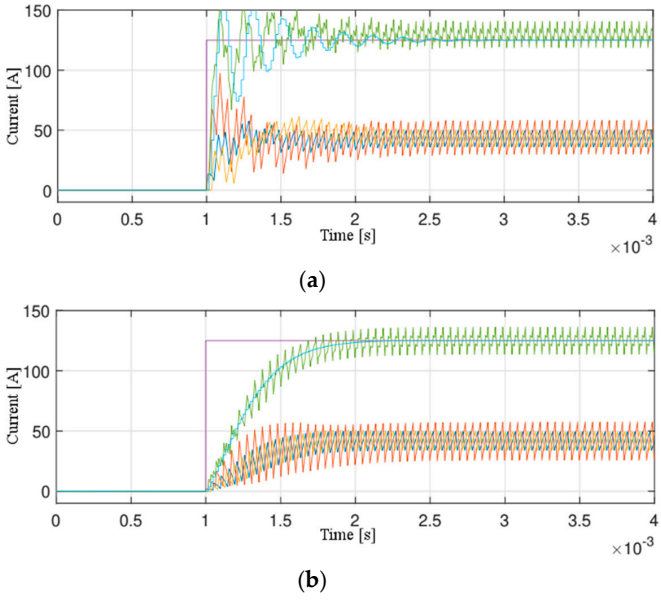


Figure 13. Total (green), total sampled (light blue), reference (violet), and inductors (blue, yellow, and red) currents under 50% inductance parameter variation (on the red leg) with the method proposed in [13] (**a**) and with the method proposed in this paper (**b**).

Finally, Figure 14 shows the total and the inductor currents under 10% V_{in} variation. Even in this case, the proposed control promptly compensates the input voltage variation reaching a new steady-state condition. In particular, the settling time has been reduced from 1.5 ms to 0.5 ms with respect to the method presented in [13].

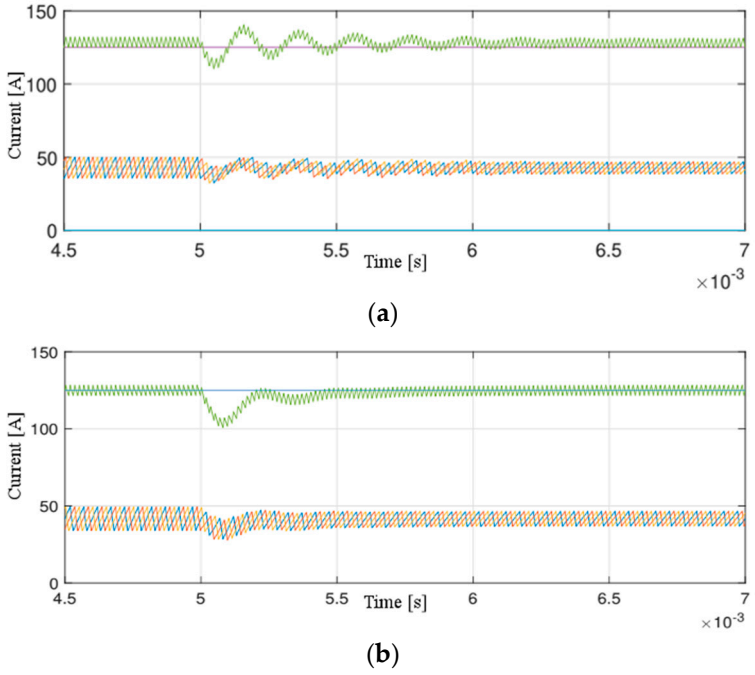


Figure 14. (green), reference (light blue), and inductors (blue, yellow, and red) currents under 10% V_{in} variation with the method proposed in [13] (**a**) and with the method proposed in this paper (**b**).

Regarding the battery charging profile, see Figure 3, other reference current profiles have been considered. Output and inductor currents under reference current variation from 0 A to 120 A within 10 A steps are shown in Figure 15. This behavior simulated the pre-charging mode control of the battery charging profile, showing that the presented control structure is suitable also with this charging profile. Moreover, Figure 16 shows the rising and falling system step response from 0 A to 125 A and from 125 A to 5 A.

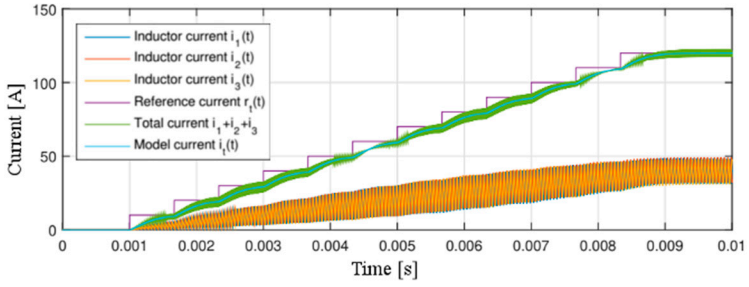


Figure 15. Total and inductor currents under reference current variation from 0 A to 120 A with 10 A steps.

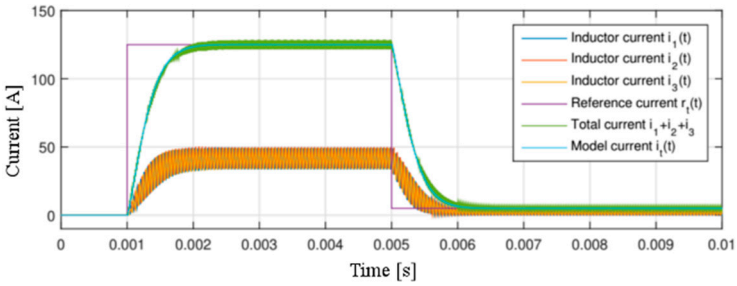


Figure 16. Rising step from 0 A to 125 A and falling step from 125 A to 5 A.

4.3. Experimental Results

The experimental tests were carried out using a small-scale hardware setup composed by a three-phase module employed in an interleaved configuration having parameters shown in Table 1 as "Case (b)". In particular, the Mitsubishi PS22A79 intelligent power IGBT module (1200 V, 50 A) was driven by a Texas Instruments Delfino F28379D DSP control card running the TMS320F28379D microcontroller unit (MCU) via optical interface links (Figure 17). Inductor currents were sensed employing Hall effect sensors LEM LA 55-P (50 A) and forwarded to the ADC inputs of the DSP board. The control scheme visible in Figure 6 (light blue background) was implemented on Simulink 9.1 and executable C code was generated using Simulink Coder, Embedded Coder, and Texas Instruments Support from Embedded Coder. Finally, employing Code Composer Studio interface, the generated code was deployed to the DSP target. In particular, the DSP board was in charge of running the proposed control method considering sampled currents as input digital signals and PWM waveforms as output signals.

The step response from 0 A to 10 A and zoom at the steady-state of the inductor current sensor outputs and output voltage are shown in Figure 18. In particular, the output current, which can be calculated by the output voltage over resistive load, reached the setpoint value in 5 ms, without oscillations. The zoom of the output signal of the inductor current sensor and the output voltage at steady-state highlights the PI control effect in the balancing of the inductor current.

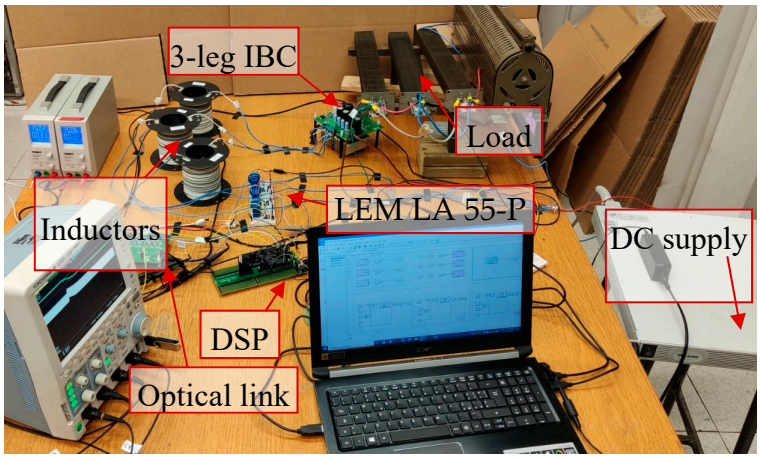
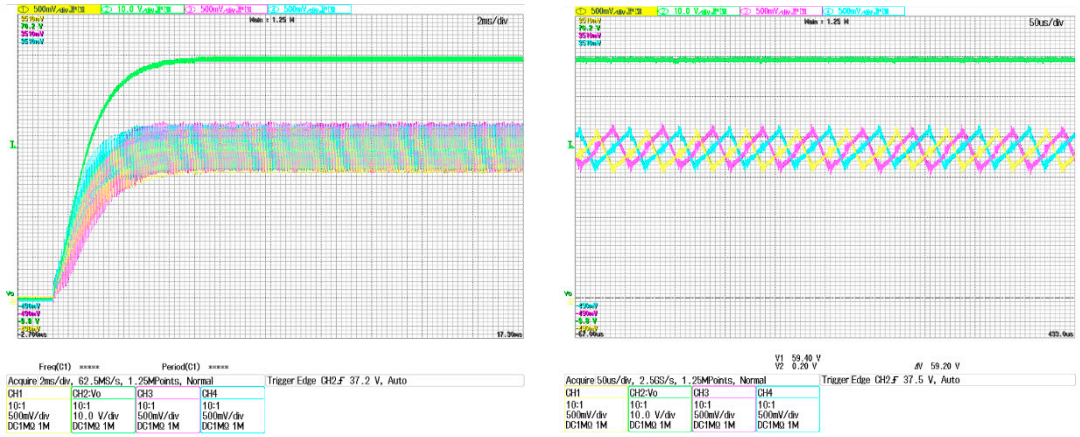


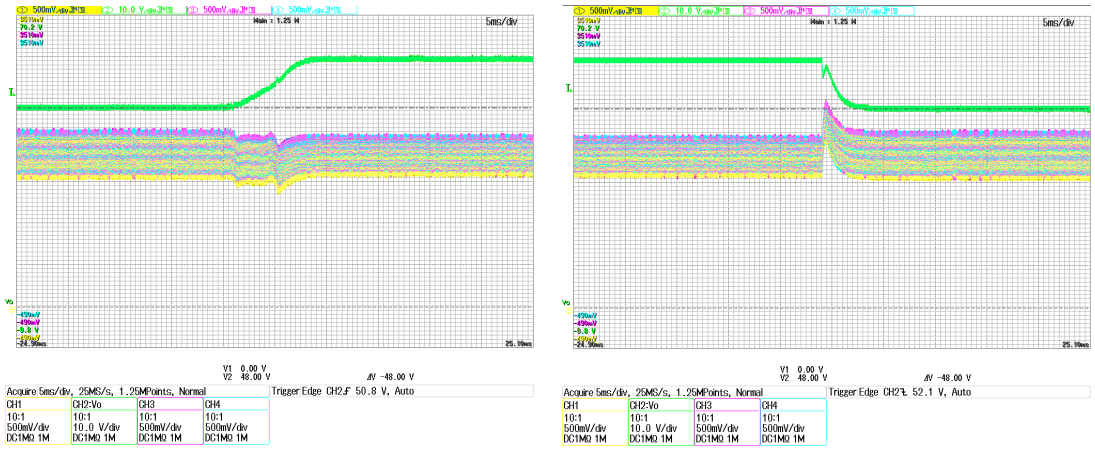
Figure 17. Experimental setup.



(**a**) (**b**)

Figure 18. Step response from 0A to 10A (**a**) and zoom in steady-state condition (**b**) of inductor currents (current transducer outputs, blue, yellow, magenta) and output voltage (green).

The outputs of the current sensors and the output voltage under 20% output load variation, i.e., from 4.75 Ω to 5.94 Ω and from 5.94 Ω to 4.75 Ω, are shown in Figure 19a,b, respectively. Despite the load perturbation, the total current $i_t(t)$ reaches the reference value (10 A), while the inductor currents balance each other since they have the same average value in both cases.



(**a**) (**b**)

Figure 19. Inductor sensor outputs (blue, yellow, magenta) and output voltage (green) under 20% output load variation, i.e., (**a**) from 4.75 Ω to 5.94 Ω and (**b**) from 5.94 Ω to 4.75 Ω.

5. Conclusions

In this work, we introduced a new design/tuning procedure for the control of an interleaved buck converter for EV charging. The challenge to guarantee good dynamic performances, even current share among the legs, as well as an acceptable level of robustness under load variations, made rules of thumb and trial-and-error methods inapplicable to the control of these converters. The approach that we proposed overcomes this problem since it directly and exactly satisfied standard design constraints such as gain crossover frequency, phase margin, and zero position error for the PIDF main controller and circulating current PIs. In order to prove the effectiveness of the proposed approach, we compared our strategy with the method introduced in [13]. Moreover, taking advantage of the generic formulation of the discrete-time model and the circulating current control, it was possible to quickly scale the system on interleaved topology employing a higher number of legs staked together. Experimental results carried out on a laboratory prototype proved the control system capabilities.

Since the load resistance (representing the battery) varied during charging procedures, future work might investigate the possibility of improving the versatility of the proposed procedure by employing a real-time measure/estimation of the load. In this way, the parameters of the PIDF controller could be updated by live DSP computations using the inversion formulae described in Section 3 turning the proposed method into an adaptive control system design procedure. Moreover, findings readily available in this paper might be used to directly tune the control system of any third party interleaved buck converter regardless of power, number of modules, switching frequency, coupling reactors, and filters.

Author Contributions: Conceptualization, S.C. and R.M.; methodology, S.C., R.M., L.N. and G.G.; software, S.C. and R.M.; validation, L.N. and G.G.; formal analysis, S.C., R.M., L.N. and G.G.; investigation, S.C. and R.M.; resources, S.C. and R.M.; data curation, S.C., R.M. and L.N.; writing—original draft preparation, S.C. and R.M.; writing—review and editing, S.C., R.M., L.N. and G.G.; visualization, S.C. and R.M.; supervision, L.N. and G.G.; project administration, S.C. and G.G. All authors have read and agreed to the published version of the manuscript.

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