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Analysis and Design of a High-Efficiency SiC MOSFET 6-Phase Boost Rectifier †

Giulia Di Nezio *, Marco di Benedetto *, Alessandro Lidozzi and Luca Solero *

C-PED Center for Power Electronics and Drives, Department of Engineering, Roma Tre University, 00146 Roma, Italy; alessandro.lidozzi@uniroma3.it

* Correspondence: giulia.dinezio@uniroma3.it (G.D.N.); marco.dibenedetto@uniroma3.it (M.d.B.); luca.solero@uniroma3.it (L.S.)

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Abstract: In this paper, the analysis and the design of a high-efficiency power electronic conversion system for offshore wind applications are presented. This system is composed of a 6-phase AC–DC converter based on the SiC power semiconductors, to be used to control the achievable power from the wind turbine electrical generator. Thanks to the phase redundancy, the proposed boost rectifier is suitable for applications where reliability and fault tolerance capability are the main targets. To select the appropriate power semiconductor devices, voltage and current ratings have to be determined. After that, the power loss equations are derived in order to evaluate the conversion efficiency. To design the appropriate DC-bus capacitor configuration, an analytical investigation is carried out by estimating the DC-bus RMS current and the voltage ripple. Finally, the thermal sizing of the system is calculated to identify a suitable heatsink. To validate the proposed analysis, the analytical results are compared to simulation ones using the Plexim/PLECS tool in the MATLAB/Simulink environment. For further validation, a prototype of the converter is built and the experimental results are carried out. The results demonstrate that the peak efficiency of the 6-phase boost rectifier can reach 98% at 100 kHz switching frequency.

Keywords: AC–DC converter; multi-phase boost rectifier; SiC power semiconductors; offshore wind

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1. Introduction

In recent years, the demand for renewable energy has grown due to concerns about global warming and environmental issues. Consequently, wind energy has become one of the most attractive renewable sources, reaching 743 GW overall in 2020 [1,2]. Offshore wind farms are gaining increased interest for two main motives: the first is the lack of space on the mainland, and the second is the wind speed being much stronger and more constant than in the onshore case [3,4]. However, in designing an offshore site, DC transmission is preferred in view of the excessive losses of AC transmission over long distances [5]. Additionally, on one side there is a variable speed generator, and on the other side there is a grid with fixed voltage and frequency. Thus, the power conversion system stage is necessary, and it is composed of an AC–DC converter in cascade with a DC–AC converter. An increasing variety of power converter topologies for wind energy conversion systems (WECS) are proposed in the literature [6–8]. These topologies are mainly classified according to the low voltage (LV) and medium voltage (MV) converters. A 3-phase 2-level voltage source converter is an example of an LV converter, whereas a multilevel converter constitutes an MV converter [9]. For this reason, it is important to know the operating voltage of the WECS in order to identify the best power converter configuration. Moreover, in offshore systems, it is preferable to realize a power electronic converter with relatively low cost, which aims to emphasize the fault tolerance capability without neglecting the conversion efficiency [10–14]. For this reason, to increase the reliability and fault tolerance

capability, a power conversion system with modular characteristics and/or redundant legs is recommended. In this way, when a converter breaks down and stops working, the wind turbine is still capable of delivering power, but with reduced capacity. This aspect is of major importance in offshore wind applications because maintenance cannot be performed routinely, and maintenance costs are higher than in the onshore case [3]. Clearly, the number of parallel modules or redundant legs must be limited, otherwise the costs could increase, and the reliability of the system could even decrease, resulting in greater complexity in terms of designing and tuning the control algorithm [15–17]. For this purpose, the 2-level converter topology with parallel legs seems to be an excellent solution in terms of simplicity, reliability, performance, and cost. Moreover, to improve the conversion efficiency, SiC power semiconductors can be used to obtain low conduction and switching power losses [18,19]. Besides, switching frequency can be enhanced, decreasing the passive components' size. Because of this, SiC MOSFET is a competitive technology, even though it is less reliable with respect to the Si IGBT [20].

An analytical method to design the SiC MOSFET 6-phase power conversion system is proposed in this paper to be used in offshore wind applications. To accomplish this task, the first phase is aimed at determining the voltage and current rating of the power semiconductors in order to select the suitable power module. Afterwards, the power losses and the efficiency as a function of the power are evaluated. The DC-bus capacitors are selected according to the analytical investigation. In particular, a detailed analysis of the DC-bus current stress and the voltage ripple, considering three different situations with phase displacement between the two 3-phase stator windings of the 6-phase electrical generator of 0°, 30°, and 60°, is carried out in this paper. Compared to [21], the thermal analysis is carried out and the experimental tests added in order to confirm the proposed analysis. The 6-phase topology, chosen for the boost converter design, is attractive thanks to the reliable and fault tolerance capabilities and subsequently to achieve lower maintenance costs, making it very useful for offshore wind applications. The power conversion system is shown in Figure 1, where it is possible to notice the presence of a 6-phase (two 3-phase windings) permanent magnet synchronous generator (PMSG), a 6-phase, 2-level boost rectifier (6P-2L BR) with a common DC-bus and the two-level voltage source inverter (2L-VSI) connected to the grid through the output filter.

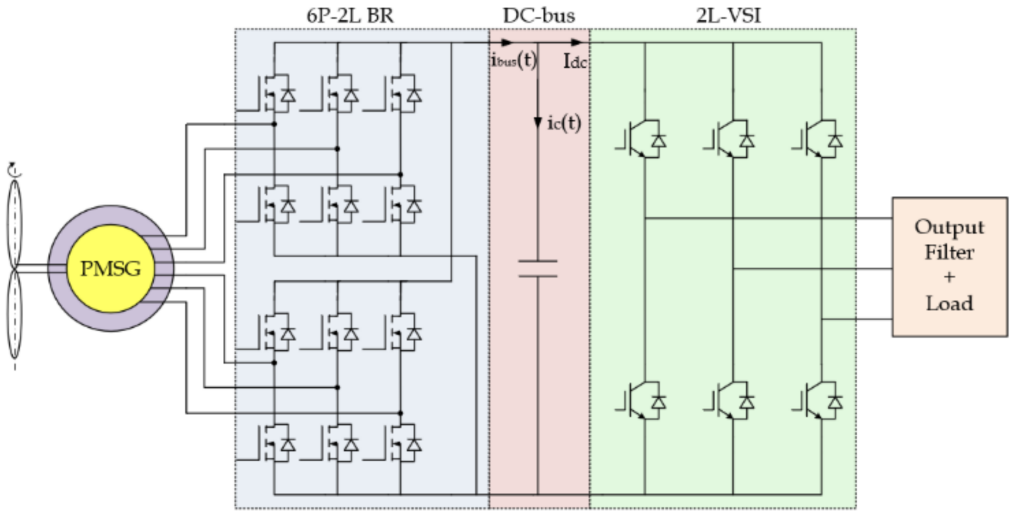


Figure 1. Power conversion system configuration.

The investigated solution is addressed to a 10kW floating offshore wind turbine prototype, to be installed in the Naples Gulf area (Italy).

This paper is organized as follows: in Section 2 the design of the 6-phase power conversion system is carried out, including the selection of the power semiconductor devices, the power loss distribution evaluation, the DC-bus rms current stress and voltage

ripple analysis, and the thermal sizing; in Section 3, the simulation and experimental results are illustrated; finally, in Section 4, the contribution of the proposed work is discussed, and the conclusions are presented.

2. 6-Phase Power Conversion System Design

This section focuses on the analysis and design of the 6-phase AC–DC converter. In particular, to design the proposed power conversion system, an analytical approach was adopted by determining several parameters, such as:

1. Voltage rating and current rating to select proper power semiconductor devices;
2. Power loss distribution for the selected power semiconductor devices;
3. DC-bus current stress and voltage ripple to select an appropriate DC-bus configuration;
4. Thermal sizing to evaluate the minimum thermal resistance in order to opt for a suitable heatsink.

2.1. Voltage Rating and Current Rating

To accurately select the power module, it is essential to evaluate the voltage rating for each semiconductor device. The voltage rating V_{MAX} is a function of two factors: the maximum blocking voltage V_{BL} during the steady state, and the overvoltage during the commutation transient according to Equation (1).

$$V_{MAX} = V_{BL} + k_R L_s \frac{di}{dt} + V_{FR} \tag{1}$$

In a two-level converter, the maximum blocking voltage is equal to the DC-bus voltage V_{BUS}. The overvoltage ΔV, instead, depends on many factors, such as the leak inductance L_S, the current transient di/dt, the coefficient k_R to consider possible resonance in the DC-bus circuit, and the voltage drop across the free-wheeling diode V_{FR} [22,23]. Therefore, the voltage rating can be estimated as in (1). In the considered application, V_{BUS} is 750 V, and the maximum blocking voltage V_{MAX} across the semiconductor devices is valued at 860 V; thus, the optimum voltage rating of the 6-phase power converter is 1200 V.

Once the maximum blocking voltage of the power semiconductor devices has been determined, it is necessary to study the current stress to which the power semiconductor devices are subjected. The current stress for each power semiconductor device can be found by resolving the equations for the average and RMS currents in (2) and (3), in which T_0 represents the fundamental period, *i(t)* is the phase current, and d_x stands for the duty cycle.

$$I_{AV,x} = \frac{1}{T_0}\int_0^{T_0} [i(t)d_x(t)]dt \tag{2}$$

$$I_{RMS,x} = \sqrt{\frac{1}{T_0}\int_0^{T_0} [i^2(t)d_x(t)]dt} \tag{3}$$

The sinusoidal phase current can be stated as in (4), where I_{rms} is the rms value of the phase current, ω_0 is the fundamental frequency, and φ is the phase displacement between the input phase voltage and the corresponding phase current.

$$i(t) = \sqrt{2} I_{rms} \sin(\omega_0 t - \varphi) \tag{4}$$

Considering a sinusoidal pulse width modulation (SPWM), the duty cycle waveform can be found as in (5), where the subscript "p" stands for the top switches, whereas the subscript "n" represents the bottom switches, and M is the modulation depth [23].

$$\begin{array}{c} d_p(t) = 1 - d(t) = \frac{1}{2}(1 - M\sin(\omega_0 t)) \\ d_n(t) = \frac{1}{2}(1 + M\sin(\omega_0 t)) \end{array} \tag{5}$$

Replacing the (4) and (5) into (2) and (3), the current stress for the power semiconductors can be obtained as in (6):

$$\begin{aligned} I_{AV,T} &= \frac{\sqrt{2}}{2} I_{rms}\left(\frac{1}{\pi} - \frac{M\cos\varphi}{4}\right) \\ I_{RMS,T} &= \sqrt{2} I_{rms}\sqrt{\frac{1}{24\pi}(3\pi - 8M\cos\varphi)} \\ I_{AV,D} &= \frac{\sqrt{2}}{2} I_{rms}\left(\frac{1}{\pi} + \frac{M\cos\varphi}{4}\right) \\ I_{RMS,D} &= \sqrt{2} I_{rms}\sqrt{\frac{1}{24\pi}(3\pi + 8M\cos\varphi)} \end{aligned} \tag{6}$$

where the subscripts "*T*" and "*D*" stand for MOSFET and diode, respectively.

The achieved values for the MOSFET average and rms currents and for the diode average and rms current are illustrated in Figure 2 as a function of the transfer power.

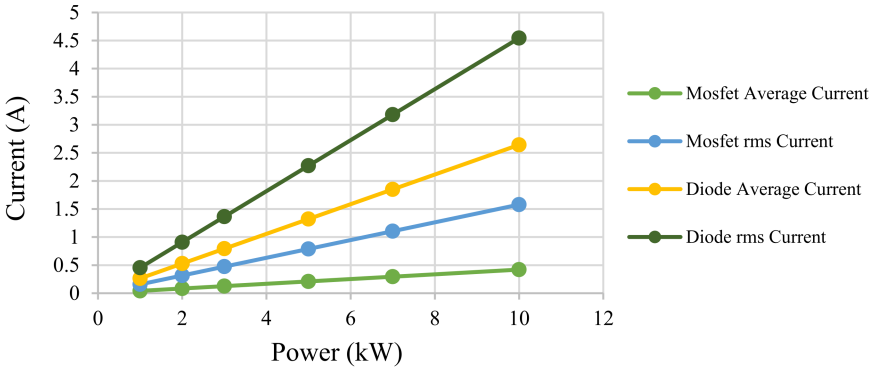


Figure 2. Average and rms current waveforms of the MOSFET and the diode as a function of the transfer power.

According to this analysis and considering a maximum operating power of 10 kW, DC-bus voltage V_{BUS} equal to 750 V, the Wolfspeed SiC MOSFET power module (part number CAB016M12FM3) was selected.

2.2. Power Loss Distribution

Starting from the values reported in the datasheet of the chosen power module, the conduction and switching losses for each semiconductor device can be calculated in order to evaluate the conversion efficiency that the power module is able to achieve. In particular, using Equation (7), it is possible to estimate the conduction losses P_c of a power semiconductor, where V_0 is the forward voltage and R_{on} is the on-state resistance: in the case of the MOSFET, the forward voltage V_0 is equal to zero; the diode, instead, presents both forward voltage and on-state resistance for the establishment of its conduction losses.

$$P_c = V_0 I_{AV,x} + R_{on} I_{RMS,x}^2 \tag{7}$$

Concerning the switching losses of the MOSFET, they can be determined by linearizing around the operative conditions the energy losses provided by the datasheet of the manufacturer. Thus, the switching losses were evaluated according to (8), in which f_{sw} is the switching frequency, and k_{on} and k_{off} are two coefficients. Particularly, by normalizing the energy loss values provided by the manufacturer on the datasheet with respect to the junction temperature, the operating voltage, and the operating current of the switching device, it is possible to obtain the two factors k_{on} and k_{off}. Once the conduction losses and switching losses for each power semiconductor device have been determined, the total losses P_{loss} of the 6-phase boost rectifier can be calculated as in (9), where $P_{c,T}$ and $P_{sw,T}$ are the conduction and switching losses related to the power switch, and $P_{c,D}$ and $P_{sw,D}$ are the

conduction and switching losses related to the power diodes. In (9), the reverse recovery losses of the SiC diodes are neglected.

$$\begin{aligned} P_{sw} &= f_{sw}\left(k_{on}+k_{off}\right)\frac{1}{T_0}\int_0^{T_0} i(t)dt = \frac{1}{\pi}f_{sw}\left(k_{on}+k_{off}\right)I_m \\ k_{on}(T_j,V_{DS},I_D) &= k_{on}(V_{DS})k_{on}(T_j)\frac{E_{on}(I_D)}{I_{D,nom}} \\ k_{off}(T_j,V_{DS},I_D) &= k_{off}(V_{DS})k_{off}(T_j)\frac{E_{off}(I_D)}{I_{D,nom}} \end{aligned} \tag{8}$$

$$P_{loss} = 12(P_{c,T} + P_{sw,T} + P_{c,D} + P_{sw,D}) \tag{9}$$

The total losses of the 6-phase boost rectifier were calculated at the switching frequency f_{sw} of respectively 20 kHz, 60 kHz, and 100 kHz, and the results are shown in Figure 3a. In Figure 3b, instead, the conversion efficiency η of the power module is shown, evaluated as in (10), where P_{in} and P_{out} are the input and output power of the conversion system, respectively.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in}-P_{loss}}{P_{in}} = 1 - \frac{P_{loss}}{P_{in}} \tag{10}$$

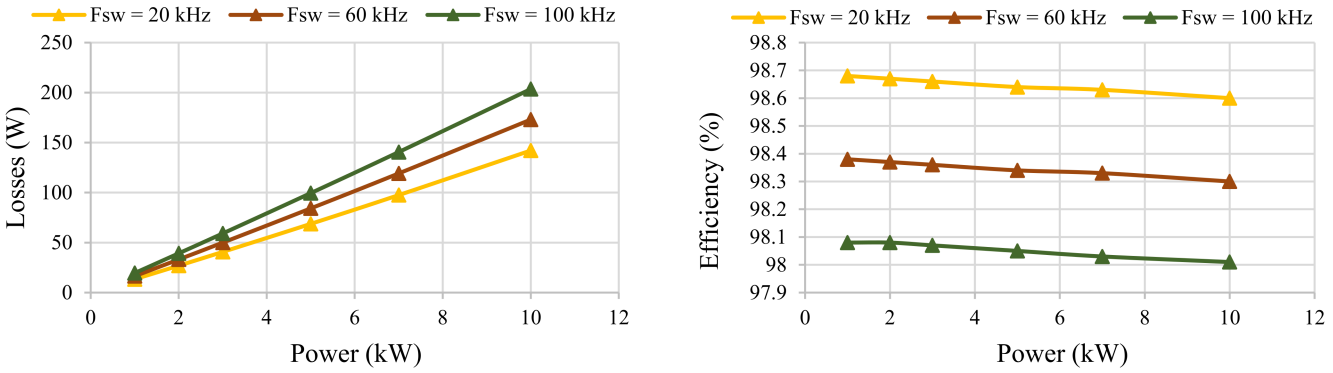


Figure 3. (**a**) Power losses P_{loss} of the 6-phase boost rectifier and (**b**) conversion efficiency assuming the switching frequency f_{sw} of 20 kHz (yellow line), 60 kHz (red line), and 100 kHz (green line), respectively.

2.3. DC-Bus Design

In the design of a power electronic conversion system, a key aspect is the sizing of the DC-bus capacitors. The most appropriate DC-bus capacitor configuration was selected according to two parameters: (1) the rms DC-bus current stress, and (2) the output voltage ripple.

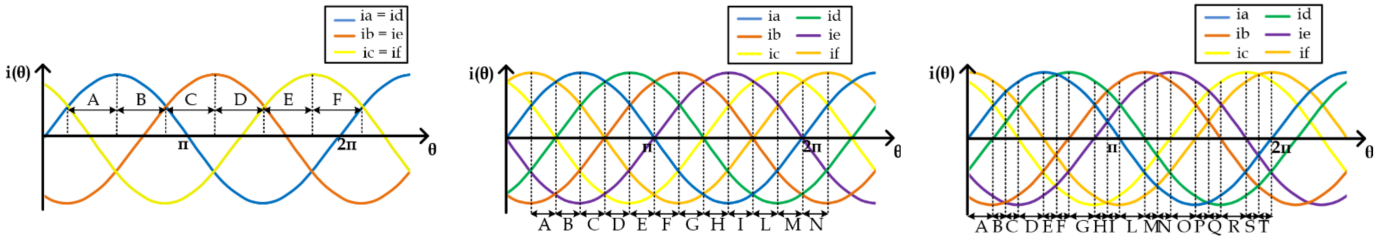
The rms current in the equivalent DC-bus capacitor can be calculated as in (11), in which I_{rms} and I_{dc} are respectively the rms current and the average current coming from the 6-phase boost rectifier. Therefore, these current values can be found by evaluating the output current of the 6-phase 2-level converter, defined as $i_{bus}(t)$ in Figure 1 [24]. The output current $i_{bus}(t)$ can be expressed as in (12), where $s_k(t)$ is the switch state and $i_k(t)$ are the input phase currents; these currents $i_k(t)$ can be formulated as in (13), assuming $k = a, b, c, d, e, f$. In particular, the electrical generator is a 6-phase PMSG having two 3-phase stator windings being arranged as a function of the displacement phase angle δ. For this reason, the DC-bus analysis was divided into three main cases, depending on the displacement phase angle δ between the stator windings.

$$I_{Crms} = \sqrt{I_{rms}^2 - I_{dc}^2} \tag{11}$$

$$i_{bus}(t) = \sum_{k=a}^{f} s_k(t) i_k(t) \tag{12}$$

$$\begin{cases} i_a = I_m \sin(\theta - \varphi) \\ i_b = I_m \sin\left(\theta - \varphi - \frac{2}{3}\pi\right) \\ i_c = I_m \sin\left(\theta - \varphi - \frac{4}{3}\pi\right) \\ i_d = I_m \sin(\theta - \varphi - \delta) \\ i_e = I_m \sin\left(\theta - \varphi - \frac{2}{3}\pi - \delta\right) \\ i_f = I_m \sin\left(\theta - \varphi - \frac{4}{3}\pi - \delta\right) \end{cases} \quad (13)$$

Applying the method as in [25], the rms current was carried out first, considering $\delta = 0°$. Afterward, the method was extended to $\delta = 30°$ and $\delta = 60°$. The three-phase current waveforms for different displacement angles δ are shown in Figure 4. As can be noticed in Figure 4b, intuitively, the best solution with reference to the voltage ripple seems to be $\delta = 60°$ with respect to $\delta = 0°$ and $\delta = 30°$. The following graphical method was carried out in order to demonstrate it. Thank to symmetry, in Figure 4a, it is possible to subdivide the sinusoidal waveforms into six intervals *A*–*F*, whose period is $\pi/3$; in Figure 4b, it is possible to distinguish 12 intervals *A*–*N*, whose period is $\pi/6$; in Figure 4c, it is possible to differentiate 18 intervals *A*–*T*, in which there is the alternance of one interval of period $\pi/6$ and two intervals of period $\pi/12$.



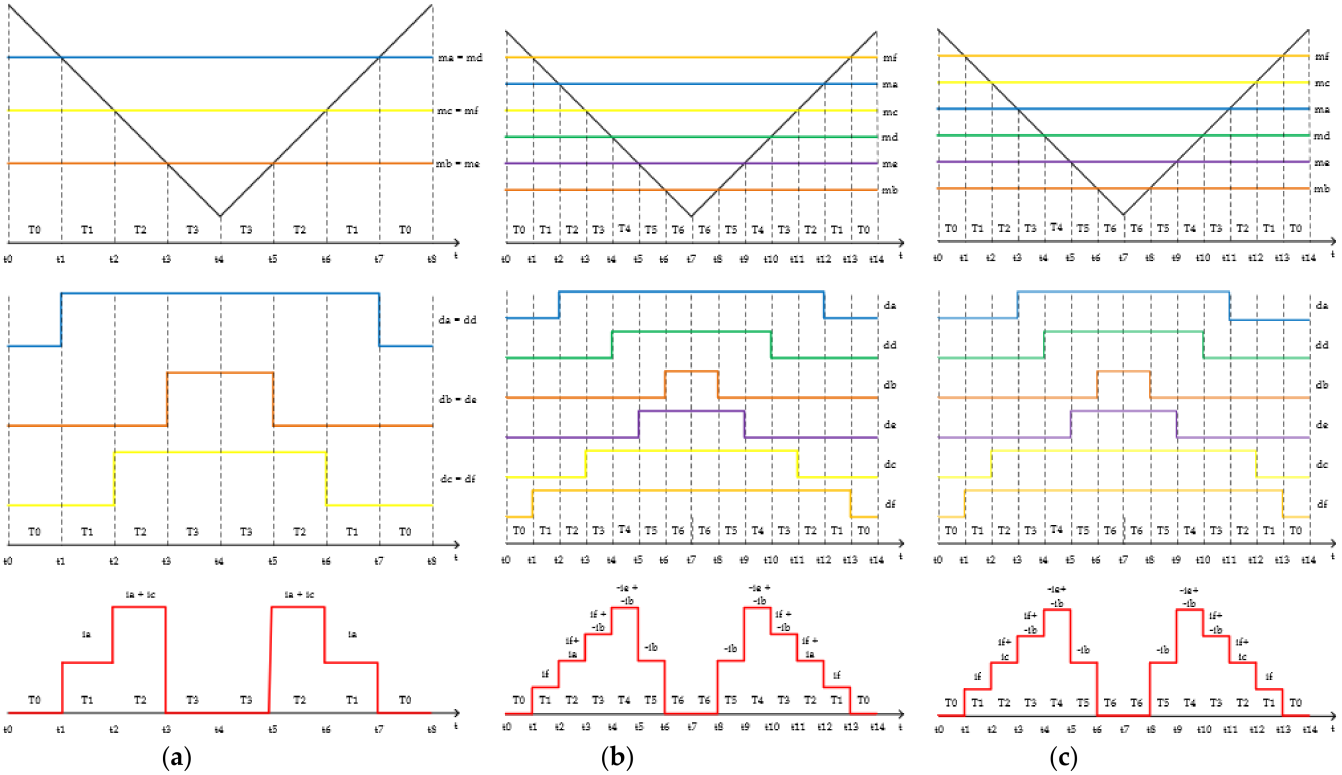
(**a**) (**b**) (**c**)

Figure 4. Phase current waveforms of the 6-phase boost rectifier considering (**a**) $\delta = 0°$, (**b**) $\delta = 60°$, and (**c**) $\delta = 30°$.

By observing the waveforms during a switching period in the interval *A*, Figure 5. can be realized: Figure 5a illustrates the waveforms of modulation depth and the carrier signal (top figure), the duty cycles for each leg (middle figure), and the output current from the converter $i_{bus}(t)$ (bottom figure) in the case of $\delta = 0°$; Figure 5b shows the same waveforms in the case of $\delta = 60°$; and Figure 5c displays the same waveforms, but in the case of $\delta = 30°$. As can be noticed from Figure 5a, it is possible to separate the switching period in eight intervals. The length of the interval T_0–T_3 can be found as in (14), where T_s is the switching period. Next, the average current into the DC-bus can be evaluated for each interval *A*–*F* in the case of $\delta = 0°$, and the solution of the integral to estimate the average current gives the same results for every interval, as reported in (15).

$$\begin{cases} T_0 = \frac{T_s}{2}(1 - d_a) = \frac{T_s}{4}(1 - M\sin\theta) \\ T_1 = \frac{T_s}{2}(d_a - d_c) = \frac{T_s}{4}\left(M\sin\theta - M\sin\left(\theta - \frac{4}{3}\pi\right)\right) \\ T_2 = \frac{T_s}{2}(d_c - d_b) = \frac{T_s}{4}\left(M\sin\left(\theta - \frac{4}{3}\pi\right) - M\sin\left(\theta - \frac{2}{3}\pi\right)\right) \\ T_3 = \frac{T_s}{2}d_b = \frac{T_s}{4}\left(1 + M\sin\left(\theta - \frac{2}{3}\pi\right)\right) \end{cases} \quad (14)$$

$$I_{dc} = \frac{3}{2}MI_m\cos\varphi \quad (15)$$



(**a**) (**b**) (**c**)

Figure 5. DC-bus current stress analysis in a switching period considering (**a**) $\delta = 0°$; (**b**) $\delta = 60°$; and (**c**) $\delta = 30°$.

Regarding the rms current in the case of $\delta = 0°$, in the interval A its value can be estimated from (16), where the ${I_{dc}}^2$ is expressed in (17).

$$I_{rmsA}^2 = \frac{3}{\pi}\int_{\pi/6}^{\pi/2} I_{dcA}^2 d\theta \tag{16}$$

$$I_{dcA}^2 = \frac{1}{T_s}\left[2\int_{t_1}^{t_2}(2i_a)^2 dt + 2\int_{t_2}^{t_3}(-2i_b)^2 dt\right] = 8\frac{T_1}{T_s}{i_a}^2 + 8\frac{T_2}{T_s}{i_b}^2 \tag{17}$$

The same process can be utilized for the other intervals B–F in order to obtain the rms current of the output current $i_{bus}(t)$ of the power converter. The achieved expression of the rms current I_{rms} is reported in (18).

$$I_{rms}^2 = \frac{\sqrt{3}}{\pi} M I_m^2 \left(4\cos^2\varphi + 1\right) \tag{18}$$

Definitively, the rms current I_{Crms} flowing into the equivalent DC-bus capacitor for $\delta = 0°$ can be written as in (19).

$$I_{Crms} = I_m \sqrt{M\left[\frac{\sqrt{3}}{\pi} + \left(\frac{4\sqrt{3}}{\pi} - \frac{9}{4}M\right)\cos^2\varphi\right]} \tag{19}$$

The same procedure can be adopted for $\delta = 60°$. Analyzing the switching period of interval A, as shown in Figure 5b, it is possible to divide it into 14 intervals T_0–T_6. By this means, calculating the average current coming from the converter and repeating the analysis for every interval A–N, even in this case, Equation (15) has been found. With

regard to the rms current I_{rms}, the formula is the same as in the previous case with $\delta = 0°$. In this case, however, the integration period is half of the previous case, as can be noticed when comparing Figure 4a,b. Then, during a switching period of the interval A, I_{rms} can be evaluated as in (20), where ${I_{dc}}^2$ can be carried out as in (21).

$$I_{rmsA}^2 = \frac{6}{\pi}\int_{\pi/6}^{\pi/3} I_{dcA}^2 d\theta = \frac{MI_m^2}{2\pi}\left[3\left(1+\sqrt{3}\right) + \left(4+2\sqrt{3}\right)\cos 2\varphi + \left(19-11\sqrt{3}\right)\sin 2\varphi\right] \tag{20}$$

$$I_{dcA}^2 = 2\frac{T_1}{T_s}{i_f}^2 + 2\frac{T_2}{T_s}\left(i_a + i_f\right)^2 + 2\frac{T_3}{T_s}\left(i_f - i_b\right)^2 + 2\frac{T_4}{T_s}(-i_b - i_e)^2 + 2\frac{T_5}{T_s}(-i_b)^2 \tag{21}$$

Performing the same calculations to obtain the rms current in interval B, the result is not the same as that in (20). In particular, the obtained expression is reported in Equation (22). Evaluating the rms current in the other ten intervals C–N, the equality in (23) can be found.

$$I_{rmsB}^2 = \frac{MI_m^2}{2\pi}\left[3\left(1+\sqrt{3}\right) + \left(4+2\sqrt{3}\right)\cos 2\varphi + \left(11\sqrt{3}-19\right)\sin 2\varphi\right] \tag{22}$$

$$\begin{array}{c} I_{rmsA}^2 = I_{rmsC}^2 = I_{rmsE}^2 = I_{rmsG}^2 = I_{rmsI}^2 = I_{rmsM}^2 \\ I_{rmsB}^2 = I_{rmsD}^2 = I_{rmsF}^2 = I_{rmsH}^2 = I_{rmsL}^2 = I_{rmsN}^2 \end{array} \tag{23}$$

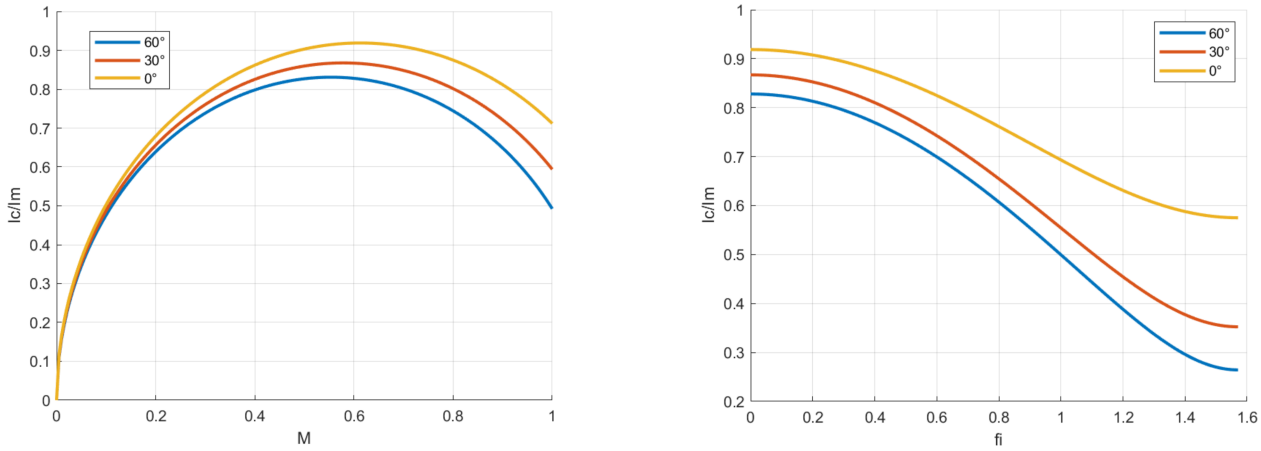
By averaging over the fundamental period, the expressions of the 12 intervals, the rms current I_{Crms} flowing through the equivalent DC-bus capacitor for $\delta = 60°$ can be evaluated as in (24).

$$I_{Crms} = I_m\sqrt{M\left[\frac{\sqrt{3}-1}{2\pi} + \left(\frac{4+2\sqrt{3}}{\pi} - \frac{9}{4}M\right)\cos^2\varphi\right]} \tag{24}$$

Applying the same method seen previously, even in the case of $\delta = 30°$, it is possible to estimate the average current as in (18) for each interval A–T Figure 4c. Instead, like the case of $\delta = 60°$, the rms current can be calculated in each interval A–T and then averaged over the fundamental period. By this means, it is possible to carry out the rms current into the equivalent DC-bus capacitor for $\delta = 30°$, as in (25).

$$I_{Crms} = I_m\sqrt{M\left[\frac{5\sqrt{3}+2\sqrt{6}-4\sqrt{2}-4}{6\pi} + \left(\frac{7\sqrt{3}+4\sqrt{6}+4\sqrt{2}-5}{3\pi} - \frac{9}{4}M\right)\cos^2\varphi\right]} \tag{25}$$

Eventually, the waveforms of I_{Crms} were plotted in MATLAB as a function of φ and M, as shown in Figure 6. The maximum values of the rms DC-bus current, normalized with respect to the peak of the phase current I_m as a function of the phase displacement δ, occur when $\cos\varphi = 1$ and M is close to 0.6 and are listed below: $I_{Crms}/I_m = 0.92$ when $\delta = 0°$, $I_{Crms}/I_m = 0.87$ when $\delta = 30°$, $I_{Crms}/I_m = 0.83$ when $\delta = 60°$.



(**a**) (**b**)

Figure 6. The rms DC-bus current normalized with respect to the peak of the phase current as a function of (**a**) the modulation depth M, and (**b**) the power factor φ, where the yellow line represents $\delta = 0°$, the red line represents $\delta = 30°$, and the blue line represents $\delta = 60°$.

To design a suitable DC-bus capacitor configuration for the 6-phase power conversion system, the second step is the evaluation of the output voltage ripple. To do this, Equation (26) is considered, where v_{C0} is the voltage initial value, ΔV_C is the voltage ripple, and $i_C(t)$ is the instantaneous current into the equivalent DC-bus capacitor reported in (27).

$$v_C = v_{C0} + \frac{1}{C}\int i_C dt = v_{C0} + \Delta V_C \tag{26}$$

$$i_C(t) = i_{bus}(t) - I_{dc} \tag{27}$$

The peak-to-peak voltage ripple can be estimated as in (28) [26].

$$\Delta v_{pp} = \max\{\Delta V_C\}_{T_{sw}} - \min\{\Delta V_C\}_{T_{sw}} \tag{28}$$

The waveforms of the instantaneous current through the equivalent capacitor $i_C(t)$ and the peak-to-peak voltage ripple Δv_{pp} over the switching period when the phase displacement δ is equal to 0° are illustrated in Figure 7. Specifically, the Δv_{pp} can be estimated considering two different cases: in the first, the current I_{dc} is lower than the phase current i_a (case A), as shown in Figure 7a; in the second, the current I_{dc} is greater than the phase current i_a (case B), as illustrated in Figure 7b. As can be seen, on the one hand, the voltage ripple Δv_{pp} shows a symmetric trend, while on the other hand the voltage ripple Δv_{pp} shows an asymmetrical behavior. Subsequently, the maximum voltage ripple Δv_{pp} can be evaluated by integrating i_C over the period $2T_3$ in the first case, and by integrating i_C over the period $2(T_0 + T_1)$ in the second case. The maximum voltage ripple Δv_{pp} can be expressed as in (29), where I_m is the maximum phase current, f_{sw} is the switching frequency, C is the equivalent capacitor value, and r_{pp} can be found as in (30) in case A and as in (31) in case B. By varying $\theta = 2\pi f_0 t$, φ, M, and combining the maximum ripple value between case A and case B, the maximum voltage ripple can be estimated for $\delta = 0°$ as in (32).

$$\Delta v_{pp} = \frac{I_m}{f_{sw}C} r_{pp}(M, \theta, \varphi) \tag{29}$$

$$r_{pp}^{A}(M, \theta, \varphi) = \frac{3}{4} M \cos\varphi \left(1 + M \sin\left(\theta - \frac{2}{3}\pi\right)\right) \tag{30}$$

$$r_{pp}^{B}(M, \theta, \varphi) = \frac{3}{4} M \cos\varphi (1 - M \sin\theta) + \left(\frac{3}{4} M \cos\varphi - \sin(\theta - \varphi)\right)\left(M \sin\theta - M \sin\left(\theta - \frac{4}{3}\pi\right)\right) \tag{31}$$

$$\Delta v_{pp} = \frac{\sqrt{3}}{4}\frac{I_m}{f_{sw}C} \tag{32}$$

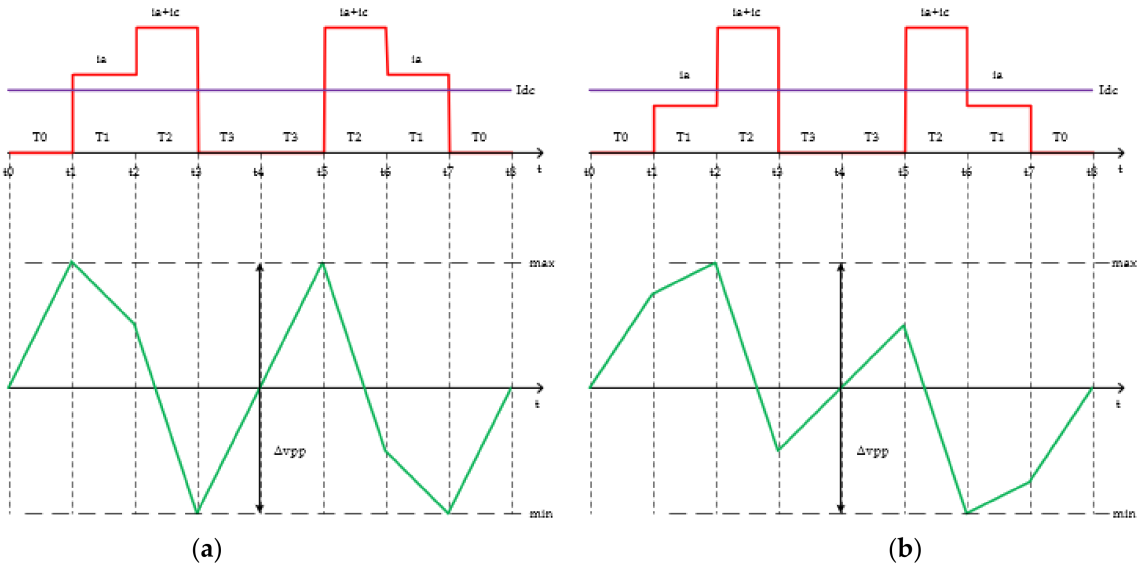


Figure 7. Voltage ripple analysis in the switching period considering $\delta = 0°$, $i_{bus}(t)$ (red trace), I_{dc} (violet trace), and voltage ripple (green trace): (**a**) shows case A, in which I_{dc} is lower than the phase current i_a; (**b**) shows case B, in which I_{dc} is greater than the phase current i_a.

Similarly, it is possible to obtain the voltage ripple Δv_{pp} in the case of $\delta = 30°$ and $\delta = 60°$. Indeed, Figure 8 shows the instantaneous current $i_C(t)$ and the peak-to-peak voltage ripple Δv_{pp} over the switching period when the phase displacement δ is equal to 30° and 60°. In this case, the waveforms, as illustrated in Figure 8, show the same behavior for both $\delta = 30°$ and $\delta = 60°$. By integrating i_C over the period $2T_6$ in case A (Figure 8a), and by integrating i_C over the period $2(T_0 + T_1 + T_2)$ in case B (Figure 8b), it is possible to obtain the maximum voltage ripple as in (29): in (33), the estimated maximum voltage ripple in the case of $\delta = 60°$ is presented; in (34), the estimated maximum voltage ripple in the case of $\delta = 30°$ is stated.

$$\Delta v_{pp} = \frac{\sqrt{3}}{8}\frac{I_m}{f_{sw}C} \tag{33}$$

$$\Delta v_{pp} = 0.261\frac{I_m}{f_{sw}C} \tag{34}$$

Summarizing the obtained results of the voltage ripple Δv_{pp} and rms DC-bus current normalized with respect to the peak of the phase current I_{Crms}/I_m as a function of the phase displacement δ in Table 1, the worst case can be defined when $\delta = 0°$ and the best case when $\delta = 60°$, as expected. It is important to say that if one increases δ over 60° or decreases it, the voltage ripple increases.

Table 1. DC-bus voltage ripple and rms current stress results.

Phase Displacement δ	Voltage Ripple Δv_{pp}	Normalized Current Stress I_{Crms}/I_m
0°	$\Delta v_{pp} = \frac{\sqrt{3}}{4}\frac{I_m}{f_{sw}C}$	0.92
30°	$\Delta v_{pp} = 0.261\frac{I_m}{f_{sw}C}$	0.87
60°	$\Delta v_{pp} = \frac{\sqrt{3}}{8}\frac{I_m}{f_{sw}C}$	0.83

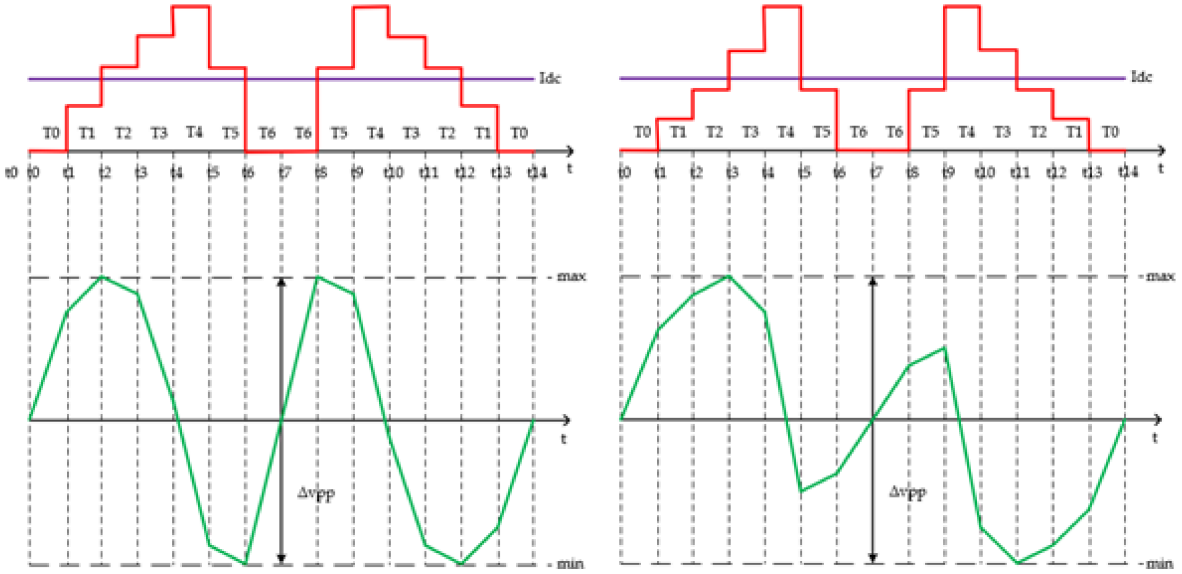


Figure 8. Voltage ripple analysis in the switching period considering $\delta = 30°$ and $\delta = 60°$, $i_{bus}(t)$ (red trace), I_{dc} (violet trace), voltage ripple (green trace): (**a**) shows case A, in which I_{dc} is lower than the phase current i_a; (**b**) shows case B, in which I_{dc} is greater than the phase current i_a.

Assuming the fault tolerance capability, if a converter fails, the power conversion system continues to deliver power, but the voltage ripple will double with respect to the best situation with $\delta = 60°$. For this reason, considering the worst case of $\delta = 0°$ and $\Delta v_{pp} = 0.1\% V_{BUS}$, the required total capacitor value is equal to 278 µF. According to this analysis, 12 TDK film capacitors (2 for each phase leg) in parallel can be used, where the single capacitor is equal to 30 µF. Knowing the equivalent series resistance (ESR) of the selected capacitor, it is possible to estimate the DC-bus capacitor losses as in (35).

$$P_{BUS} = 12ESR(I_{Crms}/12)^2 \tag{35}$$

2.4. Thermal Sizing

Thermal sizing is a fundamental step in the design of a power electronic converter. The aim is to size a heatsink capable of dissipating the heat produced by the power semiconductor devices, assuming negligible losses of the DC-bus capacitors. On the basis of the power losses shown in Figure 3, it is possible to evaluate the maximum value of the thermal resistance in order to choose a suitable heatsink.

The thermal equivalent of Ohm's law is expressed in (36).

$$\Delta T = R_{th} P_{loss} \tag{36}$$

Furthermore, an equivalent thermal circuit can be realized, as shown in Figure 9, in which T_a, T_s, T_c, and T_j are, respectively, the ambient temperature, the heatsink temperature, the case temperature, and the junction temperature of the semiconductor devices; while $R_{th(j\text{-}c)}$ is the thermal resistance between the junction of a device and the case, $R_{th(c\text{-}s)}$ is the thermal resistance between the case and the heatsink, and $R_{th(s\text{-}a)}$ is the thermal resistance between the heatsink and the environment. Assuming the maximum transfer power of 10 kW, a junction temperature $T_j = 120$ °C, and the switching frequency $f_{sw} = 100$ kHz, the maximum temperature leap between the junction temperature of the power semiconductor devices and the case temperature was carried out using Equation (36).

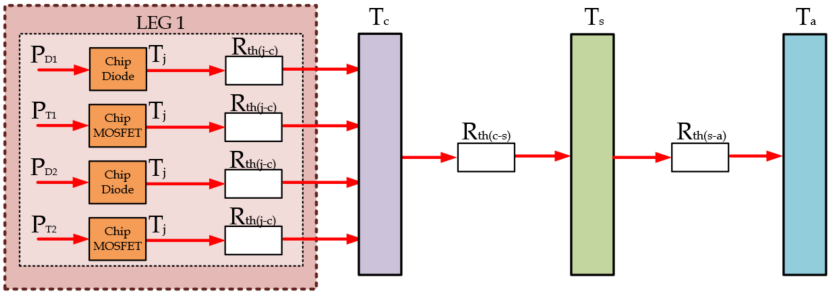


Figure 9. Equivalent thermal circuit.

Then, considering an ambient temperature T_a = 40 °C, it is possible to evaluate the thermal resistance $R_{th(s\text{-}a)}$ between the heatsink and the external environment as in (37), where $P_{loss,T}$ and $P_{loss,D}$ stand for the power losses of the MOSFET and the diode, respectively.

$$R_{th(c-a)} = \frac{T_c - T_a}{6(P_{loss,T} + P_{loss,D})} \tag{37}$$

Assuming the arrangement of three Wolfspeed power modules on a heatsink, the power losses of the MOSFET and the diode have to be multiplied for the number of the power semiconductor devices. By this means, the maximum value of the thermal resistance $R_{th(s\text{-}a)}$ = 0.72 °C/W was found. Since any heatsink with lower thermal resistance than the value obtained is suitable, Fisher Elektronik's SK 47 extruded air heatsink was considered, characterized by a thermal resistance $R_{th(s\text{-}a)}$ = 0.53 °C/W.

3. Results

To validate the proposed analysis, the analytical results were compared to simulated ones using the Plexim/PLECS tool in the MATLAB/Simulink environment. Afterward, a prototype of the converter was built and the experimental results carried out for further validation.

3.1. Simulation Results

To obtain simulation results and compare them with the obtained analytical results, a PLECS model of the power converter was realized and thermal models of the power devices created. The simulation results were carried out considering an input phase voltage of 245 V, a DC-bus voltage of 750 V, and a variable power between 1 kW and 10 kW. Figures 10a and 10b show the power losses and the efficiency related to the only power semiconductors estimated for different switching frequencies: 20 kHz, 60 kHz, and 100 kHz, respectively.

As can be seen from Figure 10b, in the case of power lower than 3 kW, the efficiency at 20 kHz is lower than the ones at 60 kHz and 100 kHz. This happens because the phase current ripple at 20 kHz is much greater than the ripple at 60 kHz and 100 kHz; thus, the power converter works in discontinuous mode for a significant part of the fundamental period. This is confirmed by the fact that the power losses at 20 kHz are higher with respect to 60 kHz and to 100 kHz in the case of output power lower than 3 kW, as shown in Figure 10a. The DC-bus rms current I_{Crms} and voltage ripple Δv_{pp} evaluated for the three phase displacements of 0°, 30°, and 60° are shown in Figure 11a,b. It can be seen in Figure 11a that the simulation results are perfectly superimposed; additionally, as can be noticed from Figure 11b, among the analyzed cases, the worst case for the voltage ripple happens at δ = 0°, whereas the best case for the voltage ripple occurs at δ = 60°.

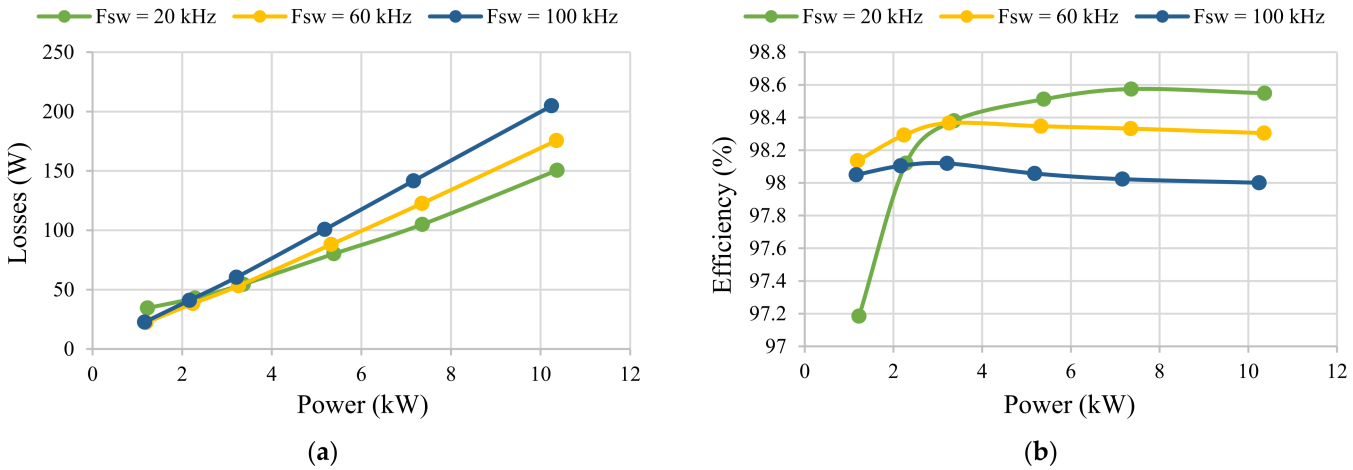


Figure 10. Simulation results of: (**a**) the power losses and (**b**) the power conversion efficiency assuming a switching frequency f_{sw} of 20 kHz (green line), 60 kHz (yellow line), and 100 kHz (blue line).

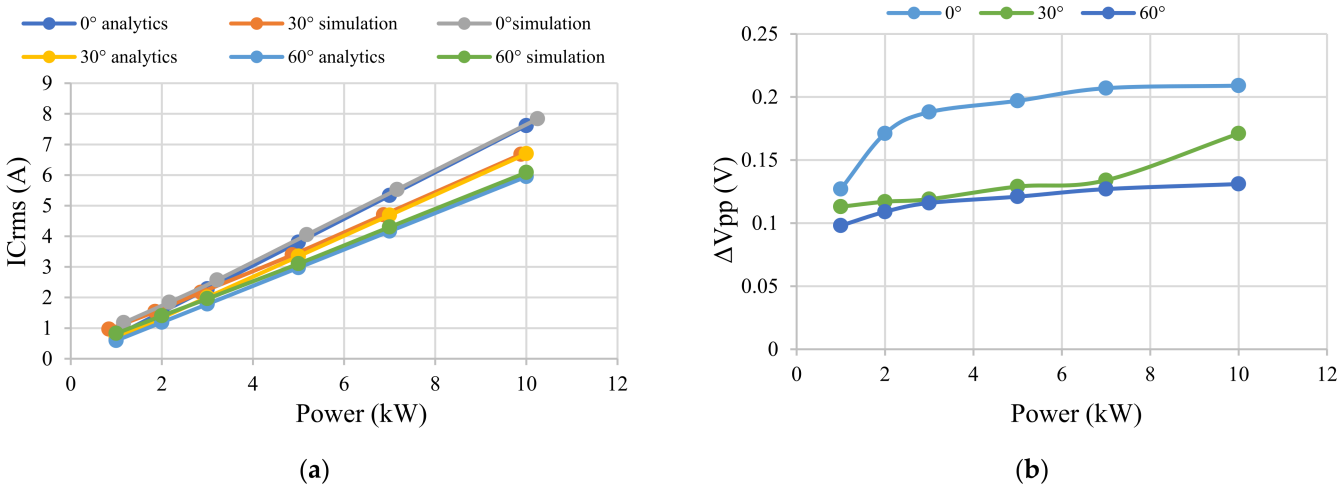


Figure 11. Simulation results of: (**a**) the DC-bus current stress, and (**b**) the voltage ripple.

3.2. Experimental Results

The prototype of the 6-phase boost rectifier was built and the experimental results carried out for further validation of the proposed analysis. The prototype of the 6-phase converter is illustrated in Figure 12. Each phase is equipped with its own driving circuit, current sensor, and two capacitors. The experimental tests were obtained using the 6-phase PMSG with the following parameters: PM machine rated speed equal to 3000 rpm, PM machine pole-pairs equal to 5, PM machine inductance equal to 0.4 mH, and flux equal to 0.11 Wb.

Figure 13a shows the back electromotive force waveforms of the 6-phase PMSG with an rms value of 160 V and the phase angle $\theta = \omega_0 t$, with ω_0 = 150 rad/s. Two of the phase currents of the 6-phase boost rectifier and the DC-bus voltage V_{BUS} are illustrated in Figure 13b, where the rms phase current is about 15 A and V_{BUS} is close to 750 V. Figure 14 shows the trend of the DC-bus rms current stress I_{Crms} and the DC-bus voltage ripple Δv_{pp} as a function of the output power at the phase displacement $\delta = 30°$, obtained by comparing the simulation and experimental results. To validate the 60° electrical drive, a hardware-in-the-loop (HIL) was used.

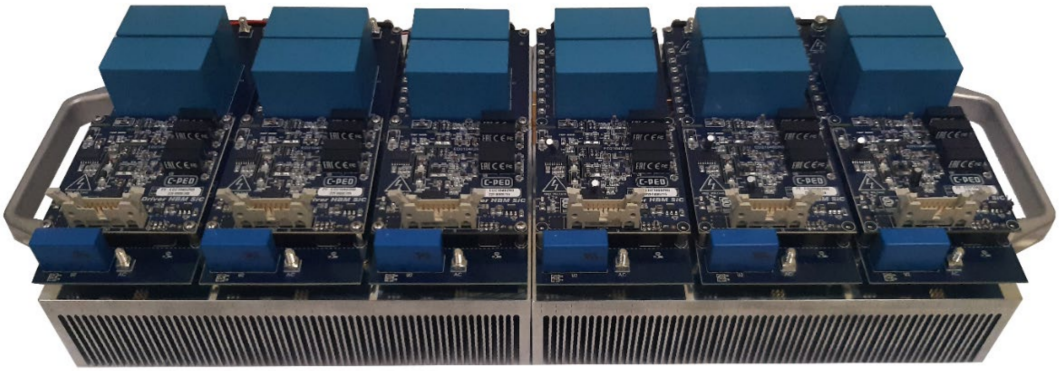
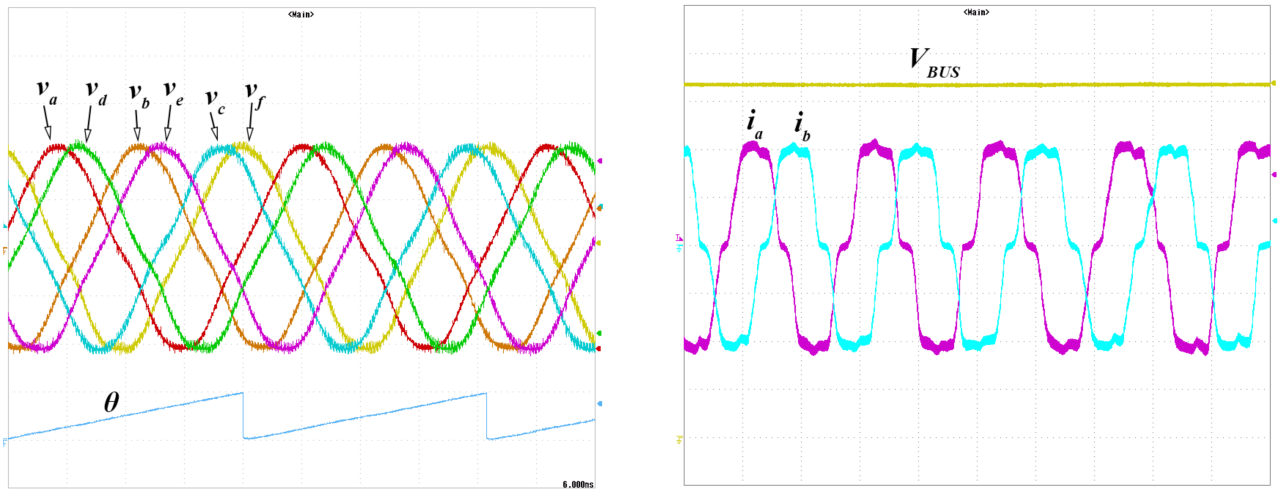
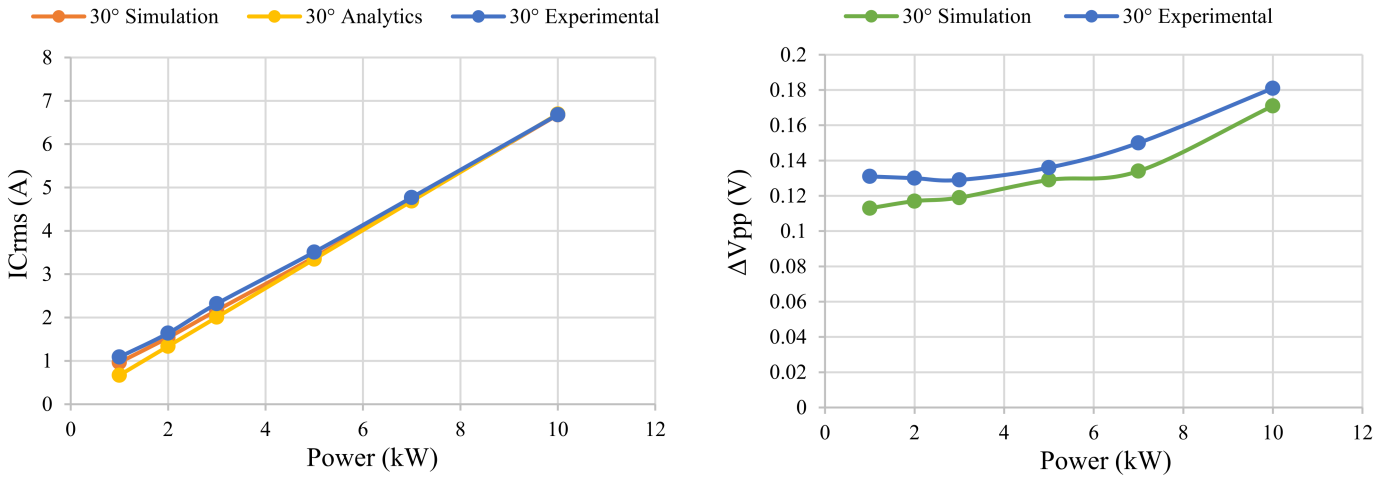


Figure 12. Prototype of the 6-phase boost rectifier.



(**a**) (**b**)

Figure 13. Experimental results of the 6-phase AC–DC converter: (**a**) back electromotive force considering the phase displacement $\delta = 30°$ (100 V/div, 10 ms/div), and (**b**) input current waveforms of two phases and DC-bus voltage V_{BUS} (yellow line) (10 A/div, 100 V/div).



(**a**) (**b**)

Figure 14. Comparison between experimental results, simulation results, and analytics results of: (**a**) the DC-bus rms current stress, and (**b**) the DC-bus voltage ripple power conversion efficiency assuming the phase displacement $\delta = 30°$.

An inverter thermal model was coded for the HIL solver and a real-time simulation was performed. The achieved results are illustrated in Figure 15, which shows the comparison between the analytics and simulation results considering $\delta = 60°$. Moreover, comparing the obtained results in Figures 14 and 15, the good agreement between the 30° and the 60° machines can be seen, validating the proposed approach. Figure 16 illustrates the comparison between the experimental results and the simulations of the conversion efficiency, considering a switching frequency of 60 kHz.

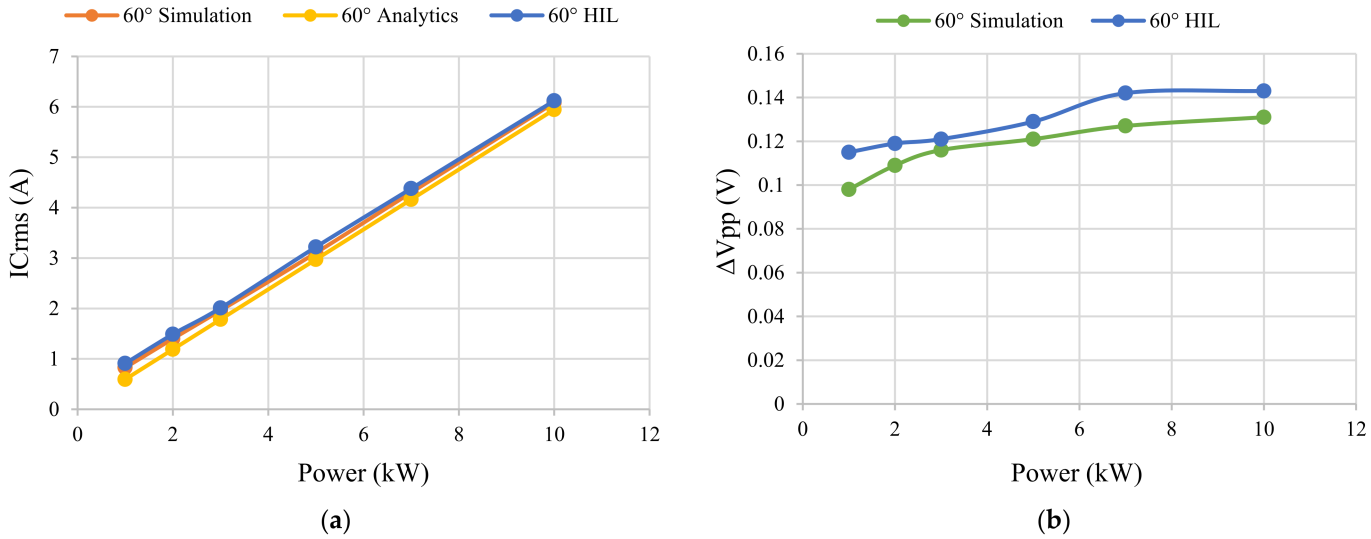


Figure 15. Comparison between HIL results, simulation results, and analytics results of: (**a**) the DC-bus rms current stress, and (**b**) the DC-bus voltage ripple power conversion efficiency assuming the phase displacement $\delta = 60°$.

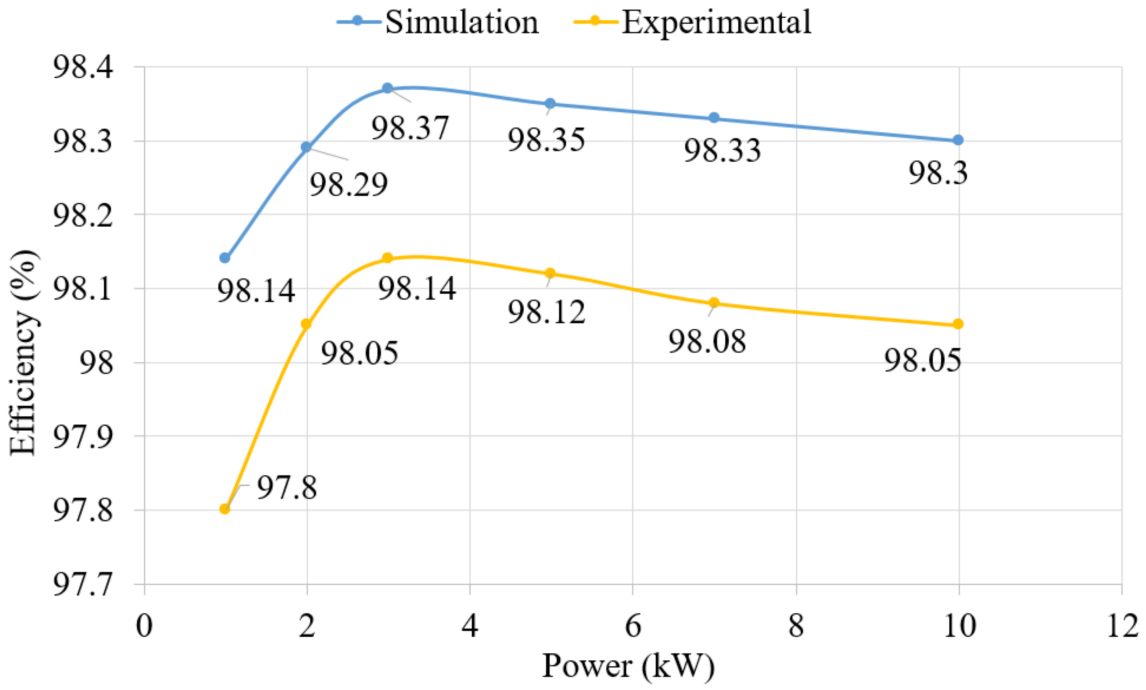


Figure 16. Efficiency as a function of the power: comparison between simulations and experimental results.

4. Conclusions

The design of a 6-phase boost rectifier was carried out. First of all, the SiC MOSFET power module (manufacturer: Wolfspeed, part number: CAB016M12FM3) was selected on the basis of the estimated voltage rating and current rating. Consequently, the power losses and efficiency were calculated for the different values of the switching frequency (20 kHz, 60 kHz, and 100 kHz). The results show that the peak efficiency of the 6-phase boost rectifier was able to reach 98% at 100 kHz switching frequency. Special attention was given to the analysis of both the DC-bus current stress and the output voltage ripple. From the obtained analysis it was found that the worst case of the DC-bus current stress and the output voltage ripple occurred when $\delta = 0°$, while the best case of the DC-bus current stress and the output voltage ripple occurred when $\delta = 60°$. To reach 0.1% V_{BUS} peak-to-peak voltage ripple, 12 film parallel capacitors (manufacturer: TDK, part number: B32778G0306K000) were selected. From the thermal sizing, the extruded air heatsink SK 47 produced by Fisher Elektronik was chosen. The simulation results obtained by creating the model in the Plexim/PLECS environment validated the analytical results. Furthermore, the prototype of the designed 6-phase boost rectifier was realized and the experimental results were carried out, validating the proposed analysis.

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