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Analysis and Design of Independent DC Bus Structure Multiport Power Electronic Transformer Based on Maximum Power Transmission Capability of Low-Voltage DC Ports

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Abstract: Owing to the diverse connection configurations of dual active bridge converters, a multiplicity of low-voltage DC port structures are anticipated to emerge in the independent DC bus structure multiport power electronic transformer (IDBS-MPET). An inadequate low-voltage DC port structure exacerbates the power imbalance in IDBS-MPET, presenting a risk of overmodulation even when transmitting relatively low levels of power. To overcome this limitation, a design scheme of IDBS-MPET topology based on the maximum power transmission capability of the low-voltage DC ports is proposed in this paper. Three topology design rules are derived from the maximum power transmission capability results of more than 80 typical IDBS-MPET topologies. The symmetrical triple cross-phase connection structure, the symmetrical double cross-phase connection structure and the single-phase connection structure are sequentially identified as the three most optimal structures of low-voltage DC ports. By employing the proposed design methodology, each low-voltage DC port achieves its maximum power transfer capability relative to other configurations. The effectiveness of the proposed design scheme is validated by an optimal designed IDBS-MPET topology with six low-voltage DC ports.

Keywords: design scheme; independent DC bus; maximum power transmission capability; multiport power electronic transformer; topology design rules

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1. Introduction

A multiport power electronic transformer (MPET) provides a competitive solution for the networking of hybrid AC/DC distribution systems due to its compatibility and advanced functionalities [1,2]. Most of the existing MPETs provide at least a medium-voltage AC port, a low-voltage AC port and a low-voltage DC port [3]. The medium-voltage AC port is indispensable for absorbing the active power from the AC grid to feed the next stage [4]. Generally, three-phase cascaded H-bridge (CHB) converters are adopted to form the medium-voltage AC port [5–7]. The low-voltage AC port provides the interfaces to conventional AC loads. Nevertheless, compared to the MPET, the conventional line frequency transformer exhibits superior performance in terms of cost-effectiveness, robustness and reliability when supplying power to conventional AC loads.

Due to the massive growth of DC resources and DC loads in the distribution network, the demand for low-voltage DC (LVDC) ports on the MPET significantly surpasses that for the low-voltage AC ports. The LVDC ports provide efficient integration of distributed generation (DG), electric vehicle (EV) charging stations, energy storage systems (ESS), data centers and other industrial DC loads [8,9]. Since the nominal voltage of DGs and DC loads are different, an MPET with multiple LVDC ports is significantly necessary. Multiple LVDC ports provide interfaces with multiple voltage levels and power levels. DGs and

linear/nonlinear DC loads can be connected to different LVDC ports, avoiding adverse interactions of direct electrical coupling.

Generally, isolated bidirectional DC-DC converters, such as dual active bridge (DAB) converters, are adopted in MPETs to produce LVDC links on each of their output terminals [10,11]. For the most part, all of the LVDC links are paralleled together to form a common DC bus, and thus only one LVDC port of single voltage level is provided [12–14]. In the later stage of the common DC bus, additional DC/DC converters are needed to meet the access requirements of DGs and DC loads of different voltage levels. These additional DC/DC converters increase the hardware cost and reduce the system efficiency.

In [15], a five-terminal hybrid AC/DC microgrid with four LVDC ports was proposed. The topology of the microgrid is the same as that of the MPET. Multiple LVDC ports are naturally obtained by separating the common DC bus into four parts without adding any additional converters. Moreover, the LVDC ports are electrically isolated from each other and each of them can be protected from the faults of the other ones. Based on the topology proposed in [15], the independent DC bus structure multiport power electronic transformer (IDBS-MPET) can be constructed. The output voltage of DABs can be controlled to meet the requirements of multiple voltage levels. The parallel quantities of DABs can be configured to meet the requirements of multiple power levels. Compared with the common DC bus structure multiport power electronic transformer (CDBS-MPET), a huge number of power semiconductor devices have been saved in the IDBS-MPET. Since the high-frequency transformer is applied in the DAB, each LVDC port is galvanically isolated from the others.

A typical IDBS-MPET is shown in Figure 1. The DAB features a multitude of output terminal connection methodologies. A diversity of parallel connection configurations for DAB output terminals can be identified. Port 1 consists of three DABs from three different phases. Port 2 comprises one DAB from a single phase. Port 6 involves DABs from two separate phases. The term 'phase' in this paper refers to the AC grid phases a, b or c. If the LVDC port is composed of paralleled DABs from two or three phases, it is called the cross-phase connection port (see Section 2). In addition, in a cross-phase connection port, the quantities of DABs distributed in each phase will be different. Therefore, DGs or DC loads of a cross-phase connection port will be distributed in two phases or three phases, and evenly or unevenly.

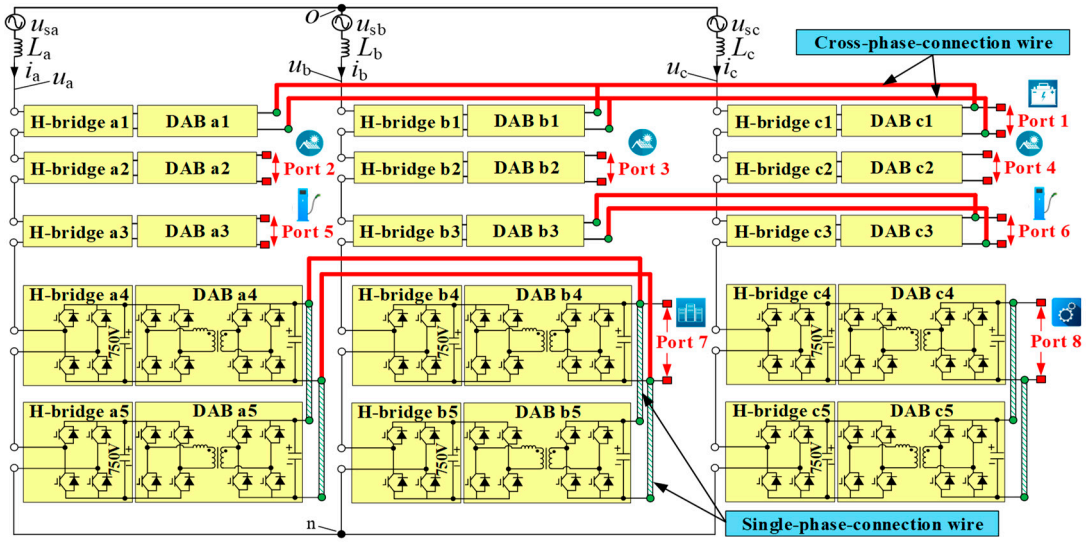

Figure 1. Independent DC bus structure multiport power electronic transformer (IDBS-MPET).

Indeed, the cross-phase-connected converters may have a positive impact on the power balancing of loads. In [16,17], a full-range power auto-balance PET is proposed. Each input-stage-side dc link is connected in parallel to three isolation- and output-stage cascaded converter chains. The three converter chains are cross-phase connected to three

output phases. In the construction of DC ports by the auto-balance PET, additional DC/DC converters are still required; however, this is not the case with the IDBS-MPET. The IDBS-MPET can flexibly and conveniently offer multiple isolated LVDC ports, which presents a significant advantage in future-oriented distribution network scenarios where DC loads are increasingly predominant. In [18,19], a multilevel converter with three AC ports (i.e., AC Port 1~3) is proposed. To avoid power imbalance, H-bridge converters in AC Port 1 are connected to one of the phases either in AC Port 2 or AC Port 3 through DABs. However, the influence of the cross-phase connection patterns of converters on the MPET's ability to deal with power imbalance has not been quantitatively analyzed. The design scheme of the cross-phase connection patterns of converters has not been studied. In the PET discussed in references [18,19], only AC ports are provided, with no provision for DC ports. In contrast, the IDBS-MPET employs a more flexible cross-phase connection approach. When constructing LVDC ports, parallel connection methods for DAB outputs allows for a more flexible distribution of loads across one, two or three phases.

In this paper, a systematic analysis and design scheme of IDBS-MPET is proposed. The main technical contributions of this paper are summarized as follows:

(1) Three basic structures of LVDC ports are established and all of the IDBS-MPET topologies can be derived based on them. Accordingly, the general graphical representation and naming method of the IDBS-MPET are given.
(2) The maximum power transmission capability (MPTC) is proposed to evaluate the capability of the IDBS-MPET to deal with a power imbalance.
(3) Three topology design rules are derived from the MPTC calculation results of more than 80 typical IDBS-MPET topologies. Based on the three topology design rules, the systematic design scheme of the IDBS-MPET topology is proposed. The optimal IDBS-MPET to deal with a power imbalance can be found quickly and easily.

The rest of this article is organized as follows. Section 2 introduces the topology configuration of the IDBS-MPET. In Section 3, the definition and calculation method of MPTC is proposed. In Section 4, three topology design rules and the systematic design scheme of the IDBS-MPET topology is proposed. In Section 5, the IDBS-MPET with six LVDC ports is designed to validate the effectiveness of the proposed design scheme. Section 6 provides a discussion. Finally, the conclusion is drawn in Section 7.

2. Topology Configuration of the IDBS-MPET

This section is composed of three parts. First, an overview of the IDBS-MPET is provided. Second, three basic structures of LVDC ports are established based on the parallel connection patterns of DAB output terminals. Third, a comprehensive graphical depiction and nomenclature approach for the IDBS-MPET are provided.

2.1. Overview of IDBS-MPET

The IDBS-MPET features a comprehensive multiport topology that effectively integrates H-bridge converters and DAB converters to form multiple LVDC ports. The topology is characterized by its three-phase input, with each phase hosting a series of H-bridges coupled to corresponding DABs. These DABs are connected in parallel, which directly yields the LVDC ports (Port 1 to Port 8) without the need for additional DC/DC converters.

As is shown in Figure 1, Port 2, 3, 4 and 5 consist of one DAB from a single phase. Port 8 consists of two DABs from a single phase. The green striped lines are used to indicate the single-phase connection wires. The LVDC port can be formed by the parallel connection of DABs from two phases, such as Port 6 and 7. Since Port 7 consists of four DABs, it will have the power supply ability for the higher power DC load. The red solid lines are used to indicate the cross-phase connection wires. The LVDC port can be formed by the parallel connection of DABs from three phases, such as Port 1. Port 1 consists of three DABs from phases a, b and c, respectively.

The properties of the IDBS-MPET can be expressed as follows:

(1) Lower hardware costs. Without adding any additional DC/DC converters, multiple LVDC ports are directly formed by the parallel connection of DABs. Therefore, a huge amount of power semiconductors in the IDBS-MPET can be saved compared with the CDBS-MPET.
(2) Cross-phase connections are adopted. As multiple LVDC ports are distributed in three phases independently, a power imbalance will arise. To better deal with the problem, the cross-phase connection patterns of DABs are adopted in the IDBS-MPET.
(3) Galvanic isolation. Since there is a high-frequency transformer in each DAB, all of the LVDC ports are galvanically isolated from each other and from the gird as well.
(4) Modularity design. All H-bridges have the same electrical parameters, and so do all DABs. The power level of the entire power electronic transformer can be improved only by expanding the number of modules.

The control techniques employed in the IDBS-MPET include the management of grid current and DC capacitor voltage in the CHB [15], voltage feedback control in the DAB [20], maximum power point control in the photovoltaic (PV) inverter [21], and charging control in EVs and ESS [22,23]. Common-duty-ratio control can be employed for paralleled DABs [24].

In order to quantify the reduction in hardware costs of the IDBS-MPET, a typical application scenario is constructed. In this application scenario, the topology of the IDBS-MPET is shown in Figure 1 and the topology of the CDBS-MPET is shown in Figure 2.

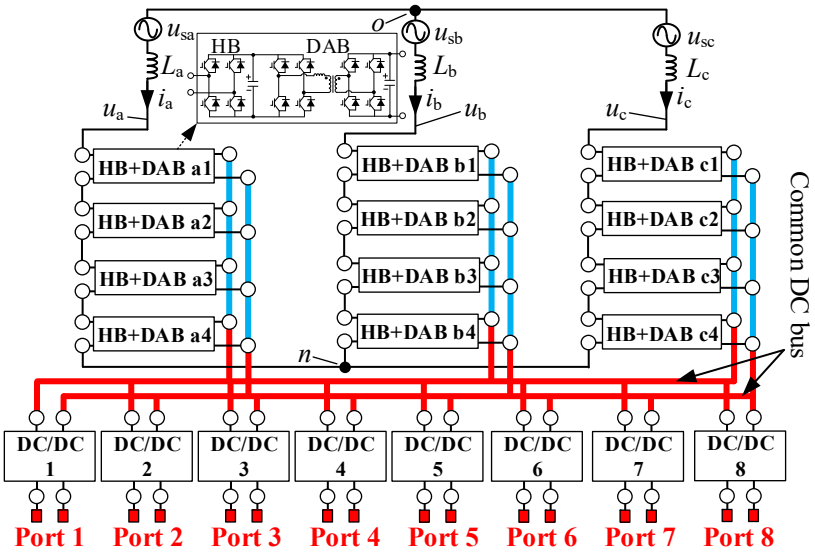

Figure 2. Common DC bus structure multiport power electronic transformer (CDBS-MPET).

Both MPETs have eight LVDC ports (i.e., Port 1 to 8) and the devices connected to Port 1 to 8 are listed in Table 1. The circuit parameters of the H-bridges and DABs in the two MPETs are the same and they are listed in Table 2. Moreover, the additional DC/DC converters (i.e., DC/DC 1 to 8) are needed in the CDBS-MPET to construct eight mutual galvanically isolated LVDC ports of different power levels and voltage levels. As shown in Figure 3, in order to meet the power level requirements, the input-parallel output-parallel (IPOP) DABs are used to construct DC/DC 1 to 8. The n in Figure 3 indicates the amount of IPOP DABs and their specific values are shown in Table 3.

The total power semiconductors in the IDBS-MPET and CDBS-MPET are shown in Figure 4. There are 180 power semiconductors in total used in the H-bridges and DABs of the IDBS-MPET. There are 300 power semiconductors in total used in the H-bridges, DABs and DC/DC 1 to 8 of the CDBS-MPET. In the same application scenario, the IDBS-MPET has reduced the hardware cost of power semiconductors by 40%.

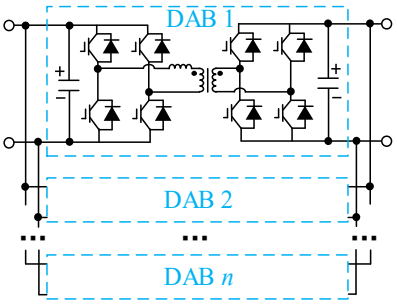

Figure 3. Structure of DC/DC 1 to 8 in CDBS-MPET.

Table 1. Devices connected to the IDBS-MPET and CDBS-MPET.

Port Name	Devices Connected to Port 1 to 8	Nominal Power and Voltages
Port 1	Energy storage	$P_{N,Port1}$ = 240 kW, $V_{N,Port1}$ = 750 V
Port 2	PV	$P_{N,Port2}$ = 80 kW, $V_{N,Port2}$ = 600 V
Port 3	PV	$P_{N,Port3}$ = 80 kW, $V_{N,Port3}$ = 600 V
Port 4	PV	$P_{N,Port4}$ = 80 kW, $V_{N,Port4}$ = 600 V
Port 5	EV fast charger	$P_{N,Port5}$ = 80 kW, $V_{N,Port5}$ = 400 V
Port 6	EV ultra-fast charger	$P_{N,Port6}$ = 160 kW, $V_{N,Port6}$ = 800 V
Port 7	Data center	$P_{N,Port7}$ = 320 kW, $V_{N,Port7}$ = 400 V
Port 8	Industrial load	$P_{N,Port8}$ = 160 kW, $V_{N,Port8}$ = 750 V

Table 2. Circuit parameters of the IDBS-MPET and CDBS-MPET.

Circuit Parameters	Value
Nominal grid line-to-line voltage RMS	2500 V
Number of H-bridge cells per phase	5
H-bridge DC voltage	750 V
DAB high-frequency transformer turn ratio	1:1
Nominal power of H-bridge	$P_{N,Hbridge}$ = 80 kW
Nominal power of DAB	$P_{N,DAB}$ = 80 kW

Table 3. The number of IPOP DABs in DC/DC 1 to 8 in the CDBS-MPET.

Name	Number of IPOP DABs
DC/DC 1	3
DC/DC 2	1
DC/DC 3	1
DC/DC 4	1
DC/DC 5	1
DC/DC 6	2
DC/DC 7	4
DC/DC 8	2

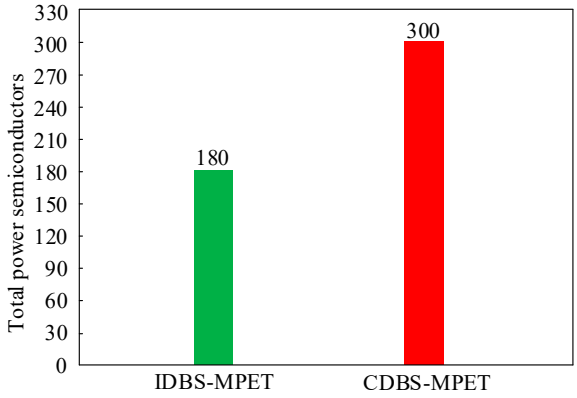

Figure 4. Total number of power semiconductors in IDBS-MPET and CDBS-MPET.

2.2. Basic Structure of LVDC Ports

Based on the connection patterns of DAB output terminals, three basic structures of LVDC ports are established. All kinds of IDBS-MPETs can be derived from the combination of the three basic structures. As is shown in Figure 5, they are the single-phase connection port (S-Port), the double cross-phase connection port (D-Port) and the triple cross-phase connection port (T-Port). In Figure 5, k, k′ and k″ all denote the grid phase a, b or c, whereas $k \neq k' \neq k''$.

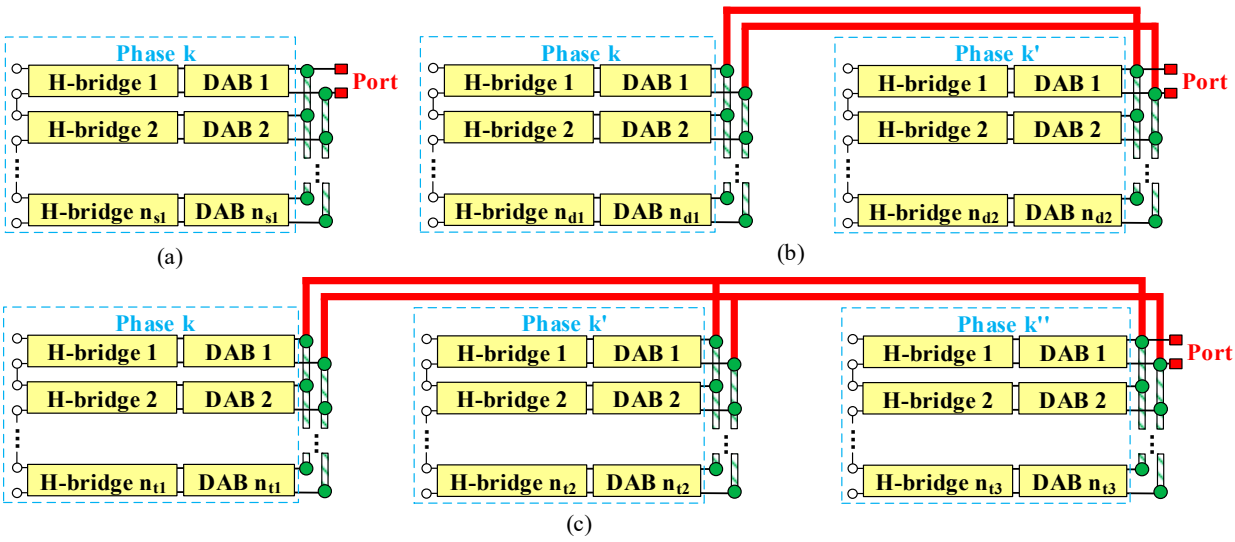

Figure 5. Basic structures of LVDC ports. (**a**) Single-phase connection port (S-Port). (**b**) Double cross-phase connection port (D-Port). (**c**) Triple cross-phase connection port (T-Port).

The S-Port consists of n_{s1} DABs from phase k. As shown in Figure 1, Port 2, Port 3, Port 4, Port 5 and Port 8 belong to the category S-Port. The DGs and DC loads connected to the S-Port are distributed in one phase. The D-Port consists of n_{d1} DABs from phase k and n_{d2} DABs from phase k′. The DGs and DC loads connected to the D-Port are distributed in two phases, evenly or unevenly. If $n_{d1} = n_{d2}$, the D-Port is denoted as a symmetrical D-Port; otherwise, it is denoted as an asymmetrical D-Port. As shown in Figure 1, Port 6 and Port 7 belong to the category D-Port and both of them are symmetrical D-Ports. The T-Port consists of n_{t1} DABs from phase k, n_{t2} DABs from phase k′ and n_{t3} DABs from phase k″. The DGs and DC loads connected to the T-Port are distributed in three phases, evenly or unevenly. If $n_{t1} = n_{t2} = n_{t3}$, the T-Port is denoted as a symmetrical T-Port; otherwise, it is denoted as an asymmetrical T-Port. As shown in Figure 1, Port 1 belongs to the category T-Port and it is a symmetrical T-Port.

2.3. Comprehensive Graphical Depiction and Nomenclature Approach for the IDBS-MPET

In order to simplify the representation of the IDBS-MPET, a comprehensive graphical depiction and nomenclature approach for the IDBS-MPET are established. The comprehensive graphical depiction and nomenclature of LVDC ports are shown in Figure 6 and Table 4. Each H-bridge and its connected DAB are combined and represented by one block. Port is abbreviated to the letter P. Red solid lines are still used to indicate the cross-phase connection wire and green striped lines are still used to indicate the single-phase connection wire. As is shown in Figure 7, it is the graphical representation of the IDBS-MPET in Figure 1.

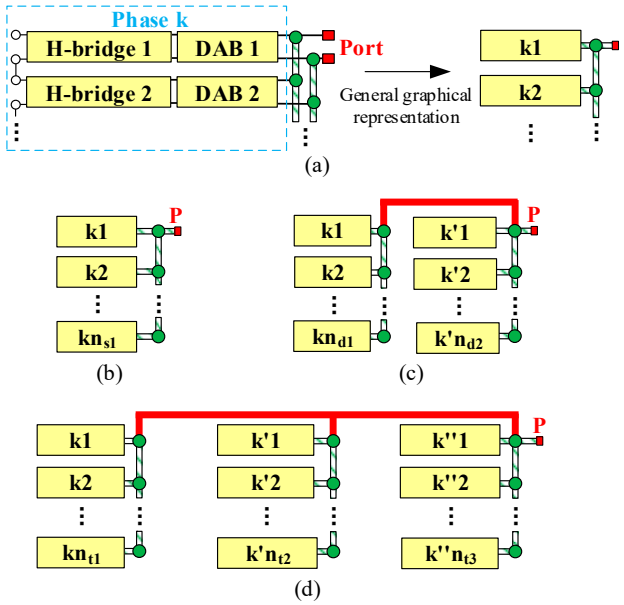

Figure 6. Graphical representation of LVDC ports. (**a**) General graphical representation of cascaded H-bridge and DAB. (**b**) S-Port. (**c**) D-Port. (**d**) T-Port.

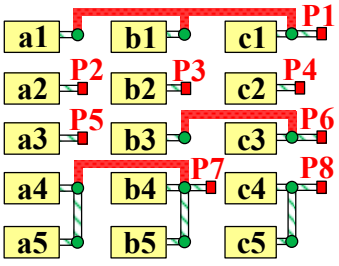

Figure 7. Graphical representation and naming of IDBS-MPET in Figure 1.

Table 4. Naming of LVDC ports.

Kinds of LVDC Ports	Naming
S-Port	$S_{(ns)(ns1)}$
D-Port	$D_{(nd)(nd1,\ nd2)}$
T-Port	$T_{(nt)(nt1,nt2,nt3)}$

The S-Port is named as $S_{(n_s)(n_{s1})}$. This means that there exists n_s S-Ports and each of them consists of n_{s1} DABs. The D-Port is named as $D_{(n_d)(n_{d1},\ n_{d2})}$. This means that there exists n_d D-Ports and each of them consists of n_{d1} DABs from phase k and n_{d2} DABs from phase k′. The T-Port is named as $T_{(n_t)(n_{t1},\ n_{t2},\ n_{t3})}$. This means that there exists n_t T-Ports and

each of them consists of n_{t1} DABs from phase k, n_{t2} DABs from phase k′ and n_{t3} DABs from phase k″.

The naming of the whole IDBS-MPET can be obtained by adding another two indicators, namely, the total quantity of H-bridge converters per phase $N_{(N_H)}$ and the total quantity of LVDC ports $P_{(N_P)}$. The $N_{(N_H)}$ indicates that there are in total N_H H-bridge converters per phase and the $P_{(N_P)}$ indicates that there are N_P LVDC ports in total. Thus, the naming of the IDBS-MPET is expressed as follows:

$$N_{(N_H)}P_{(N_P)}\text{-}S_{(n_s)(n_{s1})}D_{(n_d)(n_{d1},\,n_{d2})}T_{(n_t)(n_{t1},n_{t2},n_{t3})} \tag{1}$$

In (1), the $N_{(N_H)}P_{(N_P)}$ is called the general description part and the $S_{(n_s)(n_{s1})}D_{(n_d)(n_{d1},\,n_{d2})}$ $T_{(n_t)(n_{t1},n_{t2},n_{t3})}$ is called the LVDC port description part, written in the S, D and T sequence. The S, D and T sequence is not necessarily in one-to-one correspondence with the sequence of port numbers 1, 2, 3 and so on. The purpose of the LVDC port description part is to indicate which kinds and how many of the three basic structures of LVDC ports are used in the IDBS-MPET. In addition, it is worth mentioning that (1) is the standard form of IDBS-MPET naming. If there is more than one kind of S-Port, D-Port or T-Port in the IDBS-MPET, the $S_{(n_s)(n_{s1})}$, $D_{(n_d)(n_{d1},\,n_{d2})}$ or $T_{(n_t)(n_{t1},n_{t2},n_{t3})}$ will recur more than once in (1). The naming of the IDBS-MPET in Figure 7 will be $N_{(5)}P_{(8)}\text{-}S_{(4)(1)}S_{(1)(2)}D_{(1)(1,1)}D_{(1)(2,2)}T_{(1)(1,1,1)}$.

3. MPTC Definition and Calculation Method

Due to the various structures of LVDC ports, the DGs or DC loads of each LVDC port will be distributed in one phase, two phases or three phases, and evenly or unevenly. A power imbalance will arise in the IDBS-MPET among three phases and among H-bridge converters of each phase. When the DGs and DC loads are distributed in three phases extremely unevenly, the power imbalance will become severe, resulting in the instability of the IDBS-MPET. The optimal IDBS-MPET is the one with the maximum capability to deal with a power imbalance. In order to evaluate the capability, the MPTC is proposed in this section. This section is composed of two parts. First, the definition of the MPTC is proposed. Second, the calculation method of the MPTC is proposed.

3.1. MPTC Definition

The MPTC of an LVDC port is calculated under the condition that the IDBS-MPET operates safely and stably. However, the maximum allowable phase voltage of three-phase CHB converters is lower than the sum of the H-bridge converters' DC voltages in this phase. In addition, the maximum allowable AC voltage of each H-bridge converter is lower than its DC voltage. The over modulation of the IDBS-MPET AC phase voltage and the over modulation of the H-bridge converter AC voltage should be avoided. Thus, the constraints of the modulation ratio are expressed as follows:

$$\forall k \in \{a,b,c\}, j_n \in \{1,\ldots,N_H\} \quad \begin{cases} m_k \le 1 \\ m_{kj_n} \le 1 \end{cases} \tag{2}$$

where m_k is the modulation ratio of phase k; m_{kjn} is the modulation ratio of the j_nth H-bridge in phase k.

Then, the rated power of an LVDC port can be defined. Due to the modular design of the IDBS-MPET, the rated power of all of the DABs is the same. Let $P_{N,DAB}$ be the rated power of one DAB. If Port j consists of n_j DABs, the rated power of Port j is defined as follows:

$$P_{N,Port\,j} = n_j P_{N,DAB} \tag{3}$$

Except for Port i, if each of the other N_P-1 LVDC ports is connected to a DC load equal to the rated power of the port, it can be expressed as follows:

$$\forall j \in \{1,\ldots,N_P\}, j \ne i \quad P_{load,Port\,j} = P_{N,Port\,j} \tag{4}$$

where $P_{\text{load,Port}j}$ is the power of the DC load connected to Port j.

Then, the MPTC of Port i is defined as follows:

$$\varepsilon_{\text{MPTC,Port}i} = \frac{|P_{\text{max,Port}i} - P_{\text{min,Port}i}|}{P_{\text{N,Port}i}} \tag{5}$$

where $P_{\text{max,Port}i}$ is the maximum output power of Port i when (2) and (4) are satisfied; $P_{\text{min,Port}i}$ is the minimum output power of Port i when (2) and (4) are satisfied. The positive direction of power is defined as the direction of output power. When $P_{\text{max,Port}i}$ or $P_{\text{min,Port}i}$ assumes a positive value, this denotes the connection of a DC load to Port i, with the resultant output power being $P_{\text{max,Port}i}$ or $P_{\text{min,Port}i}$, respectively. Conversely, a negative value for $P_{\text{max,Port}i}$ or $P_{\text{min,Port}i}$ indicates the attachment of a DG to Port i. The input power to Port i is quantified as the absolute value of $P_{\text{max,Port}i}$ or $P_{\text{min,Port}i}$. From the standpoint of power flow directions, DGs can be conceptualized as negative DC loads. A detailed analysis regarding this topic is presented in Section 3.2.

The MPTC of an LVDC port should be calculated and evaluated under a unified criterion. Thus, as shown in (4) and (5), the MPTC of Port i is defined under the criterion that other LVDC ports are connected to DC loads equal to their rated power. The MPTC implies the capability of an LVDC port to adapt to load power change. Specifically, the larger value of the MPTC indicates that the LVDC port is highly adaptable to load power change. Therefore, the MPTC can be used to evaluate the construction method of LVDC ports. The structure of LVDC ports with a larger MPTC value is more preferable.

After the construction method of the LVDC ports is established based on the MPTC, all LVDC ports will be designed following it. Thus, the whole IDBS-MPET will be highly adaptable to load power change. In order to determine the optimal IDBS-MPET topology, the MPTC of the whole IDBS-MPET is proposed to evaluate the IDBS-MPET topology. It is defined as the sum of the MPTCs of all LVDC ports:

$$\varepsilon_{\text{MPTC,MPET}} = \sum_{i=1}^{N_{\text{P}}} \varepsilon_{\text{MPTC,Port}i} \tag{6}$$

3.2. MPTC Calculation Method

As shown in (5), $\varepsilon_{\text{MPTC,Port}i}$ can be obtained when $P_{\text{N,Port}i}$, $P_{\text{max,Port}i}$ and $P_{\text{min,Port}i}$ are determined. In the proposed MPTC calculation method, $P_{\text{max,Port}i}$ and $P_{\text{min,Port}i}$ will be obtained by an exhaustive search method, while (2) and (4) must be satisfied. Since $P_{\text{N,Port}i}$ and $P_{\text{N,Port}j}$ are determined when designing the electrical parameters of the whole IDBS-MPET, only the modulation ratios in (2) will be left to be determined before exhaustive searching.

Firstly, the modulation ratios of AC phase voltage m_{a}, m_{b} and m_{c} are calculated. When the load power of each DC port is uneven, power imbalance problems will arise. One efficient way to solve the interphase power imbalance of three-phase CHB converters is to inject a zero-sequence component into the converter output voltages. The fundamental component of the IDBS-MPET AC phase voltage and AC phase current can be expressed as follows:

$$\begin{cases} u_{\text{a}} = U_{\text{p}} \sin(\omega t) + U_0 \sin(\omega t + \theta_0) \\ u_{\text{b}} = U_{\text{p}} \sin(\omega t - \frac{2}{3}\pi) + U_0 \sin(\omega t + \theta_0) \\ u_{\text{c}} = U_{\text{p}} \sin(\omega t + \frac{2}{3}\pi) + U_0 \sin(\omega t + \theta_0) \end{cases} \tag{7}$$

$$\begin{cases} i_{\text{a}} = I_{\text{p}} \sin(\omega t + \varphi_{\text{p}}) \\ i_{\text{b}} = I_{\text{p}} \sin(\omega t - \frac{2}{3}\pi + \varphi_{\text{p}}) \\ i_{\text{c}} = I_{\text{p}} \sin(\omega t + \frac{2}{3}\pi + \varphi_{\text{p}}) \end{cases} \tag{8}$$

where U_{p} is the amplitude of the positive sequence component of the IDBS-MPET AC phase voltage; U_0 and θ_0 are the amplitude and phase angle of zero-sequence voltage (ZSV); I_{P} is the amplitude of the positive sequence component of the IDBS-MPET AC phase current; φ_{p} is the power factor angle; ω is the angular frequency of the grid voltage.

As the IDBS-MPET mainly deals with active power, the reactive power exchanged with the power grid is very small, which can be considered as $\varphi_{\mathrm{p}} = 0$. Then, the three-phase power of the IDBS-MPET can be calculated from (7) and (8):

$$\begin{cases} P_a = \frac{1}{2}U_{\mathrm{p}}I_{\mathrm{p}} + \frac{1}{2}U_0 I_{\mathrm{p}}\cos(\theta_0) \\ P_b = \frac{1}{2}U_{\mathrm{p}}I_{\mathrm{p}} + \frac{1}{2}U_0 I_{\mathrm{p}}\cos(\theta_0 + \frac{2}{3}\pi) \\ P_c = \frac{1}{2}U_{\mathrm{p}}I_{\mathrm{p}} + \frac{1}{2}U_0 I_{\mathrm{p}}\cos(\theta_0 - \frac{2}{3}\pi) \end{cases} \tag{9}$$

Based on (7) and (9), the U_0 and sine and cosine representation of θ_0 can be obtained as follows:

$$\begin{cases} U_0 = \frac{X_1}{\sqrt{3}I_{\mathrm{p}}} \\ \sin(\theta_0) = \frac{3U_{\mathrm{p}}I_{\mathrm{p}} - 2P_{\mathrm{a}} - 4P_{\mathrm{b}}}{X_1} \\ \cos(\theta_0) = \frac{2\sqrt{3}P_{\mathrm{a}} - \sqrt{3}U_{\mathrm{p}}I_{\mathrm{p}}}{X_1} \end{cases} \tag{10}$$

where

$$X_1 = \sqrt{(3U_{\mathrm{p}}I_{\mathrm{p}} - 2P_{\mathrm{a}} - 4P_{\mathrm{b}})^2 + 3(2P_{\mathrm{a}} - U_{\mathrm{p}}I_{\mathrm{p}})}. \tag{11}$$

According to the basic properties of trigonometric function, for any real number A, B and any angle α, β, the amplitude M_{Amp} of $A\sin(\alpha) + B\sin(\beta)$ is calculated as follows:

$$M_{\mathrm{Amp}} = \sqrt{A^2 + B^2 + 2AB\cos(\alpha - \beta)} \tag{12}$$

Based on (7), (10) and (12), the amplitudes of u_{a}, u_{b} and u_{c} can be expressed as follows:

$$\begin{cases} u_{\mathrm{am}} = \frac{\sqrt{9U_{\mathrm{p}}^2I_{\mathrm{p}}^2 - 12U_{\mathrm{p}}I_{\mathrm{p}}P_{\mathrm{a}} - 24U_{\mathrm{p}}I_{\mathrm{p}}P_{\mathrm{b}} + X_2}}{\sqrt{3}I_{\mathrm{p}}} \\ u_{\mathrm{bm}} = \frac{\sqrt{9U_{\mathrm{p}}^2I_{\mathrm{p}}^2 - 24U_{\mathrm{p}}I_{\mathrm{p}}P_{\mathrm{a}} - 12U_{\mathrm{p}}I_{\mathrm{p}}P_{\mathrm{b}} + X_2}}{\sqrt{3}I_{\mathrm{p}}} \\ u_{\mathrm{cm}} = \frac{\sqrt{27U_{\mathrm{p}}^2I_{\mathrm{p}}^2 - 36U_{\mathrm{p}}I_{\mathrm{p}}P_{\mathrm{a}} - 36U_{\mathrm{p}}I_{\mathrm{p}}P_{\mathrm{b}} + X_2}}{\sqrt{3}I_{\mathrm{p}}} \end{cases} \tag{13}$$

where

$$X_2 = 16P_{\mathrm{a}}^2 + 16P_{\mathrm{a}}P_{\mathrm{b}} + 16P_{\mathrm{b}}^2. \tag{14}$$

Let u_{dc} be the reference DC voltage of all of the H-bridge converters in the IDBS-MPET. In a steady state, the actual DC voltage of all of the H-bridge converters will track the reference value u_{dc}. Then, the modulation ratios of the AC phase voltage are expressed as follows:

$$m_k = \frac{u_{km}}{N_{\mathrm{H}}u_{\mathrm{dc}}} \tag{15}$$

Secondly, the modulation ratio m_{kjn} is calculated. In order to calculate m_{kjn}, the allocation of u_k on H-bridge kj_n must be determined. As shown in Figure 8, since the AC current of all H-bridges in phase k is the same, the allocation ratio of u_k on each H-bridge is the ratio of their output power [25]:

$$\frac{u_{\mathrm{ac},kj_n,\mathrm{m}}}{P_{\mathrm{H},kj_n}} = \frac{u_{k\mathrm{m}}}{P_k} \tag{16}$$

where $u_{\mathrm{ac},kjn}$ is the fundamental component of the H-bridge kj_n AC voltage; $u_{\mathrm{ac},kjn,\mathrm{m}}$ is the amplitude of $u_{\mathrm{ac},kjn}$; $P_{\mathrm{H},kjn}$ is the output power of the H-bridge kj_n. It is noted that (16) is valid under the condition that $P_{\mathrm{H},kjn}$ and P_k are all positive. If the H-bridge kj_n is absorbing power from the next stage, $P_{\mathrm{H},kjn}$ will be negative. Considering that P_k may also be positive or negative, the allocation ratio of $u_{\mathrm{c,F}}$ can be expressed as follows:

$$\frac{u_{\mathrm{ac},kj_n,\mathrm{m}}}{\left|P_{\mathrm{H},kj_n}\right|} = \frac{u_{k\mathrm{m}}}{|P_k|} \tag{17}$$

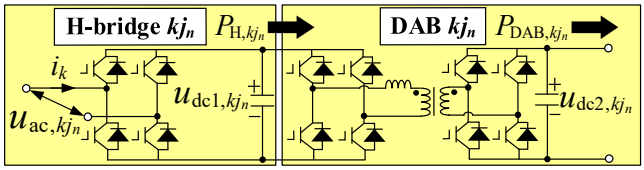

Figure 8. Structure of H-bridge and DAB.

Moreover, m_{kjn} can be calculated based on (17):

$$m_{kj_n} = \frac{u_{\mathrm{ac},kj_n,\mathrm{m}}}{u_{\mathrm{dc1},kj_n}} = \frac{u_{\mathrm{ac},kj_n,\mathrm{m}}}{u_{k\mathrm{m}}} \frac{u_{k\mathrm{m}}}{u_{\mathrm{dc1},kj_n}} = \left| \frac{P_{\mathrm{H},kj_n}}{P_k} \right| \frac{u_{k\mathrm{m}}}{u_{\mathrm{dc1},kj_n}} \tag{18}$$

where $u_{\mathrm{dc1},kjn}$ is the DC voltage of the H-bridge kj_n.

Ignoring the differences in efficiency among H-bridge converters and the differences in efficiency among DAB converters, (18) can be expressed as follows:

$$m_{kj_n} = \left| \frac{P_{\mathrm{DAB},kj_n}}{P_k} \right| \frac{u_{k\mathrm{m}}}{u_{\mathrm{dc1},kj_n}} \tag{19}$$

where $P_{\mathrm{DAB},kjn}$ is the output power of the DAB kj_n.

As mentioned before in this section, the actual DC voltage of all of the H-bridges will track the reference value u_{dc} in a steady state. Thus, (19) can be finally expressed as follows:

$$m_{kj_n} = \alpha_{kj_n} \frac{u_{k\mathrm{m}}}{u_{\mathrm{dc}}} \tag{20}$$

where

$$\alpha_{kj_n} = \left| \frac{P_{\mathrm{DAB},kj_n}}{P_k} \right|. \tag{21}$$

Generally, power balance control is applied on the parallel connected DABs. If Port j consists of n_j DABs and its output power is $P_{\mathrm{load,Port}j}$, the output power of each DAB will be $P_{\mathrm{load,Port}j}/n_j$ in a steady state. The $P_{\mathrm{DAB},kjn}$ is equal to $P_{\mathrm{load,Port}j}/n_j$. All of the $P_{\mathrm{load,Port}i}$ satisfying (2) and (4) will be found by exhaustive searching using Matlab and stored in an array. Then, $P_{\mathrm{max,Port}i}$ and $P_{\mathrm{min,Port}i}$ can be found in the array. Finally, $\varepsilon_{\mathrm{MPTC,Port}i}$ can be calculated based on (5).

4. The IDBS-MPET Design Scheme

In this section, a systematic design scheme of IDBS-MPET topology is proposed. The key point of designing an IDBS-MPET is to design the structures of the LVDC ports. The LVDC port of a larger MPTC indicates that it is highly adaptable to power change. Three topology design rules are derived from the MPTC results of LVDC ports in more than 80 typical IDBS-MPET topologies. Based on the three topology design rules, the systematic design scheme of IDBS-MPET topology is proposed. All of the LVDC ports in a newly designed IDBS-MPET will be constructed following the three topology design rules.

This section is composed of three parts. First, the analysis of the MPTC results is given. Second, three topology design rules are derived from the MPTC results. Third, the design scheme of the IDBS-MPET is proposed.

Limited by the length of this paper, only a few typical IDBS-MPET topologies and their MPTC calculation results of LVDC ports are presented in the main body. The other IDBS-MPET topologies and their MPTC calculation results are listed in the supplementary material of this paper.

4.1. Analysis of MPTC Results

Based on (15) and (20), U_{p}, u_{dc} and N_{H} should be determined before the power searching of $P_{\mathrm{load,Port}i}$ mentioned in Section 3. The rated modulation ratio m_{N} indicates the relationship of the three elements and it is defined as follows:

$$m_N = \frac{U_{\mathrm{p}}}{u_{\mathrm{dc}} N_{\mathrm{H}}} \tag{22}$$

In this paper, the MPTC calculation results of LVDC ports in all of the IDBS-MPETs are obtained under m_{N} = 0.5, 0.6, 0.7, 0.8 and 0.9. The IDBS-MPETs of $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$ (i.e., N_{H} = 6 and N_{P} = 3) are shown in Figure 9 and the MPTC calculation results of their LVDC ports are shown in Figure 10, and Tables 5 and 6.

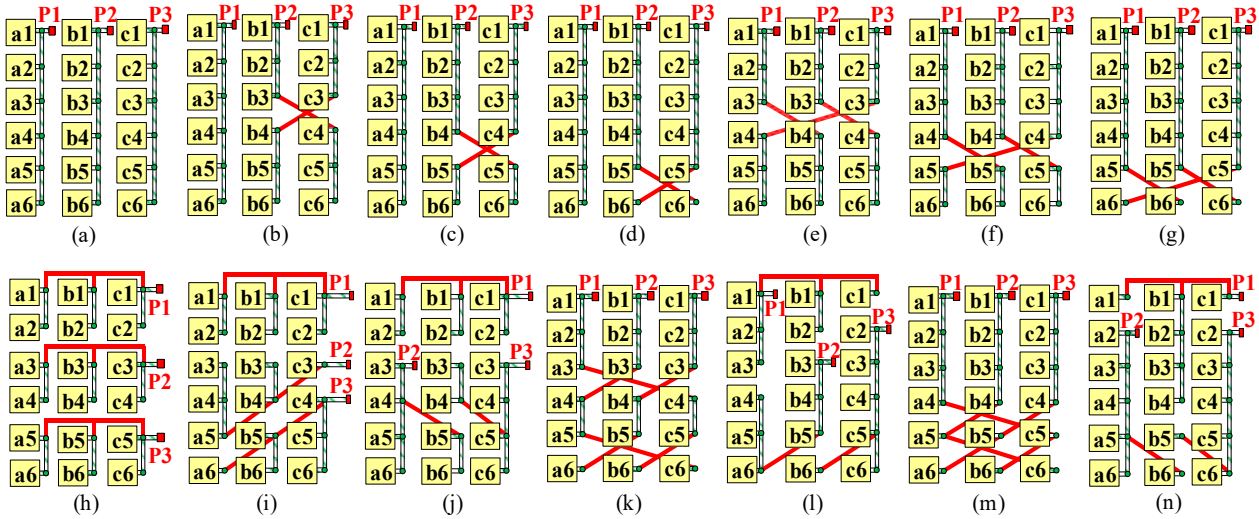

Figure 9. IDBS-MPETs of $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$. **(a)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{S}_{(3)(6)}$. **(b)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{S}_{(1)(6)}\mathrm{D}_{(2)(3,3)}$. **(c)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{S}_{(1)(6)}\mathrm{D}_{(2)(4,2)}$. **(d)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{S}_{(1)(6)}\mathrm{D}_{(2)(5,1)}$. **(e)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{D}_{(3)(3,3)}$. **(f)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{D}_{(3)(4,2)}$. **(g)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{D}_{(3)(5,1)}$. **(h)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{T}_{(3)(2,2,2)}$. **(i)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{T}_{(1)(2,2,2)}\mathrm{T}_{(2)(3,2,1)}$. **(j)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{D}_{(2)(4,2)}\mathrm{T}_{(1)(2,2,2)}$. **(k)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{T}_{(3)(3,2,1)}$. **(l)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{D}_{(1)(3,3)}\mathrm{D}_{(1)(5,1)}\mathrm{T}_{(1)(3,2,1)}$. **(m)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{T}_{(3)(4,1,1)}$. **(n)** $\mathrm{N}_{(6)}\mathrm{P}_{(3)}$-$\mathrm{D}_{(2)(5,1)}\mathrm{T}_{(1)(4,1,1)}$.

Table 5. MPTC results of LVDC ports in the IDBS-MPET with N_{H} = 6 and N_{P} = 3.

m_{N}	$\mathrm{T}_{(2,2,2)}$	$\mathrm{T}_{(3,2,1)}$	$\mathrm{T}_{(4,1,1)}$	$\mathrm{D}_{(3,3)}$	$\mathrm{D}_{(4,2)}$	$\mathrm{D}_{(5,1)}$	$\mathrm{S}_{(6)}$
0.5	4.498	3.957	3.430	3.606	3.142	2.679	4.181
0.6	2.699	2.509	2.346	2.317	2.181	2.023	2.447
0.7	1.718	1.639	1.578	1.542	1.483	1.417	1.541
0.8	1.028	1.000	0.975	0.961	0.934	0.905	0.930
0.9	0.476	0.470	0.464	0.462	0.453	0.445	0.444

Table 6. The percentage of the MPTC results of six kinds of LVDC ports relative to the MPTC results of $\mathrm{T}_{(2,2,2)}$-type LVDC port in the IDBS-MPET with N_{H} = 6 and N_{P} = 3.

m_{N}	$\mathrm{T}_{(3,2,1)}$	$\mathrm{T}_{(4,1,1)}$	$\mathrm{D}_{(3,3)}$	$\mathrm{D}_{(4,2)}$	$\mathrm{D}_{(5,1)}$	$\mathrm{S}_{(6)}$
0.5	87.97%	76.26%	80.17%	69.85%	59.56%	92.95%
0.6	92.96%	86.92%	85.85%	80.81%	74.95%	90.66%
0.7	95.40%	91.85%	89.76%	86.32%	82.48%	89.70%
0.8	97.28%	94.84%	93.48%	90.86%	88.04%	90.47%
0.9	98.74%	97.48%	97.06%	95.17%	93.49%	93.28%

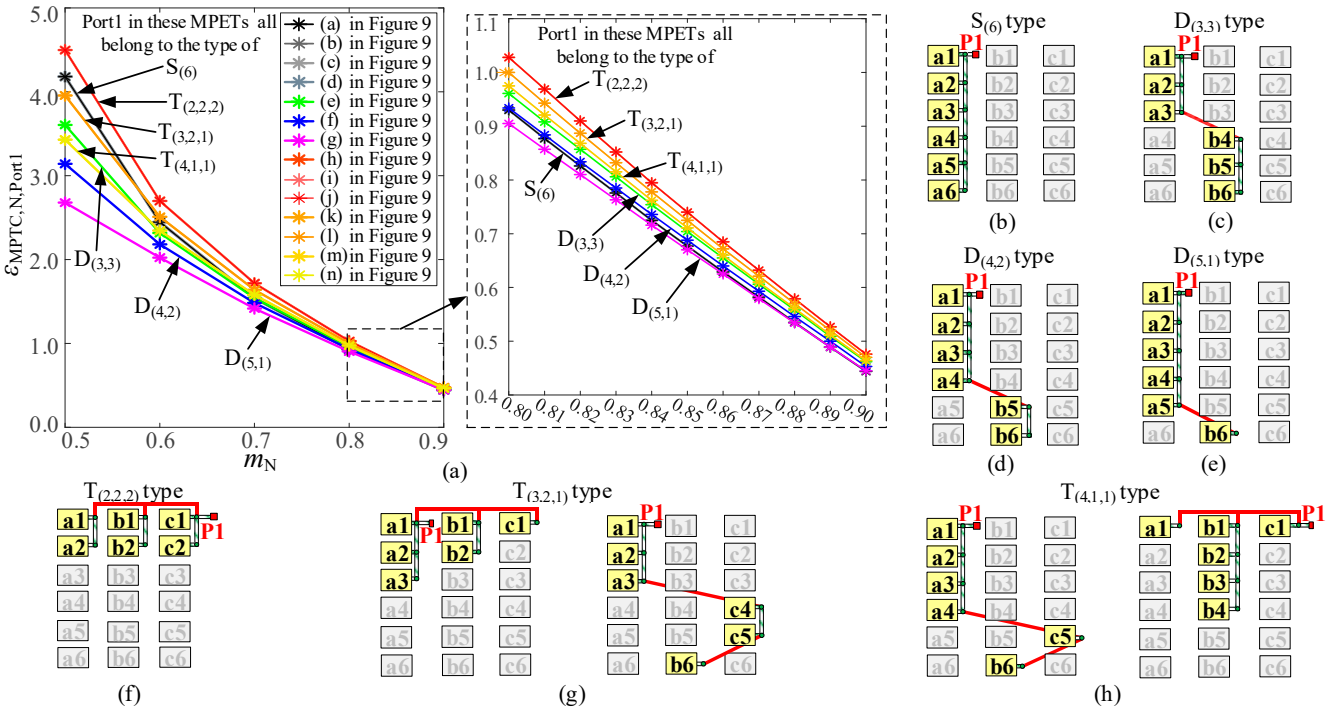

Figure 10. MPTC and the structures of Port 1 in MPETs shown in Figure 9. (**a**) MPTC of Port 1. (**b**) Port 1 of $S_{(6)}$ type. (**c**) Port 1 of $D_{(3,3)}$ type. (**d**) Port 1 of $D_{(4,2)}$ type. (**e**) Port 1 of $D_{(5,1)}$ type. (**f**) Port 1 of $T_{(2,2,2)}$ type. (**g**) Port 1 of $T_{(3,2,1)}$ type. (**h**) Port 1 of $T_{(4,1,1)}$ type.

In order to make the MPTC calculation results more intuitive, the MPTC calculation results of S-Port, D-Port and T-Port will be shown in colors of different tones. The MPTC of S-Port will be shown in neutral colors (i.e., black or gray of different saturations). The MPTC of D-Port will be shown in cold colors (i.e., green, blue, cyan or purple of different saturations). The MPTC of T-Port will be shown in warm colors (i.e., red, orange, yellow or gold of different saturations). In the figures of the MPTC calculation results, the type of the LVDC port is indicated by $S_{(ns)(ns1)}$, $D_{(nd)(nd1,\,nd2)}$ and $T_{(nt)(nt1,nt2,nt3)}$. The structures of Port 1 belonging to these types are shown in Figure 10b–h.

The MPTC results of the LVDC ports of more than 80 typical IDBS-MPET topologies show the following:

(1) The symmetrical LVDC port attains a larger MTPC value at every m_N compared to the asymmetrical ones of the same type. As mentioned in Part B of Section 2, the T-Port can be divided into symmetrical T-Port and asymmetrical T-Port, the same as for the D-Port. As shown in Figure 10a, the MPTC value of the symmetrical T-Port (i.e., $T_{(2,2,2)}$) is larger than that of asymmetrical T-Ports (i.e., $T_{(3,2,1)}$ and $T_{(4,1,1)}$) at every m_N. The MPTC value of the symmetrical D-Port (i.e., $D_{(3,3)}$) is larger than that of asymmetrical D-Ports (i.e., $D_{(4,2)}$ and $D_{(5,1)}$) at every m_N. In addition, the MPTC value becomes smaller as the structure of the LVDC port becomes more asymmetrical. For example, the MPTC value of the $T_{(4,1,1)}$ type is smaller than that of the $T_{(3,2,1)}$ type at every m_N. Therefore, the symmetrical T-Port is most preferable for the construction of the LVDC port, and the less asymmetrical T-Port can also be suitable as an option.

(2) The symmetrical T-Port attains the largest MTPC value at every m_N, and the most asymmetrical D-Port attains the smallest MTPC value at every m_N. As shown in Figure 10a, the MPTC value of the symmetrical T-Port (i.e., $T_{(2,2,2)}$) is the largest. The MPTC value of the most asymmetrical D-Port (i.e., $D_{(5,1)}$) is the smallest. Moreover, as shown in Figure 10a and in the supplementary material of this paper, the MPTC value of asymmetrical D-Ports always becomes less than that of the T-Ports, symmetrical

D-Ports and S-Ports. Therefore, it is best not to choose an asymmetrical D-Port to construct a LVDC port.

(3) The MPTC value of the S-Ports is larger than that of the D-Ports when $m_N < 0.7$, and larger than that of some extreme asymmetrical T-Ports when $m_N < 0.6$. As shown in Figure 10a, when $m_N < 0.7$, the MPTC value of the S-Port (i.e., $S_{(6)}$) is larger than that of the D-Ports (i.e., $D_{(3,3)}$, $D_{(4,2)}$ and $D_{(5,1)}$). When $m_N < 0.6$, the MPTC value of the S-Port is even larger than that of the asymmetrical T-Ports (i.e., $T_{(4,1,1)}$). The MPTC of the S-Port will become smaller than that of most T-Ports and the symmetrical D-Port when $m_N \geq 0.7$, whereas it is still larger or close to the value of the asymmetrical D-Port (i.e., $D_{(4,2)}$ and $D_{(5,1)}$). Therefore, it is much better to choose an S-Port to construct an LVDC port rather than an asymmetrical D-Port.

(4) Regardless of the type of LVDC port, the MPTC value increases with the reduction in m_N. In industrial PET products, the m_N is usually set between 0.7 and 0.9 [9,14,26]. As shown in Figure 10a, when m_N is in the range from 0.8 to 0.9, the MPTC value of any type of LVDC port is less than 1. In order to improve the MPTC of the LVDC port, it is much better to set the m_N of the IDBS-MPET in the range from 0.7 to 0.8 or even in the range from 0.6 to 0.8.

(5) For the same type of LVDC port, the arrangement of modules in each phase does not affect the MPTC. As show in Figure 10g,h, both the $T_{(3,2,1)}$- and $T_{(4,1,1)}$-type LVDC port have two variants. As shown in Figure 10a, the two variants of the $T_{(3,2,1)}$-type LVDC port have the same MPTC, and so does the $T_{(4,1,1)}$-type LVDC port.

(6) The variations in the MPTC among different configurations, especially the close performance between $S_{(6)}$ and the highest percentages in other types, can be attributed to the inherent design and operational characteristics of each configuration. For example, symmetrical configurations like $T_{(2,2,2)}$ generally offer a higher MPTC due to balanced power distribution among phases, while asymmetrical ones like $D_{(5,1)}$ might lag due to uneven load handling. The $S_{(6)}$ configuration, despite being a single-phase connection, leverages its design to maximize power transfer, thereby offering a compelling alternative for specific applications where compact design and high power-transfer capability are critical.

4.2. Three Topology Design Rules

Due to the limitations of N_H, N_P and $P_{N,Portj}$, the LVDC ports in an IDBS-MPET cannot all be constructed as symmetrical T-Ports. The S-Port and D-Port also need to be used. Three topology design rules are derived from the MPTC results.

(1) Topology design rule 1: when designing an IDBS-MPET, it is preferable that the LVDC ports are constructed as symmetrical and less asymmetrical T-Ports.

(2) Topology design rule 2: when as many LVDC ports as possible have been designed based on topology design rule 1, it is preferable that the remaining LVDC ports are constructed as symmetrical D-Ports.

(3) Topology design rule 3: when as many LVDC ports as possible have been designed based on topology design rule 1 and topology design rule 2, it is preferable that the remaining LVDC ports are constructed as S-Ports.

4.3. IDBS-MPET Design Scheme

The IDBS-MPET design scheme is given in Figure 11. The basic idea of the design scheme is that a few IDBS-MPET topologies that conform to the three topology design rules are designed preliminarily, and then, the optimal one is determined by $\Delta\varepsilon_{MPTC,MPET}$.

The IDBS-MPET design scheme contains five modules:

(1) Parameter input module. The u_{dc}, N_H can be designed based on the MVAC grid voltage. Previous studies have proved that 1200 V or 1700 V are identified as optimum blocking voltages of the power semiconductors [27]. Thus, the u_{dc} can be set around 600 V or 850 V. In industrial PET products, the m_N is usually set between 0.7 and

0.9 [14,16], so N_H can be determined by (22). The N_P, $P_{N,DAB}$ and $P_{N,Portj}$ ($j = 1...N_P$) can be designed based on the variety and the power demand of DGs and DC loads.

(2) Preliminary design module. Several IDBS-MPETs are preliminarily designed based on the three topology design rules. As mentioned in Part A of this section, the asymmetrical T-Port may gain advantage or disadvantage over the symmetrical D-Port. Moreover, the range of the advantage of the symmetrical D-Port over the S-Port may be wide or narrow. Thus, more than one IDBS-MPET topology may emerge after the preliminary designing process. It is noted the topologies will not be too much. These topologies shall be systematically identified and enumerated as MPET1, MPET2, . . ., through MPETn, for ease of reference and subsequent analysis.

(3) MPTC calculation module. The MPTCs of MPET1, . . ., MPETn are calculated based on (5), namely, $\varepsilon_{MPTC,MPET1}$, . . ., $\varepsilon_{MPTC,MPETn}$.

(4) MPET evaluation module. In order to determine the optimal topology, the evaluation index $\Delta\varepsilon_{MPTC,MPET}$ is proposed. If two MPETs are under comparison, namely, the MPETx_1 and the MPETx_2, $\Delta\varepsilon_{MPTC,MPET}$ is defined as follows:

$$\Delta\varepsilon_{MPTC,MPET} = \sum_{m_N=0.5}^{0.9} (\varepsilon_{MPTC,MPETx1,m_N} - \varepsilon_{MPTC,MPETx2,m_N}) \quad (23)$$

where $\varepsilon_{MPTC,MPETx1,mN}$ is the $\varepsilon_{MPTC,MPET}$ of MPETx_1 on m_N; $\varepsilon_{MPTC,MPETx2,mN}$ is the $\varepsilon_{MPTC,MPET}$ of MPETx_2 on m_N. The $\Delta\varepsilon_{MPTC,MPET}$ makes a comprehensive MPTC evaluation of the two MPETs on each m_N. When the $\Delta\varepsilon_{MPTC,MPET} > 0$, the MPET$x_1$ emerges as preferable compared to MPETx_2 and vice versa.

(5) Optimal topology output module. Finally, the optimal IDBS-MPET is the one that always has a positive $\Delta\varepsilon_{MPTC,MPET}$.

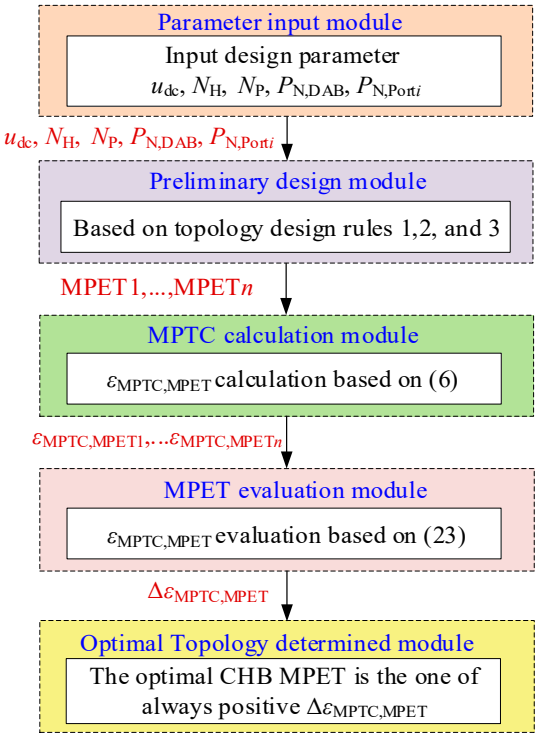

Figure 11. IDBS-MPET systematic design scheme.

5. Evaluation Results

In this section, the optimal IDBS-MPET with $N_H = 6$ and $N_P = 6$ is designed by the proposed scheme. Moreover, the MPTC evaluation is conducted with the optimal IDBS-MPET and twelve other ones not designed by the proposed scheme to validate the effectiveness of the proposed design scheme.

In the parameter input module, design parameters are determined and listed in Table 7. In the preliminary design module, each LVDC port will be designed based on the three topology design rules.

Table 7. Parameters of IDBS-MPET with $N_H = 6$ and $N_P = 6$.

Design Parameters	Value
u_{dc}	750 V
N_H	6
N_P	6
$P_{N,DAB}$	50 kW
$P_{N,Port1}$	200 kW
$P_{N,Port2}$	200 kW
$P_{N,Port3}$	150 kW
$P_{N,Port4}$	150 kW

The structures of Port 1 to 6 are shown in Figure 12. Each of Port 1 and Port 2 consists of four DABs and both of them can be constructed as asymmetrical T-Ports (i.e., $T_{(2,1,1)}$) or symmetrical D-Ports (i.e., $D_{(2,2)}$). Each of Port 3 and Port 4 consists of three DABs and both of them will be constructed as symmetrical T-Ports (i.e., $T_{(1,1,1)}$). Each of Port 5 and Port 6 consists of two DABs and both of them will be constructed as symmetrical D-Ports (i.e., $D_{(1,1)}$).

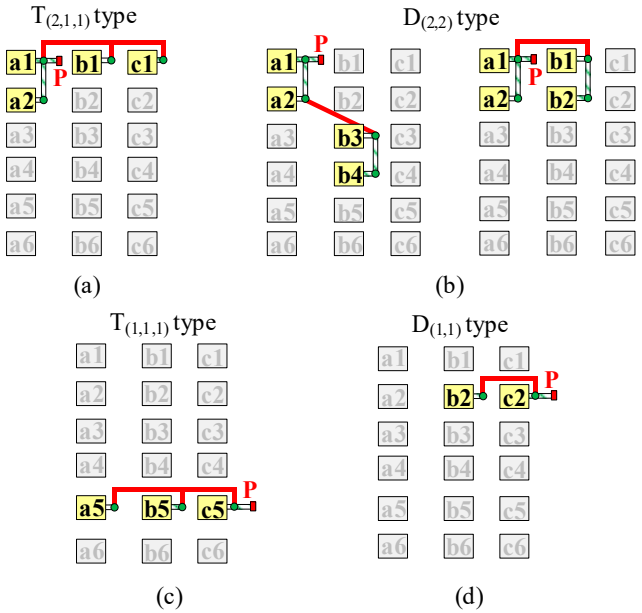

Figure 12. Structure of LVDC ports in MPETs shown in Figure 13. (**a**) Port 1 of $T_{(2,1,1)}$ type. (**b**) Port 1 of $D_{(2,2)}$ type. (**c**) Port 1 of $T_{(1,1,1)}$ type. (**d**) Port 1 of $D_{(1,1)}$ type.

By employing the proposed design methodology, each LVDC port achieves its maximum power transfer capability relative to other configurations. For the LVDC ports consisting of four DABs, the best type of configuration using the proposed methodology, i.e., $T_{(2,1,1)}$, and the worst type of configuration not using the proposed methodology, i.e., $D_{(3,1)}$, are shown in Table 8. Under every m_N, especially when $m_N < 0.8$, the LVDC port employing the proposed methodology exhibits a substantially higher maximum power and a greater absolute minimum power in comparison to alternative configurations.

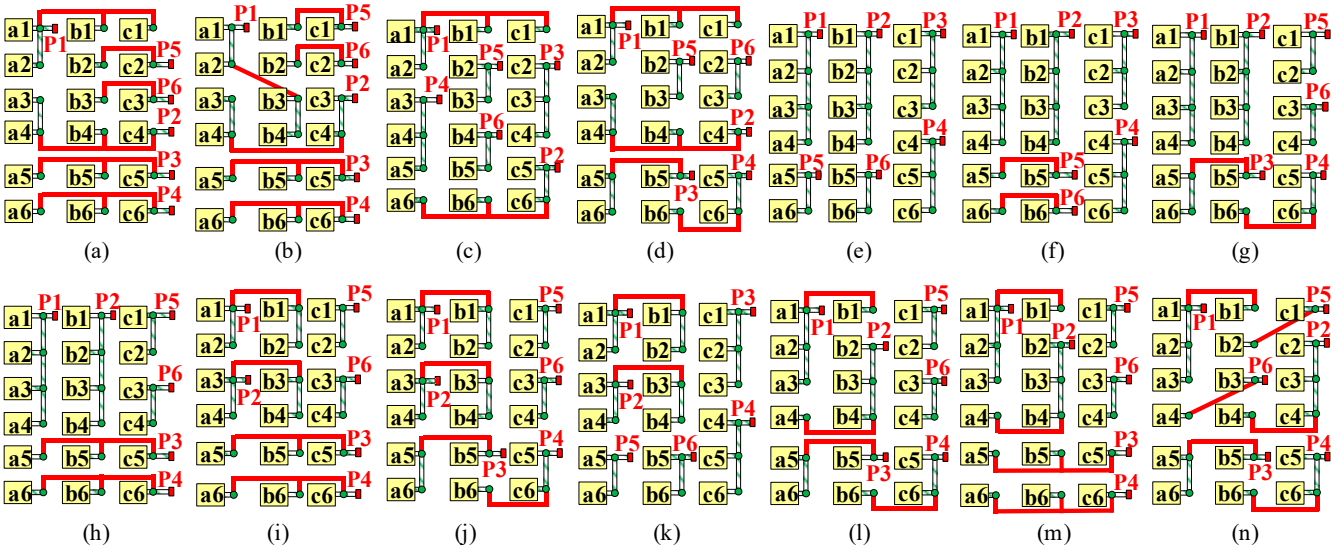

Figure 13. IDBS-MPET with $N_H = 6$ and $N_P = 6$, namely, $N_{(6)}P_{(6)}$. (**a**) $N_{(6)}P_{(6)}$-$D_{(2)(1,1)}T_{(2)(1,1,1)}T_{(2)(2,1,1)}$ is one of the preliminary designed topologies and finally emerges as the optimal one designed by the proposed design scheme. (**b**) $N_{(6)}P_{(6)}$-$D_{(2)(1,1)}D_{(2)(2,2)}T_{(2)(1,1,1)}$ is the other preliminary designed topology. (**c**) $N_{(6)}P_{(6)}$-$S_{(2)(2)}S_{(2)(3)}T_{(2)(2,1,1)}$. (**d**) $N_{(6)}P_{(6)}$-$S_{(2)(2)}D_{(2)(2,1)}T_{(2)(2,1,1)}$. (**e**) $N_{(6)}P_{(6)}$-$S_{(2)(2)}S_{(2)(3)}S_{(2)(4)}$. (**f**) $N_{(6)}P_{(6)}$-$S_{(2)(3)}S_{(2)(4)}D_{(2)(1,1)}$. (**g**) $N_{(6)}P_{(6)}$-$S_{(2)(2)}S_{(2)(4)}D_{(2)(2,1)}$. (**h**) $N_{(6)}P_{(6)}$-$S_{(2)(2)}S_{(2)(4)}T_{(2)(1,1,1)}$. (**i**) $N_{(6)}P_{(6)}$-$S_{(2)(2)}D_{(2)(2,2)}T_{(2)(1,1,1)}$. (**j**) $N_{(6)}P_{(6)}$-$S_{(2)(2)}D_{(2)(2,1)}D_{(2)(2,2)}$. (**k**) $N_{(6)}P_{(6)}$-$S_{(2)(2)}S_{(2)(3)}D_{(2)(2,2)}$. (**l**) $N_{(6)}P_{(6)}$-$S_{(2)(2)}D_{(2)(2,1)}D_{(2)(3,1)}$. (**m**) $N_{(6)}P_{(6)}$-$S_{(2)(2)}D_{(2)(3,1)}T_{(2)(1,1,1)}$. (**n**) $N_{(6)}P_{(6)}$-$D_{(2)(1,1)}D_{(2)(2,1)}D_{(2)(3,1)}$. The IDBS-MPETs in (**c**–**n**) are not designed by the proposed design scheme and they are used to be compared with (**a**) by $\varepsilon_{MPTC,MPET}$ to validate the effectiveness of the proposed design scheme.

Table 8. The maximum and minimum power of different types of LVDC ports consisting of four DABs in the IDBS-MPET in Figure 12.

Port Type	$m_N = 0.9$		$m_N = 0.8$		$m_N = 0.7$		$m_N = 0.6$		$m_N = 0.5$	
	P_{max}/kW	P_{min}/kW	P_{max}/kW	P_{min}/kW	P_{max}/kW	P_{min}/kW	P_{max}/kW	P_{min}/kW	P_{max}/kW	P_{min}/kW
$T_{(2,1,1)}$	229.4	110.9	269.0	23.6	324.8	−61.8	409.3	−145.4	551.4	−209.0
$S_{(4)}$	229.4	119.7	269.2	49.6	325.5	−17.1	411.7	−84.3	559.8	−154.9
$D_{(2,2)}$	229.4	113.8	268.5	36.7	323.2	−30.4	404.8	−88.0	539.0	−138.3
$D_{(3,1)}$	229.2	116.7	267.6	43.8	319.8	−22.6	393.8	−85.8	505.3	−122.6

At last, there are two preliminary designed topologies of the IDBS-MPET with $N_H = 6$ and $N_P = 6$, the $N_{(6)}P_{(6)}$-$D_{(2)(1,1)}T_{(2)(1,1,1)}T_{(2)(2,1,1)}$ one, i.e., (a) in Figure 13, and the $N_{(6)}P_{(6)}$-$D_{(2)(1,1)}D_{(2)(2,2)}T_{(2)(1,1,1)}$ one, i.e., (b) in Figure 13. In the MPTC calculation module, the $\varepsilon_{MPTC,MPET}$ of the two IDBS-MPETs is calculated and shown in Table 9. In the MPET evaluation module, the $\Delta\varepsilon_{MPTC,MPET}$ is calculated to be 1.94. Finally, in the optimal topology output module, the $N_{(6)}P_{(6)}$-$D_{(2)(1,1)}T_{(2)(1,1,1)}T_{(2)(2,1,1)}$ one emerges as the optimal IDBS-MPET with $N_H = 6$ and $N_P = 6$.

Twelve other IDBS-MPETs with $N_H = 6$ and $N_P = 6$ that are not designed by the proposed scheme are shown in (c)~(n) of Figure 13. The MPTC calculation results of the optimal one, namely, $N_{(6)}P_{(6)}$-$D_{(2)(1,1)}T_{(2)(1,1,1)}T_{(2)(2,1,1)}$, and twelve other IDBS-MPETs are shown in Figure 14. As shown in Table 9, the optimal IDBS-MPET designed by the proposed scheme emerges as the one which always has a positive $\Delta\varepsilon_{MPTC,MPET}$, and thus, the effectiveness of the proposed design scheme is validated.

Table 9. MPTC results of the IDBS-MPETs with $N_H = 6$ and $N_P = 6$.

m_N	$\varepsilon_{MPTC,MPET}$													
	Figure 13a	Figure 13b	Figure 13c	Figure 13d	Figure 13e	Figure 13f	Figure 13g	Figure 13h	Figure 13i	Figure 13j	Figure 13k	Figure 13l	Figure 13m	Figure 13n
0.5	22.39	21.56	22.58	22.08	22.12	21.94	21.63	22.12	21.75	21.25	21.75	20.76	21.25	20.57
0.6	17.58	16.96	17.32	17.29	16.3	16.61	16.70	17.11	17.08	16.67	16.70	16.54	16.95	16.42
0.7	13.71	13.38	13.09	13.18	12.65	12.57	12.74	13.36	13.47	12.85	12.76	12.74	13.35	12.65
0.8	9.33	9.19	8.68	8.78	8.42	8.68	8.52	8.81	8.94	8.64	8.54	8.56	8.86	8.82
0.9	4.63	4.60	4.39	4.44	4.30	4.42	4.35	4.43	4.49	4.41	4.36	4.38	4.46	4.50

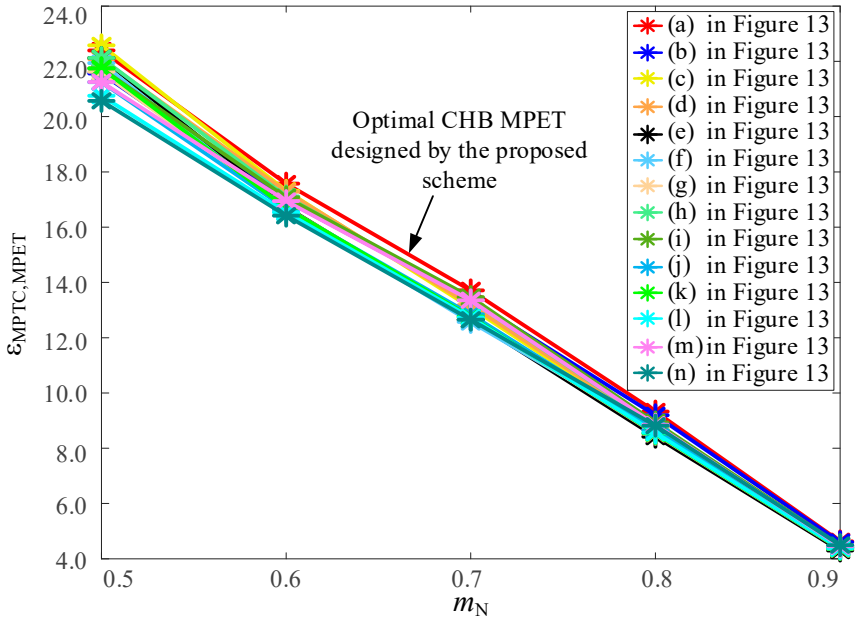

Figure 14. MPTC calculation results of IDBS-MPETs with $N_H = 6$ and $N_P = 6$, namely, $N_{(6)}P_{(6)}$.

6. Discussion

This study presented a novel design scheme for IDBS-MPET topology aimed at maximizing the power transmission capability of low-voltage DC ports. The findings reveal significant implications for the design and operation of multiport power electronic transformers in hybrid AC/DC distribution systems. By categorizing LVDC ports into three basic types (S-Port, D-Port and T-Port) and establishing a design methodology based on the maximum power transmission capability (MPTC), this research contributes a systematic approach to enhance power balance and efficiency in MPET applications.

Comparative analysis with existing MPET configurations, such as those relying on a common DC bus structure, underscores the advantages of the proposed IDBS-MPET design. Specifically, the ability to directly construct each LVDC port by paralleling the output terminals of dual active bridge (DAB) converters eliminates the need for additional DC/DC converters, thereby reducing hardware costs and improving system efficiency. This approach not only addresses the challenge of power imbalance in IDBS-MPET systems but also offers a flexible and scalable solution for integrating diverse energy resources and loads in modern electrical distribution networks.

The proposed topology design rules, derived from extensive simulations of more than 80 typical IDBS-MPET topologies, offer clear guidelines for optimizing the structure of LVDC ports. These rules highlight the preference for symmetric T-Port, symmetric D-Port and S-Port configurations in order of their optimal power transmission capabilities. Such insights are invaluable for designers and engineers seeking to develop MPET systems that can accommodate varying power levels and voltage requirements while maintaining high efficiency and reliability.

Our research highlights the impact of the rated modulation ratio m_N on the MPTC of the LVDC port in the IDBS-MPET. Specifically, we recommend setting m_N in the range from 0.7 to 0.8, or even extending it to range from 0.6 to 0.8, contrary to the conventional range from 0.7 to 0.9 used in industrial PET products. Implementing this adjustment has several practical implications:

Optimized design. This adjustment allows for a more flexible and efficient design of PET systems, enabling them to accommodate a wider range of power levels and operational conditions.

Cost-effectiveness. By optimizing the MPTC, the proposed adjustment can lead to reductions in the size and cost of PETs, making them more competitive and appealing for industrial applications.

Future research could explore the integration of advanced control strategies and power electronics technologies to further enhance the performance and adaptability of IDBS-MPET systems. Additionally, real-world implementation and testing of the proposed topology in various operational scenarios would provide empirical evidence of its benefits and limitations, paving the way for further refinements and applications in the field of power electronics and energy distribution.

7. Conclusions

In this paper, a design scheme of IDBS-MPET topology is proposed based on the MPTC of the LVDC ports. Each LVDC port is directly constructed by paralleling the output terminals of DAB converters, eliminating the need for additional DC/DC converters. The LVDC ports are categorized into three basic types: S-Port, D-Port and T-Port. A design methodology for LVDC port structures is established, with the MPTC of the LVDC ports as the evaluation metric. Through extensive simulations of the MPTC in different LVDC port structures, three topology design rules for the IDBS-MPET are derived. Symmetric T-Ports, symmetric D-Ports and S-Ports, in that order, are the optimal structures for constructing low-voltage DC ports. The proposed method allows for the design of all LVDC port structures in an IDBS-MPET given the rated voltage of the H-bridge DC side, the number of H-bridges per phase, the rated power of the DAB converters, the number of LVDC ports and the rated power of each LVDC port, following the three topology design rules.

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